POWER9 Processor Registers Specification

Volume 1

Advance

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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release.

Version	Revision Date	Description
1.1	31 January 2017	Edited Section 8 PB Chiplet (Nest Chiplet 3).
1.0	30 August 2016	Initial release.

About this Document

This document describes the registers used by the IBM® POWER9 processor. To ensure you have the most current version of this document, visit the OpenPOWER Connect website.

Who Should Read this Document

This document is intended for system software and hardware developers and application programmers who are developing products that use the POWER9 registers. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of reduced instruction set computer (RISC) processing, and details of the Power Instruction Set Architecture (ISA).

Organization

This document is divided into three volumes, of approximately equal sizes, organized by address ranges.

Volume	Address Range	Contents
1	0x0000_0000 - 0x050F_FFFF	Chip logic registers Processor bus registers
2	0x0600_0000 - 0x200F_FFFF	X bus chiplet registers[1] OB chiplet registers[1] PCI registers Cache and core registers
3	0x0700_0000 - 0x070F_FFFF	Memory controller registers[1]

1. These registers use indirect addresses in the range 0x8000_0000_0000_0000 - 0x8000_0000_0901143F.

In each volume, the table of contents lists the primary divisions in the document. Address maps at the beginning of each chapter list the registers in each chiplet in alphabetical order by mnemonic. Within each chapter, the registers themselves are arranged by their addresses. A register can have multiple addresses with different addresses for different chiplets.

Bit Significance

In the POWER9 documentation, the smallest bit number represents the most significant bit of a field, and the largest bit number represents the least significant bit of a field.

Representation of Numbers

Numbers are generally shown in decimal format, unless otherwise designated. One of the following conventions is used to indicate the numeral system, where "nn" or "NN" indicates the numerical value:

- Binary values are represented as 0bn, `nn'b, or `n'.
  Examples: 0b01, `01'b, or `01'
- Decimal values are represented as nn or `nn'd.
  Examples: 1 or `1'd
- Hexadecimal values are represented as 0xN, x`N', or `NN'h.
  Examples: 0x000000000204000D, x`000000000204000D', or `000000000204000D'h

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “X” or "x."

Representation of Enumerated Registers

To succinctly describe registers that are identical except for a numeral in the register name and mnemonic, a syntax is used that enables these “enumerated registers” to be described in a single register table.

The registers in the DP16 section are enumerated because there are five instances of the DP16 unit for each DDR PHY port. All five instances are required for each DDR PHY port, and, at the chip level, there are eight DDR PHY ports. Each DDR PHY unit is self-contained and comprises four independent ports that connect to DIMM slots. This unit is replicated twice on the POWER9 system to provide a maximum of eight ports. All of the DP16 registers are documented in one replication. The address is the only difference between the two. The first replication is on 0x0000_0000_0700_0000, and the second replication is on 0x0000_0000_0800_0000.

For example: IOM0.DDRPHY_DP16_DATA_BIT_ENABLE0_P0_[n]
8000000007 01103F (SCOM), +0x0400_0000_0000

IOM1.DDRPHY_DP16_DATA_BIT_ENABLE0_P0_[n]
8000000008 01103F (SCOM), +0x0400_0000_0000

Register Names

The following syntax is used for enumerated register names:

<register name> [n] (n = m:p) where m and p are integers

For example: TWG Control Register [n] (n = 0:15)

Mnemonic

The following syntax is used for enumerated mnemonics:

<mnemonic>_[n], where n is an integer from the enumerated register name

For example: REG_TWGDATA_[n]
REG[n]_TWGDATA

Address Offset

The following syntax is used for enumerated address offsets so that enumerated registers can be described in a single register table. The stride defines the hexadecimal integer to add to the address for each enumeration.

<address_offset>, +<stride>

For example: 0x80030, +0x10

Register Name	**DP16 DQ Enable 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_ENABLE0_P0_[n]
Address	800000000701103F (SCOM), +0x0400_0000_0000
Description	A DP16 has 24 possible single-ended data pins that can send or receive data. This register is used to enable and disable each of the 24 pins for data sending or receiving. Any pins on the DP16 that are used as strobes or clocks to capture the data must not be marked as enabled in this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DATA_BIT_ENABLE_0_15: 1b = Indicates that the DP16 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. 0b = Indicates that the DP16 bit is not used to send or receive data. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Related Documents

The following documents can be helpful when reading this specification. They are available through OpenPOWER Connect or Power.org.

POWER9 Processor User's Manual
POWER9 Processor Datasheets
Power ISA User Instruction Set Architecture - Book I (Version 3.0)
Power ISA Virtual Environment Architecture - Book II (Version 3.0)
Power ISA Operating Environment Architecture (Server Environment) - Book III-S (Version 3.0)

Terminolgy

The following terms are used in volumes 1, 2, or 3 of the *POWER9 Processor Registers Specification*.

Note: Acronyms are not typically expanded in the body of this document.

3DS	Three-dimensional stacking
AADR	Array Access Data Register
AAER	Array Access ECC Register
ABIST	Array built-in self test
ABIST/IOBIST	Array built-in self test / input/output built-in self test
ABUS	**Note:** This is not really an acronym but a name (A bus).
AC	Alternating current
ACK	Acknowledgment or acknowledge. A transmission that is sent as an affirmative response to a data transmission.
ACT	Activate
ACT#	Activate (inverted)
ADC	APSS with analog-to-digital converter
ADDR	Address
ADR	Address
ADU	Alter-display unit
AES	Advanced Encryption Standard
AFSR	Average Frequency Sample Register
AFTR	Average Frequency Threshold Register
AIB	1. ASIC interconnect bus 2. ASIC interface bus
AL	Additive latency. For more information, see the JEDEC DDR3 and DDR4 DRAM specifications.
AMF	Availability management framework
AMux	Analog multiplexer
ANA16	Analog 16 bits
AND write	Current register content is ANDed with write data and the result is stored in the register (access type WO_AND / WOX_AND).
AP	Auto-predischarge. For more information, see the JEDEC DDR3 and DDR4 DRAM specifications.
APB	Advanced peripheral bus
APIN	ADR pin. The logic macro inside DDR units for sending data to the ADR bus.
APSS	Analog power subsystem sweep. Provides real-time power measurements of voltage rails.
ARB	Architecture Review Board
ARE	Address error
ARY	Array
ASB	Advanced system bus

ASBE	Array single-bit error
ASIC	Application-specific integrated circuit
AT	Address translation
ATEST	Analog test pin
ATPG	Advanced test pattern generator
AUE	Array uncorrectable error (UE)
AVP	Architectural verification program. A custom payload used to test a processor or other host hardware or software function.
AVS	Adaptive voltage scaling
Âµ	Micron
Âµs	Microsecond
B	Byte
BA	Bank address
BAR	Base Address Register
BCDE	Block copy download engine
BCE	Block copy engine
BCEBAR	Block Copy Engine Base Address Register
BCECSR	Block Copy Engine Control and Status Register
BCUE	Block copy upload engine
BCW	Buffer control word
BDF	Bus device function
BE	1. Big-endian 2. Branch Trace Enable bit in the MSR (MSRBE) 3. Byte enable
BER	Bit error rate
BG	Bank group
BI	Burn in
BIST	Built-in self test
BL	Bit length
BL8	Burst length 8
BNDY	Boundary I/Os
BSC	Boundary scan cells
BW	Bandwidth
BYPASSN	Bypass low active
c_err_rpt	Common lib error report
CACCR	Core Analog Clock Control Register

CACSR	Core Analog Clocking Status Register
CAL	Calibration
CAM	Content-addressable memory
CAPI	Coherent Accelerator Processor Interface
CAPP	Coherent accelerator processor proxy
CAS	Column-address select
CASN	Column-address select (inverted)
CAW2	An internal pipeline stage designator
CBS	CFAM boot sequencer
CC	1. Clock controller 2. Congruence class
CCB	Change control board
CCFG	Clock control configuration
CCS	Configured command sequencer
CD	Compact disc
CDIMM	Custom dual in-line memory module
CDR	Clock and data recovery
CE	Correctable error. A hardware error that the firmware detects and corrects without impacting the state of the system.
CERR	Common lib error report
CFAM	Common field-replaceable unit (FRU) access macro
CFIR	Chiplet Fault Isolation Register
CGC	Congruence class
checkstop	A severe error inside a processor core that causes a processor core to stop all processing activities. This is the same as a system crash. The operating system is not functional.
chip select	A signal that selects one or more memory modules to respond to a command/address. An exact one-to-one correspondence exists between chip selects and ranks.
CI	1. Cache-inhibited 2. Cast-in
CID	Completer ID. When returning the completion for a transaction, the completer attaches its Bus/Dev/Func to the transaction as a CID. See also RID.
CIDSR	Core IVRM Dropout Sample Register
CK	Clock
CK#	Clock (inverted)
CKE	Clock enable
CKSW	Chicken switch: A programmable mode bit that disables a certain function or changes its behavior.

CL	Column-address select (CAS) latency
CLK	Clock
CMD, cmd	Command
CME	Core management engine
CMOS	Complementary metal-oxide semiconductor
CMSK	Logical built-in self test (LBIST) channel mask
CO	Cast-out
CP	Chip pump
CPB	Coprocessor parameter block
CPI	Cycles per instruction
CPLT	Chiplet
CPLT_CTRL	Chiplet control
CPM	Critical path monitor
CPPM	Core PCB-slave power management macro (PPM)
CPS	Cycle-per-step
CQ	1. Common queue. Refers to the interface to the SMP interconnect. 2. Completion queue
CRC	Cyclic redundancy check
CRESP	Combined response
CS	Chip select
CSID	Chip select ID
CSN	Chip select (inverted)
CTL	Control
CTLE	1. Continuous time linear equalization 2. Continuous time linear equalizer
CTRL	Control
D/A	Display/alter
DAC	Digital-to-analog converter
DACTEST	DAC test
DBG	Debug
DBSR	Debug Status Register
DC	Direct current
DCACHE	Data cache
DCBZ	Data cache block set to zero
DCD	Duty cycle distortion

DCM	Dual-chip module
DCTEST	This is a mode where test operations are executed at very low frequencies.
DDR	Double data rate
DDR3	Double data rate type three
DDR4	Double data rate type four
DDRPHY	Double data rate physical interface
DEC	Decrementer
DERR	Distributed elastic round robin
DFE	1. Decision feedback equalization 2. Decision feedback equalizer
DFI	DDR PHY interface bus
DFT	Design for test
DGEN	Data pattern generator
diag	Diagnostic
DIMM	Dual in-line memory module. A small circuit board with memory-integrated circuits containing signal and power pins on both sides of the board.
DIN	Data in
DL	Downlink
DLDCH	Downlink data channel
DLL	1. Delay-locked loop 2. Dynamic link library
DLL/VREG	Delay-locked loop/voltage regulator
DLL/ZCAL	Delay-locked loop/impedance (Z) calibrator
DMA	1. Direct memory access. A technique for using a special-purpose controller to generate the source and destination addresses for a memory or I/O transfer. 2. Direct memory attach
DP16	Data path 16
DPC	DIMMs per port
DPLL	Digital phase-locked loop
DPLLFREQ	DPLL frequency control
DQ	1. Data 2. Data bit
DQS	Data strobe
DQSCLK	Data strobe clock
DR	1. Data Relocate bit in MSR (MSRDR) 2. Dynamic reconfiguration. The capability of a system to adapt to changes in the hardware/firmware physical or logical configuration, and to be able to use the new configuration, all without having to turn the platform power off or restart the operating system. See the *Power Architecture Platform Requirements (PAPR)* document for more information.

DRAM	Dynamic random-access memory. Storage in which the cells require repetitive application of control signals to retain stored data.
DRTM	Dynamic root of trust for measurement
DSI	Data storage interrupt.
DSM	Digital state machine
DSMP	Distributed symmetric multiprocessing
DTS	Digital thermal sensor
EA	Effective address. An address generated or used by a program to reference memory. A memory-management unit translates an EA to a virtual address (VA), which it then translates to a real address (RA) that accesses real (physical) memory. The maximum size of the effective-address space is 264 bytes.
EAT	1. Effective address translation 2. Event assignment table
ECC	See error correction code
EDAT	Even data
EDI	Elastic differential interface. A bus that consists of high-speed differential I/O links. The memory bus instance of an EDI bus is a “DMI bus,” and the off-module, fabric bus (between processors) instance of an EDI bus is an “A bus.”
EDR	Error Data Register
eDRAM	Embedded dynamic random access memory
EH	Exclusive access hint
EICR	Error Inject Control Register
EIIR	External Interrupt Injection Register
EIMR	External Interrupt Mask Register
EINR	External Interrupt Input Register
EIPR	External Interrupt Polarity Register
EISR	External Interrupt Status Register
EITR	External Interrupt Type Register
ELPR	Error Log Pointer Register
EM	Electron migration
EMC	Extended memory controller
ENOP	End sync/wait step; no operation
EOT	End of transfer
EPS	1. Entry-level power supply 2. Pervasive end points
EQ	Event queue
ERAT	Effective-to-real-address translation, or a buffer or table that contains such translations, or a table entry that contains such a translation.
ERR	Error

error correction code	A code appended to a data block that can detect and correct bit errors within the block.
ERRSUM	Error summary
ERS	Early read start
ETE	Error threshold exceeded
ETU	Express transaction unit
EXT	JTAG EXTEST instruction mode
FARB	Final arbiter. Part of the memory interface command sequencer (scheduler).
FARR	Fast array unload
FBC	Fabric bus connection
FET	Field-effect transistor
FFDC	First failure data capture. A collection of data used upon fail to analyze the root cause of the failure.
FIFO	First in, first out. Refers to one way elements in a queue are processed. It is analogous to “people standing in line.”
FIR	Fault Isolation Register. Register bits that show which piece of hardware failed.
FMAX, fmax	Maximum frequency
FMIN, fmin	Minimum frequency
FMULT	Frequency multiplier
FPGA	Field-programmable gate array
FSAFE	Safe frequency
FSI	1. Flexible service interface. The FSI covers all resources, except FSI slave 0 and slave 1, when addressed from an external service element via the FSI. 2. FRU support interface
FSI2PIB	FRU support/service interface to the pervasive interconnect bus
FSM	Finite state machine
FSP	Flexible service processor. An embedded controller for internal system control tasks in IBM Power Systems™. In addition to the processor core, the following I/O interfaces are integrated into the embedded controller: I²C, JTAG, UART, GPIO, FSI.
FUNC	Functional
FW	Firmware
FWMR	Firmware Mode Register
Gbps	Gigabits per second
GCR	Global control ring
glsmux	Glitchless multiplexer
GND	Ground
GPE	General-purpose engine

GPIO	General-purpose input/output
GPO	Global PHY offset
GPR	General Purpose Register
GPTR	General Purpose Test Register
GZIP	A file format used for file compression and decompression.
H/W	Hardware
HCA	1. Host channel adapter 2. Hot/cold affinity
HID	Hardware implementation dependent
HIRES	High resolution
HLD	High-level design
HMER	Hypervisor Maintenance Exception Register
HMI	Hypervisor maintenance interrupt
HP	High performance
HPC	High-performance computing
HSS	High-speed serial
HTB	Hierarchical test block
HTML	Hypertext Markup Language
HW	Hardware
HWCTRL	Hardware control
HYP	Hypervisor
I/O	Input/output
IAR	Instruction Address Register
IAUE	Intermittent array uncorrectable error
IC	Integrated circuit
ICACHE	Instruction cache
ICE	Intermittent chip error
ICP	Interrupt control presenter
ICRR	Inter-CME Communication Receive Register
ICS	Interrupt controller source
ICSW	Initiate coprocessor store word
ID	Identification
IDCR	IVRM Dropout Configuration Register
IE	Input enable
IEEE	Institute of Electrical and Electronics Engineers

IF	Interface
IFU	Instruction fetch unit
IMA	In-memory accumulate
IMA/PPE/HTM	In-memory accumulate/Power PC® element/hardware trace macro
IMPE	Intermittent mark placed error (MPE)
INIT	Initialization
INOP	Initial sync/wait step; no operation
INT	INTEST instruction support. The INTEST instruction can be triggered through JTAG or through register control.
INTP	Interrupt presenter
INV	JTAG enable inversion macro
IO or I/O	Input/output
IOBIST	Input/output built-in self test
IOOPPE	PPE used for control of I/O macros
IOP	1. I/O processor 2. Internal operation
IOTK	I/O toolkit
IP	1. Interrupt Prefix bit in MSR (MSRIP) 2. Internet protocol
IPL	1. Initial program load. The time between when power is applied to the platform hardware and when the payload is fully functional. 2. Interrupt presenter layer
IPW	Initial pattern write
IR	1. Infrared 2. Instruction Relocate bit in the MSR register (MSRIR)
IRCD	Intermittent register clock driver
IS	Industry standard
ISA	Instruction set architecture
ISU	1. Instruction sequencing unit 2. Interrupt source unit
ITR	Inherent time redundancy
IUE	Intermittent uncorrectable error
IVRM	Internal Voltage Regulation Module
IVRMCR	IVRM Control Register
IVRMDVR	IVRM Data Value Register
JEDEC	Formerly the Joint Electron Device Engineering Council
KHz	Kilohertz
L2SFF	Level 2 (L2) star flip flop
LBIST	Logical built-in self test

LBS	LBIST
LBUS	Local bus
LCB	1. Local clock buffer 2. Logon control block
LEM	Local error macro
LFSR	Linear Feedback Shift Register
LPID	Logical partition identification
LRDIMM	Load-reduced dual in-line memory module
LSB	Least-significant bit or byte
M/S	Master/slave
MA	Memory address
malf	Malfunction alert
MASK	A pattern of bits used to accept or reject bit patterns in another set of data. Hardware interrupts are enabled and disabled by setting or clearing a string of bits, with each interrupt assigned a bit position in a mask register.
MB	1. Mailbox 2. Megabyte
MBA	Memory buffer asynchronous
MBASE	Memory base
Mbps	Megabits per second
MBR	Member
MBS	Memory buffer synchronous
MC	1. Memory channel 2. Memory controller
MCA	The portion of the memory controller that runs synchronously to the memory interface.
MCB	The portion of the memory controller that runs synchronously to the DMI interface.
MCBCM	Memory controller built-in self-test compare mask
MCBCMQ	Memory Controller Built-In Self-Test Compare Mask Register
MCBIST	Memory card built-in self test
MCBIST-RQ	Memory controller built-in self-test to sequencer reorder queue interface
MCBMCAT	Memory controller built-in self-test maintenance current address trap
MCD	Memory coherency directory
MCE	1. Machine check exception 2. Mark corrected error 3. Marked chip correctable error
MCHK	Machine check
MCU	Memory control unit

MDI	Memory directory indicator. The MDI bit specifies the current scope of the data (local versus global).
MEM	Memory
MEMCTL	Memory control
MEMCTLCLKI	Memory controller interface clock
MEMINT	Memory interface
MEMINTCLKO	Memory interface clock
MFSI	Master flexible service interface
MHz	Megahertz
MIB	Memory interface bolt-on. Enables the programmable PowerPC-lite engine (PPE) to access its local memory and pervasive interconnect bus (PIB) interface.
MISO	Master input/slave output
MISR	Multiple Input Shift Register
MMIO	Memory-mapped input/output. Refers to the mapping of the address space required by an I/O device for Load or Store operations into the system's address space.
MOSI	Master output/slave input
MPE	Mark placed error
MPR	Multipurpose Register
MPW	Modify pulse width
MR7	Mode Register 7
MRS	Mode register set
MSB	Most-significant byte
MSGSND	Message send
MSR	Machine State Register
MT/s	Megatransfers per second
MTMSR	Move to Machine State Register instruction
MTSPR	Move to Special Purpose Register instruction
MULT	Multiplier
Multiple ranks	More than one rank of memory modules, where the data buses from each rank are connected to a common data bus of a single port. Data bus connections have multiple drops equal to the number of ranks attached. When more than one rank exists, this memory is depth-expanded memory.
MUX	Multiplexer
N/A	Not applicable
N/M	Memory command throttling mechanism specifying how many (N) commands are allowed to be issued to memory within every M-wide time window.
N/P	N-channel or p-channel transistor type

N1L	The name of a type of latch
NA	Not applicable
NACK	Negative acknowledgment
NBTI	Negative bias temperature instability
NC	Not connected; that is, the data cannot be written or read by that access.
NCE	New correctable error
NCF	NVIDIA® NVLink™ configuration fatal
NCLK	Nest clock
NCU	Noncacheable unit
NCX	Same as NC, but unstable (can be changed functionally)
NFET	Negative field-effect transistor
NHTM	Nest hardware trace macro
NM	See N/M.
NMMU	Nest memory management unit
NOP	No operation. A single-cycle operation that does not affect registers or generate bus activity.
NPU	NVLink processing unit
NVF	NVLink fatal
NVLD	Non-valid read/write data address
NVT	NFET threshold voltage
NX	Nest accelerator
OCB	On-chip controller (OCC) control bridge
OCC	On-chip controller. Provides power and thermal management, power cap enforcement, over-temperature protection, and low-power mode management.
OCCERRPT	OCC Error Reporting Register
OCI	On-chip-controller interface. Interface used by power management.
ODAT	Odd data
ODT	On-die termination
OE	Output enable
OEAR	OCI Error Address Register
OESR	OCI Error Status Register
OF	Open firmware
OHA	On-chiplet hardware assist
OISR	OCC Interrupt Source Register
OITR	OCC Interrupt Type Register

OJCFG	OCC JTAG Configuration Register
OJIC	OCC JTAG Instruction and Control Register
OJSTAT	OCC JTAG Status Register
OJTDI	OCC JTAG TDI Register
OOB	Out-of-band bus
OPB	On-chip peripheral bus
OPCG	On-product clock generator
OPCGGO	On-product clock generator “GO” signal
OR write	Current register content is ORed with write data and the result is stored in the register (access type WO_OR/WOX_OR).
OS	1. Open source 2. Operating system
OSC	Oscillator
OSCSW	Oscillator switch
OTP	One-time programmable
OTPROM	One-time programmable read-only memory
p2s	Parallel-to-serial machine
PBA	1. Pending bit array 2. Per buffer addressability 3. Power management processor bus interface 4. Power bus access (used by power management)
PBAX	PBA messaging
PC	1. Performance counter 2. Personal computer 3. Pervasive core unit 4. PHY control
PCB	1. Pervasive control bus. Processor logic that provides a generic, modular structure for communication between pervasive (glue logic between chiplets) elements. The PCB is used for read and full write access. 2. Printed circuit board
PCBIF	Pervasive control bus interface
PCBMS	PCB multiplexer
PCBSLAVE	Pervasive control bus slave macro
PCI	Peripheral Component Interconnect. An all-encompassing term referring to conventional PCI, PCI-X, and PCI Express.
PCIEX	Peripheral Component Interface Express
PCIS	The synchronous part of the PCI domain
PCLK	Processor clock
PD	1. Power down 2. Presence detect
PDA	Per DRAM addressability

PDR	Power Down Register
PE	1. Parity error 2. Partitionable endpoint. The smallest entity that can be partitioned in endpoint partitioning. 3. Product engineering
PEC	PCI Express controller
PECE	Power-savings exit control enable
PECESR	PECE Sample Register
PERCAL	Periodic calibration
PERV	Pervasive
PF	1. Pad fill keyword 2. Physical function. The physical function of an IOV adapter. For more information, see the PCI-SIG *I/O Virtualization (IOV) Specifications*. 3. Prefetch machine
PFET	Positive field-effect transistor
phase rotator step	Phase rotators are used extensively within the DDR PHY to adjust delays of signals. Each phase rotator has 128 phase-rotator steps in a clock period. Therefore, delay values, or phase-rotator settings, have a granularity of 1/128 of a clock period.
PHB	1. PCIe host bridge. An entity that attaches a PCIe bus to the system. 2. Power Systems host bridge
PHY	Physical layer
PHYP	Power hypervisor
PHYTOP	Physical layer top of hierarchy
PIB	Pervasive interconnect bus. A bus that provides access from masters through external interfaces and internal masters to common PIB attached slaves. The PIB is used for read and full write access.
PIB/LPC	Pervasive interconnect bus/low pin count
PIBMEM	Memory attached to the PIB bus and used by the self-boot engine (SBE)
PID	Process ID
PIG	Programmable interrupt generator
PIN	External C4 chip input pin
PIT	Programmable interval timer
plat	Pipeline staging latch
PLL	Phase-locked loop
PLLREG	Phase-Locked Loop Register
PM	Power management
PMC	1. Performance monitor counter 2. Power management control
PMCR	Power Management Control Register

PMCRS	Power Management Control Register shadow
PMISC	Pervasive miscellaneous
PMU	Performance monitor unit
POR	Power-on reset
port	A memory interface of variable width, consisting of an address/command bus and a data bus, connected to one or more ranks of memory. When multiple ranks are connected to a port, this memory is depth-expanded memory.
PPE	Programmable PowerPC-lite engine
PPM	1. Parts per million 2. PCB-slave power-management component
PPMPIG	PPM programmable interrupt generator
PR	1. Phase rotator 2. Privileged bit in the MSR (MSRPR)
PRBS	Pseudo-random binary sequence
PRD	Processor runtime diagnostic
PRE	Mnemonic for the DDR3 and DDR4 precharge command
PRESP	Processor response
PRPG	Pseudo-random pattern generator
PSC	Parallel-to-serial communication
PSCOM	Parallel-to-serial communication
PSCOMLE	Parallel-to-serial communication light edition
PSCR	Processor Stop Control Register
PSCRS	Processor Stop Control Register shadow
PSI	Processor support interface
PSRO	Performance sort-ring oscillator
PSU	Power supply unit
PUP	Pull-up
PURR	Processor Utilization Resource Register
PVREF	Precision voltage reference
PVT	Process voltage temperature
PVTN	Process voltage temperature N-type field effect transistor
PVTP	Process voltage temperature P-type field effect transistor
PW	Partial write
QACSR	Quad Analog Clock Status Register
QCSR	Quad Configuration Status Register
QFMR	Quad Frequency Measurement Register

QIDSR	Quad/Cache IVRM Dropout Sample Register
QMFR	Quad Frequency Measurement Register
QOS, QoS	Quality of service. This usually relates to a guarantee of minimum bandwidth for streaming applications.
QPMMR	Quad Power Management Mode Register
QPMMR[FSAFE]	A field in the QPMMR register to indicate the safe frequency to drop to in the event a heartbeat is lost.
QPPM	Quad PCB slave power management (cache)
R/W	Read/write
RA	Real address. An address for physical storage, which includes physical memory, local storage, and memory-mapped I/O registers. The maximum size of the real address space is 262 bytes.
RAM	1. Random-access memory 2. Resource allocation management
RAMDBG	A register that provides access to the PPE core's XIR3 debug register
RAMEDR	A register that provides access to the PPE core's XIR4 debug register
RAMGA	A register that provides access to the PPE core's XIR2 debug register
RAMRA	A register that provides access to the PPE core's XIR1 debug register
Rank	One or more memory modules that have a common command/address bus, a common chip select, and separate data bus connections. When more than one memory module exists, this memory is width-expanded memory.
Rank group	Up to four ranks of memory that have nearly identical timing characteristics such that the same DDR PHY delay and configuration values can be used to access all ranks. This configuration allows resources in the DDR PHY to be shared.
RAS	1. Reliability, availability, and serviceability. A combination of design methodologies, system policies, and intrinsic capabilities that, taken together, balance improved hardware availability with the costs required to achieve it. Reliability is the degree to which the hardware remains free of faults. Availability is the ability of the system to continue operating despite predicted or experienced faults. Serviceability is how efficiently and nondisruptively broken hardware can be fixed. 2. Row-address strobe
RASN	Row-address strobe (inverted)
RC	1. Read control 2. Root complex. Connects a PCIe bus into the system.
RCD	Register clock driver
RCD/LRDIM	Register clock driver/load-reduced dual in-line memory module
RCE	Retry CE: A correctable data error (CE) that occurs on the retry of a previous read.
RD	Read
RDATA	Read data
RDCLK	Read clock
RDDACK	Read acknowledgment

RDIMM	Registered dual in-line memory module
RDIV	Reference clock divide
RECR	Read ECC Control Register
REF	Mnemonic used for the DDR3 and DDR4 refresh command.
REFCLK	Reference clock
REG	Register
REGF	Register file
REPR	Array repair
REQ	Request
RFIR	Recoverable FIR
RISC	Reduced instruction set computing
RISCTRACE	A tool used to reconstruct a code flow from a hardware debug trace
RJR	Receiver random jitter
RLDRAM	Reduced latency dynamic random access memory
RLO	Read latency offset
RMW	Read-modify-write
RNG	Random number generator
RO	Read only
ROM	Read-only memory
ROX	Read only but unstable. Can be changed functionally. Hardware can change the value between reads of the register.
RRQ	Read reorder queue
RTL	Register transfer level
RTT	Requester ID (RID) translation table
RTY	Retry
RUN-N, RUNN	Run the engine for N cycles
RUNTIMECTRQ	Runtime counter facility
RW	Readable and writable
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. Any write to the address clears the bits regardless of value.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RWITM	Read with intent to modify
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.

RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
RX	Receive
RXBIST	Receive built-in self test
RXCTL	Receive control
SAB	Secure access bit
SBASE	SRAM base address in the core management engine (CME), used by the CME block copy engine (BCE)
SBE	1. Self-boot engine. Initializes the processor chip and then loads or invokes the hostboot IPL firmware base image. 2. State bit entry
SC	Store clean (transactional memory value before a speculative store)
SCAN	Refers to shifting groups of latch states internal to a chip to read or write them when functionally not in use.
SCE	Symbol mark corrected error
SCM	Single-chip module
SCOM	Serial communications. SCOM is used for read and full write access.
SCOM1	Serial communications 1. SCOM1 is used for AND write access.
SCOM2	Serial communications 2. SCOM2 is used for OR write access.
SDM	Secure debug mode
SE	1. Scan enable 2. Single-step trace enabled bit in the MSR (MSRSE)
SEC	Single error correction
SEEPROM	Serial electrically erasable programmable read-only memory. An EEPROM memory device that can only be read, but which can be reprogrammed by an external programmer. Note that the hostboot is able to initiate writes to SEEPROMS connected to the circuit board through a serial bus.
SEL	Select
SEQ	Sequencer
SG	Scan gate
SHA	Secure hash algorithm
SIB	Service interface bolt-on. Allows the GPE to communicate with the PIB and the I^2C interface.
SICR	Stop Interface Control Register
Single rank	One rank of memory modules, where all the data bus connections are wired point-to-point to the DDR PHY. The data bus connections include read data, write data, read clocks/strobes, and write clock/strobes.
SIR	Security Isolation Register. Similar to a Fault Isolation Register.

SISR	Stop Interface Status Register
SKEWADJ	Analog clock skew adjust macro
SLB	Segment lookaside buffer. This buffer is used to map an effective address to a virtual address.
SM	State machine
SMDR	Same master rank, different slave rank
SMP	Symmetric multiprocessing
SMT	1. Simultaneous multithreading 2. Surface mount
SN	Snoop machine
SNOE	Scan net optimization enhancement
SNOP	Start sync/wait step; no operation
SOI	Silicon-on-insulator
SP	Service processor
SPATTN	Special attention
SPCIF	Specification
SPI	Serial peripheral interface. Refers to a 4-wire, serial, full-duplex bus with masters and slaves. Commonly used to interface with sensors, control devices, and so on in embedded systems.
SPR	Special-purpose register
SPRD	Special-purpose register data
SPS	1. Steps per sync 2. Sleep Pstate
SPURR	Scaled Processor Utilization Resource Register
SRAM	Static random access memory
SRC	Service reference code
SRQ	Store reorder queue
STEP	Supplier test enablement program
STR	Self time refresh
SUE	Special uncorrectable error
SUE/UE	Special uncorrectable error/uncorrectable error
SW	Software
SYNC	Synchronize
SYS	System
SYSCLK	System clock
TB	Time base
TBD	To be determined

TC	Traffic class. In PCIe, this defines a priority between PCI transactions within a virtual channel (VC).
TCE	1. Translation control entry. Used to translate an I/O address page number to a real page number in system memory. 2. Two-symbol correctable error
TCK	JTAG clock; test clock
TDI	Test data in
TDM	1. Time division multiplexed 2. Time domain multiplexing
TDM command mode	A DDR PHY configuration that supports two ports that share a common address/command bus. The addresses and commands for both ports are time division multiplexed on the common address/command bus. Individual chip selects select which ranks respond to a given address/command. Ranks connected to different ports can be selected to respond to the same command.
TDO	Test data out
TDR	1. Translation control entry (TCE) data random-access memory (RAM) 2. Time-domain reflectometry
TE	Test enable
TFMR	Time Facility Management Register
THD	Thread
TI	Terminate immediately
TID	Thread ID
TLB	Translation lookaside buffer. An on-chip cache that translates virtual addresses (VAs) to real addresses (RAs). A TLB caches page-table entries for the most recently accessed pages, thereby eliminating the necessity to access the page table from memory during load-store operations.
TLBI	Translation lookaside buffer invalidate
TLBIE	Translation lookaside buffer invalidate entry instruction
TM	Transactional memory
TMR	Timer
TMS	Test mode select
TOD	Time of day
TPM	1. Top of peripheral memory 2. Trusted platform module
TPMD	Trusted platform module
tREFI	Refresh interval
TSV	Trans silicon via
TWSM	Table walk state machine
TX	Transmit
TXBIST	Transmit built-in self test

TXCTL	Transmit control
TZ	Tile zone
UDE	Unconditional debug event
UE	Uncorrectable error
UI	1. User interface 2. Unit interval
UL	Uplink
ULCCH	Uplink control channel
ULDCH	Uplink data channel
UMAC	User-mode access control
VAS	Virtual accelerator switchboard
VC	Virtual channel
VCC	Voltage supply
VCO	Voltage controlled oscillator
VCTR	VDM Count Threshold Register
VDCR	VDM Droop Count Register
VDM	Voltage droop monitor
VDSR	VDM Data Sample Register
VECR	VDM Event Count Register
VGA	1. Variable gain amplifier 2. Video graphics array
VHDL	VHSIC hardware description language
VHSIC	Very high speed integrated circuit
VID	Voltage identification
VIO	Voltage I/O
VITL	Vital
VMEAS	Voltage measurement
VMX	Vector multimedia extension
VNCR	VDM Non-Droop Count Register
VPAD	Pad voltage
VPROTH	Voltage protect high
VREF	Voltage reference
VREG	1. Voltage regulator 2. Voltage regulation
VRM	Voltage regulator module
VSU	Vector scalar unit
VT	Voltage control

WAT	Workaround macro
WC	1. Worst case 2. Write control
Wdata, WDATA	Write data
WDF	Designator for the memory controller's read-modify-write data flow and associated control.
WDFCFG	Configuration facilities for the WDF logic.
WECR	Write ECC Control Register
WEN	Write enable
WLO	Write latency offset
WO	Write only
WO_1P	Write only; one pulse length is equal to one register cycle.
WO_AND	Same as RW_WAND, but the bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but the bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but the bits are write-only.
WO_n_mP	Write only pulsed. A write of ‘1’ creates a pulse for a minimum of n register clocks and a maximum of m register clocks. A read returns ‘0’.
WO_nP	Write only pulsed. A write of ‘1’ creates a pulse for n register clocks. A read returns ‘0’.
WO_OR	Same as RW_WOR, but the bits are write-only.
WO_SETPART	Same as RW_WSETPART, but the bits are write-only.
WOF	1. Who's on first? 2. Workload optimized frequency
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.
WR	Write
WRCNTL	Write control
WRD	Write data. Designator for the portion of the memory controller's write data flow that generates the outbound memory ECC check bits.
WRQ	Write reorder queue
WRT	Designator for the memory controller's write data flow.
WRTCFG	Configuration facilities for the memory controller's WRT logic.

XBUS	Note: This is not really an acronym but a name (X bus).
XCR	External Control Register
XER	Fixed-Point Exception Register
XFIR	X Fault Isolation Register
XIR	1. External Interface Register 2. External interface to the PPE IR Register
XIVR	External Interrupt Vector Register for the OCC (405)
XOR	Exclusive OR
XSCOM	Extended SCOM. Special, fast SCOM that allows the processor cores to directly SCOM the PIB. Processor buses must be enabled to the slave processor chips for the master processor to XSCOM them.
XSR	External Status Register for PPE
XSTOP	Checkstop
ZCAL	Impedance (Z) calibration
ZCNTLCPURO	Periodic impedance (Z) calibration
ZCONTROL	Impedance (Z) control
ZQ	I/O impedance
ZQCal	I/O impedance calibration

1. POWER9 Processor Overview

The POWER9 processor is a superscalar symmetric multiprocessor designed for use in servers and large-cluster systems. It uses 14 nm technology with 17 metal layers. The POWER9 processor can have up to 24 cores enabled on a single chip. It supports direct-attach memory. It supports a maximum symmetric multiprocessing (SMP) size of two sockets and is targeted for scale-out workloads. Each POWER9 core supports up to four threads using simultaneous multithreading (SMT). The SMT can be dynamically tuned so that each core has one, two, or four threads

This document describes the POWER9 registers and related accessing method.

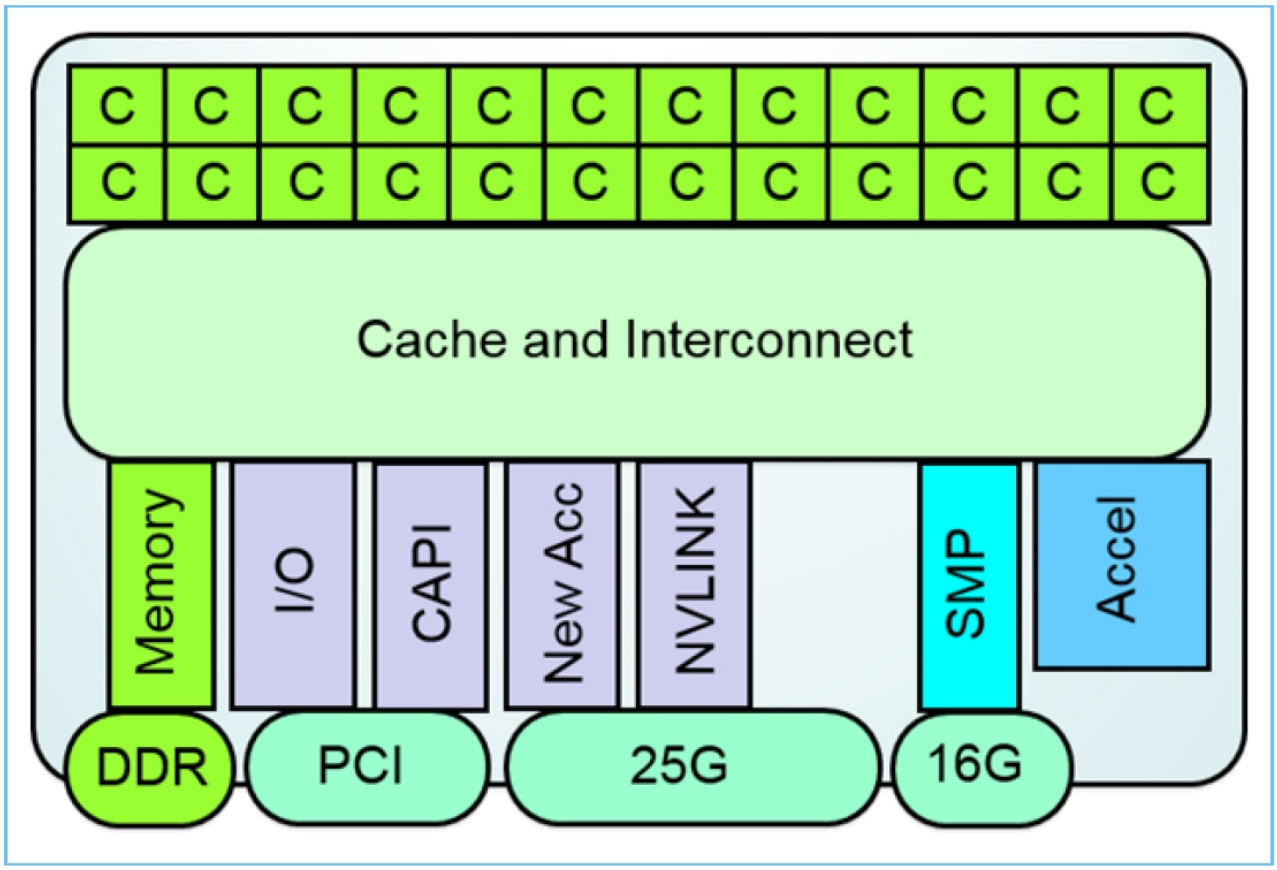
1.1 POWER9 Processor Features

Figure 1 on page 32 shows the POWER9 processor, which supports the following features:

- Twenty-four POWER9 chiplets, which contain one POWER9 core, an L2 cache, and an L3 cache.
  - On-chip accelerators.
  - Coherent Accelerator Processor Interface (CAPI), which enables an FPGA or ASIC to connect coherently to the POWER9 processor SMP interconnect via the PCIe bus.
  - On-chip compression, encryption, and data movement initiated by the hypervisor, GZIP engine, or nest MMU to enable user access to all accelerators.

    - In-core user invocation of encryption using the Advanced Encryption Standard (AES) and the secure hash algorithm (SHA).
- Two memory controllers that support direct-attached DDR4 memory:
    - Support four direct-attach memory buses (DDR 0, 1, 6, and 7).
    - Support ×4 and ×8, 4 - 16 Gb DRAMs and 3D stacked DRAMs.
    - Support registered dual in-line memory modules (RDIMMs) and lad-reduced dual in-line memory modules (LRDIMMs).
- Processor SMP interconnect.
    - Supports one inter-node SMP X bus link.
    - Maximum two-socket SMP.
- Three PCIe controllers (PEC) with 16 lanes of PCI Express Gen 4 I/O.
    - PEC0: one ×16 lanes.
    - PEC1: two ×8 lanes (bifurcation).
    - PEC2: one ×16 lane mode, two ×8 lanes (bifurcation), or one ×8 lane and two ×4 lanes (trifurcation).
    - PEC0 and PEC2 support CAPI 2.0.
- Power management.
- Pervasive interface.

Figure 1: POWER9 Processor General Diagram



1.2 POWER9 Processor Pervasive Structure

Figure 2 on page 33 shows the POWER9 chip from a pervasive-centric point of view. The different colors denote different chiplets from a pervasive perspective. Each chiplet consists of one global clock controller and multiple local clock controllers, which enable a chiplet to service multiple different clock regions. Multiple clock regions can run at the same frequency, but can be turned off independently. The chip contains 24 cores capable of running at different frequencies. The pervasive logic supports these 24 cores.

Figure 2: POWER9 Processor from a Pervasive Point of View

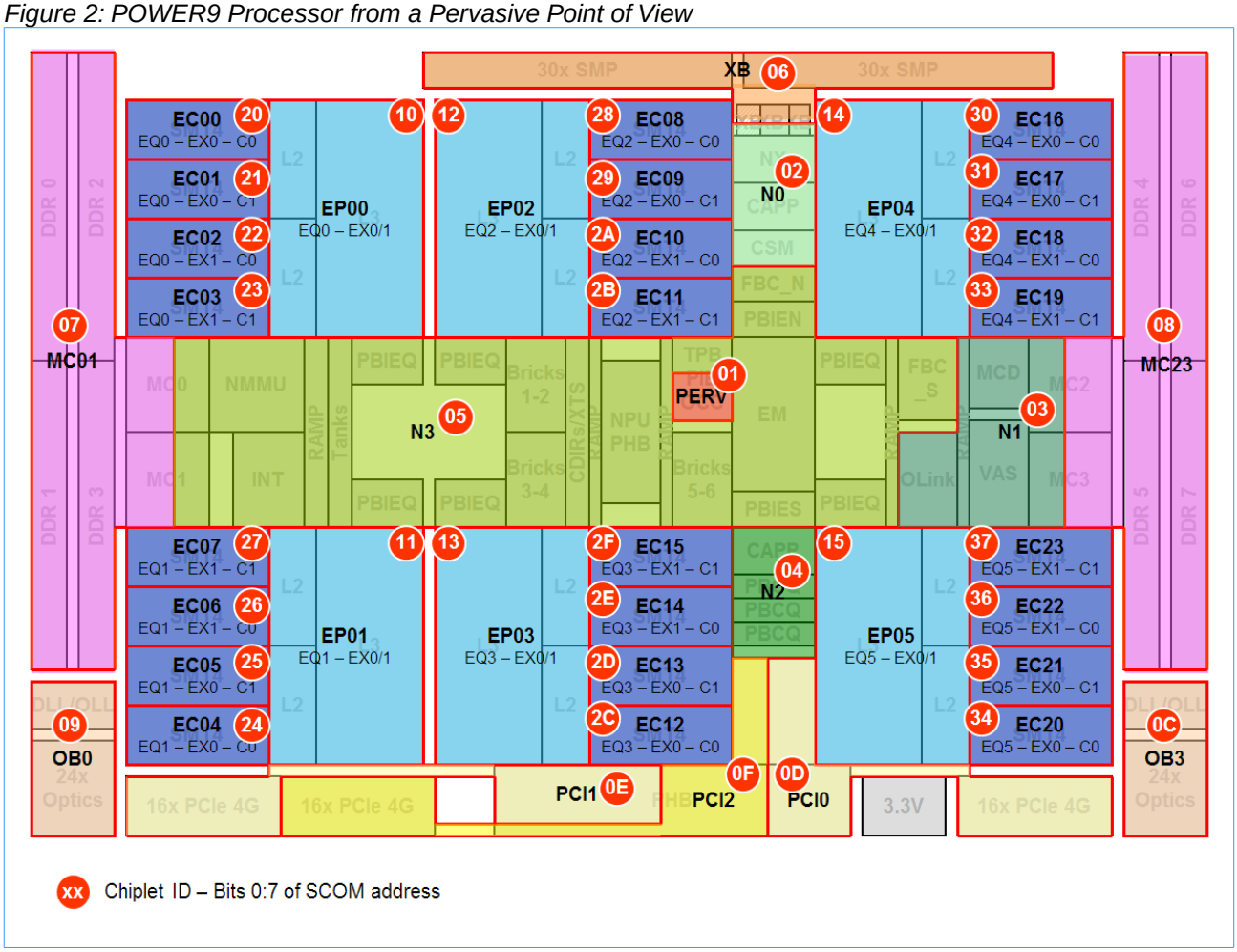
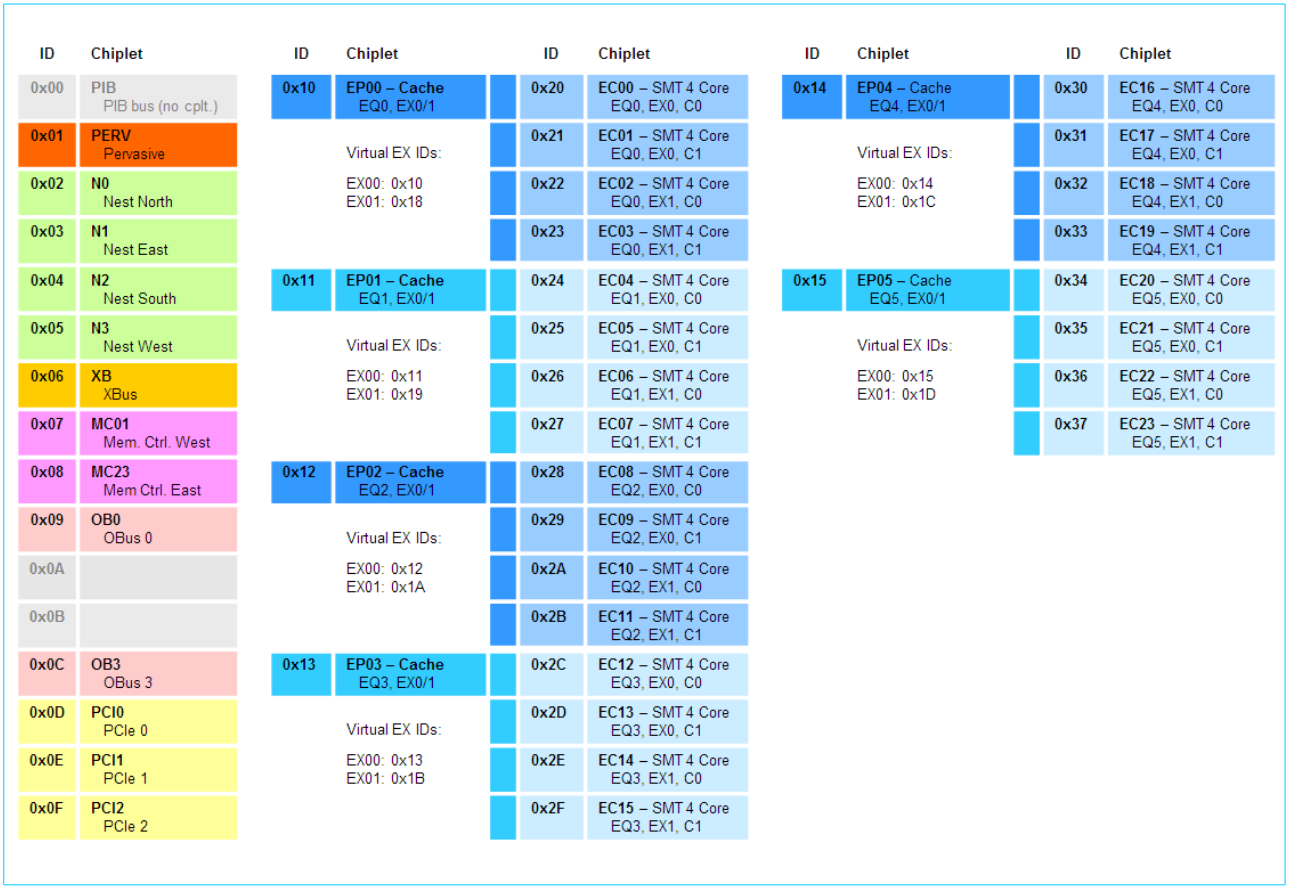


Figure 3 on page 34 lists the chiplets in the design, and their controlling pervasive blocks, by chiplet ID.

Figure 3 POWER9 Chiplets and IDs



ID	Chiplet
0x00	PIB PIB bus (no cplt.)
0x01	PERV Pervasive
0x02	N0 Nest North
0x03	N1 Nest East
0x04	N2 Nest South
0x05	N3 Nest West
0x06	XB XBus
0x07	MC01 Mem. Ctrl. West
0x08	MC23 Mem Ctrl. East
0x09	OB0 OBus 0
0x0A	
0x0B	
0x0C	OB3 OBus 3
0x0D	PCI0 PCIe 0
0x0E	PCI1 PCIe 1
0x0F	PCI2 PCIe 2

ID	Chiplet	ID	Chiplet
0x10	EP00 – Cache EQ0, EX0/1	0x20	EC00 – SMT 4 Core EQ0, EX0, C0
	Virtual EX IDs: EX00: 0x10 EX01: 0x18	0x21	EC01 – SMT 4 Core EQ0, EX0, C1
		0x22	EC02 – SMT 4 Core EQ0, EX1, C0
		0x23	EC03 – SMT 4 Core EQ0, EX1, C1
0x11	EP01 – Cache EQ1, EX0/1	0x24	EC04 – SMT 4 Core EQ1, EX0, C0
	Virtual EX IDs: EX00: 0x11 EX01: 0x19	0x25	EC05 – SMT 4 Core EQ1, EX0, C1
		0x26	EC06 – SMT 4 Core EQ1, EX1, C0
		0x27	EC07 – SMT 4 Core EQ1, EX1, C1
0x12	EP02 – Cache EQ2, EX0/1	0x28	EC08 – SMT 4 Core EQ2, EX0, C0
	Virtual EX IDs: EX00: 0x12 EX01: 0x1A	0x29	EC09 – SMT 4 Core EQ2, EX0, C1
		0x2A	EC10 – SMT 4 Core EQ2, EX1, C0
		0x2B	EC11 – SMT 4 Core EQ2, EX1, C1
0x13	EP03 – Cache EQ3, EX0/1	0x2C	EC12 – SMT 4 Core EQ3, EX0, C0
	Virtual EX IDs: EX00: 0x13 EX01: 0x1B	0x2D	EC13 – SMT 4 Core EQ3, EX0, C1
		0x2E	EC14 – SMT 4 Core EQ3, EX1, C0
		0x2F	EC15 – SMT 4 Core EQ3, EX1, C1

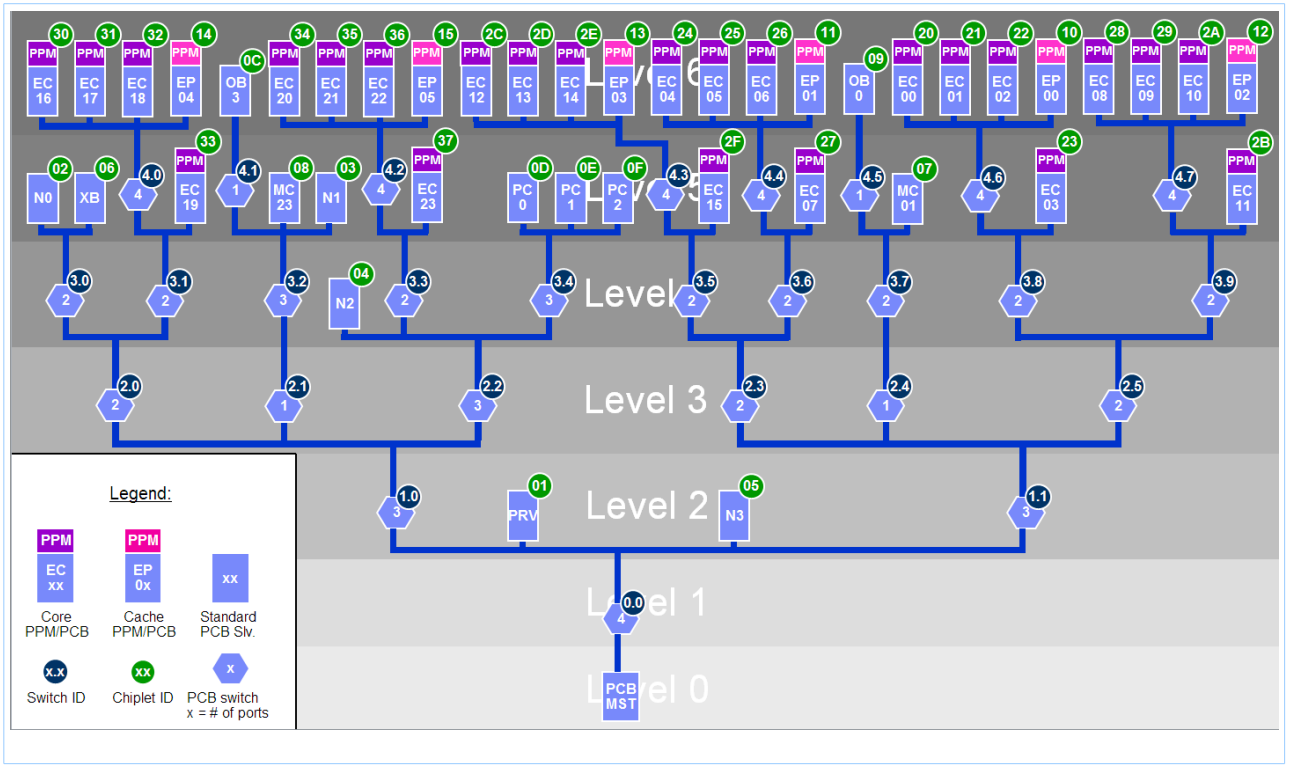
ID	Chiplet	ID	Chiplet
0x14	EP04 – Cache EQ4, EX0/1	0x30	EC16 – SMT 4 Core EQ4, EX0, C0
	Virtual EX IDs: EX00: 0x14 EX01: 0x1C	0x31	EC17 – SMT 4 Core EQ4, EX0, C1
		0x32	EC18 – SMT 4 Core EQ4, EX1, C0
		0x33	EC19 – SMT 4 Core EQ4, EX1, C1
0x15	EP05 – Cache EQ5, EX0/1	0x34	EC20 – SMT 4 Core EQ5, EX0, C0
	Virtual EX IDs: EX00: 0x15 EX01: 0x1D	0x35	EC21 – SMT 4 Core EQ5, EX0, C1
		0x36	EC22 – SMT 4 Core EQ5, EX1, C0
		0x37	EC23 – SMT 4 Core EQ5, EX1, C1

1.2.1 Pervasive Control Bus and Pervasive Interconnect Bus

The pervasive control bus (PCB) provides a generic, modular structure for communication between the pervasive elements. The PCB provides the POWER9 pervasive unit with an interface to the pervasive functions on the various POWER9 processor chiplets. For this purpose, a PCB master is implemented inside the POWER9 pervasive logic. This master, by means of the PCB interconnect, communicates with the PCB slave located in each chiplet. The PCB master sends commands, such as read and write requests, to the PCB slaves. The slaves, on the other hand, respond to the commands received from the master, and also notify the master of interrupts that occur in the slave's chiplet.

Figure 4 on page 35 shows the PCB structure that services all the chiplets.

Figure 4: Pervasive Control Bus Structure and Chiplets



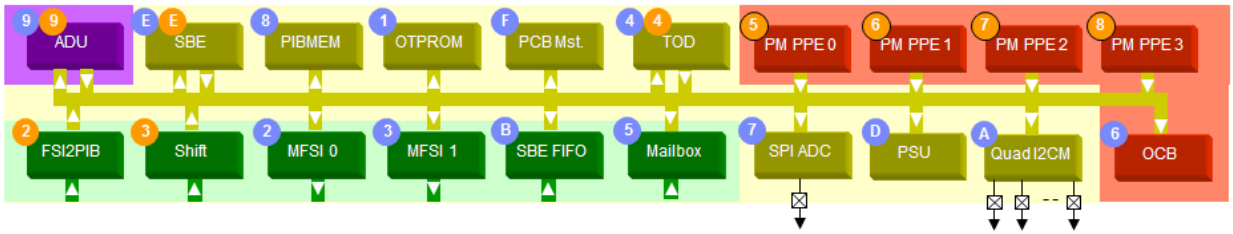
The PCB switch features two independent channels for the PCB topology. The downstream input channel provides a fan-out to the downstream output ports, which are connected either to another switch in a multistage topology or directly to a slave. The upstream output channel is arbitrated between requests from the upstream input ports, which is the case when replying to a multicast operation.

The pervasive interconnect bus (PIB) provides access from the masters via the external interfaces and the internal masters to the common PIB-attached slaves. *Figure 5* on page 36 shows the PIB masters and slaves.

- The external interfaces include the I²C slave and the flexible service interface (FSI).
- The internal masters include the FSI shift engine, FSI2PIB, and the XSCOM/alter-display unit (ADU).
- The PIB-attached slaves include the PCB master, PIB2OPB, general-purpose register (GPR), I²C master, and the I²C slave.

The PIB facilitates transactions between multiple PIB masters and multiple PIB slaves. For each transaction, the PIB arbiter establishes a point-to-point connection between a single requesting master and a single slave uniquely addressed by the master.

Figure 5: PIB Masters and Slaves



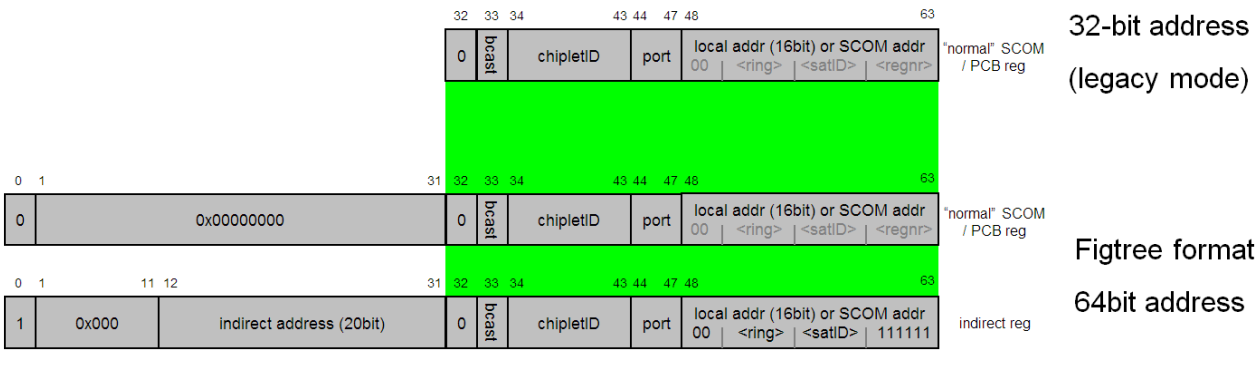
- Pervasive Interconnect Bus (PIB):
  - 9 PIB master (2x CFAM, 4x OCC, 1x Bridge, 2x PIB domain)
  - 13 PIB slaves (4x CFAM, 1x OCC, 1x Bridge, 7x PIB domain)
- Pervasive Connect Bus (PCB):
  - Root in PIB (PCB Master)
  - Provides tree-like switch network to all chiplets
  - 30 Chiplets defined as of now
- PIB & PCB domain run at 465 - 600 MHz (Nest Clock 4:1)
- PIB & PCB domain get initialized (scan0 & clock start) by the pervasive clock controller which is controlled by the new *CFAM Boot Sequencer* (CBS)
- PIB & PCB are trusted domains – no direct access from Service Elements (FSP/BMC) in secured chips

ID #	Master	Domain	Slave	Domain
0x0	LBUS		LBUS	
0x1	free		OTPROM	pib
0x2	FSI2PIB	cfam	FSI Master 0	cfam
0x3	FSISHIFT	cfam	FSI Master 1	cfam
0x4	TOD	pib	TOD	pib
0x5	PM PPE 0	occ	FSI Mailbox	cfam
0x6	PM PPE 1	occ	OCI Bridge	occ
0x7	PM PPE 2	occ	SPI ADC	pib
0x8	PM PPE 3	occ	PIBMEM	pib
0x9	ADU	bridge	ADU	bridge
0xA	free		I2C master	pib
0xB	free		SBE FIFO	cfam
0xC	free		free	
0xD	free		PSU	pib
0xE	SBE	pib	SBE	pib
0xF	CME		PCB Master	pib

1.2.2 PCB Address Space

Figure 6 shows the address format used to access all pervasive facilities. The legacy 32-bit format is shown as well as the translation in the 64-bit format (add 32 zeros as the most-significant bits). The new extended address format that enables access to the large address SCOM satellites (up to 31 bits) is also listed. The most significant bit is '1' in that case.

Figure 6: Common Pervasive Address Map Format

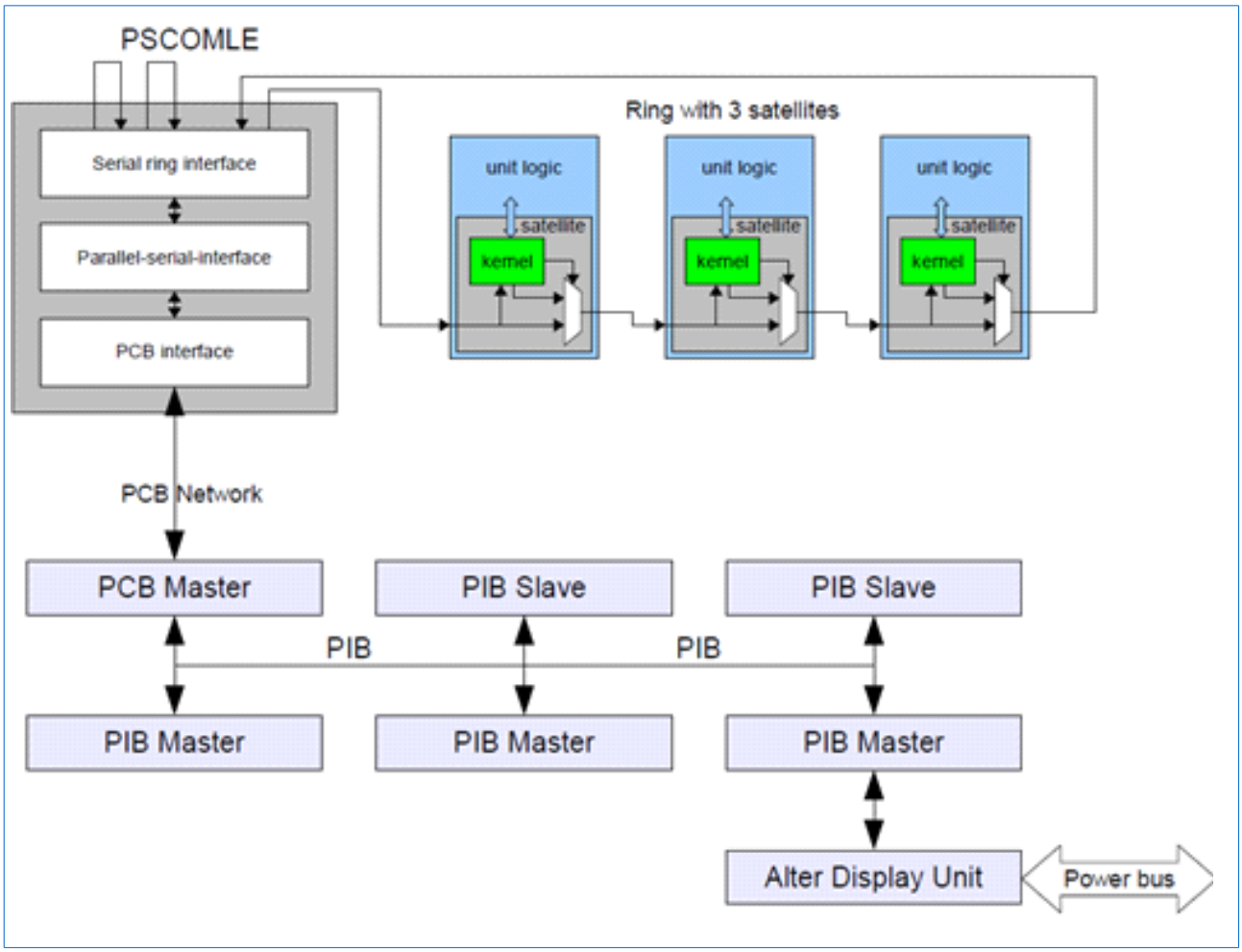


1.2.3 SCOM

SCOM provides a serial communication infrastructure within the pervasive infrastructure. The central control unit is referred to as the parallel-to-serial communication light edition (PSCOMLE). It controls all communication with respect to the serial interface. The end-point nodes are referred to as satellites. A satellite is located in the unit logic. The satellites are connected to the PSCOMLE and each other in a physical ring. The PSCOMLE can support up to 15 rings. Each ring has a local address space that is used to address an individual satellite in a given ring and within the unit logic that uses the satellite with a dedicated register. If this address space is not sufficient, an indirect address can be used to further extend the address range within a satellite.

Figure 7 shows the principal pervasive infrastructure to access the SCOM-enabled registers in a chiplet. A SCOM access can be initiated from the masters connected to the PIB, such as the ADU. SCOM satellites are distributed inside the chiplet and are organized in serial SCOM rings. For each chiplet, there is one instance of the PSCOMLE macro that receives the request from the PCB network.

Figure 7: Infrastructure to Access SCOM Registers

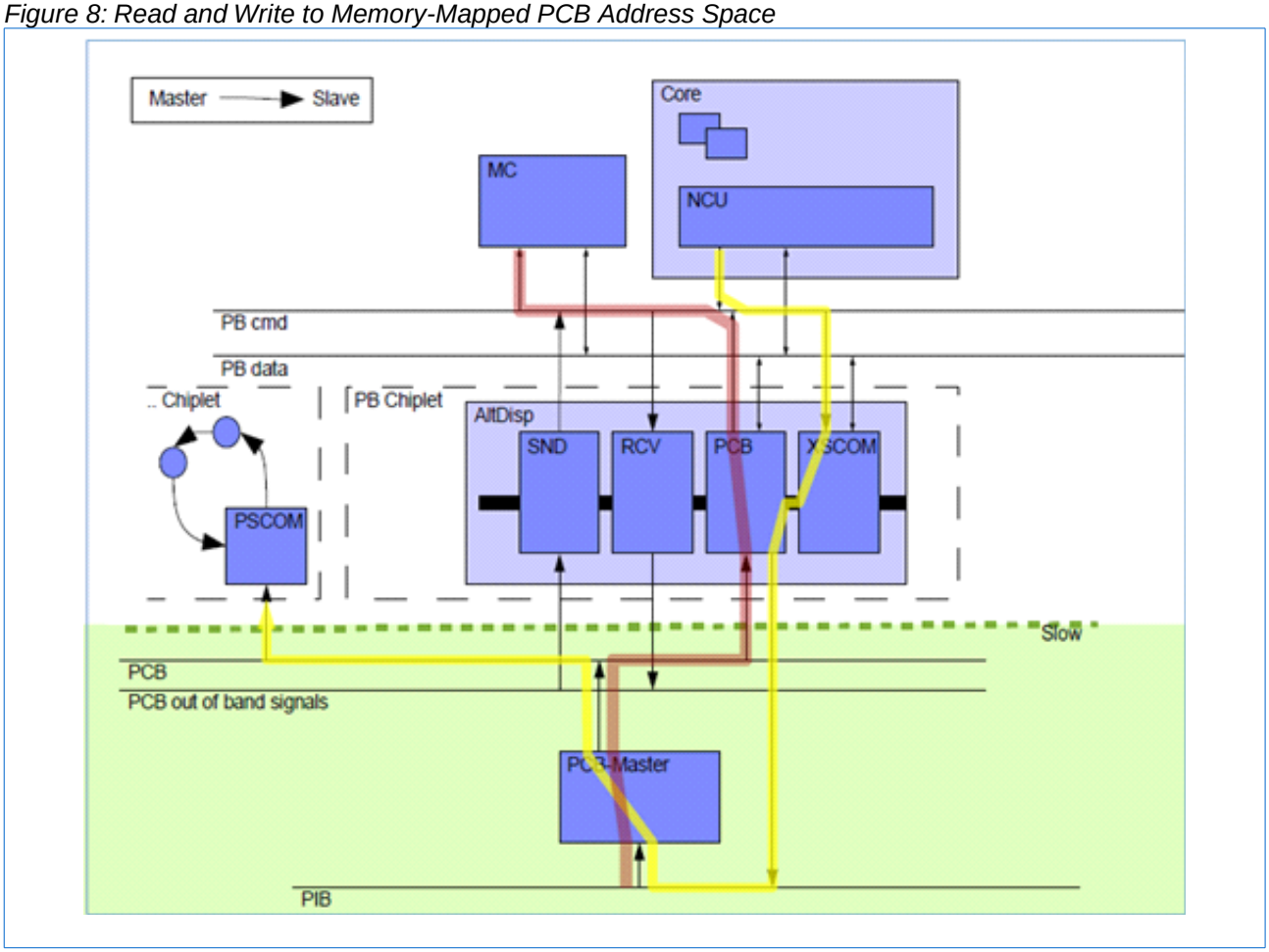


1.2.4 XSCOM

The alter/display unit (ADU) acts as a bridge between the processor bus and the PCB. The ADU enables access to any memory-mapped PIB/PCB register in the system by external SCOM (XSCOM.) The XSCOM is responsible for handling memory-mapped PIB/PCB register access, which originates from the non-pervasive logic of the processor. For example, a read/write operation can originate from a processor core and is presented on the processor bus by the non-cacheable unit (NCU). The alter/display unit XSCOM routes the request through a PIB master to the PIB. The PIB master notifies the ADU when it is complete. For a read operation, the ADU routes the resulting data to the processor bus, which sends the information back to the requester (in the example, the NCU). It then arrives at the core. The XSCOM memory-mapped address range, by default, locates at 0x0003FC0000000000.

Figure 8 shows an example of a read and write to a memory-mapped PCB address space.

Figure 8: Read and Write to Memory-Mapped PCB Address Space



1.3 Register Accessing Type

A register can have multiple addresses, with a different address for different chiplets. The types of access permitted can vary by chiplets. *Table 1* on page 39 summarizes the valid register access types.

Table 1: Register Access Types

Access Type	Description
NC	Not connected; the data cannot be written or read by that access.
NCX	Same as NC, but unstable. Can be changed functionally.
RO	Read only. Only to be used if a bit is tied. Status bits should be ROX.
ROX	Same as RO, but unstable. Can be changed functionally.
ROX_CLRPART	Same as ROX, but a read access clears the bits after they have been accessed.
RW	Readable and writable.
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. A write of a ‘1’ clears the bit. A write of a ‘0’ does nothing.
RW_WCLRPART	Readable and writable. Any write to the address clears the bits regardless of the value.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RW_WSETPART	Readable and writable. Any write to the address sets the bits regardless of the value.
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.
RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
WO	Same as RW, but bits are write-only.
WO_1P	Write only; one pulse length is equal to one register cycle.
WO_AND	Same as RW_WAND, but bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but bits are write-only.
WO_n_mP	Write-only pulsed. A write of ‘1’ creates a pulse for a minimum of n register clocks and a maximum of m register clocks. A read returns ‘0’.
WO_nP	Write-only pulsed. A write of ‘1’ creates a pulse for n register clocks. A read returns ‘0’.
WO_OR	Same as RW_WOR, but bits are write-only.
WO_SETPART	Same as RW_WSETPART, but bits are write-only.
WOX	Same as WO, but unstable. Can be changed functionally.
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.

Access Type	Description
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.

2. TP Chiplets

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
BRIDGE.AD.ADS_XSCOM_CMD_REG	0x000000000009001C	384
BRIDGE.AD.ADU_HANG_DIV_REG	0x0000000000090050	390
BRIDGE.AD.ALTD_ADDR_REG	0x0000000000090000	377
BRIDGE.AD.ALTD_CMD_REG	0x0000000000090001	378
BRIDGE.AD.ALTD_DATA_REG	0x0000000000090004	380
BRIDGE.AD.ALTD_OPTION_REG	0x0000000000090002	379
BRIDGE.AD.ALTD_STATUS_REG	0x0000000000090003	379
BRIDGE.AD.FORCE_ECC_REG	0x000000000009000D	380
BRIDGE.AD.IO_DATA_REG	0x0000000000090030	388
BRIDGE.AD.LPC_BASE_REG	0x0000000000090040	389
BRIDGE.AD.LPC_CMD_REG	0x0000000000090041	389
BRIDGE.AD.LPC_DATA_REG	0x0000000000090042	389
BRIDGE.AD.LPC_STATUS_REG	0x0000000000090043	390
BRIDGE.AD.PIB_CMD_REG	0x0000000000090031	388
BRIDGE.AD.PIB_DATA_REG	0x0000000000090032	388
BRIDGE.AD.PIB_RESET_REG	0x0000000000090033	389
BRIDGE.AD.RCV_ERRLOG0_REG	0x0000000000090022	386
BRIDGE.AD.RCV_ERRLOG1_REG	0x0000000000090023	387
BRIDGE.AD.SND_MODE_REG	0x0000000000090021	385
BRIDGE.AD.SND_STAT_REG	0x0000000000090020	384
BRIDGE.AD.TOD_CMD_REG	0x000000000009002A	388
BRIDGE.AD.TOD_DATA_RCV_REG	0x0000000000090029	387
BRIDGE.AD.TOD_DATA_SND_REG	0x0000000000090028	387
BRIDGE.AD.XSCOM_BASE_REG	0x0000000000090010	381
BRIDGE.AD.XSCOM_DAT0_REG	0x000000000009001E	384
BRIDGE.AD.XSCOM_DAT1_REG	0x000000000009001F	384
BRIDGE.AD.XSCOM_ERR_REG	0x0000000000090013	382
BRIDGE.AD.XSCOM_LOG_REG	0x0000000000090012	382
BRIDGE.AD.XSCOM_MODE_REG	0x0000000000090011	381
BRIDGE.AD.XSCOM_RCVED_STAT_REG	0x0000000000090018	383
TP.TPCHIP.OCC.OCI.GPE0.GPE.MIB.MIB_XIICAC	0x0000000000060019	203
TP.TPCHIP.OCC.OCI.GPE0.GPE.MIB.MIB_XIMEM	0x0000000000060017	202
TP.TPCHIP.OCC.OCI.GPE0.GPE.MIB.MIB_XISGB	0x0000000000060018	203
TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIDBGPRO	0x0000000000060015	201
TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIRAMDBG	0x0000000000060013	200
TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIRAMEDR	0x0000000000060014	201
TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIRAMGA	0x0000000000060012	200
TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIRAMRA	0x0000000000060011	200
TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIXCR	0x0000000000060010	199
TP.TPCHIP.OCC.OCI.GPE0.GPEDBG	0x0000000000060002	197
TP.TPCHIP.OCC.OCI.GPE0.GPEIVPR	0x0000000000060001	196
TP.TPCHIP.OCC.OCI.GPE0.GPEMACR	0x0000000000060004	198

Mnemonic	Address	Page
TP.TPCHIP.OCC.OCI.GPE0.GPENXIXCR	0x0000000000060010	199
TP.TPCHIP.OCC.OCI.GPE0.GPESTR	0x0000000000060003	198
TP.TPCHIP.OCC.OCI.GPE0.GPETSEL	0x0000000000060000	196
TP.TPCHIP.OCC.OCI.GPE0.GPEXIEDR	0x0000000000060023	206
TP.TPCHIP.OCC.OCI.GPE0.GPEXIIAR	0x0000000000060025	207
TP.TPCHIP.OCC.OCI.GPE0.GPEXIIR	0x0000000000060024	206
TP.TPCHIP.OCC.OCI.GPE0.GPEXISPRG0	0x0000000000060022	206
TP.TPCHIP.OCC.OCI.GPE0.GPEXIXCR	0x0000000000060020	204
TP.TPCHIP.OCC.OCI.GPE0.GPEXIXSR	0x0000000000060021	204
TP.TPCHIP.OCC.OCI.GPE0.MIB_XIDCAC	0x000000000006001A	204
TP.TPCHIP.OCC.OCI.GPE1.GPE.MIB.MIB_XIICAC	0x0000000000062019	214
TP.TPCHIP.OCC.OCI.GPE1.GPE.MIB.MIB_XIMEM	0x0000000000062017	213
TP.TPCHIP.OCC.OCI.GPE1.GPE.MIB.MIB_XISGB	0x0000000000062018	214
TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIDBGPRO	0x0000000000062015	212
TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIRAMDBG	0x0000000000062013	211
TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIRAMEDR	0x0000000000062014	212
TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIRAMGA	0x0000000000062012	211
TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIRAMRA	0x0000000000062011	210
TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIXCR	0x0000000000062010	210
TP.TPCHIP.OCC.OCI.GPE1.GPEDBG	0x0000000000062002	207
TP.TPCHIP.OCC.OCI.GPE1.GPEIVPR	0x0000000000062001	207
TP.TPCHIP.OCC.OCI.GPE1.GPEMACR	0x0000000000062004	209
TP.TPCHIP.OCC.OCI.GPE1.GPENXIXCR	0x0000000000062010	210
TP.TPCHIP.OCC.OCI.GPE1.GPESTR	0x0000000000062003	208
TP.TPCHIP.OCC.OCI.GPE1.GPETSEL	0x0000000000062000	207
TP.TPCHIP.OCC.OCI.GPE1.GPEXIEDR	0x0000000000062023	216
TP.TPCHIP.OCC.OCI.GPE1.GPEXIIAR	0x0000000000062025	217
TP.TPCHIP.OCC.OCI.GPE1.GPEXIIR	0x0000000000062024	217
TP.TPCHIP.OCC.OCI.GPE1.GPEXISPRG0	0x0000000000062022	216
TP.TPCHIP.OCC.OCI.GPE1.GPEXIXCR	0x0000000000062020	215
TP.TPCHIP.OCC.OCI.GPE1.GPEXIXSR	0x0000000000062021	215
TP.TPCHIP.OCC.OCI.GPE1.MIB_XIDCAC	0x000000000006201A	215
TP.TPCHIP.OCC.OCI.GPE2.GPE.MIB.MIB_XIICAC	0x0000000000064019	224
TP.TPCHIP.OCC.OCI.GPE2.GPE.MIB.MIB_XIMEM	0x0000000000064017	223
TP.TPCHIP.OCC.OCI.GPE2.GPE.MIB.MIB_XISGB	0x0000000000064018	224
TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIDBGPRO	0x0000000000064015	222
TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIRAMDBG	0x0000000000064013	221
TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIRAMEDR	0x0000000000064014	222
TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIRAMGA	0x0000000000064012	221
TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIRAMRA	0x0000000000064011	221
TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIXCR	0x0000000000064010	220
TP.TPCHIP.OCC.OCI.GPE2.GPEDBG	0x0000000000064002	218
TP.TPCHIP.OCC.OCI.GPE2.GPEIVPR	0x0000000000064001	217
TP.TPCHIP.OCC.OCI.GPE2.GPEMACR	0x0000000000064004	219
TP.TPCHIP.OCC.OCI.GPE2.GPENXIXCR	0x0000000000064010	220
TP.TPCHIP.OCC.OCI.GPE2.GPESTR	0x0000000000064003	219
TP.TPCHIP.OCC.OCI.GPE2.GPETSEL	0x0000000000064000	217
TP.TPCHIP.OCC.OCI.GPE2.GPEXIEDR	0x0000000000064023	227

Mnemonic	Address	Page
TP.TPCHIP.OCC.OCI.GPE2.GPEXIIAR	0x0000000000064025	228
TP.TPCHIP.OCC.OCI.GPE2.GPEXIIR	0x0000000000064024	227
TP.TPCHIP.OCC.OCI.GPE2.GPEXISPRG0	0x0000000000064022	227
TP.TPCHIP.OCC.OCI.GPE2.GPEXIXCR	0x0000000000064020	225
TP.TPCHIP.OCC.OCI.GPE2.GPEXIXSR	0x0000000000064021	225
TP.TPCHIP.OCC.OCI.GPE2.MIB_XIDCAC	0x000000000006401A	225
TP.TPCHIP.OCC.OCI.GPE3.GPE.MIB.MIB_XIICAC	0x0000000000066019	235
TP.TPCHIP.OCC.OCI.GPE3.GPE.MIB.MIB_XIMEM	0x0000000000066017	234
TP.TPCHIP.OCC.OCI.GPE3.GPE.MIB.MIB_XISGB	0x0000000000066018	235
TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIDBGPRO	0x0000000000066015	233
TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIRAMDBG	0x0000000000066013	232
TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIRAMEDR	0x0000000000066014	233
TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIRAMGA	0x0000000000066012	232
TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIRAMRA	0x0000000000066011	231
TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIXCR	0x0000000000066010	231
TP.TPCHIP.OCC.OCI.GPE3.GPEDBG	0x0000000000066002	228
TP.TPCHIP.OCC.OCI.GPE3.GPEIVPR	0x0000000000066001	228
TP.TPCHIP.OCC.OCI.GPE3.GPEMACR	0x0000000000066004	230
TP.TPCHIP.OCC.OCI.GPE3.GPENXIXCR	0x0000000000066010	231
TP.TPCHIP.OCC.OCI.GPE3.GPESTR	0x0000000000066003	229
TP.TPCHIP.OCC.OCI.GPE3.GPETSEL	0x0000000000066000	228
TP.TPCHIP.OCC.OCI.GPE3.GPEXIEDR	0x0000000000066023	237
TP.TPCHIP.OCC.OCI.GPE3.GPEXIIAR	0x0000000000066025	238
TP.TPCHIP.OCC.OCI.GPE3.GPEXIIR	0x0000000000066024	238
TP.TPCHIP.OCC.OCI.GPE3.GPEXISPRG0	0x0000000000066022	237
TP.TPCHIP.OCC.OCI.GPE3.GPEXIXCR	0x0000000000066020	236
TP.TPCHIP.OCC.OCI.GPE3.GPEXIXSR	0x0000000000066021	236
TP.TPCHIP.OCC.OCI.GPE3.MIB_XIDCAC	0x000000000006601A	236
TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJCFG	0x000000000006D004	349
TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJFRST	0x000000000006D007	349
TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJIC	0x000000000006D008	350
TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJSTAT	0x000000000006D00B	350
TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJTDI	0x000000000006D00C	351
TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJTDO	0x000000000006D00D	351
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_CCSR	0x000000000006C090	258
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G0ISR0	0x000000000006C064	251
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G0ISR1	0x000000000006C074	253
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G1ISR0	0x000000000006C065	251
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G1ISR1	0x000000000006C075	253
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G2ISR0	0x000000000006C066	251
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G2ISR1	0x000000000006C076	253
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G3ISR0	0x000000000006C067	252
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G3ISR1	0x000000000006C077	253
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCMD0A	0x000000000006C707	337
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCMD0B	0x000000000006C717	340
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCMD1A	0x000000000006C727	343
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCMD1B	0x000000000006C737	346
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL10A	0x000000000006C702	336

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TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL10B	0x000000000006C712	339
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL11A	0x000000000006C722	342
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL11B	0x000000000006C732	345
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL20A	0x000000000006C703	337
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL20B	0x000000000006C713	340
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL21A	0x000000000006C723	343
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL21B	0x000000000006C733	346
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLF0A	0x000000000006C700	335
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLF0B	0x000000000006C710	338
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLF1A	0x000000000006C720	341
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLF1B	0x000000000006C730	344
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLS0A	0x000000000006C701	336
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLS0B	0x000000000006C711	339
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLS1A	0x000000000006C721	342
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLS1B	0x000000000006C731	345
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SRD0A	0x000000000006C709	338
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SRD0B	0x000000000006C719	341
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SRD1A	0x000000000006C729	344
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SRD1B	0x000000000006C739	347
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SST0A	0x000000000006C706	337
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SST0B	0x000000000006C716	340
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SST1A	0x000000000006C726	343
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SST1B	0x000000000006C736	346
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SWD0A	0x000000000006C708	338
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SWD0B	0x000000000006C718	341
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SWD1A	0x000000000006C728	344
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SWD1B	0x000000000006C738	347
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR0	0x000000000006C208	266
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR1	0x000000000006C218	271
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR2	0x000000000006C228	276
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR3	0x000000000006C238	281
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR0	0x000000000006C20C	267
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR1	0x000000000006C21C	272
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR2	0x000000000006C22C	277
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR3	0x000000000006C23C	282
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSR0	0x000000000006C20A	267
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSR1	0x000000000006C21A	272
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSR2	0x000000000006C22A	277
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSR3	0x000000000006C23A	282
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES0	0x000000000006C206	266
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES1	0x000000000006C216	271
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES2	0x000000000006C226	276
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES3	0x000000000006C236	281
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR0	0x000000000006C203	263
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR1	0x000000000006C213	269
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR2	0x000000000006C223	274
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR3	0x000000000006C233	279
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS0	0x000000000006C204	263

Mnemonic	Address	Page
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS1	0x000000000006C214	269
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS2	0x000000000006C224	274
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS3	0x000000000006C234	279
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHI0	0x000000000006C205	266
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHI1	0x000000000006C215	271
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHI2	0x000000000006C225	276
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHI3	0x000000000006C235	281
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR0	0x000000000006C200	261
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR1	0x000000000006C210	267
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR2	0x000000000006C220	272
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR3	0x000000000006C230	277
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS0	0x000000000006C201	262
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS1	0x000000000006C211	267
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS2	0x000000000006C221	272
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS3	0x000000000006C231	278
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLI0	0x000000000006C202	263
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLI1	0x000000000006C212	269
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLI2	0x000000000006C222	274
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLI3	0x000000000006C232	279
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCFLG	0x000000000006C08A	258
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCHBR	0x000000000006C08F	258
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCMISC	0x000000000006C080	254
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCS0	0x000000000006C086	257
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCS1	0x000000000006C087	257
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCS2	0x000000000006C088	257
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCICFG	0x000000000006C085	255
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCISR0	0x000000000006C061	250
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCISR1	0x000000000006C071	252
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_ODISR0	0x000000000006C063	251
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_ODISR1	0x000000000006C073	252
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OEHDR	0x000000000006C084	255
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OHTMCR	0x000000000006C083	254
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIEPR0	0x000000000006C00C	244
TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIEPR1	0x000000000006C02C	248
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TP.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIRACT1	0x0000000001010807	491
TP.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIRMASK	0x0000000001010803	488
TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV0	0x000000000006A004	239
TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV1	0x000000000006A005	240
TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV2	0x000000000006A006	240
TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV3	0x000000000006A007	240
TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRCHSW	0x000000000006A008	240
TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SREAR	0x000000000006A003	239
TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRMAP	0x000000000006A002	239
TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRMR	0x000000000006A001	238
TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART0_REGISTER	0x0000000000018000	78
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TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART11_REGISTER	0x000000000001800B	80
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TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART22_REGISTER	0x0000000000018016	83
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TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART28_REGISTER	0x000000000001801C	84
TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART29_REGISTER	0x000000000001801D	84
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TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART56_REGISTER	0x0000000000018038	90
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TP.TPCHIP.TPC.EPS.THERM.SKITTER_DATA2	0x000000000105001B	531
TP.TPCHIP.TPC.EPS.THERM.SKITTER_FORCE_REG	0x0000000001050014	530
TP.TPCHIP.TPC.EPS.THERM.SKITTER_MODE_REG	0x0000000001050010	527
TP.TPCHIP.TPC.EPS.THERM.THERM_MODE_REG	0x000000000105000F	526
TP.TPCHIP.TPC.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000105001C	532
TP.TPCHIP.TPC.ERROR_STATUS	0x000000000103000F	511
TP.TPCHIP.TPC.FIR_MASK	0x0000000001040002	518
TP.TPCHIP.TPC.HOSTATTN	0x0000000001040009	520
TP.TPCHIP.TPC.HOSTATTN_MASK	0x000000000104001A	526
TP.TPCHIP.TPC.ITR.FMU.FMU_FORCE_OP_REG	0x0000000001020003	494
TP.TPCHIP.TPC.ITR.FMU.FMU_KVREF_DATAREG	0x0000000001020004	494
TP.TPCHIP.TPC.ITR.FMU.FMU_MODE_REG	0x0000000001020000	493
TP.TPCHIP.TPC.ITR.FMU.FMU_OSC_CNTR1_REG	0x0000000001020001	493
TP.TPCHIP.TPC.ITR.FMU.FMU_OSC_CNTR2_REG	0x0000000001020002	494
TP.TPCHIP.TPC.ITR.FMU.FMU_PULSE_GEN_REG	0x0000000001020001	494
TP.TPCHIP.TPC.ITR.FMU.FMU_VMEAS_MAX_RESULT	0x0000000001020008	495
TP.TPCHIP.TPC.ITR.FMU.FMU_VMEAS_MIN_RESULT	0x0000000001020009	496
TP.TPCHIP.TPC.ITR.FMU.KVREF_AND_VMEAS_MODE_STATUS_REG	0x0000000001020007	495
TP.TPCHIP.TPC.ITR.FMU.KVREF_TUNE_DATA	0x0000000001020005	495
TP.TPCHIP.TPC.ITR.FMU.VMEAS_RESULT_REG	0x0000000001020006	495
TP.TPCHIP.TPC.ITR.OSCERR.OSCERR_HOLD	0x0000000001020019	496
TP.TPCHIP.TPC.ITR.OSCERR.OSCERR_MASK	0x000000000102001A	496
TP.TPCHIP.TPC.ITR.OSCERR.OSCERR_MCODE	0x000000000102001B	496
TP.TPCHIP.TPC.LOCAL_FIR	0x000000000104000A	520
TP.TPCHIP.TPC.LOCAL_XSTOP_ERR	0x0000000001040018	525
TP.TPCHIP.TPC.LOCAL_XSTOP_MASK	0x0000000001040019	525
TP.TPCHIP.TPC.OPCG_ALIGN	0x0000000001030001	497
TP.TPCHIP.TPC.OPCG_CAPT1	0x0000000001030010	512
TP.TPCHIP.TPC.OPCG_CAPT2	0x0000000001030011	512
TP.TPCHIP.TPC.OPCG_CAPT3	0x0000000001030012	514
TP.TPCHIP.TPC.OPCG_REG0	0x0000000001030002	499
TP.TPCHIP.TPC.OPCG_REG1	0x0000000001030003	501
TP.TPCHIP.TPC.OPCG_REG2	0x0000000001030004	502
TP.TPCHIP.TPC.RFIR	0x0000000001040001	517
TP.TPCHIP.TPC.SCAN_REGION_TYPE	0x0000000001030005	502
TP.TPCHIP.TPC.SPATTN	0x0000000001040004	518
TP.TPCHIP.TPC.SPA_MASK	0x0000000001040007	519
TP.TPCHIP.TPC.SYNC_CONFIG	0x0000000001030000	497
TP.TPCHIP.TPC.TRA0.TR0.TRACE_HI_DATA_REG	0x0000000001010400	465
TP.TPCHIP.TPC.TRA0.TR0.TRACE_LO_DATA_REG	0x0000000001010401	465
TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRCTRL_CONFIG	0x0000000001010402	465
TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x0000000001010403	466
TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x0000000001010404	466

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TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_2	0x0000000001010405	466
TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x0000000001010406	466
TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x0000000001010407	467
TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x0000000001010408	467
TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x0000000001010409	467
TP.TPCHIP.TPC.TRA0.TR1.TRACE_HI_DATA_REG	0x0000000001010440	468
TP.TPCHIP.TPC.TRA0.TR1.TRACE_LO_DATA_REG	0x0000000001010441	469
TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRCTRL_CONFIG	0x0000000001010442	469
TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_0	0x0000000001010443	469
TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_1	0x0000000001010444	470
TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_2	0x0000000001010445	470
TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_3	0x0000000001010446	470
TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_4	0x0000000001010447	470
TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_5	0x0000000001010448	470
TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_9	0x0000000001010449	471
TP.TPCHIP.TPC.XFIR	0x0000000001040000	516
TP.TPCHIP.TPC.XSTOP1	0x000000000103000C	508
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TP.TPCHIP.TPC.XSTOP3	0x000000000103000E	510
TP.TPVSB.FSI.W.FSI_I2C.COMMAND_REGISTER_A	0x0000000000001801	68
TP.TPVSB.FSI.W.FSI_I2C.EXTENDED_STATUS_A	0x0000000000001808	71
TP.TPVSB.FSI.W.FSI_I2C.FIFO1_REGISTER_READ_A	0x0000000000001800	68
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TP.TPVSB.FSI.W.FSI_I2C.IMM_RESET_ERR_A	0x0000000000001808	72
TP.TPVSB.FSI.W.FSI_I2C.IMM_RESET_I2C_A	0x0000000000001807	70
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TP.TPVSB.FSI.W.FSI_I2C.IMM_RESET_S_SDA_A	0x000000000000180D	73
TP.TPVSB.FSI.W.FSI_I2C.IMM_SET_S_SCL_A	0x0000000000001809	72
TP.TPVSB.FSI.W.FSI_I2C.IMM_SET_S_SDA_A	0x000000000000180C	73
TP.TPVSB.FSI.W.FSI_I2C.INTERRUPTS_A	0x0000000000001806	70
TP.TPVSB.FSI.W.FSI_I2C.INTERRUPT_COND_A	0x0000000000001805	70
TP.TPVSB.FSI.W.FSI_I2C.INTERRUPT_MASK_REGISTER_A	0x0000000000001804	69
TP.TPVSB.FSI.W.FSI_I2C.INTERRUPT_MASK_REGISTER_READ_A	0x0000000000001804	69
TP.TPVSB.FSI.W.FSI_I2C.MODE_REGISTER_A	0x0000000000001802	68
TP.TPVSB.FSI.W.FSI_I2C.RESIDUAL_FRONT_END_BACK_END_LENGTH_A	0x0000000000001809	72
TP.TPVSB.FSI.W.FSI_I2C.STATUS_REGISTER_ENGINE_A	0x0000000000001807	71
TP.TPVSB.FSI.W.FSI_I2C.WATER_MARK_REGISTER_A	0x0000000000001803	69
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_CS	0x0000000000050001	144
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_EL	0x0000000000050003	144
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_EL_HIST	0x0000000000050006	145
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_TR	0x0000000000050002	144
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.DOORBELL_STATUS_CONTROL_1A	0x0000000000050020	156
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_13	0x000000000005004D	167
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_8	0x0000000000050048	166
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_0	0x00000000000500C0	171
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_1	0x00000000000500C1	171
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_10	0x00000000000500CA	173
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_11	0x00000000000500CB	173
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_12	0x00000000000500CC	173
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_15	0x00000000000500CF	174
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_4	0x00000000000500C4	171
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_5	0x00000000000500C5	172
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_6	0x00000000000500C6	172
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_7	0x00000000000500C7	172
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_8	0x00000000000500C8	172
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_9	0x00000000000500C9	172
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_0	0x0000000000050100	174
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_12	0x000000000005010C	176
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_13	0x000000000005010D	176
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_14	0x000000000005010E	177
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_15	0x000000000005010F	177
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_4	0x0000000000050104	175
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_5	0x0000000000050105	175
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_6	0x0000000000050106	175
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_7	0x0000000000050107	175
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_8	0x0000000000050108	175
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_9	0x0000000000050109	176
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_0_A	0x0000000000050021	157
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_0_B	0x0000000000050025	157
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_1_B	0x0000000000050026	157
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_2_A	0x0000000000050023	157
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_2_B	0x0000000000050027	158
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_SLAVE_A_DOORBELL_INTERRUPT_MASK_1	0x0000000000050033	161
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_2_HEADER_COMMAND_0_A	0x0000000000050029	158
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_2_HEADER_COMMAND_2_A	0x000000000005002B	159
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_2_HEADER_COMMAND_2_B	0x000000000005002F	159
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_A_DOORBELL_ERROR_STATUS	0x0000000000050031	160
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_A_DOORBELL_INTERRUPT	0x0000000000050032	161
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_B_DOORBELL_ERROR_STATUS	0x0000000000050030	159
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_B_DOORBELL_INTERRUPT	0x0000000000050035	162
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_B_DOORBELL_INTERRUPT_MASK_1	0x0000000000050036	162
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL0	0x000000000005001A	153
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL1	0x000000000005001B	154
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL1_CLEAR	0x000000000005013B	195
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL1_COPY	0x000000000005011B	179
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL1_SET	0x000000000005012B	187
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL0	0x0000000000050010	147
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL0_CLEAR	0x0000000000050130	188
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL0_COPY	0x0000000000050110	177
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL0_SET	0x0000000000050120	179
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL1	0x0000000000050011	147
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL1_CLEAR	0x0000000000050131	188
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL1_COPY	0x0000000000050111	177
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL1_SET	0x0000000000050121	180
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL2_CLEAR	0x0000000000050132	189
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL2_SET	0x0000000000050122	181
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TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL3_CLEAR	0x0000000000050133	190
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL3_COPY	0x0000000000050113	178
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL3_SET	0x0000000000050123	182
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL4	0x0000000000050014	150
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL4_CLEAR	0x0000000000050134	191
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL4_COPY	0x0000000000050114	178
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL4_SET	0x0000000000050124	182
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL5	0x0000000000050015	150
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL5_CLEAR	0x0000000000050135	191
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL5_COPY	0x0000000000050115	178
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL5_SET	0x0000000000050125	182
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL6	0x0000000000050016	151
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL6_CLEAR	0x0000000000050136	192
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL6_COPY	0x0000000000050116	178
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL6_SET	0x0000000000050126	183
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL7	0x0000000000050017	151
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL7_CLEAR	0x0000000000050137	192
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL7_COPY	0x0000000000050117	178
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL7_SET	0x0000000000050127	184
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL8	0x0000000000050018	152
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL8_CLEAR	0x0000000000050138	193
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL8_COPY	0x0000000000050118	179
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL8_SET	0x0000000000050128	185
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SB_CS	0x0000000000050008	145
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SB_MSG	0x0000000000050009	145
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_1	0x0000000000050038	163
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_2	0x0000000000050039	163
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_3	0x000000000005003A	163
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_4	0x000000000005003B	163

Mnemonic	Address	Page
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_5	0x000000000005003C	163
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_6	0x000000000005003D	164
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_7	0x000000000005003E	164
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_8	0x000000000005003F	164
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SNS1LTH	0x000000000005001D	155
TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SNS2LTH	0x000000000005001E	155
TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_DOWNFIFO_DATA_IN	0x00000000000B0010	437
TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_DOWNFIFO_REQ_RESET	0x00000000000B0013	438
TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_DOWNFIFO_SIG_EOT	0x00000000000B0012	438
TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_DOWNFIFO_STATUS	0x00000000000B0011	438
TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_UPFIFO_ACK_EOT	0x00000000000B0005	437
TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_UPFIFO_DATA_OUT	0x00000000000B0000	436
TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_UPFIFO_RESET	0x00000000000B0004	437
TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_UPFIFO_STATUS	0x00000000000B0001	437
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CMD_WRDAT	0x0000000000020000	106
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CRSIC	0x0000000000020005	108
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CRSIM	0x0000000000020006	108
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CRSIS	0x0000000000020007	108
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.LSTAT	0x0000000000020002	108
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.RESET	0x0000000000020004	108
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.RSIC	0x0000000000020008	109
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.RSIM	0x0000000000020009	109
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.RSIS	0x000000000002000A	109
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.STAT_RDDAT_ERRES	0x0000000000020001	107
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.CMD_WRDAT	0x0000000000020010	109
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.CRSIC	0x0000000000020015	111
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.CRSIM	0x0000000000020016	111
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.CRSIS	0x0000000000020017	111
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.LSTAT	0x0000000000020012	111
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.RESET	0x0000000000020014	111
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.RSIC	0x0000000000020018	112
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.RSIM	0x0000000000020019	112
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.RSIS	0x000000000002001A	112
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.STAT_RDDAT_ERRES	0x0000000000020011	110
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CMD_WRDAT	0x0000000000030000	112
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIC	0x0000000000030005	114
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIM	0x0000000000030006	114
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIS	0x0000000000030007	114
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.LSTAT	0x0000000000030002	114
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RESET	0x0000000000030004	114
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIC	0x0000000000030008	115
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIM	0x0000000000030009	115
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIS	0x000000000003000A	115

Mnemonic	Address	Page
TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.STAT_RDDAT_ERRES	0x0000000000030001	113

The POWER9 processor registers are listed in the following tables.

Register Name	FIFO1 Register Read A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.FIFO1_REGISTER_READ_A
Address	0000000000001800 (SCOM)
Description	FIFO1 Register Read A

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_0: Because FIFO is not a normal register, it cannot be completely verified in REGCHK. Thus, this register is a dummy register that is used to maintain the address in HTML FIFO data byte 0. It should be able to read or write 1 byte.
8:31	RO	constant = 0b00000000000000000000000

Register Name	Command Register A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.COMMAND_REGISTER_A
Address	0000000000001801 (SCOM)
Description	Command Register A

Bits	SCOM	Field Mnemonic: Description
0	RWX	WITH_START_0: Decides if the start command is issued during the beginning of the operation.
1	RWX	WITH_ADDRESS_0: Decides if the device address is sent during the beginning of the operation.
2	RWX	READ_CONTINUE_0: Decides if the next read operation is continuation of present operation.
3	RWX	WITH_STOP_0: Decides if the stop command is issued during the end of the operation.
4:7	RWX	NOT_USED_0: Not used.
8:14	RWX	DEVICE_ADDRESS_0: The device address of the slave on the I2C bus.
15	RWX	READ_NOT_WRITE_0: I2C read or write.
16:31	RWX	LENGTH_IN_BYTES_0: The length of bytes to be accessed through the I2C bus.

Register Name	Mode Register A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.MODE_REGISTER_A
Address	0000000000001802 (SCOM)
Description	Mode Register A

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus.

Bits	SCOM	Field Mnemonic: Description
8:9	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus.
10:15	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus.
16:21	RWX	PORT_NUMBER_0: Port number.
22:26	RO	constant = 0b00000
27	RWX	CHKSW_I2C_BUSY_0: A debug switch to switch between the Port Busy Register and I2C busy muxing logic. **Note**: If you do not enable the chicken switch, the older logic behavior occurs.
28	RWX	FGAT_MODE_0: FGAT mode.
29	RWX	DIAG_MODE_0: Diagnostic mode.
30	RWX	PACING_ALLOW_MODE_0: Pacing allow mode.
31	RWX	WRAP_MODE_0: Wrap mode.

Register Name	**Water Mark Register A**
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.WATER_MARK_REGISTER_A
Address	0000000000001803 (SCOM)
Description	Water Mark Register A

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	RWX	WATERMARK_REG_0: Watermark register.

Register Name	**Interrupt Mask Register A**
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.INTERRUPT_MASK_REGISTER_A
Address	0000000000001804 (SCOM) 0000000000001805 (SCOM1) 0000000000001806 (SCOM2)
Description	Interrupt Mask Register A

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:15	RO	RO	RO	constant = 0b0000000000000000
16:31	WOX	WOX_OR	WOX_AND	INT_MASK_0: Interrupt mask register.

Register Name	**Interrupt Mask Register Read A**
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.INTERRUPT_MASK_REGISTER_READ_A
Address	0000000000001804 (SCOM)
Description	Interrupt Mask Register Read A

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	ROX	INT_MASK_0: Interrupt mask register

Register Name	Interrupt Condition A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.INTERRUPT_COND_A
Address	0000000000001805 (SCOM)
Description	Interrupt Condition A

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16	ROX	INVALID_CMD_0: Invalid command. A new command was given when the old command was not yet completed.
17	ROX	LBUS_PARITY_ERROR_0: Local bus parity error.
18	ROX	BE_OV_ERROR_0: Back end overrun error. A write to a full or a read to an empty FIFO reply occurred.
19	ROX	BE_ACC_ERROR_0: Back end access error. More data than requested was written or read.
20	ROX	ARBITRATION_LOST_ERROR_0: Arbitration lost error. The I2C bus was held by some other master when access was attempted.
21	ROX	NACK_RECEIVED_ERROR_0: NACK received error. The slave did not respond with the acknowledgment.
22	ROX	DATA_REQUEST_0: Data request. The FIFO must be accessed more to fulfill the expectation.
23	ROX	INT_CONDS_CMD_COMPLETE_0
24	ROX	STOP_ERROR_0: Stop error. Cannot send the stop condition to the bus.
25	ROX	INT_CONDS_I2C_BUSY_0
26	ROX	INT_CONDS_NOT_I2C_BUSY_0
27	RO	constant = 0b0
28	ROX	INT_CONDS_SCL_EQ_1_0
29	ROX	INT_CONDS_SCL_EQ_0_0
30	ROX	INT_CONDS_SDA_EQ_1_0
31	ROX	INT_CONDS_SDA_EQ_0_0

Register Name	Interrupt Register A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.INTERRUPTS_A
Address	0000000000001806 (SCOM)
Description	Interrupts Register A

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	INTS_0

Register Name	IMM Reset I2C A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.IMM_RESET_I2C_A
Address	0000000000001807 (SCOM)
Description	IMM Reset I2C A

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_I2C_0: Resets the command, mode, watermark, interrupt mask, and status registers.

Register Name	Status Register Engine A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.STATUS_REGISTER_ENGINE_A
Address	0000000000001807 (SCOM)
Description	Status Register Engine A

Bits	SCOM	Field Mnemonic: Description
0	ROX	INVALID_CMD_0: Invalid command. A new command was given when the old command was not yet completed.
1	ROX	LBUS_PARITY_ERROR_0: Local bus parity error.
2	ROX	BE_OV_ERROR_0: Back-end overrun error. A write to a full or a read to an empty FIFO reply occurred.
3	ROX	BE_ACC_ERROR_0: Back-end access error. More data than requested was written or read.
4	ROX	ARBITRATION_LOST_ERROR_0: Arbitration lost error. The I2C bus was held by some other master when access was attempted.
5	ROX	NACK_RECEIVED_ERROR_0: NACK received error. The slave did not respond with the acknowledgment.
6	ROX	DATA_REQUEST_0: Data request. The FIFO must be accessed more to fulfill the expectation.
7	ROX	CMD_COMPLETE_0: Indicates the completion of command.
8	ROX	STOP_ERROR_0: Stop error. Cannot send the stop condition to the bus.
9:15	ROX	MAX_NUM_OF_PORTS_0. The maximum number of ports that are defined for this engine.
16	ROX	ANY_I2C_INT_0
17:18	RO	constant = 0b00
19	ROX	I2C_PORT_HISTORY_BUSY_0
20	ROX	SCL_SYN_0
21	ROX	SDA_SYN_0
22	ROX	i2c_busy_0: The I2C bus is occupied.
23	ROX	SELF_BUSY_0: Self busy. The I2C bus is occupied by itself.
24:27	RO	constant = 0b0000
28:31	ROX	FIFO_ENTRY_COUNT_0: The number of bytes that are present in the FIFO.

Register Name	Extended Status A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.EXTENDED_STATUS_A
Address	0000000000001808 (SCOM)
Description	Extended Status A

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_SIZE_0: The total FIFO size.
8:10	RO	constant = 0b000
11:15	ROX	MSM_CURR_STATE_0: The current state.
16	ROX	SCL_SYN_EXT_0
17	ROX	SDA_SYN_EXT_0
18	ROX	S_SCL_0: The clock input for wrap mode.

Bits	SCOM	Field Mnemonic: Description
19	ROX	S_SDA_0: Data input for wrap mode.
20	ROX	M_SCL_0. The clock output for wrap mode.
21	ROX	M_SDA_0. The data output for wrap mode.
22	ROX	HIGH_WATER_0: The FIFO reached the highest water level.
23	ROX	LOW_WATER_0. The FIFO reached the lowest water level.
24	ROX	I2C_BUSY_EXT_0. The I2C bus is busy.
25	ROX	SELF_BUSY_0: Self busy. The I2C bus is occupied by itself.
26:31	RO	constant = 0b010111

Register Name	**IMM Reset ERR A**
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.IMM_RESET_ERR_A
Address	0000000000001808 (SCOM)
Description	IMM Reset ERR A

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_ERRORS_0. Resets the FIFO, some status bits, and the state machine.

Register Name	**IMM Sets SCL_A**
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.IMM_SET_S_SCL_A
Address	0000000000001809 (SCOM)
Description	IMM Sets SCL_A

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SCL_0. Sets output S_SCL.

Register Name	**Residual Front End Back End Length A**
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.RESIDUAL_FRONT_END_BACK_END_LENGTH_A
Address	0000000000001809 (SCOM)
Description	Residual Front End Back End Length A

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	RESID_FE_LEN_0: Residual front end length register.
16:31	ROX	RESID_BE_LEN_0: Residual back end length register.

Register Name	**I2C Busy Register A**
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.I2C_BUSY_REGISTER_A
Address	000000000000180A (SCOM)
Description	I2C Busy Register A

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PORT_BUSY_0. The corresponding port is busy. If it is ‘1’, no one can access the port. If it is ‘0’, it can be accessed.

Register Name	IMM Resets SCL_A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.IMM_RESET_S_SCL_A
Address	000000000000180B (SCOM)
Description	IMM Resets SCL_A

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SCL_0: Resets output S_SCL.

Register Name	IMM Sets SDA_A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.IMM_SET_S_SDA_A
Address	000000000000180C (SCOM)
Description	IMM Set S SDA A

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SDA_0: Sets output S_SDA.

Register Name	IMM Resets SDA_A
Mnemonic	TP.TPVSB.FSI.W.FSI_I2C.IMM_RESET_S_SDA_A
Address	000000000000180D (SCOM)
Description	IMM Resets SDA_A

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SDA_0. Resets output S_SDA.

Register Name	Command Register Fast Mode
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.COMMAND_REGISTER
Address	0000000000010000 (SCOM)
Description	Command Register Fast Mode.

Bits	SCOM	Field Mnemonic: Description
0	RW	CMD_REG_BIT_WITHSTART: This bit is used to initiate operation. It is a don’t care for the OTP ROM controller.
1	RW	CMD_REG_BIT_WITHADDR: This bit is used to initiate operation. It is a don’t care for the OTP ROM controller.
2	RW	CMD_REG_BIT_READCONT: This bit is used to initiate operation. It is a don’t care for the OTP ROM controller.
3	RW	CMD_REG_BIT_WITHSTOP: This bit is used to initiate operation. It is a don’t care for the OTP ROM controller.

Bits	SCOM	Field Mnemonic: Description
4:7	RW	CMD_REG_LENGTH: The length of real data excluding register address. Permitted values are 4 and 8. 4 = Requesting for four bytes of read data. 8 = Requesting for eight bytes of read data. MAXIMUM_READ = 8. Only permitted value.
8:14	RW	UNUSED_8_14: Reserved. Not used.
15	RW	CMD_REG_BIT_RNW: To enable read, program a ‘1’. A ‘0’ is an invalid option.
16:22	RW	UNUSED_16_22: Reserved. Not used.
23:25	RW	REG_ADDR_LEN: 000 = Address increment if address field is ‘0’. 001= One byte of CMD_REG_ADDR is valid. 010= Two bytes of CMD_REG_ADDR are valid 011= Three bytes of CMD_REG_ADDR are valid. 111= Four bytes of CMD_REG_ADDR are valid.
26:31	RW	UNUSED_26_31: Reserved. Not used.
32:39	RW	CMD_REG_ADDR_1: Read the address read from the first byte.
40:47	RW	CMD_REG_ADDR_2: Read the address read from the second byte.
48:55	RW	CMD_REG_ADDR_3 Read the address read from the third byte.
56:63	RW	CMD_REG_ADDR_4: Read the address read from the fourth byte.

Register Name	Reset Register
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.RESET_REGISTER
Address	0000000000010001 (SCOM)
Description	Reset Register

Bits	SCOM	Field Mnemonic: Description
0	WO	CHICKEN_SWITCH: Used to enable or disable AR012 PIB error reporting enhancement feature. 0 = Enable 1 = Disable

Register Name	Status Register
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.STATUS_REGISTER
Address	0000000000010002 (SCOM)
Description	Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	STATUS_ADDR_NVLD: Address is invalid.
1	ROX	STATUS_WRITE_NVLD: Write is invalid.
2	ROX	STATUS_READ_NVLD: Read is invalid.
3	ROX	STATUS_INVLD_CMD_ERR: Invalid command register fields are programmed.
4	ROX	STATUS_CORR_ERR: ECC correctable error.
5	ROX	STATUS_UNCORR_ERROR: ECC uncorrectable error.
6:37	ROX	STATUS_DATA_REG_0_31: First 4 bytes of read Data Register [0:31].
38	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
39:43	ROX	STATUS_UNUSED_39_43: Unused.
44	ROX	STATUS_CTRL_BUSY: OTP ROM controller is busy.
45	ROX	STATUS_DCOMP_ERR: Decompression engine error.
46	ROX	STATUS_INVLD_PRGM_ERR: Invalid program operation error.
47:51	ROX	STATUS_UNUSED_47_51: Unused.
52	ROX	STATUS_COMMAND_COMPLETE: Operation complete for a fast mode read operation or a programming operation.
53	ROX	STATUS_UNUSED_53: Unused.
54	ROX	STATUS_RDWR_OP_BUSY: Read/write operation controller logic busy.
55	ROX	STATUS_DCOMP_ENGINE_BUSY: Decompression engine busy.
56:63	ROX	STATUS_RD_DATA_COUNT: Valid read data count. 0x08 for OTP ROM.

Register Name	Data Register for Fast Mode Read Data
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.DATA_REGISTER
Address	0000000000010003 (SCOM)
Description	Data Register for Fast Mode Read Data

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	OTP_DATA_REGISTER: Fast mode read data.

Register Name	Security Switch Register
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.SECURITY_SWITCH_REGISTER
Address	0000000000010005 (SCOM) 0000000000010006 (SCOM1)
Description	Register for secure boot features

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	RW_WOR	WO_CLEAR	SECURITY_SWITCH_SECURE_ACCESS: Indicates status of secure access bit from the FSI mailbox. It is used by the CFAM to disable the FSI2PIB (SCOM) and shift (SCAN and DMA) engines. Also, it is used to disable the CFAM I2CM access to the SBE SEEPROMs and emulated JTAG access path to OCC PowerPC.
1	RW_WOR	WO_CLEAR	SECURITY_SWITCH_LATE_LAUNCH_PRIMARY: Late launch primary security. Checks which chip is initiating DRTM late launch sequence.
2	RW_WOR	WO_CLEAR	SECURITY_SWITCH_LATE_LAUNCH_SECONDARY: Late launch secondary security. Checks which chip is initiating DRTM late launch sequence.
3	RW_WOR	WO_CLEAR	SECURITY_SWITCH_LOCAL_QUIESCE_ACHIEVED: Local quiesce achieved. Checks whether THE chip has been successfully quiesced. It is reset by local SBE/HFW during DRTM late launch code.
4	RW_WOR	NCX	SECURITY_SWITCH_SEEPROM_UPDATE_LOCK: Prevent write access to SEEPROM and prevent reset of THE SAB in the FSI mailbox by the PIB.
5	RW_WOR	WO_CLEAR	SECURITY_SWITCH_LOCALITY_4_ACCESS: Used by the PIB I2CM to gate all write access to TPMD. It is set by the local SBE after all chips in the system have been evaluated as quiesced.

Bits	SCOM	SCOM1	Field Mnemonic: Description
6	RW_WOR	WO_CLEAR	SECURITY_SWITCH_SECURE_DEBUG: Indicates secure chip debug mode. From FSI mailbox. Used by FSI2PIB engine to enable FSP SCOM access to the SBE. It is also used by the SBE to switch PPE into debug mode, which restricts PPE capabilities to read-out internal register space only.
7	RW_WOR	WO_CLEAR	SECURITY_SWITCH_CMFSI_ACCESS_PROTCT: Prevents any access to the CMFSI ports from the FSI slave if this bit is set.
8	RW_WOR	NCX	SECURITY_SWITCH_ABUS_SECURITY_LOCK: Consumed by ABUS logic (processor bus) and protects mailbox access.
9	RW_WOR	NCX	SECURITY_SWITCH_NX_RAND_NUM_GEN_LOCK: Consumed by NX random generator lock.
10	RW_WOR	WO_CLEAR	SECURITY_SWITCH_PROT_EX_SPARE0: Spare going to EX.
11	RW_WOR	WO_CLEAR	SECURITY_SWITCH_PROT_EX_SPARE1: Spare going to EX.
12	RW_WOR	WO_CLEAR	SECURITY_SWITCH_I2CM_TPM_DECONFIG_PROTECT: Security switch to control access to all five write I2C device IDs of the TPM.
13	RW_WOR	WO_CLEAR	SECURITY_SWITCH_PROT_TP_SPARE0: TP spare.
14	RW_WOR	WO_CLEAR	SECURITY_SWITCH_PROT_TP_SPARE1: TP spare.
15	RW_WOR	WO_CLEAR	SECURITY_SWITCH_PROT_TP_SPARE2: TP spare.

Register Name	Mode Register to Enable Features
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.MODE_REGISTER
Address	0000000000010008 (SCOM)
Description	Register to enable the decompression engine, run ECC checking operations, and programming enablement

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_DCOMP_ENABLE: Used to enable the decompression engine. The default value is ‘0’.
1	RW	MODE_ECC_ENABLE: Enable ECC checking (only for read operation). The default value = ‘1’. If ECC is enabled, set to ‘1’. Otherwise, set to ‘0’. If this bit is set to ‘1’, it assumes that ECC is stored in OTPROMs and follows ECC enabled addressing. For debug purposes, set this bit to ‘0’ to dump the all locations contents of OTPROM(s).
2	RW	MODE_PROGRAM_ENABLE: Enable programming in SCOM mode. Default value is ‘0’.
3	RW	MODE_ECC_CHK_DISABLE: Set this bit ‘1’ to disable ECC check. Set to ‘0’ to disable ECC check. Default value is ‘0’. This bit is valid only when bit 1 of this register set to ‘1’ and ECC is enabled.
4:15	RW	MODE_UNUSED_4_15: Unused.
16:31	RW	MODE_CLK_RATE_SEL: Used to select clock rate. Based on the Tprg requirement of OTP ROM. Current values are: 40 MHz: 0xC8 200 MHz: 0x3E8 800 MHz: 0xFA0.

Register Name	Program eFUSE Locations
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.PRGM_REGISTER
Address	0000000000010009 (SCOM)
Description	Used to program eFUSE locations

Bits	SCOM	Field Mnemonic: Description
0:31	RW	PRGM_PRGM_ADDR: The address of the OTP ROM location to be programmed.
32:37	RW	PRGM_PRG_BIT_LOCATION: The bit location in 64 bits to be fused.

Register Name	Probe Protection Control Outputs
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.PROBE_PROTECT_STATUS
Address	000000000001000A (SCOM)
Description	Probe Protection Control Outputs

Bits	SCOM	Field Mnemonic: Description
0:41	ROX	PROBE_PROTECT_STATUS_BITS: Status of probe protection outputs.

Register Name	Disable Force PFET
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.DISABLE_FORCE_PFET_OFF
Address	000000000001000D (SCOM)
Description	Register used to disable force PFET off control from fuse status.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	DISABLE_FORCE_PFET_OFF_REG: 1 = Disable force PFET off (Disables fuse control on PFET control). PFET is forced to on (IFF FSI GP bit forced on). 0 = No overrides. Based on fuse content and FSI GP BIT. PFET is forced to on/off.
30:41	RW	RESERVED_DISABLE_FORCE_PFET_OFF: Reserved for future usage.

Register Name	Export Regulation Control Register
Mnemonic	TP.TPCHIP.PIB.OTP.OTPC_M.EXPORT_REGL_CTRL
Address	000000000001000E (SCOM)
Description	Export regulation control register

Bits	SCOM	Field Mnemonic: Description
0	RW	EXPORT_CTRL_TP_NX_ALLOW_CRYPTO_DC: 1 = Replicates the behavior of blown fuses for TP_NX_ALLOW_CYRPTO_DC regardless of fuse content. 0 = Allows the fuse to control the fuse bit. The initial value is ‘0’.
1	RW	EXPORT_CTRL_TP_EX_FUSE_VMX_CRYPTO_DIS_DC: 1 = Replicates the behavior of blown fuses for TP_EX_FUSE_MVX_CRYPTO_DIS_DC regardless of fuse content. 0 = Export regulation content based on the fuse content. The initial value is ‘0’.
2	RW	EXPORT_CTRL_TP_EX_FUSE_FP_THROTTLE_EN_DC: Used to disable TP_EX_FUSE_FP_THROTTLE_EN_DC without the fuse blown. 1 = Replicates the behavior of blown fuses for TP_EX_FUSE_FP_THROTTLE_EN_DC regardless of fuse content. 0 = Export regulation output is based on fuse content The initial value is ‘0’.

Bits	SCOM	Field Mnemonic: Description
3	RW	EXPORT_CTRL_TP_PB_FUSE_TOPOLOGY_2CHIP: Used to apply limits on chip topology without the fuse blown. 1 = Replicates the behavior of blown fuses for TP_PB_FUSE_TOPOLOGY_2CHIP regardless of fuse content. 0 = Export regulation output is based on fuse content. The initial value is '0'.
4:5	RW	EXPORT_CTRL_TP_PB_FUSE_TOPOLOGY_GROUP: Used to apply limits on chip topology without the fuse blown. 1 = Replicates the behavior of blown fuses for TP_PB_FUSE_TOPOLOGY_GROUP [0:1] regardless of fuse content. 0 = Export regulation output is based on fuse content.
6	RW	EXPORT_CTRL_TP_NP_NVLINK_DISABLE: Used to apply limits on chip topology without the fuse blown. 1 = Replicates the behavior blown fuses for TP_NP_NVLINK_DISABLE export regulation output. 0 = Export regulation output is based on fuse content.

Register Name	Part 0 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART0_REGISTER
Address	0000000000018000 (SCOM)
Description	Contains part 0 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location.

Register Name	Part 1 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART1_REGISTER
Address	0000000000018001 (SCOM)
Description	Contains part 1 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location.

Register Name	Part 2 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART2_REGISTER
Address	0000000000018002 (SCOM)
Description	Contains part 2 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location.

Register Name	Part 3 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART3_REGISTER
Address	0000000000018003 (SCOM)
Description	Contains part 3 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location.

Register Name	Part 4 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART4_REGISTER
Address	0000000000018004 (SCOM)
Description	Contains part 4 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location.

Register Name	Part 5 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART5_REGISTER
Address	0000000000018005 (SCOM)
Description	Contains part 5 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location.

Register Name	Part 6 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART6_REGISTER
Address	0000000000018006 (SCOM)
Description	Contains part 6 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location.

Register Name	Part 7 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART7_REGISTER
Address	0000000000018007 (SCOM)
Description	Contains part 7 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location.

Register Name	Part 8 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART8_REGISTER
Address	0000000000018008 (SCOM)
Description	Contains part 8 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location.

Register Name	Part 9 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART9_REGISTER
Address	0000000000018009 (SCOM)
Description	Contains part 9 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location.

Register Name	Part 10 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART10_REGISTER
Address	000000000001800A (SCOM)
Description	Contains part 10 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location.

Register Name	Part 11 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART11_REGISTER
Address	000000000001800B (SCOM)
Description	Contains part 11 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location.

Register Name	Part 12 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART12_REGISTER
Address	000000000001800C (SCOM)
Description	Contains part 12 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location.

Register Name	Part 13 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART13_REGISTER
Address	000000000001800D (SCOM)
Description	Contains part 13 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location.

Register Name	Part 14 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART14_REGISTER
Address	000000000001800E (SCOM)
Description	Contains part 14 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location.

Register Name	Part 15 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART15_REGISTER
Address	000000000001800F (SCOM)
Description	Contains part 15 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location.

Register Name	Part 16 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART16_REGISTER
Address	0000000000018010 (SCOM)
Description	Contains part 16 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location.

Register Name	Part 17 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART17_REGISTER
Address	0000000000018011 (SCOM)
Description	Contains part 17 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location.

Register Name	Part 18 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART18_REGISTER
Address	0000000000018012 (SCOM)
Description	Contains part 18 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location.

Register Name	Part 19 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART19_REGISTER
Address	0000000000018013 (SCOM)
Description	Contains part 19 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location.

Register Name	Part 20 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART20_REGISTER
Address	0000000000018014 (SCOM)
Description	Contains part 20 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location.

Register Name	Part 21 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART21_REGISTER
Address	0000000000018015 (SCOM)
Description	Contains part 21 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location.

Register Name	Part 22 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART22_REGISTER
Address	0000000000018016 (SCOM)
Description	Contains part 22 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location.

Register Name	Part 23 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART23_REGISTER
Address	0000000000018017 (SCOM)
Description	Contains part 23 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location.

Register Name	Part 24 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART24_REGISTER
Address	0000000000018018 (SCOM)
Description	Contains part 24 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location.

Register Name	Part 25 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART25_REGISTER
Address	0000000000018019 (SCOM)
Description	Contains part 25 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location.

Register Name	Part 26 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART26_REGISTER
Address	000000000001801A (SCOM)
Description	Contains part 26 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location.

Register Name	Part 27 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART27_REGISTER
Address	000000000001801B (SCOM)
Description	Contains part 27 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location.

Register Name	Part 28 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART28_REGISTER
Address	000000000001801C (SCOM)
Description	Contains part 28 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location.

Register Name	Part 29 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART29_REGISTER
Address	000000000001801D (SCOM)
Description	Contains part 29 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location.

Register Name	Part 30 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART30_REGISTER
Address	000000000001801E (SCOM)
Description	Contains part 30 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location.

Register Name	Part 31 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART31_REGISTER
Address	000000000001801F (SCOM)
Description	Contains part 31 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location.

Register Name	Part 32 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART32_REGISTER
Address	0000000000018020 (SCOM)
Description	Contains part 32 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location.

Register Name	Part 33 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART33_REGISTER
Address	0000000000018021 (SCOM)
Description	Contains part 33 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location.

Register Name	Part 34 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART34_REGISTER
Address	0000000000018022 (SCOM)
Description	Contains part 34 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location.

Register Name	Part 35 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART35_REGISTER
Address	0000000000018023 (SCOM)
Description	Contains part 35 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location.

Register Name	Part 36 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART36_REGISTER
Address	0000000000018024 (SCOM)
Description	Contains part 36 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location.

Register Name	Part 37 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART37_REGISTER
Address	0000000000018025 (SCOM)
Description	Contains part 37 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location.

Register Name	Part 38 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART38_REGISTER
Address	0000000000018026 (SCOM)
Description	Contains part 38 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location.

Register Name	Part 39 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART39_REGISTER
Address	0000000000018027 (SCOM)
Description	Contains part 39 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location.

Register Name	Part 40 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART40_REGISTER
Address	0000000000018028 (SCOM)
Description	Contains part 40 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location.

Register Name	Part 41 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART41_REGISTER
Address	0000000000018029 (SCOM)
Description	Contains part 41 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location.

Register Name	Part 42 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART42_REGISTER
Address	000000000001802A (SCOM)
Description	Contains part 42 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location.

Register Name	Part 43 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART43_REGISTER
Address	000000000001802B (SCOM)
Description	Contains part 43 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location.

Register Name	Part 44 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART44_REGISTER
Address	000000000001802C (SCOM)
Description	Contains part 44 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location.

Register Name	Part 45 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART45_REGISTER
Address	000000000001802D (SCOM)
Description	Contains part 45 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location.

Register Name	Part 46 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART46_REGISTER
Address	000000000001802E (SCOM)
Description	Contains part 46 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location.

Register Name	Part 47 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART47_REGISTER
Address	000000000001802F (SCOM)
Description	Contains part 47 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location.

Register Name	Part 48 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART48_REGISTER
Address	0000000000018030 (SCOM)
Description	Contains part 48 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location.

Register Name	Part 49 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART49_REGISTER
Address	0000000000018031 (SCOM)
Description	Contains part 49 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location.

Register Name	Part 50 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART50_REGISTER
Address	0000000000018032 (SCOM)
Description	Contains part 50 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location.

Register Name	Part 51 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART51_REGISTER
Address	0000000000018033 (SCOM)
Description	Contains part 51 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location.

Register Name	Part 52 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART52_REGISTER
Address	0000000000018034 (SCOM)
Description	Contains part 52 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location.

Register Name	Part 53 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART53_REGISTER
Address	0000000000018035 (SCOM)
Description	Contains part 53 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location.

Register Name	Part 54 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART54_REGISTER
Address	0000000000018036 (SCOM)
Description	Contains part 54 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location.

Register Name	Part 55 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART55_REGISTER
Address	0000000000018037 (SCOM)
Description	Contains part 55 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location.

Register Name	Part 56 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART56_REGISTER
Address	0000000000018038 (SCOM)
Description	Contains part 56 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location.

Register Name	Part 57 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART57_REGISTER
Address	0000000000018039 (SCOM)
Description	Contains part 57 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location.

Register Name	Part 58 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART58_REGISTER
Address	000000000001803A (SCOM)
Description	Contains part 58 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location.

Register Name	Part 59 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART59_REGISTER
Address	000000000001803B (SCOM)
Description	Contains part 59 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location.

Register Name	Part 60 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART60_REGISTER
Address	000000000001803C (SCOM)
Description	Contains part 60 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location.

Register Name	Part 61 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART61_REGISTER
Address	000000000001803D (SCOM)
Description	Contains part 61 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location.

Register Name	Part 62 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART62_REGISTER
Address	000000000001803E (SCOM)
Description	Contains part 62 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location.

Register Name	Part 63 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#0.OTPROM.ECID_PART63_REGISTER
Address	000000000001803F (SCOM)
Description	Contains part 63 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location.

Register Name	Part 0 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART0_REGISTER
Address	0000000000018040 (SCOM)
Description	Contains part 0 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location.

Register Name	Part 1 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART1_REGISTER
Address	0000000000018041 (SCOM)
Description	Contains part 1 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location.

Register Name	Part 2 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART2_REGISTER
Address	0000000000018042 (SCOM)
Description	Contains part 2 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location.

Register Name	Part 3 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART3_REGISTER
Address	0000000000018043 (SCOM)
Description	Contains part 3 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location.

Register Name	Part 4 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART4_REGISTER
Address	0000000000018044 (SCOM)
Description	Contains part 4 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location.

Register Name	Part 5 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART5_REGISTER
Address	0000000000018045 (SCOM)
Description	Contains part 5 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location.

Register Name	Part 6 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART6_REGISTER
Address	0000000000018046 (SCOM)
Description	Contains part 6 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location.

Register Name	Part 7 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART7_REGISTER
Address	0000000000018047 (SCOM)
Description	Contains part 7 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location.

Register Name	Part 8 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART8_REGISTER
Address	0000000000018048 (SCOM)
Description	Contains part 8 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location.

Register Name	Part 9 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART9_REGISTER
Address	0000000000018049 (SCOM)
Description	Contains part 9 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location.

Register Name	Part 10 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART10_REGISTER
Address	000000000001804A (SCOM)
Description	Contains part 10 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location.

Register Name	Part 11 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART11_REGISTER
Address	000000000001804B (SCOM)
Description	Contains part 11 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location.

Register Name	Part 12 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART12_REGISTER
Address	000000000001804C (SCOM)
Description	Contains part 12 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location.

Register Name	Part 13 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART13_REGISTER
Address	000000000001804D (SCOM)
Description	Contains part 13 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location.

Register Name	Part 14 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART14_REGISTER
Address	000000000001804E (SCOM)
Description	Contains part 14 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location.

Register Name	Part 15 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART15_REGISTER
Address	000000000001804F (SCOM)
Description	Contains part 15 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location.

Register Name	Part 16 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART16_REGISTER
Address	0000000000018050 (SCOM)
Description	Contains part 16 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location.

Register Name	Part 17 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART17_REGISTER
Address	0000000000018051 (SCOM)
Description	Contains part 17 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location.

Register Name	Part 18 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART18_REGISTER
Address	0000000000018052 (SCOM)
Description	Contains part 18 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location.

Register Name	Part 19 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART19_REGISTER
Address	0000000000018053 (SCOM)
Description	Contains part 19 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location.

Register Name	Part 20 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART20_REGISTER
Address	0000000000018054 (SCOM)
Description	Contains part 20 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location.

Register Name	Part 21 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART21_REGISTER
Address	0000000000018055 (SCOM)
Description	Contains part 21 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location.

Register Name	Part 22 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART22_REGISTER
Address	0000000000018056 (SCOM)
Description	Contains part 22 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location.

Register Name	Part 23 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART23_REGISTER
Address	0000000000018057 (SCOM)
Description	Contains part 23 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location.

Register Name	Part 24 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART24_REGISTER
Address	0000000000018058 (SCOM)
Description	Contains part 24 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location.

Register Name	Part 25 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART25_REGISTER
Address	0000000000018059 (SCOM)
Description	Contains part 25 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location.

Register Name	Part 26 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART26_REGISTER
Address	000000000001805A (SCOM)
Description	Contains part 26 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location.

Register Name	Part 27 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART27_REGISTER
Address	000000000001805B (SCOM)
Description	Contains part 27 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location.

Register Name	Part 28 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART28_REGISTER
Address	000000000001805C (SCOM)
Description	Contains part 28 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location.

Register Name	Part 29 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART29_REGISTER
Address	000000000001805D (SCOM)
Description	Contains part 29 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location.

Register Name	Part 30 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART30_REGISTER
Address	000000000001805E (SCOM)
Description	Contains part 30 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location.

Register Name	Part 31 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART31_REGISTER
Address	000000000001805F (SCOM)
Description	Contains part 31 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location.

Register Name	Part 32 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART32_REGISTER
Address	0000000000018060 (SCOM)
Description	Contains part 32 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location.

Register Name	Part 33 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART33_REGISTER
Address	0000000000018061 (SCOM)
Description	Contains part 33 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location.

Register Name	Part 34 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART34_REGISTER
Address	0000000000018062 (SCOM)
Description	Contains part 34 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location.

Register Name	Part 35 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART35_REGISTER
Address	0000000000018063 (SCOM)
Description	Contains part 35 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location.

Register Name	Part 36 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART36_REGISTER
Address	0000000000018064 (SCOM)
Description	Contains part 36 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location.

Register Name	Part 37 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART37_REGISTER
Address	0000000000018065 (SCOM)
Description	Contains part 37 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location.

Register Name	Part 38 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART38_REGISTER
Address	0000000000018066 (SCOM)
Description	Contains part 38 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location.

Register Name	Part 39 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART39_REGISTER
Address	0000000000018067 (SCOM)
Description	Contains part 39 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location.

Register Name	Part 40 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART40_REGISTER
Address	0000000000018068 (SCOM)
Description	Contains part 40 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location.

Register Name	Part 41 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART41_REGISTER
Address	0000000000018069 (SCOM)
Description	Contains part 41 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location.

Register Name	Part 42 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART42_REGISTER
Address	000000000001806A (SCOM)
Description	Contains part 42 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location.

Register Name	Part 43 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART43_REGISTER
Address	000000000001806B (SCOM)
Description	Contains part 43 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location.

Register Name	Part 44 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART44_REGISTER
Address	000000000001806C (SCOM)
Description	Contains part 44 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location.

Register Name	Part 45 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART45_REGISTER
Address	000000000001806D (SCOM)
Description	Contains part 45 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location.

Register Name	Part 46 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART46_REGISTER
Address	000000000001806E (SCOM)
Description	Contains part 46 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location.

Register Name	Part 47 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART47_REGISTER
Address	000000000001806F (SCOM)
Description	Contains part 47 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location.

Register Name	Part 48 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART48_REGISTER
Address	0000000000018070 (SCOM)
Description	Contains part 48 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location.

Register Name	Part 49 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART49_REGISTER
Address	0000000000018071 (SCOM)
Description	Contains part 49 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location.

Register Name	Part 50 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART50_REGISTER
Address	0000000000018072 (SCOM)
Description	Contains part 50 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location.

Register Name	Part 51 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART51_REGISTER
Address	0000000000018073 (SCOM)
Description	Contains part 51 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location.

Register Name	Part 52 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART52_REGISTER
Address	0000000000018074 (SCOM)
Description	Contains part 52 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location.

Register Name	Part 53 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART53_REGISTER
Address	0000000000018075 (SCOM)
Description	Contains part 53 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location.

Register Name	Part 54 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART54_REGISTER
Address	0000000000018076 (SCOM)
Description	Contains part 54 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location.

Register Name	Part 55 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART55_REGISTER
Address	0000000000018077 (SCOM)
Description	Contains part 55 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location.

Register Name	Part 56 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART56_REGISTER
Address	0000000000018078 (SCOM)
Description	Contains part 56 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location.

Register Name	Part 57 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART57_REGISTER
Address	0000000000018079 (SCOM)
Description	Contains part 57 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location.

Register Name	Part 58 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART58_REGISTER
Address	000000000001807A (SCOM)
Description	Contains part 58 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location.

Register Name	Part 59 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART59_REGISTER
Address	000000000001807B (SCOM)
Description	Contains part 59 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location.

Register Name	Part 60 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART60_REGISTER
Address	000000000001807C (SCOM)
Description	Contains part 60 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location.

Register Name	Part 61 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART61_REGISTER
Address	000000000001807D (SCOM)
Description	Contains part 61 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location.

Register Name	Part 62 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART62_REGISTER
Address	000000000001807E (SCOM)
Description	Contains part 62 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location.

Register Name	Part 63 of the eFUSE
Mnemonic	TP.TPCHIP.OTPROM.MULT_OTPROM_WITH_ECC.OTPROM_GEN#1.OTPROM.ECID_PART63_REGISTER
Address	000000000001807F (SCOM)
Description	Contains part 63 of the eFUSE.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location.

Register Name	FSI PIB2OPB Command and Write Data
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CMD_WRDAT
Address	0000000000020000 (SCOM)
Description	The PIB2OPB Command and Write Data register is used to access FSI master ports through the PIB. FSI0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0	RW	WRITE_NOT_READ: Write not read.
1:31	RW	Reserved field.
32:63	RW	Reserved field.

Register Name	FSI PIB2OPB Status and Read Data
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.STAT_RDDAT_ERRES
Address	0000000000020001 (SCOM)
Description	The PIB2OPB Status and Read Data register is used to access FSI master ports by using the PIB. FSI0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0	RO	Reserved field.
1	RO	CMD_PARITY_ERROR: Command parity check.
2	RO	WR_DATA_PARITY_ERROR: Write data parity check.
3	RO	RD_DATA_PARITY_ERROR: Read data parity check.
4	RO	LCK_STATUS_PARITY_ERROR: Locked status parity check.
5	RO	FSM_PARITY_ERROR: OPB master protocol FSM parity check.
6	RO	Reserved.
7	RO	Reserved field.
8	RO	OPB_PARITY_ERROR: OPB read data parity check during valid.
9	RO	Reserved field.
10	RO	Reserved field.
11	RO	Reserved field.
12	RO	Reserved field.
13	RO	Reserved field.
14	RO	Reserved field.
15	RO	Reserved field.
16	RO	Reserved field.
17	RO	Reserved field.
18	RO	Reserved field.
19	RO	Reserved field.
20	RO	Reserved field.
21	RO	Reserved field.
22:23	RO	Reserved.
24	RO	Reserved field.
25	RO	Reserved field.
26	RO	Reserved field.
27	RO	Reserved field.
28	RO	Reserved field.
29	RO	Reserved field.
30:31	RO	Reserved.
32:63	RO	Reserved field.

Register Name	FSI PIB2OPB Locked Status
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.LSTAT
Address	0000000000020002 (SCOM)
Description	PIB2OPB FSI master ports locked status through the PIB. FSI0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Reserved.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PIB2OPB Unit Reset
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.RESET
Address	0000000000020004 (SCOM)
Description	PIB2OPB unit reset.

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Unit reset.

Register Name	FSI PIB2OPB cMFSI Remote Slave Interrupt
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CRSIC
Address	0000000000020005 (SCOM)
Description	PIB2OPB interrupts of the cMFSI port. Attached FSI slaves are read and cleared by using the PIB. FSI0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW_WCLEAR	Reserved.

Register Name	FSI PIB2OPB cMFSI Remote Slave Interrupt Mask
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CRSIM
Address	0000000000020006 (SCOM)
Description	PIB2OPB mask for interrupts of the cMFSI port. Attached FSI slaves are read and written by using the PIB. FSI0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	FSI PIB2OPB cMFSI Remote Slave Interrupt Status
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CRSIS
Address	0000000000020007 (SCOM)
Description	PIB2OPB status of interrupts of the cMFSI port. Attached FSI slaves PIB are read by using the PIB. FSI0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Reserved.

Register Name	FSI PIB2OPB MFSI Remote Slave Interrupt
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.RSIC
Address	0000000000020008 (SCOM)
Description	PIB2OPB interrupts of the MFSI port. Attached FSI slaves are read and cleared by using the PIB. FSI0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW_WCLEAR	Reserved.

Register Name	FSI PIB2OPB MFSI Remote Slave Interrupt Mask
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.RSIM
Address	0000000000020009 (SCOM)
Description	PIB2OPB mask for interrupts of the MFSI port. Attached FSI slaves are read and written by using PIB. FSI0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	FSI PIB2OPB MFSI Remote Slave Interrupt Status
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.RSIS
Address	000000000002000A (SCOM)
Description	PIB2OPB status of Interrupts of MFSI port. Attached FSI slaves PIB read is by using the PIB. FSI0 host access through ports and lower address is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Reserved.

Register Name	FSI PIB2OPB Command and Write Data
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.CMD_WRDAT
Address	0000000000020010 (SCOM)
Description	PIB2OPB Command and Write-Data Register is used to access the FSI master ports by using the PIB. FSI0 host accesses through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0	RW	WRITE_NOT_READ: Write not read.
1:31	RW	Reserved field.
32:63	RW	Reserved field.

Register Name	FSI PIB2OPB Status and Read Data
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.STAT_RDDAT_ERRES
Address	0000000000020011 (SCOM)
Description	PIB2OPB Status and Read-Data register is used to access the FSI master ports by using the PIB. FSI0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0	RO	Reserved field.
1	RO	CMD_PARITY_ERROR: Command parity check.
2	RO	WR_DATA_PARITY_ERROR: Write data parity check.
3	RO	RD_DATA_PARITY_ERROR: Read data parity check.
4	RO	LCK_STATUS_PARITY_ERROR: Locked status parity check.
5	RO	FSM_PARITY_ERROR: OPB master protocol FSM parity check.
6	RO	Reserved.
7	RO	Reserved field.
8	RO	OPB_PARITY_ERROR: OPB read data parity check during valid.
9	RO	Reserved field.
10	RO	Reserved field.
11	RO	Reserved field.
12	RO	Reserved field.
13	RO	Reserved field.
14	RO	Reserved field.
15	RO	Reserved field.
16	RO	Reserved field.
17	RO	Reserved field.
18	RO	Reserved field.
19	RO	Reserved field.
20	RO	Reserved field.
21	RO	Reserved field.
22:23	RO	Reserved.
24	RO	Reserved field.
25	RO	Reserved field.
26	RO	Reserved field.
27	RO	Reserved field.
28	RO	Reserved field.
29	RO	Reserved field.
30:31	RO	Reserved.
32:63	RO	Reserved field.

Register Name	FSI PIB2OPB Locked Status
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.LSTAT
Address	0000000000020012 (SCOM)
Description	PIB2OPB FSI master ports lock status is shown by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Reserved.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PIB2OPB Unit Reset
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.RESET
Address	0000000000020014 (SCOM)
Description	PIB2OPB unit reset

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Unit reset.

Register Name	FSI PIB2OPB cMFSI Remote Slave Interrupt
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.CRSIC
Address	0000000000020015 (SCOM)
Description	PIB2OPB interrupts of the cMFSI port. Attached FSI slaves are read and cleared by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW_WCLEAR	Reserved.

Register Name	FSI PIB2OPB cMFSI Remote Slave Interrupt Mask
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.CRSIM
Address	0000000000020016 (SCOM)
Description	PIB2OPB mask for interrupts of the cMFSI port. Attached FSI slaves are read and written by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	FSI PIB2OPB cMFSI Remote Slave Interrupt Status
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.CRSIS
Address	0000000000020017 (SCOM)
Description	PIB2OPB status of interrupts of cMFSI port. Attached FSI slaves PIB are read by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Reserved.

Register Name	FSI PIB2OPB MFSI Remote Slave Interrupt
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.RSIC
Address	0000000000020018 (SCOM)
Description	PIB2OPB Interrupts of MFSI port. Attached FSI slaves are read and cleared by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW_WCLEAR	Reserved.

Register Name	FSI PIB2OPB MFSI Remote Slave Interrupt Mask
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.RSIM
Address	0000000000020019 (SCOM)
Description	PIB2OPB mask for interrupts of the MFSI port. Attached FSI slaves are read and written by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	FSI PIB2OPB MFSI Remote Slave Interrupt Status
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#1.P.RSIS
Address	000000000002001A (SCOM)
Description	PIB2OPB status of interrupts of MFSI port. Attached FSI slaves PIB are read by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Reserved.

Register Name	FSI PIB2OPB Command and Write Data
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CMD_WRDAT
Address	0000000000030000 (SCOM)
Description	The PIB2OPB command and write-data register is used to access FSI Master ports by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0	RW	WRITE_NOT_READ: Write not read.
1:31	RW	Reserved field.
32:63	RW	Reserved field.

Register Name	FSI PIB2OPB Status and Read Data
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.STAT_RDDAT_ERRES
Address	0000000000030001 (SCOM)
Description	The PIB2OPB status and read data register is used to access FSI master ports by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0	RO	Reserved field.
1	RO	CMD_PARITY_ERROR: Command parity check.
2	RO	WR_DATA_PARITY_ERROR: Write data parity check.
3	RO	RD_DATA_PARITY_ERROR: Read data parity check.
4	RO	LCK_STATUS_PARITY_ERROR: Locked status parity check.
5	RO	FSM_PARITY_ERROR: OPB master protocol FSM parity check.
6	RO	Reserved.
7	RO	Reserved field.
8	RO	OPB_PARITY_ERROR: OPB read data parity check during valid.
9	RO	Reserved field.
10	RO	Reserved field.
11	RO	Reserved field.
12	RO	Reserved field.
13	RO	Reserved field.
14	RO	Reserved field.
15	RO	Reserved field.
16	RO	Reserved field.
17	RO	Reserved field.
18	RO	Reserved field.
19	RO	Reserved field.
20	RO	Reserved field.
21	RO	Reserved field.
22:23	RO	Reserved.
24	RO	Reserved field.
25	RO	Reserved field.
26	RO	Reserved field.
27	RO	Reserved field.
28	RO	Reserved field.
29	RO	Reserved field.
30:31	RO	Reserved.
32:63	RO	Reserved field.

Register Name	FSI PIB2OPB Locked Status
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.LSTAT
Address	0000000000030002 (SCOM)
Description	PIB2OPB FSI Master ports locked status by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Reserved.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PIB2OPB Unit Reset
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RESET
Address	0000000000030004 (SCOM)
Description	PIB2OPB unit reset

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Unit reset.

Register Name	FSI PIB2OPB cMFSI Remote Slave Interrupt
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIC
Address	0000000000030005 (SCOM)
Description	PIB2OPB Interrupts of cMFSI port. Attached FSI slaves are read and cleared by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW_WCLEAR	Reserved.

Register Name	FSI PIB2OPB cMFSI Remote Slave Interrupt Mask
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIM
Address	0000000000030006 (SCOM)
Description	PIB2OPB Mask for Interrupts of cMFSI port. Attached FSI slaves are read and written by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	FSI PIB2OPB cMFSI Remote Slave Interrupt Status
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIS
Address	0000000000030007 (SCOM)
Description	PIB2OPB Status of Interrupts of cMFSI port. Attached FSI slaves PIB are read by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Reserved.

Register Name	FSI PIB2OPB MFSI Remote Slave Interrupt
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIC
Address	0000000000030008 (SCOM)
Description	PIB2OPB interrupts of MFSI port. Attached FSI slaves are read and cleared by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW_WCLEAR	Reserved.

Register Name	FSI PIB2OPB MFSI Remote Slave Interrupt Mask
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIM
Address	0000000000030009 (SCOM)
Description	PIB2OPB mask for interrupts of the MFSI port. Attached FSI slaves are read and written by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	FSI PIB2OPB MFSI Remote Slave Interrupt Status
Mnemonic	TP.TPVSB.FSI.W.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIS
Address	000000000003000A (SCOM)
Description	PIB2OPB Status of Interrupts of MFSI port. Attached FSI slaves PIB are read by using the PIB. FSI 0 host access through ports and lower addresses is for the host only.

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Reserved.

Register Name	TOD: Setup for Master Paths Control Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_M_PATH_CTRL_REG
Address	0000000000040000 (SCOM)
Description	Used for oscillator validity, step alignment, sync pulse frequency, and step check.

Bits	SCOM	Field Mnemonic: Description
0	RW	M_PATH_0_OSC_NOT_VALID: Indicates whether the oscillator attached to master path-0 is not valid. 0 = Valid oscillator is attached to master path-0. 1 = No valid oscillator is attached to master path-0.
1	RW	M_PATH_1_OSC_NOT_VALID: Indicates whether the oscillator attached to master path-1 is not valid. 0 = Valid oscillator is attached to master path-1. 1 = No valid oscillator is attached to master path-1.

Bits	SCOM	Field Mnemonic: Description
2	RW	M_PATH_0_STEP_ALIGN_DISABLE: Master path-0. Indicates alignment of master path-0 step to master path-1 step is active 0 = Alignment of master path-0 step to master path-1 step is active. 1 = Alignment of master path-0 step to master path-1 Step is not active.
3	RW	M_PATH_1_STEP_ALIGN_DISABLE: Indicates whether alignment of master path-1 step to master path-0 step is active. 0 = Alignment of master path-1 step to master path-0 step is active. 1 = Alignment of master path-1 step to master path-0 step is not active.
4	RW	M_PATH_STEP_CREATE_DUAL_EDGE_DISABLE: For master path-01 step creation, determines whether both edges or only the rising edge of the oscillator is sampled. 0 = Sample both edges of the oscillator. 1 = Sample only the rising edge of the oscillator.
5:7	RW	M_PATH_SYNC_CREATE_SPS_SELECT: Master path: sync create: steps per sync (SPS) select: number of STEP pulses per SYNC pulse.
8:11	RW	M_PATH_0_STEP_CHECK_CPS_DEVIATION: Master path-0: step check: CPS deviation.
12	RW	M_PATH_0_STEP_CHECK_CONSTANT_CPS_ENABLE: Determines whether measured CPS or constant CPS is used for step check CPS deviation for master path 0. 0 = Measured CPS is used for the step check CPS deviation 1 = Constant CPS is used for the step check CPS deviation
13:15	RW	M_PATH_0_STEP_CHECK_VALIDITY_COUNT: Master path-0 step check. Specifies the number of received steps before the step is declared as valid.
16:19	RW	M_PATH_1_STEP_CHECK_CPS_DEVIATION: The CPS deviation for master path-1 step check.
20	RW	M_PATH_1_STEP_CHECK_CONSTANT_CPS_ENABLE: Determines whether measured CPS or constant CPS is used for step check CPS deviation for master path 1. 0 = Measured CPS is used for the step check CPS deviation 1 = Constant CPS is used for the step check CPS deviation.
21:23	RW	M_PATH_1_STEP_CHECK_VALIDITY_COUNT: Master path-1: step check: validity count. Defines the number of received steps before the step is declared as valid.
24:25	RW	M_PATH_STEP_CHECK_CPS_DEVIATION_FACTOR: Master path-01: step check: CPS deviation factor.
26	RW	M_PATH_0_LOCAL_STEP_MODE_ENABLE: Master path-0: local step mode: enable. 0 = Steps are generated from the 16 MHz oscillator-0. 1 = Steps are generated locally using the mesh clock.
27	RW	M_PATH_1_LOCAL_STEP_MODE_ENABLE: Master path-1: local step mode: enable. 0 = Steps are generated from the 16 MHz oscillator-0. 1 = Steps are generated locally using the mesh clock.
28	RW	M_PATH_0_STEP_STEER_ENABLE: Master path-0: step steering enable. 0 = Steering of master path-0 step is not active. 1 = Steering of master path-0 step is active.
29	RW	M_PATH_1_STEP_STEER_ENABLE: Master path-1: step steering enable. 0 = Steering of master path-1 step is not active. 1 = Steering of master path-1 step is active.
30:31	RW	REG_0X00_SPARE_30_31: Spares.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**TOD: Primary Configuration Distribution Port Control Register 0**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_PRI_PORT_0_CTRL_REG
Address	0000000000040001 (SCOM)
Description	Control register 0 for the primary configuration distribution port.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	PRI_PORT_0_RX_SELECT: Distribution: primary configuration: port-0 RX select.
3	RW	REG_0X01_SPARE_03: Spares.
4:5	RWX	PRI_X0_PORT_0_TX_SELECT: Distribution: primary configuration: X0 port-0 TX select.
6:7	RWX	PRI_X1_PORT_0_TX_SELECT: Distribution: primary configuration: X1 port-0 TX select.
8:9	RWX	PRI_X2_PORT_0_TX_SELECT: Distribution: primary configuration: X2 port-0 TX select.
10:11	RWX	PRI_X3_PORT_0_TX_SELECT: Distribution: primary configuration: X3 port-0 TX select.
12:13	RWX	PRI_X4_PORT_0_TX_SELECT: Distribution: primary configuration: X4 port-0 TX select.
14:15	RWX	PRI_X5_PORT_0_TX_SELECT: Distribution: primary configuration: X5 port-0 TX select.
16:17	RWX	PRI_X6_PORT_0_TX_SELECT: Distribution: primary configuration: X6 port-0 TX select.
18:19	RWX	PRI_X7_PORT_0_TX_SELECT: Distribution: primary configuration: X7 port-0 TX select.
20	RW	PRI_X0_PORT_0_TX_ENABLE: Distribution: primary configuration: X0 port-0 TX enable. 0 = Port configured as receiver. 1 = Port configured as sender.
21	RW	PRI_X1_PORT_0_TX_ENABLE: Distribution: primary configuration: X1 port-0 TX enable. 0 = Port configured as receiver. 1 = Port configured as sender.
22	RW	PRI_X2_PORT_0_TX_ENABLE: Distribution: primary configuration: X2 port-0 TX enable. 0 = Port configured as receiver. 1 = Port configured as sender.
23	RW	PRI_X3_PORT_0_TX_ENABLE: Distribution: primary configuration: X3 port-0 TX enable. 0 = Port configured as receiver. 1 = Port configured as sender.
24	RW	PRI_X4_PORT_0_TX_ENABLE: Distribution: primary configuration: X4 port-0 TX enable. 0 = Port configured as receiver. 1 = Port configured as sender.
25	RW	PRI_X5_PORT_0_TX_ENABLE: Distribution: primary configuration: X5 port-0 TX enable. 0 = Port configured as receiver. 1 = Port configured as sender.
26	RW	PRI_X6_PORT_0_TX_ENABLE: Distribution: primary configuration: X6 port-0 TX enable. 0 = Port configured as receiver. 1 = Port configured as sender.
27	RW	PRI_X7_PORT_0_TX_ENABLE: Distribution: primary configuration: X7 port-0 TX enable. 0 = Port configured as receiver. 1 = Port configured as sender.
28:31	RW	REG_0X01_SPARE_28_31: Spares.
32:39	RW	PRI_I_PATH_DELAY_VALUE: Internal path: primary configuration: delay value.
40:63	RO	constant = 0b000000000000000000000000

Register Name	**TOD: Primary Configuration Distribution Port Control Register 1**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_PRI_PORT_1_CTRL_REG
Address	0000000000040002 (SCOM)
Description	Control register 1 for the primary configuration distribution port.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	PRI_PORT_1_RX_SELECT: Distribution: primary configuration: port-1 RX select.

Bits	SCOM	Field Mnemonic: Description
3	RW	REG_0X02_SPARE_03: Spares.
4:5	RWX	PRI_X0_PORT_1_TX_SELECT: Distribution: primary configuration: X0 port-1 TX select.
6:7	RWX	PRI_X1_PORT_1_TX_SELECT: Distribution: primary configuration: X1 port-1 TX select.
8:9	RWX	PRI_X2_PORT_1_TX_SELECT: Distribution: primary configuration: X2 port-1 TX select.
10:11	RWX	PRI_X3_PORT_1_TX_SELECT: Distribution: primary configuration: X3 port-1 TX select.
12:13	RWX	PRI_X4_PORT_1_TX_SELECT: Distribution: primary configuration: X4 port-1 TX select.
14:15	RWX	PRI_X5_PORT_1_TX_SELECT: Distribution: primary configuration: X5 port-1 TX select.
16:17	RWX	PRI_X6_PORT_1_TX_SELECT: Distribution: primary configuration: X6 port-1 TX select.
18:19	RWX	PRI_X7_PORT_1_TX_SELECT: Distribution: primary configuration: X7 port-1 TX select.
20	RW	PRI_X0_PORT_1_TX_ENABLE: Distribution: primary configuration: X0 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
21	RW	PRI_X1_PORT_1_TX_ENABLE: Distribution: primary configuration: X1 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
22	RW	PRI_X2_PORT_1_TX_ENABLE: Distribution: primary configuration: X2 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
23	RW	PRI_X3_PORT_1_TX_ENABLE: Distribution: primary configuration: X3 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
24	RW	PRI_X4_PORT_1_TX_ENABLE: Distribution: primary configuration: X4 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
25	RW	PRI_X5_PORT_1_TX_ENABLE: Distribution: primary configuration: X5 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
26	RW	PRI_X6_PORT_1_TX_ENABLE: Distribution: primary configuration: X6 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
27	RW	PRI_X7_PORT_1_TX_ENABLE: Distribution: primary configuration: X7 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
28:31	RW	REG_0X02_SPARE_28_31: Spares.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**TOD: Secondary Configuration Distribution Port Control Register 0**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_SEC_PORT_0_CTRL_REG
Address	0000000000040003 (SCOM)
Description	Control register 0 for the secondary configuration distribution port.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SEC_PORT_0_RX_SELECT: Distribution: secondary configuration: port-0 RX select.
3	RW	REG_0X03_SPARE_03: Spares.
4:5	RWX	SEC_X0_PORT_0_TX_SELECT: Distribution: secondary configuration: X0 port-0 TX select.

Bits	SCOM	Field Mnemonic: Description
6:7	RWX	SEC_X1_PORT_0_TX_SELECT: Distribution: secondary configuration: X1 port-0 TX select.
8:9	RWX	SEC_X2_PORT_0_TX_SELECT: Distribution: secondary configuration: X2 port-0 TX select.
10:11	RWX	SEC_X3_PORT_0_TX_SELECT: Distribution: secondary configuration: X3 port-0 TX select.
12:13	RWX	SEC_X4_PORT_0_TX_SELECT: Distribution: secondary configuration: X4 port-0 TX select.
14:15	RWX	SEC_X5_PORT_0_TX_SELECT: Distribution: secondary configuration: X5 port-0 TX select.
16:17	RWX	SEC_X6_PORT_0_TX_SELECT: Distribution: secondary configuration: X6 port-0 TX select.
18:19	RWX	SEC_X7_PORT_0_TX_SELECT: Distribution: secondary configuration: X7 port-0 TX select.
20	RW	SEC_X0_PORT_0_TX_ENABLE: Distribution: secondary configuration: X0 port-0 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
21	RW	SEC_X1_PORT_0_TX_ENABLE: Distribution: secondary configuration: X1 port-0 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
22	RW	SEC_X2_PORT_0_TX_ENABLE: Distribution: secondary configuration: X2 port-0 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
23	RW	SEC_X3_PORT_0_TX_ENABLE: Distribution: secondary configuration: X3 port-0 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
24	RW	SEC_X4_PORT_0_TX_ENABLE: Distribution: secondary configuration: X4 port-0 TX enable 0 = Port configured as receiver 1 = Port configured as sender.
25	RW	SEC_X5_PORT_0_TX_ENABLE: Distribution: secondary configuration: X5 port-0 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
26	RW	SEC_X6_PORT_0_TX_ENABLE: Distribution: secondary configuration: X6 port-0 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
27	RW	SEC_X7_PORT_0_TX_ENABLE: Distribution: secondary configuration: X7 port-0 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
28:31	RW	REG_0X03_SPARE_28_31: Spares.
32:39	RW	SEC_I_PATH_DELAY_VALUE: Internal path: secondary configuration: delay value.
40:63	RO	constant = 0b000000000000000000000000

Register Name	TOD: Secondary Configuration Distribution Port Control Register 1
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_SEC_PORT_1_CTRL_REG
Address	0000000000040004 (SCOM)
Description	Control register 1 for the secondary configuration distribution port.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SEC_PORT_1_RX_SELECT: Distribution: secondary configuration: port-1 RX select.
3	RW	REG_0X04_SPARE_03: Spares.
4:5	RWX	SEC_X0_PORT_1_TX_SELECT: Distribution: secondary configuration: X0 port-1 TX select.
6:7	RWX	SEC_X1_PORT_1_TX_SELECT: Distribution: secondary configuration: X1 port-1 TX select.

Bits	SCOM	Field Mnemonic: Description
8:9	RWX	SEC_X2_PORT_1_TX_SELECT: Distribution: secondary configuration: X2 port-1 TX select.
10:11	RWX	SEC_X3_PORT_1_TX_SELECT: Distribution: secondary configuration: X3 port-1 TX select.
12:13	RWX	SEC_X4_PORT_1_TX_SELECT: Distribution: secondary configuration: X4 port-1 TX select.
14:15	RWX	SEC_X5_PORT_1_TX_SELECT: Distribution: secondary configuration: X5 port-1 TX select.
16:17	RWX	SEC_X6_PORT_1_TX_SELECT: Distribution: secondary configuration: X6 port-1 TX select.
18:19	RWX	SEC_X7_PORT_1_TX_SELECT: Distribution: secondary configuration: X7 port-1 TX select.
20	RW	SEC_X0_PORT_1_TX_ENABLE: Distribution: secondary configuration: X0 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
21	RW	SEC_X1_PORT_1_TX_ENABLE: Distribution: secondary configuration: X1 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
22	RW	SEC_X2_PORT_1_TX_ENABLE: Distribution: secondary configuration: X2 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
23	RW	SEC_X3_PORT_1_TX_ENABLE: Distribution: secondary configuration: X3 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
24	RW	SEC_X4_PORT_1_TX_ENABLE: Distribution: secondary configuration: X4 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
25	RW	SEC_X5_PORT_1_TX_ENABLE: Distribution: secondary configuration: X5 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
26	RW	SEC_X6_PORT_1_TX_ENABLE: Distribution: secondary configuration: X6 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
27	RW	SEC_X7_PORT_1_TX_ENABLE: Distribution: secondary configuration: X7 port-1 TX enable 0 = Port configured as receiver. 1 = Port configured as sender.
28:31	RW	REG_0X04_SPARE_28_31: Spares.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	TOD: Slave Path Control Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_S_PATH_CTRL_REG
Address	0000000000040005 (SCOM)
Description	TOD: Slave Path Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	PRI_S_PATH_SELECT: Primary configuration: slave path select.
1	RW	REG_0X05_SPARE_01: Spares.
2	RW	S_PATH_M_PATH_CPS_ENABLE: Slave path-01: use of master path CPS: enable. 0 = Do not use master path CPS. 1 = Use master path CPS.

Bits	SCOM	Field Mnemonic: Description
3	RW	S_PATH_REMOTE_SYNC_DISABLE: Slave path-01: remote sync: disable. 0 = Use Syncs from master TOD. Steps are generated locally. 1 = Use steps-syncs from master TOD.
4	RW	SEC_S_PATH_SELECT: Secondary configuration: slave path select.
5	RW	REG_0X05_SPARE_05: Spares.
6:7	RW	S_PATH_STEP_CHECK_CPS_DEVIATION_FACTOR: Slave path-01: step check: CPS deviation factor.
8:11	RW	S_PATH_0_STEP_CHECK_CPS_DEVIATI1 = Slave path-0: step check: CPS deviation.
12	RW	S_PATH_0_STEP_CHECK_CONSTANT_CPS_ENABLE: Slave path-0: step check: constant CPS enable 0 = Measured CPS is used for the step check CPS deviation 1 = Constant CPS is used for the step check CPS deviation
13:15	RW	S_PATH_0_STEP_CHECK_VALIDITY_COUNT: Slave path-0: step check: validity count. Defines the number of received steps before the step is declared as valid is enabled.
16:19	RW	S_PATH_1_STEP_CHECK_CPS_DEVIATION: Slave path-1: Step check: CPS deviation.
20	RW	S_PATH_1_STEP_CHECK_CONSTANT_CPS_ENABLE: Slave path-1: Step check: constant CPS enable 0 = Measured CPS is used for the step check CPS deviation. 1 = Constant CPS is used for the step check CPS deviation.
21:23	RW	S_PATH_1_STEP_CHECK_VALIDITY_COUNT: Slave path-1: Step check: validity count. Defines the number of received steps before the step is declared as valid.
24	RW	S_PATH_REMOTE_SYNC_ERROR_DISABLE: Slave path-01: Remote sync: Error disable. 0 = Enable remote sync error as a step error. 1 = Do not enable remote sync error as a step error.
25	RW	S_PATH_REMOTE_SYNC_CHECK_M_CPS_DISABLE: Slave path-01: Remote sync: sync-step check: disable use of master path CPS. 0 = Use master path CPS. 1 = Do not use master path CPS.
26:27	RW	S_PATH_REMOTE_SYNC_CHECK_CPS_DEVIATION_FACTOR: Slave path-01: remote sync: sync-step check: CPS deviation factor.
28:31	RW	S_PATH_REMOTE_SYNC_CHECK_CPS_DEVIATION: Slave path-01: remote sync: sync-step check: CPS deviation.
32:39	RW	S_PATH_REMOTE_SYNC_MISS_COUNT_MAX: Slave path-01: remote sync: maximum of SYNC miss counts: 0 - 255 syncs.
40:63	RO	constant = 0b000000000000000000000000

Register Name	TOD: Internal Path Control Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_I_PATH_CTRL_REG
Address	0000000000040006 (SCOM)
Description	TOD: Internal Path Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	I_PATH_DELAY_DISABLE: Internal path: delay disable. 0 = Delay enabled. 1 = Delay disabled.
1	RW	I_PATH_DELAY_ADJUST_DISABLE: Internal path: delay adjust disable. 0 = Delay adjust enabled. 1 = Delay adjust disabled.
2:4	RW	REG_0X06_SPARE_02_04: Spares.

Bits	SCOM	Field Mnemonic: Description
5	RW	I_PATH_STEP_CHECK_STEP_SELECT: Internal path: step check: step select. 0 = Step from master or slave path is checked. 1 = Step sent to the core is checked.
6:7	RWX	I_PATH_STEP_CHECK_CPS_DEVIATION_FACTOR: Internal path: step check: CPS deviation factor.
8:11	RW	I_PATH_STEP_CHECK_CPS_DEVIATION: Internal path: step check: CPS deviation.
12	RW	I_PATH_STEP_CHECK_CONSTANT_CPS_ENABLE: Internal path: step check: constant CPS enable. 0 = Measured CPS is used for the step check CPS deviation. 1 = Constant CPS is used for the step check CPS deviation.
13:15	RW	I_PATH_STEP_CHECK_VALIDITY_COUNT: Internal path: step check: validity count. Defines the number of received steps before the step is declared as valid.
16:21	RW	REG_0X06_SPARE_16_21: Spares.
22:31	ROX	I_PATH_DELAY_ADJUST_VALUE: Internal path: adjusted delay value. If the adjustment is enable, the value indicates the adjusted delay value otherwise it indicates the raw delay (primary or secondary).
32:39	RWX	I_PATH_CPS: Internal path: CPS In write mode, the value is used to load the CPS for the constant CPS for the step checker. In read mode the value shows the actual CPS in the internal path.
40:63	RO	constant = 0b000000000000000000000000

Register Name	**TOD: Primary/Secondary Configuration Control Register**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_PSS_MSS_CTRL_REG
Address	0000000000040007 (SCOM)
Description	Master/slave select: master path select: slave path select: step check setup

Bits	SCOM	Field Mnemonic: Description
0	RWX	PRI_M_PATH_SELECT: Primary configuration: master path select. 0 = Master path-0 is selected. 1 = Master path-1 is selected.
1	RWX	PRI_M_S_TOD_SELECT: Primary configuration: master-slave TOD select. 0 = TOD is slave. 1 = TOD is master.
2	RWX	PRI_M_S_DRAWER_SELECT: Primary configuration: master-slave drawer select. 0 = Drawer is slave. 1 = Drawer is master It is just used for TOD internal power gating.
3	RWX	PRI_S_PATH_1_STEP_CHECK_ENABLE: Primary configuration: slave path-1: step check enable. 0 = Step check disabled. 1 = Step check enabled.
4	RWX	PRI_M_PATH_0_STEP_CHECK_ENABLE: Primary configuration: master path-0: step check enable. 0 = Step check disabled. 1 = Step check enabled.
5	RWX	PRI_M_PATH_1_STEP_CHECK_ENABLE: Primary configuration: master path-1: step check enable. 0 = Step check disabled. 1 = Step check enabled.
6	RWX	PRI_S_PATH_0_STEP_CHECK_ENABLE: Primary configuration: slave path-0: step check enable. 0 = Step check disabled. 1 = Step check enabled.

Bits	SCOM	Field Mnemonic: Description
7	RWX	PRI_I_PATH_STEP_CHECK_ENABLE: Primary configuration: internal path: step check enable. 0 = Step check disabled. 1 = Step check enabled.
8	RWX	SEC_M_PATH_SELECT: Secondary configuration: master path select. 0 = Master path-0 is selected. 1 = Master path-1 is selected.
9	RWX	SEC_M_S_TOD_SELECT: Secondary configuration: master-slave TOD select. 0 = TOD is slave. 1 = TOD is master.
10	RWX	SEC_M_S_DRAWER_SELECT: Secondary configuration: master-slave drawer select. 0 = Drawer is slave. 1 = Drawer is master. It is used for TOD internal power gating.
11	RWX	SEC_S_PATH_1_STEP_CHECK_ENABLE: Secondary configuration: slave path-1: step check enable. 0 = Step check disabled. 1 = Step check enabled.
12	RWX	SEC_M_PATH_0_STEP_CHECK_ENABLE: Secondary configuration: master path-0: step check enable. 0 = Step check disabled. 1 = Step check enabled.
13	RWX	SEC_M_PATH_1_STEP_CHECK_ENABLE: Secondary configuration: master path-1: step check enable. 0 = Step check disabled. 1 = Step check enabled.
14	RWX	SEC_S_PATH_0_STEP_CHECK_ENABLE: Secondary configuration: slave path-0: step check enable. 0 = Step check disabled. 1 = Step check enabled.
15	RWX	SEC_I_PATH_STEP_CHECK_ENABLE: Secondary configuration: internal path: step check enable. 0 = Step check disabled. 1 = Step check enabled.
16	RW	PSS_SWITCH_SYNC_ERROR_DISABLE: Miscellaneous error sync hold mode. 0 = Gating of one sync on topology switch (type-01) to force TOD sync check error except for the backup TOD master. 1 = Disable sync-gating.
17	RWX	I_PATH_STEP_CHECK_CPS_DEVIATION_X_DISABLE: Internal path: Step check: enlarge CPS deviation: that is, CPS deviation factor = 8. 0 = Enabled. 1 = Disabled.
18	RW	STEP_CHECK_ENABLE_CHICKEN_SWITCH: Type-2: Step check enable: debug switch. 0 = New behavior 1 = Old behavior (POWER7).
19	RW	REG_0X07_SPARE_19: Spares.
20	RW	REG_0X07_SPARE_20: Spares.
21	RW	MISC_RESYNC_OSC_FROM_TOD: Miscellaneous 0 = Disable resynchronization of master OSC sync pulse from TOD synchronization bit. 1 = Enable resynchronization of master OSC sync pulse from TOD synchronization bit legacy.
22:31	RW	REG_0X07_SPARE_22_31: Spares.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	TOD: Primary/Secondary Configuration Status Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_PSS_MSS_STATUS_REG
Address	0000000000040008 (SCOM)
Description	Register to configure Primary and secondary status,-oscillator validity, master/slave status, the selected master path, the selected slave path, and step validity.

Bits	SCOM	Field Mnemonic: Description
0:2	RWX	PRI_SEC_SELECT: Primary and secondary configuration select.
3	RW	REG_0X08_SPARE_03: Spares.
4	ROX	M_PATH_0_OSC_NOT_VALID_STATUS: Master path-0: oscillator not valid.
5	ROX	M_PATH_1_OSC_NOT_VALID_STATUS: Master path-0: oscillator not valid.
6	ROX	M_PATH_0_STEP_CHECK_VALID: Master path-0: step check: Step valid.
7	ROX	M_PATH_1_STEP_CHECK_VALID: Master path-1: step check: Step valid.
8	ROX	S_PATH_0_STEP_CHECK_VALID: Slave path-0: step check: step valid.
9	ROX	I_PATH_STEP_CHECK_VALID: Internal path: step check: step valid.
10	ROX	S_PATH_1_STEP_CHECK_VALID: Slave path-1: step check: step valid.
11	ROX	IS_SPECIAL_STATUS: Control: backup master: status indicating take-over.
12	ROX	PRI_M_PATH_SELECT_STATUS: Primary configuration: master path select.
13	ROX	PRI_M_S_TOD_SELECT_STATUS: Primary configuration: master-slave TOD select.
14	ROX	PRI_M_S_DRAWER_SELECT_STATUS: Primary configuration: master-slave drawer select.
15	ROX	PRI_S_PATH_SELECT_STATUS: Primary configuration: slave path select.
16	ROX	SEC_M_PATH_SELECT_STATUS: Secondary configuration: master path select.
17	ROX	SEC_M_S_TOD_SELECT_STATUS: Secondary configuration: master-slave TOD select.
18	ROX	SEC_M_S_DRAWER_SELECT_STATUS: Secondary configuration: master-slave drawer select.
19	ROX	SEC_S_PATH_SELECT_STATUS: Secondary configuration: slave path select.
20	ROX	IS_RUNNING: Status: TOD is running.
21	ROX	IS_PRIMARY: Status: TOD is using primary configuration.
22	ROX	IS_SECONDARY: Status: TOD is using secondary configuration.
23	ROX	IS_ACTIVE_MASTER: Status: TOD is active master.
24	ROX	IS_BACKUP_MASTER: Status: TOD is backup master.
25	ROX	IS_SLAVE: Status: TOD is slave.
26	ROX	M_PATH_SELECT: Status: TOD is using master path 0 or 1.
27	ROX	S_PATH_SELECT: Status: TOD is using slave path 0 or 1.
28	ROX	M_PATH_0_STEP_ALIGN_VALID_SWITCH: Master path-0: step alignment: valid switch flag.
29	ROX	M_PATH_1_STEP_ALIGN_VALID_SWITCH: Master path-1: step alignment: valid switch flag.
30	RW	REG_0X08_SPARE_30: Spares.
31	RWX	M_PATH_SWITCH_TRIGGER: Master path switch trigger.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	TOD: Master Path Status Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_M_PATH_STATUS_REG
Address	0000000000040009 (SCOM)
Description	Step alignment threshold: cycle-per-step (CPS) TOD reset triggering. A write into this register triggers the following resets (if the corresponding enable bits in reg_0x0B are active): Master path-0 step creation CPS counter reset. Master path-0 step alignment threshold reset. Master path-1 step creation CPS counter reset. Master path-1 step alignment threshold reset.

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	M_PATH_0_STEP_ALIGN_THRESHOLD: Master path-0: step align threshold.
8:15	RWX	M_PATH_0_CPS: Master path-0: CPS: In write mode the value is used to load the CPS for: The local step generation The constant CPS for the step checker
16:23	RWX	M_PATH_1_STEP_ALIGN_THRESHOLD: Master path-1: step align threshold.
24:31	RWX	M_PATH_1_CPS: Master path-1: CPS: In write mode the value is used to load the CPS for: The local step generation The constant CPS for the step checker
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	TOD: Slave Path Status Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_S_PATH_STATUS_REG
Address	000000000004000A (SCOM)
Description	Contains cycle-per-step (CPS) TOD reset triggering. A write into this register triggers the following resets (if the corresponding enable bits in reg_0x0B are active): Master path-0 step alignment FSM reset Master path-1 step alignment FSM reset Slave path-0 step creation CPS counter reset Slave path-1 step creation CPS counter reset

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	M_PATH_0_STEP_ALIGN_FSM_STATE: Master path-0: step alignment: FSM state.
4:7	RWX	M_PATH_1_STEP_ALIGN_FSM_STATE: Master path-1: step alignment: FSM state.
8:12	RWX	I_PATH_DELAY_ADJUST_RATIO: Internal path: delay: adjustment ratio.
13:15	RW	REG_0X0A_SPARE_13_15: Spares.
16:23	RWX	S_PATH_0_CPS: Slave path-0: CPS: In write mode the value is used: To load the CPS for the constant CPS for the step checker if this mode is enabled, see Section Master Path Unit: Step checking mode To load the CPS for the remote sync component if this mode is enabled, see Section Slave Path Unit: Step creation component
24:31	RWX	S_PATH_1_CPS: Slave path-1: CPS: In write mode the value is used to load the CPS for the constant CPS for the step checker.
32:39	RWX	S_PATH_0_REMOTE_SYNC_LATE_SYNC_COUNT: Slave path-0: counter of mesh-clock cycles elapsed between locally created SYNC and remote SYNC.
40:47	RWX	S_PATH_1_REMOTE_SYNC_LATE_SYNC_COUNT: Slave path-1: counter of mesh-clock cycles elapsed between locally created SYNC and remote SYNC.
48:63	RO	constant = 0b0000000000000000

Register Name	TOD: Miscellaneous, TOD Reset Triggering
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_MISC_RESET_REG
Address	000000000004000B (SCOM)
Description	Master path-0 SYNC create counter reset. Master path-1 SYNC create counter reset. A write into this register triggers the following resets (if the corresponding enable bits in reg_0x0B are active).

Bits	SCOM	Field Mnemonic: Description
0	RW	M_PATH_0_STEP_CREATE_THRESHOLD_RESET_ENABLE: Master path-0: step create: threshold reset enable. Master path-0: step alignment: FSM reset enable.
1	RW	M_PATH_0_STEP_ALIGN_THRESHOLD_RESET_ENABLE: Master path-0: step alignment: threshold reset enable. Master path-1: step alignment: FSM reset enable.
2	RW	M_PATH_1_STEP_CREATE_THRESHOLD_RESET_ENABLE: Master path-1: step create: threshold reset enable. Slave path-1: step RX: CPS reset enable. Slave path-1: step RX: remote sync reset enable, if the remote sync mode is enabled.
3	RW	M_PATH_1_STEP_ALIGN_THRESHOLD_RESET_ENABLE: Master path-1: step alignment: threshold reset enable. Slave path-0: step RX: CPS reset enable. Slave path-0: step RX: remote sync reset enable, if the remote sync mode is enabled.
4:5	RW	REG_0X0B_SPARE_04_05: Spares.
6	RW	DISTR_STEP_SYNC_TX_SYNC_RESET_DISABLE: Distribution: step-sync TX synchronous reset disable 0 = Enable step-sync TX synchronous reset. 1 = Disable step-sync TX synchronous reset.
7	RW	CORE_STEP_SYNC_TX_SYNC_RESET_DISABLE: Core: step-sync TX reset synchronous disable 0 = Enable step-sync TX synchronous reset. 1 = Disable step-sync TX synchronous reset.
8	RW	PROBE_0_TOGGLE_ENABLE: Probe output-0: toggle enable.
9	RW	PROBE_1_TOGGLE_ENABLE: Probe output-1: toggle enable.
10	RW	PROBE_2_TOGGLE_ENABLE: Probe output-2: toggle enable.
11	RW	PROBE_3_TOGGLE_ENABLE: Probe output-3: toggle enable.
12	RW	DISTR_STEP_SYNC_TX_RESET_DISABLE: Distribution: step-sync TX reset disable 0 = Enable step-sync TX reset 1 = Disable step-sync TX reset.
13	RW	DISTR_STEP_SYNC_TX_RESET_TRIGGER: Distribution: step-sync TX reset triggering.
14	RW	CORE_STEP_SYNC_TX_RESET_ENABLE: Core: step-sync TX reset enable 0 = Disable step-sync TX reset. 1 = Enable step-sync TX reset.
15	RW	CORE_STEP_SYNC_TX_RESET_TRIGGER: Core: step-sync TX reset triggering.
16	RW	TRACE_ENABLE: Trace: tracing enable.
17	RW	REG_0X0B_SPARE_17: Spares.
18:19	RW	TRACE_DATA_SELECT: Trace: trace data select. Select one of the 4 blocks of 88-bit data.
20	RW	M_PATH_0_SYNC_CREATE_COUNTER_RESET_ENABLE: Master path-0: SYNC create: counter reset enable.
21	RW	M_PATH_1_SYNC_CREATE_COUNTER_RESET_ENABLE: Master path-1: sync create: counter reset enable.

Bits	SCOM	Field Mnemonic: Description
22	RWX	I_PATH_DELAY_TWOS_COMPL_LOAD: Internal path: delay: two’s complement load.
23	RWX	I_PATH_DELAY_ADJUST_RESET: Internal path: delay: adjust reset.
24:32	RWX	I_PATH_DELAY_TWOS_COMPL_LOAD_VALUE: Internal path: delay: two's complement load value.
33:39	RW	REG_0X0B_SPARE_33_39: Spares.
40:63	RO	constant = 0b00000000000000000000000

Register Name	**TOD: Probe Data Select Register**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_PROBE_SELECT_REG
Address	000000000004000C (SCOM)
Description	TOD: Probe Data Select Register

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PROBE_0_DATA_SELECT: Probe-0: input data select.
8:15	RW	PROBE_1_DATA_SELECT: Probe-1: input data select.
16:23	RW	PROBE_2_DATA_SELECT: Probe-2: input data select.
24:31	RW	PROBE_3_DATA_SELECT: Probe-3: input data select.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**TOD: Timer Register**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TIMER_REG
Address	000000000004000D (SCOM)
Description	TOD: Timer Register

Bits	SCOM	Field Mnemonic: Description
0:59	RW	TIMER_VALUE: Timer value.
60:62	RW	REG_0X0D_SPARE_60_62: Spares.
63	ROX	TIMER_STATUS: Timer status 0 = Output is off. 1 = Output is on.

Register Name	**TOD: Master Path**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_M_PATH_0_STEP_STEER_REG
Address	000000000004000E (SCOM)
Description	This is a 0-step steering register. It has step steering configuration and step steering status. Reading bits 33:63 shows the actual value of the step steering counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	M_PATH_0_STEP_STEER_MODE: Master path-0: step steering: mode 0 = Increment mode. The step period increases, and the TOD ticks slower. 1 = Decrement mode. The step period decreases, and the TOD ticks faster.
1:31	RW	M_PATH_0_STEP_STEER_RATE: Master path-0: step steering: rate.

Bits	SCOM	Field Mnemonic: Description
32	RW	M_PATH_0_STEP_STEER_COUNTER_LOAD_FLAG: Master path-0: step steering: counter load flag 0 = Disable loading of the steer counter with data specified in bits 32:63. 1 = Enable loading of the steer counter with data specified in bits 32:63.
33:63	RWX	M_PATH_0_STEP_STEER_COUNTER_LOAD_VALUE: Master path-0: step steering: steer counter load value.

Register Name	**TOD: Master Path**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_M_PATH_1_STEP_STEER_REG
Address	000000000004000F (SCOM)
Description	This is a 1-step steering register. It has step steering configuration and step steering status. Reading bits 33:63 shows the actual value of the step steering counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	M_PATH_1_STEP_STEER_MODE: Master path-1: step steering: mode. 0 = Increment mode. The step period increases, and the TOD ticks slower 1 = Decrement mode. The step period decreases, and the TOD ticks faster.
1:31	RW	M_PATH_1_STEP_STEER_RATE: Master path-1: step steering: rate.
32	RW	M_PATH_1_STEP_STEER_COUNTER_LOAD_FLAG: Master path-1: step steering: counter load flag. 0 = Disable loading of the steer counter with data specified in bits 32:63 1 = Enable loading of the steer counter with data specified in bits 32:63.
33:63	RWX	M_PATH_1_STEP_STEER_COUNTER_LOAD_VALUE: Master path-1: step steering: steer counter load value.

Register Name	**TOD: Chip Control Register**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_CHIP_CTRL_REG
Address	0000000000040010 (SCOM)
Description	TOD: Chip Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	TIMEBASE_ENABLE: Time base enable.
1:3	RW	I_PATH_CORE_SYNC_PERIOD_SELECT: Internal path: core SYNC period select.
4	RW	I_PATH_SYNC_CHECK_DISABLE: Internal path: SYNC check disable. 0 = TOD SYNC check enable. 1 = TOD SYNC check disable.
5	RW	TX_TTYPE_PIB_MST_FSM_STATE_DISABLE: TX TType: PIB master. FSM state: enable. 0 = Disabled. 1 = Enabled.
6	RW	RX_TTYPE_1_ON_STEP_ENABLE: RX TType-1: Enable the synchronization of the TType-1 on occurrence of a step. 0 = Disable. 1 = Enable.
7	RW	MOVE_TOD_TO_TB_ON_2X_SYNC_ENABLE: Move-TOD-to-time base on 2x sync boundary: enable 0 = Move-TOD-to-time base on 1x SYNC boundary. 1 = Move-TOD-to-time base on 2x SYNC boundary.

Bits	SCOM	Field Mnemonic: Description
8	RW	USE_TB_SYNC_MECHANISM: Use time base sync mechanism 0 = Use sync mechanism. 1 = Use the tb_enable signal as a sync event.
9	RW	USE_TB_STEP_SYNC: Use time base step sync. 0 = Use step-sync from the internal path 1 = Use programmable cycle counter for step.
10:15	RW	LOW_ORDER_STEP_VALUE: Low-order step value needed for USE_TB_STEP_SYNC as the programmable cycle counter for creating a step.
16	RW	DISTRIBUTION_BROADCAST_MODE_ENABLE: Distribution: enable broadcast mode. 0 = Distribution is done by specific routing of the signals from one TOD (master or slave) to another slave. 1 = Distribution is done by broadcasting the signals from the active master to any slave in the system.
17:18	RW	REG_0X10_SPARE_17_18: Spares.
19:23	RW	REG_0X10_SPARE_19_23: Spares.
24:25	RW	REG_0X10_SPARE_24_25: Spares.
26	WO	TX_TTYPE_PIB_MST_IF_RESET: TX TType: PIB master interface reset. Request a PIB master reset to the PIB arbiter. The reset request is sent to the PIB arbiter after a delay of four steps.
27	RW	REG_0X10_SPARE_27: Spares.
28	RW	M_PATH_CLOCK_OFF_ENABLE: Master path: clock gating enable. 0 = Disable. 1 = Enable clock gating function of the oscillator valid bits TOD_M_PATH_CTRL_REG (@0x00[0:1]).
29	RW	REG_0X10_SPARE_29: Spares.
30	RW	XSTOP_GATE: System checkstop gate. 0 = Stop TOD when a system checkstop occurs. 1 = Keep TOD running when a system checkstop occurs.
31	RW	STICKY_ERROR_INJECT_ENABLE: Sticky error inject enable.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	TOD: TX TTYPE
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TX_TTYPE_0_REG
Address	0000000000040011 (SCOM)
Description	TX TType triggering register 0.

Bits	SCOM	Field Mnemonic: Description
0	WO	TX_TTYPE_0_TRIGGER: TX TTYPE-0 trigger.
1:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: TX TTYPE
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TX_TTYPE_1_REG
Address	0000000000040012 (SCOM)
Description	TX TType triggering register 1.

Bits	SCOM	Field Mnemonic: Description
0	WO	TX_TTYPE_1_TRIGGER: TX TTYPE-1 trigger.

Bits	SCOM	Field Mnemonic: Description
1:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: TX TTYPE
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TX_TTYPE_2_REG
Address	0000000000040013 (SCOM)
Description	TX TType triggering register 2.

Bits	SCOM	Field Mnemonic: Description
0	WO	TX_TTYPE_2_TRIGGER: TX TTYPE-2 trigger.
1:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: TX TTYPE
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TX_TTYPE_3_REG
Address	0000000000040014 (SCOM)
Description	TX TType triggering register 3.

Bits	SCOM	Field Mnemonic: Description
0	WO	TX_TTYPE_3_TRIGGER: TX TTYPE-3 trigger.
1:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: TX TTYPE
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TX_TTYPE_4_REG
Address	0000000000040015 (SCOM)
Description	TX TType triggering register 4.

Bits	SCOM	Field Mnemonic: Description
0	WO	TX_TTYPE_4_TRIGGER: TX TTYPE-4 trigger.
1:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: TX TTYPE
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TX_TTYPE_5_REG
Address	0000000000040016 (SCOM)
Description	TX TType triggering register 5.

Bits	SCOM	Field Mnemonic: Description
0	WO	TX_TTYPE_5_TRIGGER: TX TTYPE-5 trigger.
1:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: Move
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_MOVE_TOD_TO_TB_REG
Address	0000000000040017 (SCOM)
Description	TOD-to-timebase triggering register.

Bits	SCOM	Field Mnemonic: Description
0	WO	MOVE_TOD_TO_TB_TRIGGER: Move TOD-to-timebase trigger.
1:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: Load
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_LOAD_TOD_MOD_REG
Address	0000000000040018 (SCOM)
Description	TOD-mod triggering register. This register sets the FSM in NOT_SET state.

Bits	SCOM	Field Mnemonic: Description
0	WO	FSM_LOAD_TOD_MOD_TRIGGER: FSM: LOAD_TOD_MOD trigger.
1	WO	FSM_LOAD_TOD_MOD_SYNC_ENABLE: FSM: LOAD_TOD_MOD sync enable when the FSM is in NOT_SET state 0 = No sync sent to the core when the FSM is in NOT_SET state. 1 = Sync sent to the core when the FSM is in NOT_SET state.
2:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: Trace Data Set Register 1
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TRACE_DATA_1_REG
Address	000000000004001D (SCOM)
Description	Trace Data Set Register 1

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	TRACE_DATA_SET_1: Trace: data set-1.

Register Name	TOD: Trace Data Set Register 2
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TRACE_DATA_2_REG
Address	000000000004001E (SCOM)
Description	Trace Data Set Register 2

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	TRACE_DATA_SET_2: Trace: data set-2.

Register Name	TOD: Trace Data Set Register 3
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TRACE_DATA_3_REG
Address	000000000004001F (SCOM)
Description	Trace Data Set Register 3

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	TRACE_DATA_SET_3: Trace: data set-3.

Register Name	TOD: Time Value Register 60
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_VALUE_REG
Address	0000000000040020 (SCOM)
Description	Bit TOD and 4-bit who's-on-first (WOF) incrementers

Bits	SCOM	Field Mnemonic: Description
0:59	ROX	TOD_VALUE: Internal path: time-of-day register value.
60:63	RWX	WOF_COUNTER_VALUE: Who's-on-first (WOF): counter value.

Register Name	TOD: Load Register TOD Incrementer: 60
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_LOAD_TOD_REG
Address	0000000000040021 (SCOM)
Description	Bit TOD and 4-bit WOF on read: Returns all 0s when the TOD is not running. On write: go to wait for sync state when data bit 6) = ‘0’ (load TOD). Otherwise, go to stopped state (load TOD data63).

Bits	SCOM	Field Mnemonic: Description
0:59	RWX	LOAD_TOD_VALUE: Internal path: load TOD value.
60:63	RWX	WOF: who's-on-first (WOF) incrementer.

Register Name	TOD: Start TOD Triggering Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_START_TOD_REG
Address	0000000000040022 (SCOM)
Description	TOD: Start TOD triggering register. Goes to running state when data bit [02] = ‘0’. Otherwise, go to wait for sync state.

Bits	SCOM	Field Mnemonic: Description
0	WO	FSM_START_TOD_TRIGGER: FSM: Start TOD trigger.
1	RW	REG_0X22_SPARE_01: Spares.
2	WO	FSM_START_TOD_DATA02: FSM: Start TOD data 02 trigger.
3:7	RW	REG_0X22_SPARE_03_07: Spares.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	TOD: Low-Order Step Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_LOW_ORDER_STEP_REG
Address	0000000000040023 (SCOM)
Description	TOD: Low-Order Step Register

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	LOW_ORDER_STEP_COUNTER_VALUE: Low-order step. Counter value is used for use OSC B configuration for internal step creation.
6:7	RW	REG_0X23_SPARE_06_07: Spares.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: FSM Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_FSM_REG
Address	0000000000040024 (SCOM)
Description	TOD: FSM Register

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	I_PATH_FSM_STATE: Internal path. TOD FSM state (TOD is running in the following states: x‘02’, x‘0A’, x‘0E’). 0000 = Error.
4	ROX	TOD_IS_RUNNING: TOD running indicator.
5:7	RW	REG_0X24_SPARE_05_07: Spares.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: TX TType Control Register
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_TX_TTYPE_CTRL_REG
Address	0000000000040027 (SCOM)
Description	TOD: TX TType Control Register

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MOVE_TOD_TO_TB_CORE_ADDRESS: TX TType: move TOD to timebase: configuration of core address. Must be configured before issuing a MOVE_CHIP_TOD_TO_TB command. Bits [0:31] are used to configure the core address. This mode is activated by enabling bit [35].
24:31	RW	MOVE_TOD_TO_TB_CORE_ID: TX TType: move TOD to timebase: configuration of core address. Must be configured before issuing a MOVE_CHIP_TOD_TO_TB command. 000 = Reserved. 001 = Multicast bit (0b1 for multicast) 011 … 100 = PIB slave address is 0b01xxxx where xxxx is the core ID.
32	RW	TX_TTYPE_4_SEND_MODE: TX TType: TType-4 send mode. Qualification of TType4 is sent out through Fabric when receiving a TType-3 by Fabric. Must be configured before issuing a TType-3 command. 0 = Send TType-4 if TOD is master. 1 = Send TType-4 if enabled (bit-33).
33	RW	TX_TTYPE_4_SEND_ENABLE: TX TType: TType-4 send enable. 0 = Disabled to send out TType-4. 1 = Enabled to send out TType-4.

Bits	SCOM	Field Mnemonic: Description
34	RW	REG_0X27_SPARE_34: Spares.
35	RW	MOVE_TOD_TO_TB_CORE_ADDRESS_ENABLE: TX TType: move TOD to timebase. Enables the full configuration of the core address.
36	RW	REG_0X27_SPARE_36: Spares.
37:39	ROX	TX_TTYPE_PIB_FSM_STATE: TX TType: PIB master FSM state.
40:63	RO	constant = 0b000000000000000000000000

Register Name	**TOD: RX TType Control Register**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_RX_TTYPE_CTRL_REG
Address	0000000000040029 (SCOM)
Description	This register is used by the Alter Display Unit (ADU) to transmit the TType data it receives from the processor bus.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	RX_TTYPE_DATA: RX TType: Data. See the TType Format section of the workbook for the data format.

Register Name	**TOD: Error and Interrupt Register**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_ERROR_REG
Address	0000000000040030 (SCOM)
Description	TOD: Error and Interrupt Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	REG_0X00_DATA_PARITY_ERROR: Error: master path control register (0x00): Data parity error.
1	RWX	M_PATH_0_PARITY_ERROR: Error: master path-0: parity error.
2	RWX	M_PATH_1_PARITY_ERROR: Error: master path-1: parity error.
3	RWX	REG_0X01_DATA_PARITY_ERROR: Error: port-0 primary configuration register (0x01): data parity error.
4	RWX	REG_0X02_DATA_PARITY_ERROR: Error: port-1 primary configuration register (0x02): data parity error.
5	RWX	REG_0X03_DATA_PARITY_ERROR: Error: port-0 secondary configuration register (0x03): data parity error.
6	RWX	REG_0X04_DATA_PARITY_ERROR: Error: port-1 secondary configuration register (0x04): data parity error.
7	RWX	REG_0X05_DATA_PARITY_ERROR: Error: slave path control register (0x05): data parity error.
8	RWX	REG_0X06_DATA_PARITY_ERROR: Error: internal path control register (0x06): data parity error.
9	RWX	REG_0X07_DATA_PARITY_ERROR: Error: primary/secondary master/slave control register (0x07): data parity error.
10	RWX	S_PATH_0_PARITY_ERROR: Error: slave path-0: parity error.
11	RWX	REG_0X08_DATA_PARITY_ERROR: Error: primary/secondary master/slave status register (0x07): data parity error.
12	RWX	REG_0X09_DATA_PARITY_ERROR: Error: master path status register (0x09): data parity error.
13	RWX	REG_0X0A_DATA_PARITY_ERROR: Error: slave path status register (0x0a): data parity error.
14	RWX	M_PATH_0_STEP_CHECK_ERROR: Error: master path-0: step check error.
15	RWX	M_PATH_1_STEP_CHECK_ERROR: Error: master path-1: step check error.
16	RWX	S_PATH_0_STEP_CHECK_ERROR: Error: slave path-0: step check error.

Bits	SCOM	Field Mnemonic: Description
17	RWX	I_PATH_STEP_CHECK_ERROR: Error: internal path: step check error.
18	RWX	PSS_HAM: Error: PSS hamming distance.
19	RWX	REG_0X0B_DATA_PARITY_ERROR: Error: miscellaneous, reset register (0x0b): data parity error.
20	RWX	S_PATH_1_PARITY_ERROR: Error: slave path-0: parity error.
21	RWX	S_PATH_1_STEP_CHECK_ERROR: Error: slave path-1: step check error.
22	RWX	I_PATH_DELAY_STEP_CHECK_PARITY_ERROR: Error: internal path: delay, step check components: parity error.
23	RWX	REG_0X0C_DATA_PARITY_ERROR: Error. A data parity error of the following registers: Probe Data Select Register (0x0c) Timer Register (0x0d).
24	RWX	REG_0X11_0X12_0X13_0X14_0X15_0X16_DATA_PARITY_ERROR: Error. A data parity error occurred on one of the following TX-TType trigger registers: TX TType-0 Triggering Register (0x11) TX TType-1 Triggering Register (0x12) TX TType-2 Triggering Register (0x13) TX TType-3 Triggering Register (0x14) TX TType-4 Triggering Register (0x15) TX TType-5 Triggering Register (0x16)
25	RWX	REG_0X17_0X18_0X21_0X22_DATA_PARITY_ERROR: Error A data parity error on one of the following trigger registers: Move-TOD-to-Timebase Triggering Register (0x17) Load-TOD-Mod Register (0x18) Load Register (0x21) Start-TOD Register (0x22)
26	RWX	REG_0X1D_0X1E_0X1F_DATA_PARITY_ERROR: Error: A Data parity error on one of the following trace data registers: Trace data set-1 register (0x1d) Trace data set-2 register (0x1e) Trace data set-3 register (0x1f)
27	RWX	REG_0X20_DATA_PARITY_ERROR: Error: time value register (0x20): data parity error.
28	RWX	REG_0X23_DATA_PARITY_ERROR: Error: low-order step register (0x23): data parity error.
29	RWX	REG_0X24_DATA_PARITY_ERROR: Error: FSM register (0x24): data parity error.
30	RWX	REG_0X29_DATA_PARITY_ERROR: Error: RX-TType control register: data parity error.
31	RWX	REG_0X30_0X31_0X32_0X33_DATA_PARITY_ERROR: Error A data parity error occurred on one of the following error handling registers: Error register (0x30) Error inject register (0x31) Error mask register (0x32) Core interrupt mask register (0x33)
32	RWX	REG_0X10_DATA_PARITY_ERROR: Error: chip control register (0x10): data parity error.
33	RWX	I_PATH_SYNC_CHECK_ERROR: Error: internal path: SYNC check.
34	RWX	I_PATH_FSM_STATE_PARITY_ERROR: Error: internal path: FSM state parity error.
35	RWX	I_PATH_TIME_REG_PARITY_ERROR: Error: internal path. Time register parity error.
36	RWX	I_PATH_TIME_REG_OVERFLOW: Error: internal path. Time register overflow.
37	RWX	WOF_LOW_ORDER_STEP_COUNTER_PARITY_ERROR: Error: WOF counter or low-order-step counter: parity error.
38	RWX	RX_TTYPE_0: Status: received TType-0.

Bits	SCOM	Field Mnemonic: Description
39	RWX	RX_TTYPE_1: Status: received TType-1.
40	RWX	RX_TTYPE_2: Status: received TType-2.
41	RWX	RX_TTYPE_3: Status: received TType-3.
42	RWX	RX_TTYPE_4: Status: received TType-4.
43	RWX	RX_TTYPE_5: Status: received TType-5 when FSM is in running state.
44	RWX	PIB_SLAVE_ADDR_INVALID_ERROR: Error: PIB slave: invalid address.
45	RWX	PIB_SLAVE_WRITE_INVALID_ERROR: Error: PIB slave: invalid write.
46	RWX	PIB_SLAVE_READ_INVALID_ERROR: Error: PIB slave: invalid read.
47	RWX	PIB_SLAVE_ADDR_PARITY_ERROR: Error: PIB slave: Address parity error.
48	RWX	PIB_SLAVE_DATA_PARITY_ERROR: Error: PIB slave: data parity error.
49	RWX	REG_0X27_DATA_PARITY_ERROR: Error: TType control register(0x27): data parity error.
50:52	RWX	PIB_MASTER_RSP_INFO_ERROR: Error: PIB master: response infoerror info = 000: no error info > 000: error
53	RWX	RX_TTYPE_INVALID_ERROR: Error: received invalid TType ROM register 0x21.
54	RWX	RX_TTYPE_4_DATA_PARITY_ERROR: Error: data parity error on received TType-4 from register 0x21.
55	RWX	PIB_MASTER_REQUEST_ERROR: Error: PIB master; request while busy error.
56	RWX	PIB_RESET_DURING_PIB_ACCESS_ERROR: Error: PIB reset received during a PIB master or PIB slave operation.
57	RWX	EXTERNAL_XSTOP_ERROR: Error: TOD received an external checkstop.
58	RWX	SPARE_ERROR_58: Error: spare.
59	RWX	SPARE_ERROR_59: Error: spare.
60	RWX	SPARE_ERROR_60: Error: spare.
61	RWX	SPARE_ERROR_61: Error: spare.
62	RWX	OSCSWITCH_INTERRUPT: Error: Interrupt from the oscillator switch.
63	RWX	SPARE_ERROR_63: Error: spare.

Register Name	**TOD: Error and Interrupt Inject Register**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_ERROR_INJECT_REG
Address	0000000000040031 (SCOM)
Description	TOD: Error And Interrupt Inject Register

Bits	SCOM	Field Mnemonic: Description
0	WO	REG_0X00_DATA_PARITY_ERROR_INJECT: Error inject: master path control register (0x00): data parity error.
1	WO	M_PATH_0_PARITY_ERROR_INJECT: Error inject: master path-0: parity error.
2	WO	M_PATH_1_PARITY_ERROR_INJECT: Error inject: master path-1: parity error.
3	WO	REG_0X01_DATA_PARITY_ERROR_INJECT: Error inject: port-0 primary configuration register (0x01): data parity error.
4	WO	REG_0X02_DATA_PARITY_ERROR_INJECT: Error inject: port-1 primary configuration register (0x02): data parity error.

Bits	SCOM	Field Mnemonic: Description
5	WO	REG_0X03_DATA_PARITY_ERROR_INJECT: Error inject: port-0 secondary configuration register (0x03): data parity error.
6	WO	REG_0X04_DATA_PARITY_ERROR_INJECT: Error inject: port-1 secondary configuration register (0x04): data parity error.
7	WO	REG_0X05_DATA_PARITY_ERROR_INJECT: Error inject: slave path control register (0x05): data parity error.
8	WO	REG_0X06_DATA_PARITY_ERROR_INJECT: Error inject: internal path control register (0x06): data parity error.
9	WO	REG_0X07_DATA_PARITY_ERROR_INJECT: Error inject: primary/secondary master/slave control register (0x07): data parity error.
10	WO	S_PATH_0_PARITY_ERROR_INJECT: Error inject: slave path-0: parity error.
11	WO	REG_0X08_DATA_PARITY_ERROR_INJECT: Error inject: primary/secondary master/slave status register (0x07): data parity error.
12	WO	REG_0X09_DATA_PARITY_ERROR_INJECT: Error inject: master path status register (0x09): data parity error.
13	WO	REG_0X0A_DATA_PARITY_ERROR_INJECT: Error inject: slave path status register (0x0a): data parity error.
14	WO	M_PATH_0_STEP_CHECK_ERROR_INJECT: Error inject: master path-0: step check error.
15	WO	M_PATH_1_STEP_CHECK_ERROR_INJECT: Error inject: master path-1: step check error.
16	WO	S_PATH_0_STEP_CHECK_ERROR_INJECT: Error inject: slave path-0: step check error.
17	WO	I_PATH_STEP_CHECK_ERROR_INJECT: Error inject: internal path: step check error.
18	WO	PSS_HAM_INJECT: Error inject: PSS hamming distance.
19	WO	REG_0X0B_DATA_PARITY_ERROR_INJECT: Error inject: miscellaneous, reset register (0x0b): data parity error.
20	WO	S_PATH_1_PARITY_ERROR_INJECT: Error inject: slave path-0: parity error.
21	WO	S_PATH_1_STEP_CHECK_ERROR_INJECT: Error inject: slave path-1: step check error.
22	WO	I_PATH_DELAY_STEP_CHECK_PARITY_ERROR_INJECT: Error inject: internal path: delay, step check components: parity error.
23	WO	REG_0X0C_DATA_PARITY_ERROR_INJECT: Error inject: data parity error of the following registers: Probe data select register (0x0c). Timer register (0x0D).
24	WO	REG_0X11_0X12_0X13_0X14_0X15_0X16_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on the following TX-TType trigger registers: TX TType-0 triggering register (0x11) TX TType-1 triggering register (0x12) TX TType-2 triggering register (0x13) TX TType-3 triggering register (0x14) TX TType-4 triggering register (0x15) TX TType-5 triggering register (0x16)
25	WO	REG_0X17_0X18_0X21_0X22_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on the following trigger registers: Move-TOD-to-timebase triggering register (0x17) Load-TOD-mod register (0x18) Load register (0x21) Start-TOD register (0x22)

Bits	SCOM	Field Mnemonic: Description
26	WO	REG_0X1D_0X1E_0X1F_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on the following trace data registers: Trace data set-1 register (0x1d) Trace data set-2 register (0x1e) Trace data set-3 register (0x1f)
27	WO	REG_0X20_DATA_PARITY_ERROR_INJECT: Error inject: time value register (0x20): data parity error.
28	WO	REG_0X23_DATA_PARITY_ERROR_INJECT: Error inject: low-order step register (0x23): data parity error.
29	WO	REG_0X24_DATA_PARITY_ERROR_INJECT: Error inject: FSM register (0x24): data parity error.
30	WO	REG_0X29_DATA_PARITY_ERROR_INJECT: Error inject: RX-TType control register: data parity error.
31	WO	REG_0X30_0X31_0X32_0X33_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on the following error handling registers: Error register (0x30) Error mask register (0x32) Core interrupt mask register (0x33)
32	WO	REG_0X10_DATA_PARITY_ERROR_INJECT: Error inject: chip control register (0x10): data parity error.
33	WO	I_PATH_SYNC_CHECK_ERROR_INJECT: Error inject: internal path: SYNC check.
34	WO	I_PATH_FSM_STATE_PARITY_ERROR_INJECT: Error inject: internal path: FSM state parity error.
35	WO	I_PATH_TIME_REG_PARITY_ERROR_INJECT: Error inject: time register: parity error.
36	WO	I_PATH_TIME_REG_OVERFLOW_INJECT: Error inject: internal path: time register overflow.
37	WO	WOF_LOW_ORDER_STEP_COUNTER_PARITY_ERROR_INJECT: Error inject: WOF counter or low-order-step counter: parity error.
38	WO	RX_TTYPE_0_INJECT: Error inject: received TType-0.
39	WO	RX_TTYPE_1_INJECT: Error inject: received TType-1.
40	WO	RX_TTYPE_2_INJECT: Error inject: received TType-2.
41	WO	RX_TTYPE_3_INJECT: Error inject: received TType-3.
42	WO	RX_TTYPE_4_INJECT: Error inject: received TType-4.
43	WO	RX_TTYPE_5_INJECT: Error inject: received TType-5 when FSM is in running state.
44	WO	PIB_SLAVE_ADDR_INVALID_ERROR_INJECT: Error inject: PIB slave: invalid address.
45	WO	PIB_SLAVE_WRITE_INVALID_ERROR_INJECT: Error inject: PIB slave: invalid write.
46	WO	PIB_SLAVE_READ_INVALID_ERROR_INJECT: Error inject: PIB slave: invalid read.
47	WO	PIB_SLAVE_ADDR_PARITY_ERROR_INJECT: Error inject: PIB slave: Address parity error.
48	WO	PIB_SLAVE_DATA_PARITY_ERROR_INJECT: Error inject: PIB slave: data parity error.
49	WO	REG_0X27_DATA_PARITY_ERROR_INJECT: Error inject: TType control register(0x27): data parity error.
50:52	WO	PIB_MASTER_RSP_INFO_ERROR_INJECT: Error inject: PIB master: response infoerror.
53	WO	RX_TTYPE_INVALID_ERROR_INJECT: Error inject: received invalid TType from register 0x21.
54	WO	RX_TTYPE_4_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on received TType-4 from register 0x21.
55	WO	PIB_MASTER_REQUEST_ERROR_INJECT: Error inject: PIB master; request while busy error.
56	WO	PIB_RESET_DURING_PIB_ACCESS_ERROR_INJECT: Error inject: PIB reset received during a PIB master or PIB slave operation.
57	WO	EXTERNAL_XSTOP_ERROR_INJECT: Error inject: TOD received an external checkstop.
58	WO	SPARE_ERROR_INJECT_58: Error inject: spare.
59	WO	SPARE_ERROR_INJECT_59: Error inject: spare.

Bits	SCOM	Field Mnemonic: Description
60	WO	SPARE_ERROR_INJECT_60: Error inject: spare.
61	WO	SPARE_ERROR_INJECT_61: Error inject: spare.
62	WO	OSCSWITCH_INTERRUPT_INJECT: Error inject: Interrupt from the oscillator switch.
63	WO	CORE_STEP_ERROR_INJECT: Error inject: to suppress one step to core timebase.

Register Name	**TOD: Error Mask Register Mask: Error Reporting Component (C_ERR_RPT)**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_ERROR_MASK_REG
Address	0000000000040032 (SCOM)
Description	TOD: Error mask register mask of the error reporting component (c_err_rpt)

Bits	SCOM	Field Mnemonic: Description
0	RWX	REG_0X00_DATA_PARITY_ERROR_MASK: Error mask: master path control register (0x00): data parity error.
1	RWX	M_PATH_0_PARITY_ERROR_MASK: Error mask: master path-0: parity error.
2	RWX	M_PATH_1_PARITY_ERROR_MASK: Error mask: master path-1: parity error.
3	RWX	REG_0X01_DATA_PARITY_ERROR_MASK: Error mask: port-0 primary configuration register (0x01): data parity error.
4	RWX	REG_0X02_DATA_PARITY_ERROR_MASK: Error mask: port-1 primary configuration register (0x02): data parity error.
5	RWX	REG_0X03_DATA_PARITY_ERROR_MASK: Error mask: port-0 secondary configuration register (0x03): data parity error.
6	RWX	REG_0X04_DATA_PARITY_ERROR_MASK: Error mask: port-1 secondary configuration register (0x04): data parity error.
7	RWX	REG_0X05_DATA_PARITY_ERROR_MASK: Error mask: slave path control register (0x05): data parity error.
8	RWX	REG_0X06_DATA_PARITY_ERROR_MASK: Error mask: internal path control register (0x06): data parity error.
9	RWX	REG_0X07_DATA_PARITY_ERROR_MASK: Error mask: primary/secondary master/slave control register (0x07): data parity error.
10	RWX	S_PATH_0_PARITY_ERROR_MASK: Error mask: slave path-0: parity error.
11	RWX	REG_0X08_DATA_PARITY_ERROR_MASK: Error mask: primary/secondary master/slave status register (0x07): data parity error.
12	RWX	REG_0X09_DATA_PARITY_ERROR_MASK: Error mask: master path status register (0x09): data parity error.
13	RWX	REG_0X0A_DATA_PARITY_ERROR_MASK: Error mask: slave path status register (0x0a): data parity error.
14	RWX	M_PATH_0_STEP_CHECK_ERROR_MASK: Error mask: master path-0: step check error.
15	RWX	M_PATH_1_STEP_CHECK_ERROR_MASK: Error mask: master path-1: step check error.
16	RWX	S_PATH_0_STEP_CHECK_ERROR_MASK: Error mask: slave path-0: step check error.
17	RWX	I_PATH_STEP_CHECK_ERROR_MASK: Error mask: internal path: Step check error.
18	RWX	PSS_HAM_MASK: Error mask: PSS hamming distance.
19	RWX	REG_0X0B_DATA_PARITY_ERROR_MASK: Error mask: miscellaneous, reset register (0x0b): data parity error.
20	RWX	S_PATH_1_PARITY_ERROR_MASK: Error mask: slave path-0: parity error.

Bits	SCOM	Field Mnemonic: Description
21	RWX	S_PATH_1_STEP_CHECK_ERROR_MASK: Error mask: slave path-1: step check error.
22	RWX	I_PATH_DELAY_STEP_CHECK_PARITY_ERROR_MASK: Error mask: internal path: delay, step check components: parity error.
23	RWX	REG_0X0C_DATA_PARITY_ERROR_MASK: Error mask: data parity error of the following registers: Probe data select register (0x0c) Timer register (0x0d)
24	RWX	REG_0X11_0X12_0X13_0X14_0X15_0X16_DATA_PARITY_ERROR_MASK: Error mask: data parity error on one of the following TX-TType trigger registers: TX TType-0 triggering register (0x11) TX TType-1 triggering register (0x12) TX TType-2 triggering register (0x13) TX TType-3 triggering register (0x14) TX TType-4 triggering register (0x15) TX TType-5 triggering register (0x16)
25	RWX	REG_0X17_0X18_0X21_0X22_DATA_PARITY_ERROR_MASK: Error mask: data parity error on one of the following trigger registers: move-TOD-to-timebase triggering register (0x17) TX TType-0 triggering register (0x11)load-TOD-mod register (0x18) TX TType-0 triggering register (0x11)load register (0x21) TX TType-0 triggering register (0x11)start-TOD register (0x22)
26	RWX	REG_0X1D_0X1E_0X1F_DATA_PARITY_ERROR_MASK: Error mask: data parity error on one of the following trace data registers: TX TType-0 triggering register (0x11)trace data set-1 register (0x1d) TX TType-0 triggering register (0x11)trace data set-2 register (0x1e) TX TType-0 triggering register (0x11)trace data set-3 register (0x1f).
27	RWX	REG_0X20_DATA_PARITY_ERROR_MASK: Error mask: time value register (0x20): data parity error.
28	RWX	REG_0X23_DATA_PARITY_ERROR_MASK: Error mask: low-order step register (0x23): data parity error.
29	RWX	REG_0X24_DATA_PARITY_ERROR_MASK: Error mask: FSM register (0x24): data parity error.
30	RWX	REG_0X29_DATA_PARITY_ERROR_MASK: Error mask: RX-TType control register: data parity error.
31	RWX	REG_0X30_0X31_0X32_0X33_DATA_PARITY_ERROR_MASK: Error mask: data parity error on one of the following error handling registers: Error register (0x30) Error inject register (0x31) Error mask register (0x32) Error interrupt mask register (0x33)
32	RWX	REG_0X10_DATA_PARITY_ERROR_MASK: Error mask: chip control register (0x10): data parity error.
33	RWX	I_PATH_SYNC_CHECK_ERROR_MASK: Error mask: internal path: SYNC check.
34	RWX	I_PATH_FSM_STATE_PARITY_ERROR_MASK: Error mask: internal path: FSM state parity error.
35	RWX	I_PATH_TIME_REG_PARITY_ERROR_MASK: Error mask: internal path: time register: parity error.
36	RWX	I_PATH_TIME_REG_OVERFLOW_MASK: Error mask: internal path: time register overflow.
37	RWX	WOF_LOW_ORDER_STEP_COUNTER_PARITY_ERROR_MASK: Error mask: WOF counter or Low-Order-Step counter: parity error.
38	RWX	RX_TTYPE_0_MASK: Error mask: received TType-0.
39	RWX	RX_TTYPE_1_MASK: Error mask: received TType-1.
40	RWX	RX_TTYPE_2_MASK: Error mask: received TType-2.
41	RWX	RX_TTYPE_3_MASK: Error mask: received TType-3.
42	RWX	RX_TTYPE_4_MASK: Error mask: received TType-4.
43	RWX	RX_TTYPE_5_MASK: Error mask: received TType-5 when FSM is in running state.

Bits	SCOM	Field Mnemonic: Description
44	RWX	PIB_SLAVE_ADDR_INVALID_ERROR_MASK: Error mask: PIB slave: invalid address.
45	RWX	PIB_SLAVE_WRITE_INVALID_ERROR_MASK: Error mask: PIB slave: invalid write.
46	RWX	PIB_SLAVE_READ_INVALID_ERROR_MASK: Error mask: PIB slave: invalid read.
47	RWX	PIB_SLAVE_ADDR_PARITY_ERROR_MASK: Error mask: PIB slave: Address parity error.
48	RWX	PIB_SLAVE_DATA_PARITY_ERROR_MASK: Error mask: PIB slave: data parity error.
49	RWX	REG_0X27_DATA_PARITY_ERROR_MASK: Error mask: TType control register(0x27): data parity error.
50:52	RWX	PIB_MASTER_RSP_INFO_ERROR_MASK: Error mask: PIB master: response infoerror.
53	RWX	RX_TTYPE_INVALID_ERROR_MASK: Error mask: received invalid TType from register 0x21.
54	RWX	RX_TTYPE_4_DATA_PARITY_ERROR_MASK: Error mask: data parity error on received TType-4 from register 0x21.
55	RWX	PIB_MASTER_REQUEST_ERROR_MASK: Error mask: PIB master; request while busy error.
56	RWX	PIB_RESET_DURING_PIB_ACCESS_ERROR_MASK: Error mask: PIB reset received during a PIB master or PIB slave operation.
57	RWX	EXTERNAL_XSTOP_ERROR_MASK: Error mask: TOD received an external checkstop.
58	RWX	SPARE_ERROR_MASK_58: Error mask: spare.
59	RWX	SPARE_ERROR_MASK_59: Error mask: spare.
60	RWX	SPARE_ERROR_MASK_60: Error mask: spare.
61	RWX	SPARE_ERROR_MASK_61: Error mask: spare.
62	RWX	OSCSWITCH_INTERRUPT_MASK: Error mask: Interrupt from the oscillator switch.
63	RWX	SPARE_ERROR_MASK_63: Error mask: spare.

Register Name	**TOD: Route Specific Errors to the CORE or FIR**
Mnemonic	TP.TPCHIP.PIB.TOD.TOD_ERROR_ROUTING_REG
Address	0000000000040033 (SCOM)
Description	TOD: Routes specific errors either to the CORE or to the FIR

Bits	SCOM	Field Mnemonic: Description
0	RW	REG_0X00_DATA_PARITY_ERROR_ROUTING: Error routing: master path control register (0x00): data parity error.
1	RW	M_PATH_0_PARITY_ERROR_ROUTING: Error routing: master path-0: parity error.
2	RW	M_PATH_1_PARITY_ERROR_ROUTING: Error routing: master path-1: parity error.
3	RW	REG_0X01_DATA_PARITY_ERROR_ROUTING: Error routing: port-0 primary configuration register (0x01): data parity error.
4	RW	REG_0X02_DATA_PARITY_ERROR_ROUTING: Error routing: port-1 primary configuration register (0x02): data parity error.
5	RW	REG_0X03_DATA_PARITY_ERROR_ROUTING: Error routing: port-0 secondary configuration register (0x03): data parity error.
6	RW	REG_0X04_DATA_PARITY_ERROR_ROUTING: Error routing: port-1 secondary configuration register (0x04): data parity error.
7	RW	REG_0X05_DATA_PARITY_ERROR_ROUTING: Error routing: slave path control register (0x05): data parity error.

Bits	SCOM	Field Mnemonic: Description
8	RW	REG_0X06_DATA_PARITY_ERROR_ROUTING: Error routing: internal path control register (0x06): data parity error.
9	RW	REG_0X07_DATA_PARITY_ERROR_ROUTING: Error routing: primary/secondary or master/slave control register (0x07): data parity error.
10	RW	S_PATH_0_PARITY_ERROR_ROUTING: Error routing: slave path-0: parity error.
11	RW	REG_0X08_DATA_PARITY_ERROR_ROUTING: Error routing: primary/secondary or master/slave status register (0x07): data parity error.
12	RW	REG_0X09_DATA_PARITY_ERROR_ROUTING: Error routing: master path status register (0x09): data parity error.
13	RW	REG_0X0A_DATA_PARITY_ERROR_ROUTING: Error routing: slave path status register (0x0a): data parity error.
14	RW	M_PATH_0_STEP_CHECK_ERROR_ROUTING: Error routing: master path-0: step check error.
15	RW	M_PATH_1_STEP_CHECK_ERROR_ROUTING: Error routing: master path-1: step check error.
16	RW	S_PATH_0_STEP_CHECK_ERROR_ROUTING: Error routing: slave path-0: step check error.
17	RW	I_PATH_STEP_CHECK_ERROR_ROUTING: Error routing: internal path: step check error.
18	RW	PSS_HAM_CORE_INTERRUPT_MASK: Error routing: PSS hamming distance.
19	RW	REG_0X0B_DATA_PARITY_ERROR_ROUTING: Error routing: miscellaneous, reset register (0x0b): data parity error.
20	RW	S_PATH_1_PARITY_ERROR_ROUTING: Error routing: slave path-0: parity error.
21	RW	S_PATH_1_STEP_CHECK_ERROR_ROUTING: Error routing: slave path-1: step check error.
22	RW	I_PATH_DELAY_STEP_CHECK_PARITY_ERROR_ROUTING: Error routing: internal path: delay, step check components: parity error.
23	RW	REG_0X0C_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error of the following registers: TX TType-0 triggering register (0x11) Probe data select register (0x0c) Timer register (0x0d)
24	RW	REG_0X11_0X12_0X13_0X14_0X15_0X16_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on one of the following TX-TType trigger registers: TX TType-0 triggering register (0x11) TX TType-1 triggering register (0x12) TX TType-2 triggering register (0x13) TX TType-3 triggering register (0x14) TX TType-4 triggering register (0x15) TX TType-5 triggering register (0x16)
25	RW	REG_0X17_0X18_0X21_0X22_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on one of the following trigger registers: Move-TOD-to-timebase triggering register (0x17) Load-TOD-mod register (0x18) Load register (0x21) Start-tod register (0x22)
26	RW	REG_0X1D_0X1E_0X1F_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on one of the following trace data registers: Trace data set-1 register (0x1d) Trace data set-2 register (0x1e) Trace data set-3 register (0x1f)
27	RW	REG_0X20_DATA_PARITY_ERROR_ROUTING: Error routing: time value register (0x20): data parity error.
28	RW	REG_0X23_DATA_PARITY_ERROR_ROUTING: Error routing: low-order step register (0x23): data parity error.
29	RW	REG_0X24_DATA_PARITY_ERROR_ROUTING: Error routing: FSM register (0x24): data parity error.

Bits	SCOM	Field Mnemonic: Description
30	RW	REG_0X29_DATA_PARITY_ERROR_ROUTING: Error routing: RX-TType control register: data parity error.
31	RW	REG_0X30_0X31_0X32_0X33_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on one of the following error handling registers: Error register (0x30) Error inject register (0x31) Error mask register (0x32) Core interrupt mask register (0x33)
32	RW	REG_0X10_DATA_PARITY_ERROR_ROUTING: Error routing: chip control register (0x10): data parity error.
33	RW	I_PATH_SYNC_CHECK_ERROR_ROUTING: Error routing: internal path: SYNC check.
34	RW	I_PATH_FSM_STATE_PARITY_ERROR_ROUTING: Error routing: internal path: FSM state parity error.
35	RW	I_PATH_TIME_REG_PARITY_ERROR_ROUTING: Error routing: internal path: time register: parity error.
36	RW	I_PATH_TIME_REG_OVERFLOW_CORE_INTERRUPT: Error routing: internal path: time register overflow.
37	RW	WOF_LOW_ORDER_STEP_COUNTER_PARITY_ERROR_ROUTING: Error routing: WOF counter or low-order-step counter: parity error.
38	RW	RX_TTYPE_0_ERROR_ROUTING: Error routing: received TType-0.
39	RW	RX_TTYPE_1_ERROR_ROUTING: Error routing: received TType-1.
40	RW	RX_TTYPE_2_ERROR_ROUTING: Error routing: received TType-2.
41	RW	RX_TTYPE_3_ERROR_ROUTING: Error routing: received TType-3.
42	RW	RX_TTYPE_4_ERROR_ROUTING: Error routing: received TType-4.
43	RW	RX_TTYPE_5_ERROR_ROUTING: Error routing: received TType-5 when FSM is in running state.
44	RW	PIB_SLAVE_ADDR_INVALID_ERROR_ROUTING: Error routing: PIB slave: invalid address.
45	RW	PIB_SLAVE_WRITE_INVALID_ERROR_ROUTING: Error routing: PIB slave: invalid write.
46	RW	PIB_SLAVE_READ_INVALID_ERROR_ROUTING: Error routing: PIB slave: invalid read.
47	RW	PIB_SLAVE_ADDR_PARITY_ERROR_ROUTING: Error routing: PIB slave: Address parity error.
48	RW	PIB_SLAVE_DATA_PARITY_ERROR_ROUTING: Error routing: PIB slave: data parity error.
49	RW	REG_0X27_DATA_PARITY_ERROR_ROUTING: Error routing: TType control register(0x27): data parity error.
50:52	RW	PIB_MASTER_RSP_INFO_ERROR_ROUTING: Error routing: PIB master: response information error.
53	RW	RX_TTYPE_INVALID_ERROR_ROUTING: Error routing: received invalid TType from register 0x21.
54	RW	RX_TTYPE_4_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on received TType-4 from register 0x21.
55	RW	PIB_MASTER_REQUEST_ERROR_ROUTING: Error routing: PIB master; request while busy error.
56	RW	PIB_RESET_DURING_PIB_ACCESS_ERROR_ROUTING: Error routing: PIB reset received during a PIB master or PIB slave operation.
57	RW	EXTERNAL_XSTOP_ERROR_ROUTING: Error routing: TOD received an external checkstop.
58	RW	SPARE_ERROR_ROUTING_58: Error routing: spare.
59	RW	SPARE_ERROR_ROUTING_59: Error routing: spare.
60	RW	SPARE_ERROR_ROUTING_60: Error routing: spare.
61	RW	SPARE_ERROR_ROUTING_61: Error routing: spare.
62	RW	OSCSWITCH_INTERRUPT_ROUTING: Error routing: interrupt from the oscillator switch.
63	RW	SPARE_ERROR_ROUTING_63: Error routing: spare.

Register Name	CBS Control/Status Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_CS
Address	0000000000050001 (SCOM)
Description	CBS Control/Status Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	CBS_CS_START_BOOT_SEQUENCER: Start boot sequencer explicitly.
1	RWX	CBS_CS_1_UNUSED: Unused.
2	RWX	CBS_CS_OPTION_SKIP_SCAN0_CLOCKSTART: If set, the SCAN0 and CLOCKSTART commands are skipped. Used for memory-preserved reIPL.
3	RWX	CBS_CS_OPTION_PREVENT_SBE_START: If set, start of SBE is suppressed.
4	RWX	CBS_CS_SECURE_ACCESS_BIT: Secure access bit (SAB).
5	ROX	CBS_CS_SAMPLED_SMD_PIN: Sampled state of secure mode disable (SMD) C4 pin.
6:15	RWX	CBS_CS_STATE_MACHINE_TRANSITION_DELAY: Defines transition delay of the boot sequencer state machine. Default value = 128 + 32 FSI cycles.
16:31	ROX	CBS_CS_INTERNAL_STATE_VECTOR: Current state of the CBS state machine.

Register Name	CBS Trace Register 0
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_TR
Address	0000000000050002 (SCOM)
Description	CBS Trace Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX	CBS_TR_SIGNATURE: CBS signature holds the visited states of the last boot sequence.
16:21	RWX	CBS_TR_UNUSED: Unused.
22:31	RWX	CBS_TR_TRANS_DELAY: Programmed transition delay of last boot sequence.

Register Name	CBS Trace Register 1
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_EL
Address	0000000000050003 (SCOM)
Description	CBS Trace Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved.

Register Name	CBS Trace Register 2
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_TR_HIST
Address	0000000000050005 (SCOM)
Description	CBS Trace Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved.

Register Name	CBS Trace Register 3
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_EL_HIST
Address	0000000000050006 (SCOM)
Description	CBS Trace Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved.

Register Name	Selfboot Control/Status Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SB_CS
Address	0000000000050008 (SCOM)
Description	Selfboot Control/Status Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SB_CS_SECURE_DEBUG_MODE: sticky bit: secure debug mode (SDM).
1:11	RW	Reserved.
12	RW	SB_CS_START_RESTART_VECTOR0: SBE start or restart IPL code execution.
13	RW	SB_CS_START_RESTART_VECTOR1: SBE start or restart runtime code execution.
14	RW	SB_CS_INTERRUPT_S0: SBE interrupt S0.
15	RW	SB_CS_INTERRUPT_S1: SBE interrupt S1.
16	RW	SB_CS_BYPASSING_RESET_SEQUENCE_PIB_I2CM: If set, the PIB I2CM reset command is skipped.
17	RW	SB_CS_SELECT_SECONDARY_SEEPROM: If set, the secondary SEEPROM is selected.
18:24	RW	Reserved.
25:31	RW	SB_CS_DEBUG_BOLT_ON_CONTROL_BITS: SBE debug bolt-on control bits.

Register Name	Selfboot Message Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SB_MSG
Address	0000000000050009 (SCOM)
Description	Selfboot Message Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved.

Register Name	Debug CBS Pervasive Clock Controller
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.CBS_STAT
Address	000000000005000B (SCOM)
Description	Debug CBS Pervasive Clock Controller

Bits	SCOM	Field Mnemonic: Description
0	ROX	CBS_STAT_DBG_RESET_EP: Reset endpoint. The CC and CTRL are in reset state.
1	ROX	CBS_STAT_DBG_OPCG_IP: OPCG in progress, not in idle.
2	ROX	CBS_STAT_DBG_VITL_CLKOFF: VITL HLD stopped. When enabled, plat-depth cycles are required to switch this latch.
3	ROX	CBS_STAT_DBG_TEST_ENABLE: Test enable.
4	ROX	CBS_STAT_DBG_CBS_REQ: CBS interface - request (latched).
5:7	ROX	CBS_STAT_DBG_CBS_CMD: CBS interface - command (latched).
8:12	ROX	CBS_STAT_DBG_CBS_STATE: CBS command state machine. 00000 = Idle.
13	ROX	CBS_STAT_DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.
14	ROX	CBS_STAT_DBG_PROTOCOL_ERROR: CBS Protocol Error - REQ raised. Although the state machine is not in idle state, a RESET_EP operation is required to clear this bit. There is no impact on IPL.
15	ROX	CBS_STAT_DBG_PCB_IDLE: PCB interface in idle state.
16:19	ROX	CBS_STAT_DBG_CURRENT_OPCG_MODE: Current or latest OPCG mode. 0000 = NOP 0001 = LBIST 0010 = ABIST 0011 = RUN-N 0100 = SCAN0 0101 = SCAN 0110 = SCAN rotate 0111 = SCAN wth update DR. 1000 = SCAN with capture DR 1001 = Clock change request, 10101 … 1111 = Unused.
20:23	ROX	CBS_STAT_DBG_LAST_OPCG_MODE: Previous OPCG mode.
24	ROX	CBS_STAT_DBG_PCB_ERROR: PCB interface error. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS debug information to the CC Error Register.
25	ROX	CBS_STAT_DBG_PARITY_ERROR: Any parity error, non-PCB parity. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS debug information to the CC Error Register.
26	ROX	CBS_STAT_DBG_CC_ERROR: Any other CC error. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS debug information to the CC Error Register.
27	ROX	CBS_STAT_DBG_CHIPLET_IS_ALIGNED: This bit is set to 1 when the valid align pulse is sent out.
28	ROX	CBS_STAT_DBG_PCB_REQUEST_SINCE_RESET: A reset clears this bit and the first PCB request sets it.
29	ROX	CBS_STAT_DBG_PARANOIA_TEST_ENABLE_CHANGE: The rising or falling edge on test enable after reset. This bit requires a reset endpoint operation to clear. There is no impact on IPL.
30	ROX	CBS_STAT_DBG_PARANOIA_VITL_CLKOFF_CHANGE: The rising or falling edge on VITL_CLKOFF after a reset. This bit requires a reset endpoint operation to clear. There is no impact on IPL.
31	ROX	CBS_STAT_DBG_TP_TPFSI_CBS_ACK: A representation of a CC acknowledgment went to the FSI.

Register Name	Root Control 0 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL0
Address	0000000000050010 (SCOM)
Description	Root Control 0 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	FENCE0_DC: A dedicated fence for observing the OSC switch.
1	RW	TPFSI_TP_FENCE_VTLIO_DC:
2	RW	TPFSI_TPI2C_BUS_FENCE_DC:
3:5	RW	TPCFSI_OPB_SW0_FENCE_DC:
6:7	RW	TPCFSI_OPB_SW1_FENCE_DC:
8	RW	FENCE1_DC:
9	RW	FENCE2_DC:
10	RW	FENCE3_DC:
11	RW	FENCE4_DC:
12	RW	FENCE5_DC:
13	RW	FENCE6_DC:
14	RW	SPARE_FENCE_CONTROL:
15	RW	VDD2VIO_LVL_FENCE_DC:
16	RW	PIB2PCB_DC:
17	RW	OOB_MUX:
18	RW	ROOT_CTRL0_18_SPARE_MUX_CONTROL:
19	RW	ROOT_CTRL0_19_SPARE_MUX_CONTROL:
20	RW	FSI_CC_VSB_CBS_REQ:
21:23	RW	FSI_CC_VSB_CBS_CMD:
24	RW	ROOT_CTRL0_24_SPARE_CBS_CONTROL:
25	RW	ROOT_CTRL0_25_SPARE_CBS_CONTROL:
26	RW	ROOT_CTRL0_26_SPARE_CBS_CONTROL:
27	RW	ROOT_CTRL0_27_SPARE_CBS_CONTROL:
28	RW	ROOT_CTRL0_28_SPARE_RESET:
29	RW	ROOT_CTRL0_29_SPARE_RESET:
30	RW	PCB_RESET_DC:
31	RW	GLOBAL_EP_RESET_DC:

Register Name	Root Control 1 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL1
Address	0000000000050011 (SCOM)
Description	Root Control 1 Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	TP_PROBE0_SEL_DC:
4:7	RW	TP_PROBE1_SEL_DC:
8	RW	TP_PROBE_MESH_SEL_DC:
9	RW	TP_PROBE_DRV_EN_DC:
10	RW	TP_PROBE_HIGHDRIVE_DC:
11:12	RW	TP_FSI_PROBE_SEL_DC:
13	RW	ROOT_CTRL1_13_SPARE_PROBE:
14	RW	ROOT_CTRL1_14_SPARE_PROBE:
15	RW	ROOT_CTRL1_15_SPARE_PROBE:
16	RW	TP_IDDQ_DC:
17	RW	SPARE_RI_CONTROL:
18	RW	SPARE_DI_CONTROL:
19	RW	TP_RI_DC_B:
20	RW	TP_DI1_DC_B:
21	RW	TP_DI2_DC_B:
22	RW	ROOT_CTRL1_22_SPARE_TEST:
23	RW	ROOT_CTRL1_23_SPARE_TEST:
24	RW	TP_TEST_BURNIN_MODE_DC:
25	RW	TPFSI_ARRAY_SET_VBL_TO_VDD_DC:
26	RW	TPFSI_TP_LOWFREQTEST_REFCLK_DC_UNUSED:
27	RW	TP_GLBCK_MEM_TESTCLK_SEL_DC:
28	RW	ROOT_CTRL1_28_SPARE_TEST_CONTROL:
29	RW	ROOT_CTRL1_29_SPARE_TEST_CONTROL:
30	RW	ROOT_CTRL1_30_SPARE_TEST_CONTROL:
31	RW	ROOT_CTRL1_31_SPARE_TEST_CONTROL:

Register Name	Root Control 2 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL2
Address	0000000000050012 (SCOM)
Description	Root Control 2 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	TPFSI_TP_VSB_DBG_PCB_ASYNC_EN_DC:
1	RW	TPFSI_TP_VSB_DBG_PCB_DATA_PAR_DIS_DC:
2	RW	TPFSI_TP_VSB_DBG_PCB_TYPE_PAR_DIS_DC:
3	RW	TPFSI_TP_VSB_PCB_GSD_LATCHED_MODE_DC:
4	RW	TP_PIB_VSB_DISABLE_PARITY_DC:
5	RW	TP_PIB_TRACE_MODE_DATA_DC: Trace mode to the PIB.
6	RW	TP_PIB_VSB_SBE_TRACE_MODE: Trace mode to the SBE.

Bits	SCOM	Field Mnemonic: Description
7	RW	TP_TPCPERV_VSB_TRACE_STOP: Trace stop signal to the DBG macro.
8:10	RW	TP_GPIO_PIB_TIMEOUT:
11	RW	SPARE_PIB_CONTROL:
12	RW	TPCFSI_OPB_SW_RESET_DC:
13	RW	ROOT_CTRL2_13_SPARE_OPB_CONTROL:
14	RW	ROOT_CTRL2_14_SPARE_OPB_CONTROL:
15	RW	ROOT_CTRL2_15_SPARE_OPB_CONTROL:
16	RW	TPFSI_TP_EDRAM_CTRL_GATE:
17	RW	TP_GLBCK_VSB_NEST_VREGDLY_SHUTOFF_DC:
18	RW	TPFSI_TP_PFET_FORCE_OFF_DC:
19	RW	TPFSI_TP_PFET_OVERRIDE_ON_DC_N:
20	RW	TPFSI_TC_HSSPORWREN_ALLOW:
21	RW	ROOT_CTRL2_21_FREE_USAGE:
22	RW	ROOT_CTRL2_22_FREE_USAGE:
23	RW	ROOT_CTRL2_23_FREE_USAGE:
24	RW	TP_IO_VSB_OP0A_V1P8_EN:
25	RW	TP_IO_VSB_OP0B_V1P8_EN:
26	RW	ROOT_CTRL2_26_FREE_USAGE:
27	RW	ROOT_CTRL2_27_FREE_USAGE:
28	RW	ROOT_CTRL2_28_FREE_USAGE:
29	RW	ROOT_CTRL2_29_FREE_USAGE:
30	RW	TP_IO_VSB_OP3A_V1P8_EN:
31	RW	TP_IO_VSB_OP3B_V1P8_EN:

Register Name	Root Control 3 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL3
Address	0000000000050013 (SCOM)
Description	Root Control 3 Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	OSCSWITCH_CNTL0_DC:
16:19	RW	TP_GLBCK_VSB_PCIESW_USEOSC_DC:
20:23	RW	TP_GLBCK_VSB_PCIESW_TWEAK_DC:
24:31	RW	OSCSWITCH_CNTL1_DC:

Register Name	Root Control 4 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL4
Address	0000000000050014 (SCOM)
Description	Root Control 4 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	TP_OSCSWITCH_VSB_ROOT_CTRL4:

Register Name	Root Control 5 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL5
Address	0000000000050015 (SCOM)
Description	Root Control 5 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	TPFSI_OSCSW_ERRINJ0_DC:
3:5	RW	TPFSI_OSCSW_ERRINJ1_DC:
6:7	RW	TPFSI_OSCSW_TWEAK_DC:
8:11	RW	TPFSI_OSCSW_SKEW_ADJUST_DC:
12:14	RW	TPFSI_OSCSW_SNS_CONTENT_SEL_DC:
15	RW	ROOT_CTRL5_15_SPARE_OSC:
16	RW	ROOT_CTRL5_16_SPARE_OSC:
17	RW	ROOT_CTRL5_17_SPARE_OSC:
18	RW	ROOT_CTRL5_18_SPARE_OSC:
19	RW	ROOT_CTRL5_19_SPARE_OSC:
20	RW	ROOT_CTRL5_20_SPARE_OSC:
21	RW	ROOT_CTRL5_21_SPARE_OSC:
22	RW	ROOT_CTRL5_22_SPARE_OSC:
23	RW	ROOT_CTRL5_23_SPARE_OSC:
24	RW	ROOT_CTRL5_24_SPARE_OSC:
25	RW	ROOT_CTRL5_25_SPARE_OSC:
26	RW	ROOT_CTRL5_26_SPARE_OSC:
27	RW	ROOT_CTRL5_27_SPARE_OSC:
28	RW	ROOT_CTRL5_28_SPARE_OSC:
29	RW	ROOT_CTRL5_29_SPARE_OSC:
30	RW	ROOT_CTRL5_30_SPARE_OSC:
31	RW	ROOT_CTRL5_31_SPARE_OSC:

Register Name	Root Control 6 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL6
Address	0000000000050016 (SCOM)
Description	Root Control 6 Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	TP_PLLREFCLK_RCVR_TERM_DC:
2:3	RW	TP_PCIREFCLK_RCVR_TERM_DC:
4	RW	REFCLK_0_TERM_DIS_DC:
5	RW	REFCLK_1_TERM_DIS_DC:
6	RW	ROOT_CTRL6_6_SPARE_TERM_DIS:
7	RW	ROOT_CTRL6_7_SPARE_TERM_DIS:
8	RW	TPFSI_OSCSW0_PGOOD_N:
9	RW	TPFSI_OSCSW1_PGOOD:
10	RW	ROOT_CTRL6_10_SPARE_REFCLOCK:
11	RW	ROOT_CTRL6_11_SPARE_REFCLOCK:
12:23	RW	TPFSI_OFFCHIP_REFCLK_EN_DC:
24	RW	GP_TP_GLBCK_VSB_NEST_MESH_SEL_DC:
25	RW	ROOT_CTRL6_25_SPARE_REFCLOCK_CONTROL:
26	RW	ROOT_CTRL6_26_SPARE_REFCLOCK_CONTROL:
27	RW	TPFSI_ALTREFCLK_SEL:
28	RW	TPFSI_ALTREFCLK_SE1:
29	RW	ROOT_CTRL6_29_SPARE_REFCLOCK_CONTROL:
30	RW	ROOT_CTRL6_30_SPARE_REFCLOCK_CONTROL:
31	RW	ROOT_CTRL6_31_SPARE_REFCLOCK_CONTROL:

Register Name	Root Control 7 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL7
Address	0000000000050017 (SCOM)
Description	Root Control 7 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	ROOT_CTRL7_0_SPARE_SECTOR_BUFFER_CONTROL:
1	RW	ROOT_CTRL7_1_SPARE_SECTOR_BUFFER_CONTROL:
2	RW	ROOT_CTRL7_2_SPARE_SECTOR_BUFFER_CONTROL:
3	RW	ROOT_CTRL7_3_SPARE_SECTOR_BUFFER_CONTROL:
4	RW	ROOT_CTRL7_4_SPARE_SECTOR_BUFFER_CONTROL:
5	RW	ROOT_CTRL7_5_SPARE_SECTOR_BUFFER_CONTROL:
6	RW	ROOT_CTRL7_6_SPARE_SECTOR_BUFFER_CONTROL:
7	RW	ROOT_CTRL7_7_SPARE_SECTOR_BUFFER_CONTROL:

Bits	SCOM	Field Mnemonic: Description
8	RW	ROOT_CTRL7_8_SPARE_SECTOR_BUFFER_CONTROL:
9	RW	ROOT_CTRL7_9_SPARE_SECTOR_BUFFER_CONTROL:
10	RW	ROOT_CTRL7_10_SPARE_SECTOR_BUFFER_CONTROL:
11	RW	ROOT_CTRL7_11_SPARE_SECTOR_BUFFER_CONTROL:
12	RW	ROOT_CTRL7_12_SPARE_SECTOR_BUFFER_CONTROL:
13	RW	ROOT_CTRL7_13_SPARE_SECTOR_BUFFER_CONTROL:
14	RW	ROOT_CTRL7_14_SPARE_SECTOR_BUFFER_CONTROL:
15	RW	ROOT_CTRL7_15_SPARE_SECTOR_BUFFER_CONTROL:
16	RW	ROOT_CTRL7_16_SPARE_RESONANT_CLOCKING_CONTROL:
17	RW	ROOT_CTRL7_17_SPARE_RESONANT_CLOCKING_CONTROL:
18	RW	ROOT_CTRL7_18_SPARE_RESONANT_CLOCKING_CONTROL:
19	RW	ROOT_CTRL7_19_SPARE_RESONANT_CLOCKING_CONTROL:
20	RW	ROOT_CTRL7_20_SPARE_RESONANT_CLOCKING_CONTROL:
21	RW	ROOT_CTRL7_21_SPARE_RESONANT_CLOCKING_CONTROL:
22	RW	ROOT_CTRL7_22_SPARE_RESONANT_CLOCKING_CONTROL:
23	RW	ROOT_CTRL7_23_SPARE_RESONANT_CLOCKING_CONTROL:
24	RW	ROOT_CTRL7_24_SPARE_RESONANT_CLOCKING_CONTROL:
25	RW	ROOT_CTRL7_25_SPARE_RESONANT_CLOCKING_CONTROL:
26	RW	ROOT_CTRL7_26_SPARE_RESONANT_CLOCKING_CONTROL:
27	RW	ROOT_CTRL7_27_SPARE_RESONANT_CLOCKING_CONTROL:
28	RW	ROOT_CTRL7_28_SPARE_RESONANT_CLOCKING_CONTROL:
29	RW	ROOT_CTRL7_29_SPARE_RESONANT_CLOCKING_CONTROL:
30	RW	ROOT_CTRL7_30_SPARE_RESONANT_CLOCKING_CONTROL:
31	RW	ROOT_CTRL7_31_SPARE_RESONANT_CLOCKING_CONTROL:

Register Name	Root Control 8 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL8
Address	0000000000050018 (SCOM)
Description	Root Control 8 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	TP_SS0_PLL_RESET:
1	RW	TP_SS0_PLL_BYPASS:
2	RW	TP_SS0_PLL_TEST_EN:
3	RW	ROOT_CTRL8_3_SPARE_SS_PLL_CONTROL:
4	RW	TP_FILT0_PLL_RESET:
5	RW	TP_FILT0_PLL_BYPASS:
6	RW	TP_FILT0_PLL_TEST_EN:
7	RW	SPARE_FILT0_PLL:

Bits	SCOM	Field Mnemonic: Description
8	RW	TP_FILT1_PLL_RESET:
9	RW	TP_FILT1_PLL_BYPASS:
10	RW	TP_FILT1_PLL_TEST_EN:
11	RW	SPARE_FILT1_PLL:
12	RW	TP_PLL_TEST_EN:
13	RW	TP_PLL_FORCE_OUT_EN_DC:
14	RW	ROOT_CTRL8_14_SPARE_PLL:
15	RW	ROOT_CTRL8_15_SPARE_PLL:
16	RW	TP_CLK_ASYNC_RESET_DC:
17	RW	TP_CLK_DIV_BYPASS_EN_DC:
18	RW	TP_CLK_PDLY_BYPASS1_EN_DC:
19	RW	TP_CLK_PDLY_BYPASS2_EN_DC:
20	RW	ROOT_CTRL8_20_SPARE_PLL_CONTROL:
21	RW	ROOT_CTRL8_21_SPARE_PLL_CONTROL:
22	RW	ROOT_CTRL8_22_SPARE_PLL_CONTROL:
23	RW	ROOT_CTRL8_23_SPARE_PLL_CONTROL:
24	RW	TP_FSI_CLKIN_SEL_DC:
25	RW	ROOT_CTRL8_25_SPARE_CLKIN_CONTROL:
26	RW	ROOT_CTRL8_26_SPARE_CLKIN_CONTROL:
27	RW	ROOT_CTRL8_27_SPARE_CLKIN_CONTROL:
28	RW	TP_PLL_CLKIN_SEL1_DC:
29	RW	TP_PLL_CLKIN_SEL2_DC:
30	RW	TP_PLL_CLKIN_SEL3_DC:
31	RW	TP_PLL_CLKIN_SEL4_DC:

Register Name	Pervasive Control 0 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL0
Address	000000000005001A (SCOM)
Description	PERVASIVE CONTROL 0 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	TP_CHIPLET_EN_DC:
1	RW	TP_PCB_EP_RESET_DC:
2	RW	PERV_CTRL0_2_RESERVED:
3	RW	TP_PLL_TEST_EN_DC:
4	RW	TP_PLLRST_DC:
5	RW	TP_PLLBYP_DC:
6	RW	TP_VITL_SCAN_CLK_DC:
7	RW	TP_VITL_SCIN_DC:

Bits	SCOM	Field Mnemonic: Description
8	RW	PERV_CTRL0_8_RESERVED:
9	RW	TP_FLUSH_ALIGN_OVERWRITE:
10	RW	TP_ARRAY_WRITE_ASSIST_EN_DC:
11	RW	TP_VITL_ACT_DIS_DC:
12	RW	TP_VITL_MPW1_DC_N:
13	RW	TP_VITL_MPW2_DC_N:
14	RW	TP_VITL_MPW3_DC_N:
15	RW	TP_VITL_DELAY_LCLKR_DC:
16	RW	TP_VITL_CLKOFF_DC:
17	RW	TP_FLUSH_SCAN_DC_N:
18	RW	TP_FENCE_EN_DC:
19	RW	TP_RI_DC_N:
20	RW	TP_DI1_DC_N:
21	RW	TP_DI2_DC_N:
22	RW	PERV_CTRL0_22_RESERVED:
23	RW	PERV_CTRL0_23_RESERVED:
24	RW	PERV_CTRL0_24_RESERVED:
25	RW	TP_FENCE_PCB_DC:
26	RW	TP_LVLTRANS_FENCE_DC:
27	RW	TP_EDRAM_ENABLE_DC:
28	RW	PERV_CTRL0_28_RESERVED_FOR_HTB:
29	RW	PERV_CTRL0_29_RESERVED_FOR_HTB:
30	RW	PERV_CTRL0_30_RESERVED_FOR_HTB:
31	RW	PERV_CTRL0_31_RESERVED_FOR_HTB:

Register Name	Pervasive Control 1 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL1
Address	000000000005001B (SCOM)
Description	Pervasive Control 1 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	UNUSED1:
1	RW	UNUSED2:
2	RW	UNUSED3:
3	RW	PERV_CTRL1_3_RESERVED:
4	RW	PERV_CTRL1_4_RESERVED:
5	RW	PERV_CTRL1_5_RESERVED:
6	RW	PERV_CTRL1_6_RESERVED:
7	RW	PERV_CTRL1_7_RESERVED:

Bits	SCOM	Field Mnemonic: Description
8	RW	PERV_CTRL1_8_RESERVED:
9	RW	PERV_CTRL1_9_RESERVED:
10	RW	PERV_CTRL1_10_RESERVED:
11	RW	PERV_CTRL1_11_RESERVED:
12	RW	PERV_CTRL1_12_RESERVED:
13	RW	PERV_CTRL1_13_RESERVED:
14	RW	PERV_CTRL1_14_RESERVED:
15	RW	PERV_CTRL1_15_RESERVED:
16:19	RW	TP_SEC_BUF_DRV_STRENGTH_DC:
20	RW	PERV_CTRL1_20_RESERVED:
21	RW	PERV_CTRL1_21_RESERVED:
22	RW	PERV_CTRL1_22_RESERVED:
23	RW	PERV_CTRL1_23_RESERVED:
24	RW	PERV_CTRL1_24_RESERVED:
25	RW	TP_CLK_PULSE_ENABLE_DC:
26:27	RW	TP_CLK_PULSE_MODE_DC:
28	RW	TP_RESCLK_DIS_DC:
29	RW	TP_CPM_CAL_SET:
30	RW	PERV_CTRL1_30_RESERVED:
31	RW	TP_PCB_PM_MUX_SEL_DC:

Register Name	OSC Switch Sense 1 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SNS1LTH
Address	000000000005001D (SCOM)
Description	OSC Switch Sense 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	SNS1_UNUSED_0_31: Not used.

Register Name	OSC Switch Sense 2 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SNS2LTH
Address	000000000005001E (SCOM)
Description	OSC Switch Sense 2 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	SNS2_UNUSED_0_31: Not used.

Register Name	GP Write Protection Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.GPWRP
Address	000000000005001F (SCOM)
Description	GP Write Protection Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX	MAGIC_COOKIE: This field must be programmed to 0x4453 to enable write protection.
16:31	RWX	EN_OR_DIS_WRITE_PROTECTION: If this field is equal to xFFFF, write protection is disabled. If this field is not equal to xFFFF, this part and the magic cookie form. x'0000' = Register number of root control 0 x'0001' = Register number of root control 1 x'0002' = Register number of root control 2 x'0003' = Register number of root control 3 x'0004' = Register number of root control 4 x'0005' = Register number of root control 5 x'0006' = Register number of root control 6 x'0007' = Register number of root control 7 x'0008' = Register number of root control 8 x'000a' = Register number of perv control 0 x'000b' = Register number of perv control 1

Register Name	Doorbell 1 Status and Control Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.DOORBELL_STATUS_CONTROL_1A
Address	0000000000050020 (SCOM)
Description	Used to control the doorbell 1 and indicate doorbell1 status.

Bits	SCOM	Field Mnemonic: Description
0	RWX	DSC1_PERMISSION_TO_SEND_DOORBELL_1: Permission to send doorbell 1.
1	RWX	DSC1_ABORT_DOORBELL_1: Abort doorbell 1.
2	RWX	DSC1_LBUS_SLAVE_1B_PENDING: FSI/LBUS slave-B pending doorbell 1.
3	RWX_WCLEAR	DSC1_PIB_SLAVE_1A_PENDING: Host/PIB slave-A pending doorbell 1.
4	ROX	DSC1_UNUSED_1A_27: Reserved.
5	RWX	DSC1_XDN_DOORBELL_1: Xdn doorbell 1.
6	RWX_WCLEAR	DSC1_XUP_DOORBELL_1: Xup doorbell 1.
7	ROX	DSC1_UNUSED_1A_24: Reserved.
8:11	RWX	DSC1_HEADER_COUNT_1A: Header count (host/PIB slave-A).
12:19	RWX	DSC1_DATA_COUNT_1A: Data count (host/PIB slave-A).
20:23	RWX_WCLEAR	DSC1_HEADER_COUNT_1B: Header count (FSI/LBUS slave-B).
24:31	RWX_WCLEAR	DSC1_DATA_COUNT_1B: Data count (FSI/LBUS slave-B).

Register Name	Hold the Header/Command 0A Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_0_A
Address	0000000000050021 (SCOM)
Description	Hold the header/command information for the doorbell.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	M1HC0A_MAILBOX_1_HEADER_COMMAND_0_A: Mailbox 1 header/command 0A information.

Register Name	Hold the Header/Command 1A Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_1_A
Address	0000000000050022 (SCOM)
Description	Hold the header/command information for the doorbell.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	M1HC1A_MAILBOX_1_HEADER_COMMAND_1_A: Mailbox1 header/command1A information.

Register Name	Hold the Header/Command 2A Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_2_A
Address	0000000000050023 (SCOM)
Description	Hold the header/command information for the doorbell.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	M1HC2A_MAILBOX_1_HEADER_COMMAND_2_A: Mailbox 1 header/command 2A information.

Register Name	Hold the Header/Command 0B Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_0_B
Address	0000000000050025 (SCOM)
Description	Hold the header/command information for the doorbell.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	M1HC0B_MAILBOX_1_HEADER_COMMAND_0_B: Mailbox 1 header/command 0B information.

Register Name	Hold the Header/Command 1B Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_1_B
Address	0000000000050026 (SCOM)
Description	Hold the header/command information for the doorbell.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	M1HC1B_MAILBOX_1_HEADER_COMMAND_1_B: Mailbox 1 header/command 1B information.

Register Name	Hold the Header/Command 2B Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_HEADER_COMMAND_2_B
Address	0000000000050027 (SCOM)
Description	Hold the header/command information for the doorbell

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	M1HC2B_MAILBOX_1_HEADER_COMMAND_2_B: Mailbox 1 header/command 2B information.

Register Name	Control the Doorbell 2 and Indicate Status
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.DOORBELL_STATUS_CONTROL_2A
Address	0000000000050028 (SCOM)
Description	Used to control the doorbell 2 and indicate status

Bits	SCOM	Field Mnemonic: Description
0	RWX	DSC2_PERMISSION_TO_SEND_DOORBELL_2: Permission to send doorbell 1.
1	RWX	DSC2_ABORT_DOORBELL_2: Abort Doorbell 1.
2	RWX	DSC2_LBUS_SLAVE_2B_PENDING: FSI/LBUS slave-B pending doorbell 1.
3	RWX_WCLEAR	DSC2_PIB_SLAVE_2A_PENDING: Host/PIB slave-A pending doorbell 1.
4	ROX	DSC2_UNUSED_2A_27: Reserved.
5	RWX	DSC2_XDN_DOORBELL_2: Xdn doorbell 1.
6	RWX_WCLEAR	DSC2_XUP_DOORBELL_2: Xup doorbell 1.
7	ROX	DSC2_UNUSED_2A_24: Reserved.
8:11	RWX	DSC2_HEADER_COUNT_2A: Header count (host/PIB slave-A).
12:19	RWX	DSC2_DATA_COUNT_2A: Data count (host/PIB slave-A).
20:23	RWX_WCLEAR	DSC2_HEADER_COUNT_2B: Header count (FSI/LBUS slave-B).
24:31	RWX_WCLEAR	DSC2_DATA_COUNT_2B: Data count (FSI/LBUS slave-B).

Register Name	Hold the Header/Command 0A Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_2_HEADER_COMMAND_0_A
Address	0000000000050029 (SCOM)
Description	Hold the header/command information for the doorbell

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	M2HC0A_MAILBOX_2_HEADER_COMMAND_0_A: Mailbox 2 header/command 0A information.

Register Name	Hold The Header/Command 1A Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_2_HEADER_COMMAND_1_A
Address	000000000005002A (SCOM)
Description	Hold the header/command information for the doorbell

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	M2HC1A_MAILBOX_2_HEADER_COMMAND_1_A: Mailbox 2 header/command 1A information.

Register Name	Hold the Header/Command 2A Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_2_HEADER_COMMAND_2_A
Address	000000000005002B (SCOM)
Description	Hold the header/command information for the doorbell

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	M2HC2A_MAILBOX_2_HEADER_COMMAND_2_A: Mailbox 2 header/command 2A information.

Register Name	Hold the Header/Command 0B Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_2_HEADER_COMMAND_0_B
Address	000000000005002D (SCOM)
Description	Hold the header/command information for the doorbell

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	M2HC0B_MAILBOX_2_HEADER_COMMAND_0_B: Mailbox 2 header/command 0B information.

Register Name	Hold the Header/Command 1B Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_2_HEADER_COMMAND_1_B
Address	000000000005002E (SCOM)
Description	Hold the header/command information for the doorbell.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	M2HC1B_MAILBOX_2_HEADER_COMMAND_1_B: Mailbox 2 header/command 1B information.

Register Name	Hold the Header/Command 2B Information for the Doorbell
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_2_HEADER_COMMAND_2_B
Address	000000000005002F (SCOM)
Description	Hold the header/command information for the doorbell

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	M2HC2B_MAILBOX_2_HEADER_COMMAND_2_B: Mailbox 2 header/command 2B information.

Register Name	Failed Doorbell Operation Status
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_B_DOORBELL_ERROR_STATUS
Address	0000000000050030 (SCOM)
Description	Contains the status of a failed doorbell operation.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	MSBDES_UNUSED_B_31_28: Reserved.
4	ROX	MSBDES_ILLEGAL_OPERATION_ATTEMPTED_1: Illegal operation attempted 1.
5	ROX	MSBDES_WRITE_FULL_PIB_SLAVE_A_MAILBOX_ERROR_1: Write full host/PIB slave-A mailbox error 1.
6	ROX	MSBDES_READ_EMPTY_PIB_SLAVE_A_MAILBOX_ERROR_1: Read empty host/PIB slave-A mailbox error 1.
7	ROX	MSBDES_PIB_SLAVE_A_RAM_PARITY_ERROR_DETECTED_1: Host/PIB slave-A RAM parity error detected 1.
8:14	ROX	MSBDES_ADDRESS_OF_PIB_PARITY_ERROR_1: The address of host/PIB slave-A RAM that caused parity error 1.
15	ROX	MSBDES_CLEAR_STATUS_1: Clear status error of bits [27:17]. Resets complete mailbox and arbiter state machine.
16:19	ROX	MSBDES_UNUSED_B_15_12: Reserved.
20	ROX	MSBDES_ILLEGAL_OPERATION_ATTEMPTED_2: Illegal operation attempted 2.
21	ROX	MSBDES_WRITE_FULL_PIB_SLAVE_A_MAILBOX_ERROR_2: Write full host/PIB slave-A mailbox error 2.
22	ROX	MSBDES_READ_EMPTY_PIB_SLAVE_A_MAILBOX_ERROR_2: Read empty host/PIB slave-A mailbox error 2.
23	ROX	MSBDES_PIB_SLAVE_A_RAM_PARITY_ERROR_DETECTED_2: Host/PIB slave-A RAM parity error detected 2.
24:30	ROX	MSBDES_ADDRESS_OF_PIB_PARITY_ERROR_2: The address of host/PIB slave-A RAM that caused parity error 2.
31	ROX	MSBDES_CLEAR_STATUS_2: Clear status errors bit [11:1]. Resets complete mailbox and arbiter state machine.

Register Name	Failed Doorbell Operation Status
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_A_DOORBELL_ERROR_STATUS
Address	0000000000050031 (SCOM)
Description	Contains the status of a failed doorbell operation.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	MSADES_UNUSED_A_31_28: Reserved.
4	ROX	MSADES_ILLEGAL_OPERATION_ATTEMPTED_1: Illegal operation 1 attempted.
5	ROX	MSADES_WRITE_FULL_PIB_SLAVE_A_MAILBOX_ERROR_1: Write full host/PIB slave-A mail error 1 occurred.
6	ROX	MSADES_READ_EMPTY_PIB_SLAVE_A_MAILBOX_ERROR_1: Read empty host/PIB slave-A mail error 1 occurred.
7	ROX	MSADES_LBUS_SLAVE_B_RAM_PARITY_ERROR_DETECTED_1: Host/PIB slave-A RAM parity error detected 1.
8:14	ROX	MSADES_ADDRESS_OF_LBUS_PARITY_ERROR_1: The address of the FSI/LBUS slave-B RAM that caused parity error 1.
15	ROX	MSADES_CLEAR_STATUS_1: Clear status errors bit [27:17]. Resets complete mailbox and arbiter state machine.
16:19	ROX	MSADES_UNUSED_A_15_12: Reserved.
20	ROX	MSADES_ILLEGAL_OPERATION_ATTEMPTED_2: Illegal operation 2 attempted.

Bits	SCOM	Field Mnemonic: Description
21	ROX	MSADES_WRITE_FULL_PIB_SLAVE_A_MAILBOX_ERROR_2: Write full host/PIB slave-A mail error 2 occurred.
22	ROX	MSADES_READ_EMPTY_PIB_SLAVE_A_MAILBOX_ERROR_2: Read empty host/PIB slave-A mail error 2 occurred.
23	ROX	MSADES_LBUS_SLAVE_B_RAM_PARITY_ERROR_DETECTED_2: Host/PIB slave-A RAM parity error 2 detected.
24:30	ROX	MSADES_ADDRESS_OF_LBUS_PARITY_ERROR_2: The address of FSI/LBUS slave-B RAM caused parity error 2.
31	ROX	MSADES_CLEAR_STATUS_2: Clear status errors bit [11:1]. Resets complete mailbox and arbiter state machine.

Register Name	Interrupt Host/PIB Slave Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_A_DOORBELL_INTERRUPT
Address	0000000000050032 (SCOM)
Description	Interrupt Host/PIB Slave Register.

Bits	SCOM	Field Mnemonic: Description
0:2	RWX_WCLEAR	MSADI_UNUSED_31_11:
3:7	ROX	MSADI_UNUSED_31_11:
8:10	RWX_WCLEAR	MSADI_UNUSED_31_11:
11:20	ROX	MSADI_UNUSED_31_11:
21	ROX	MSADI_PIB_SLAVE_A_DOORBELL_ERROR_MAILBOX_2: Host/PIB slave-A doorbell error mailbox 2 occurred.
22	ROX	MSADI_XUP_MAILBOX_2: Xup mailbox 2.
23	ROX	MSADI_PIB_SLAVE_A_PENDING_MAILBOX_2: Host/PIB slave-A pending mailbox 2.
24:28	ROX	MSADI_UNUSED_7_3:
29	ROX	MSADI_PIB_SLAVE_A_DOORBELL_ERROR_MAILBOX_1: Host/PIB slave-A doorbell error mailbox 1 occurred.
30	ROX	MSADI_XUP_MAILBOX_1: Xup mailbox 1.
31	ROX	MSADI_PIB_SLAVE_A_PENDING_MAILBOX_1: Host/PIB slave-A pending mailbox 1.

Register Name	Mask Bits for The Host/PIB Slave Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_1_SLAVE_A_DOORBELL_INTERRUPT_MASK_1
Address	0000000000050033 (SCOM) 0000000000050034 (SCOM1)
Description	A doorbell interrupts

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:28	RO	RO	constant = 0b00000000000000000000000000000
29	RWX_WOR	WOX_CLEAR	M1SASIM1_ENABLE_PIB_SLAVE_A_DOORBELL_ERROR_MAILBOX_1: Enable Host/PIB slave-A doorbell error mailbox 1.

Bits	SCOM	SCOM1	Field Mnemonic: Description
30	RWX_WOR	WOX_CLEAR	M1SASIM1_ENABLE_XUP_MAILBOX_1: Enable Xup mailbox 1.
31	RWX_WOR	WOX_CLEAR	M1SASIM1_ENABLE_PIB_SLAVE_A_PENDING_MAILBOX_1: Enable host/PIB slave-A pending mailbox 1.

Register Name	Interrupt FSI/LBUS Slave Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_B_DOORBELL_INTERRUPT
Address	0000000000050035 (SCOM)
Description	Interrupt FSI/LBUS Slave Register

Bits	SCOM	Field Mnemonic: Description
0:23	RO	constant = 0b00000000000000000000000
24	ROX	Reserved field.
25	ROX	Reserved field.
26	ROX	MSBDI_LBUS_SLAVE_B_DOORBELL_ERROR_MAILBOX_2: FSI/LBUS slave-B doorbell error mailbox 2 occurred.
27	ROX	MSBDI_LBUS_SLAVE_B_DOORBELL_ERROR_MAILBOX_1: FSI/LBUS slave-B doorbell error mailbox 1 occurred.
28	ROX	MSBDI_XDN_MAILBOX_2: Xdn mailbox 2.
29	ROX	MSBDI_XDN_MAILBOX_1: Xdn mailbox 1.
30	ROX	MSBDI_LBUS_SLAVE_B_PENDING_MAILBOX_2: FSI/LBUS slave-B pending mailbox 2.
31	ROX	MSBDI_LBUS_SLAVE_B_PENDING_MAILBOX_1: FSI/LBUS slave-B pending mailbox 1.

Register Name	Mask Bits for the FSI/LBUS Slave Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.MAILBOX_SLAVE_B_DOORBELL_INTERRUPT_MASK_1
Address	0000000000050036 (SCOM)
Description	B doorbell interrupts.

Bits	SCOM	Field Mnemonic: Description
0:23	RO	constant = 0b00000000000000000000000
24	ROX	MSBDIM1_ENABLE_LBUS_SLAVE_B_PENDING_MAILBOX_1: FSI/LBUS slave-B pending mailbox 1.
25	ROX	MSBDIM1_ENABLE_LBUS_SLAVE_B_PENDING_MAILBOX_2: FSI/LBUS slave-B pending mailbox 2.
26	ROX	MSBDIM1_ENABLE_XDN_MAILBOX_1: Enable Xdn mailbox 1.
27	ROX	MSBDIM1_ENABLE_XDN_MAILBOX_2: Enable Xdn mailbox 2.
28	ROX	MSBDIM1_ENABLE_LBUS_SLAVE_B_DOORBELL_ERROR_MAILBOX_1: Enable FSI/LBUS slave-B doorbell error mailbox 1.
29	ROX	MSBDIM1_ENABLE_LBUS_SLAVE_B_DOORBELL_ERROR_MAILBOX_2: Enable FSI/LBUS slave-B doorbell error mailbox 2.
30	ROX	MSBDIM1_ENABLE_ABORT_MAILBOX_1: Enable abort mailbox 1.
31	ROX	MSBDIM1_ENABLE_ABORT_MAILBOX_2: Enable abort mailbox 2.

Register Name	Scratch Register Number 1
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_1
Address	0000000000050038 (SCOM)
Description	Scratch Register Number 1

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SR_SCRATCH_REGISTER_1: Scratch 1 register.

Register Name	Scratch Register Number 2
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_2
Address	0000000000050039 (SCOM)
Description	Scratch Register Number 2

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SR_SCRATCH_REGISTER_2: Scratch 2 register.

Register Name	Scratch Register Number 3
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_3
Address	000000000005003A (SCOM)
Description	Scratch Register Number 3

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SR_SCRATCH_REGISTER_3: Scratch 3 register.

Register Name	Scratch Register Number 4
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_4
Address	000000000005003B (SCOM)
Description	Scratch Register Number 4

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SR_SCRATCH_REGISTER_4: Scratch 4 register.

Register Name	Scratch Register Number 5
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_5
Address	000000000005003C (SCOM)
Description	Scratch Register Number 5

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SR_SCRATCH_REGISTER_5: Scratch 5 register.

Register Name	Scratch Register Number 6
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_6
Address	000000000005003D (SCOM)
Description	Scratch Register Number 6

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SR_SCRATCH_REGISTER_6: Scratch 6 register.

Register Name	Scratch Register Number 7
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_7
Address	000000000005003E (SCOM)
Description	Scratch Register Number 7

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SR_SCRATCH_REGISTER_7: Scratch 7 register.

Register Name	Scratch Register Number 8
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_8
Address	000000000005003F (SCOM)
Description	Scratch Register Number 8

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SR_SCRATCH_REGISTER_8: Scratch 8 register.

Register Name	Mailbox 1 Data Area (Host) Register 0
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_0
Address	0000000000050040 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 0

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 1
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_1
Address	0000000000050041 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 1

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 2
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_2
Address	0000000000050042 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 2

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 3
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_3
Address	0000000000050043 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 3

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 4
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_4
Address	0000000000050044 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 4

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 5
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_5
Address	0000000000050045 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 5

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 6
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_6
Address	0000000000050046 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 6

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 7
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_7
Address	0000000000050047 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 7

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 8
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_8
Address	0000000000050048 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 8

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 9
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_9
Address	0000000000050049 (SCOM)
Description	Mailbox 1 Data Area (Host) Register 9

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 10
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_10
Address	000000000005004A (SCOM)
Description	Mailbox 1 Data Area (Host) Register 10

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 11
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_11
Address	000000000005004B (SCOM)
Description	Mailbox 1 Data Area (Host) Register 11

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 12
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_12
Address	000000000005004C (SCOM)
Description	Mailbox 1 Data Area (Host) Register 12

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 13
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_13
Address	000000000005004D (SCOM)
Description	Mailbox 1 Data Area (Host) Register 13

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 14
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_14
Address	000000000005004E (SCOM)
Description	Mailbox 1 Data Area (Host) Register 14

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (Host) Register 15
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1A_DATA_AREA_15
Address	000000000005004F (SCOM)
Description	Mailbox 1 Data Area (Host) Register 15

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 0
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_0
Address	0000000000050080 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 0

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 1
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_1
Address	0000000000050081 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 1

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 2
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_2
Address	0000000000050082 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 2

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 3
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_3
Address	0000000000050083 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 3

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 4
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_4
Address	0000000000050084 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 4

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 5
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_5
Address	0000000000050085 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 5

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 6
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_6
Address	0000000000050086 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 6

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 7
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_7
Address	0000000000050087 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 7

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 8
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_8
Address	0000000000050088 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 8

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 9
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_9
Address	0000000000050089 (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 9

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 10
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_10
Address	000000000005008A (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 10

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 11
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_11
Address	000000000005008B (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 11

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 12
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_12
Address	000000000005008C (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 12

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 13
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_13
Address	000000000005008D (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 13

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 14
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_14
Address	000000000005008E (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 14

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 1 Data Area (FSI) Register 15
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M1B_DATA_AREA_15
Address	000000000005008F (SCOM)
Description	Mailbox 1 Data Area (FSI) Register 15

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 0
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_0
Address	00000000000500C0 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 0

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 1
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_1
Address	00000000000500C1 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 1

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 2
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_2
Address	00000000000500C2 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 2

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 3
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_3
Address	00000000000500C3 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 3

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 4
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_4
Address	00000000000500C4 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 4

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 5
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_5
Address	00000000000500C5 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 5

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 6
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_6
Address	00000000000500C6 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 6

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 7
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_7
Address	00000000000500C7 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 7

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 8
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_8
Address	00000000000500C8 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 8

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 9
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_9
Address	00000000000500C9 (SCOM)
Description	Mailbox 2 Data Area (Host) Register 9

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 10
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_10
Address	00000000000500CA (SCOM)
Description	Mailbox 2 Data Area (Host) Register 10

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 11
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_11
Address	00000000000500CB (SCOM)
Description	Mailbox 2 Data Area (Host) Register 11

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 12
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_12
Address	00000000000500CC (SCOM)
Description	Mailbox 2 Data Area (Host) Register 12

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 13
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_13
Address	00000000000500CD (SCOM)
Description	Mailbox 2 Data Area (Host) Register 13

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 14
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_14
Address	00000000000500CE (SCOM)
Description	Mailbox 2 Data Area (Host) Register 14

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (Host) Register 15
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2A_DATA_AREA_15
Address	00000000000500CF (SCOM)
Description	Mailbox 2 Data Area (Host) Register 15

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 0
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_0
Address	0000000000050100 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 0

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 1
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_1
Address	0000000000050101 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 1

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 2
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_2
Address	0000000000050102 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 2

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 3
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_3
Address	0000000000050103 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 3

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 4
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_4
Address	0000000000050104 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 4

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 5
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_5
Address	0000000000050105 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 5

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 6
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_6
Address	0000000000050106 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 6

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 7
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_7
Address	0000000000050107 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 7

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 8
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_8
Address	0000000000050108 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 8

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 9
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_9
Address	0000000000050109 (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 9

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 10
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_10
Address	000000000005010A (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 10

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 11
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_11
Address	000000000005010B (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 11

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 12
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_12
Address	000000000005010C (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 12

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 13
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_13
Address	000000000005010D (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 13

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 14
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_14
Address	000000000005010E (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 14

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Mailbox 2 Data Area (FSI) Register 15
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.M2B_DATA_AREA_15
Address	000000000005010F (SCOM)
Description	Mailbox 2 Data Area (FSI) Register 15

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved field.

Register Name	Root Control Copy 0 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL0_COPY
Address	0000000000050110 (SCOM)
Description	Root Control Copy 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	Root Control Copy 1 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL1_COPY
Address	0000000000050111 (SCOM)
Description	Root Control Copy 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	Root Control Copy 2 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL2_COPY
Address	0000000000050112 (SCOM)
Description	Root Control Copy 2 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	Root Control Copy 3 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL3_COPY
Address	0000000000050113 (SCOM)
Description	Root Control Copy 3 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	Root Control Copy 4 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL4_COPY
Address	0000000000050114 (SCOM)
Description	Root Control Copy 4 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	Root Control Copy 5 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL5_COPY
Address	0000000000050115 (SCOM)
Description	Root Control Copy 5 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	Root Control Copy 6 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL6_COPY
Address	0000000000050116 (SCOM)
Description	Root Control Copy 6 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	Root Control Copy 7 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL7_COPY
Address	0000000000050117 (SCOM)
Description	Root Control Copy 7 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	Root Control Copy 8 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL8_COPY
Address	0000000000050118 (SCOM)
Description	Root Control Copy 8 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	PERV Control Copy 0 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL0_COPY
Address	000000000005011A (SCOM)
Description	PERV Control Copy 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	PERV Control Copy 1 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL1_COPY
Address	000000000005011B (SCOM)
Description	PERV Control Copy 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	Reserved field.

Register Name	Set Function of Root Control 0 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL0_SET
Address	0000000000050120 (SCOM)
Description	SET function of Root Control 0 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_OR	FENCE0_DC: A dedicated fence for observing the OSC switch.
1	WO_OR	TPFSI_TP_FENCE_VTLIO_DC:
2	WO_OR	TPFSI_TPI2C_BUS_FENCE_DC:
3:5	WO_OR	TPCFSI_OPB_SW0_FENCE_DC:
6:7	WO_OR	TPCFSI_OPB_SW1_FENCE_DC:
8	WO_OR	FENCE1_DC:
9	WO_OR	FENCE2_DC:
10	WO_OR	FENCE3_DC:
11	WO_OR	FENCE4_DC:
12	WO_OR	FENCE5_DC:

Bits	SCOM	Field Mnemonic: Description
13	WO_OR	FENCE6_DC:
14	WO_OR	SPARE_FENCE_CONTROL:
15	WO_OR	VDD2VIO_LVL_FENCE_DC:
16	WO_OR	PIB2PCB_DC:
17	WO_OR	OOB_MUX:
18	WO_OR	ROOT_CTRL0_18_SPARE_MUX_CONTROL:
19	WO_OR	ROOT_CTRL0_19_SPARE_MUX_CONTROL:
20	WO_OR	FSI_CC_VSB_CBS_REQ:
21:23	WO_OR	FSI_CC_VSB_CBS_CMD:
24	WO_OR	ROOT_CTRL0_24_SPARE_CBS_CONTROL:
25	WO_OR	ROOT_CTRL0_25_SPARE_CBS_CONTROL:
26	WO_OR	ROOT_CTRL0_26_SPARE_CBS_CONTROL:
27	WO_OR	ROOT_CTRL0_27_SPARE_CBS_CONTROL:
28	WO_OR	ROOT_CTRL0_28_SPARE_RESET:
29	WO_OR	ROOT_CTRL0_29_SPARE_RESET:
30	WO_OR	PCB_RESET_DC:
31	WO_OR	GLOBAL_EP_RESET_DC:

Register Name	Set Function of Root Control 1 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL1_SET
Address	0000000000050121 (SCOM)
Description	Set Function of Root Control 1 Register

Bits	SCOM	Field Mnemonic: Description
0:3	WO_OR	TP_PROBE0_SEL_DC:
4:7	WO_OR	TP_PROBE1_SEL_DC:
8	WO_OR	TP_PROBE_MESH_SEL_DC:
9	WO_OR	TP_PROBE_DRV_EN_DC:
10	WO_OR	TP_PROBE_HIGHDRIVE_DC:
11:12	WO_OR	TP_FSI_PROBE_SEL_DC:
13	WO_OR	ROOT_CTRL1_13_SPARE_PROBE:
14	WO_OR	ROOT_CTRL1_14_SPARE_PROBE:
15	WO_OR	ROOT_CTRL1_15_SPARE_PROBE:
16	WO_OR	TP_IDDQ_DC:
17	WO_OR	SPARE_RI_CONTROL:
18	WO_OR	SPARE_DI_CONTROL:
19	WO_OR	TP_RI_DC_B:
20	WO_OR	TP_DI1_DC_B:
21	WO_OR	TP_DI2_DC_B:

Bits	SCOM	Field Mnemonic: Description
22	WO_OR	ROOT_CTRL1_22_SPARE_TEST:
23	WO_OR	ROOT_CTRL1_23_SPARE_TEST:
24	WO_OR	TP_TEST_BURNIN_MODE_DC:
25	WO_OR	TPFSI_ARRAY_SET_VBL_TO_VDD_DC:
26	WO_OR	TPFSI_TP_LOWFREQTEST_REFCLK_DC_UNUSED:
27	WO_OR	TP_GLBCK_MEM_TESTCLK_SEL_DC:
28	WO_OR	ROOT_CTRL1_28_SPARE_TEST_CONTROL:
29	WO_OR	ROOT_CTRL1_29_SPARE_TEST_CONTROL:
30	WO_OR	ROOT_CTRL1_30_SPARE_TEST_CONTROL:
31	WO_OR	ROOT_CTRL1_31_SPARE_TEST_CONTROL:

Register Name	Set Function of Root Control 2 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL2_SET
Address	0000000000050122 (SCOM)
Description	Set Function of Root Control 2 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_OR	TPFSI_TP_VSB_DBG_PCB_ASYNC_EN_DC:
1	WO_OR	TPFSI_TP_VSB_DBG_PCB_DATA_PAR_DIS_DC:
2	WO_OR	TPFSI_TP_VSB_DBG_PCB_TYPE_PAR_DIS_DC:
3	WO_OR	TPFSI_TP_VSB_PCB_GSD_LATCHED_MODE_DC:
4	WO_OR	TP_PIB_VSB_DISABLE_PARITY_DC:
5	WO_OR	TP_PIB_TRACE_MODE_DATA_DC: Trace mode to PIB.
6	WO_OR	TP_PIB_VSB_SBE_TRACE_MODE: Trace mode to SBE.
7	WO_OR	TP_TPCPERV_VSB_TRACE_STOP: Trace stop signal to DBG macro.
8:10	WO_OR	TP_GPIO_PIB_TIMEOUT:
11	WO_OR	SPARE_PIB_CONTROL:
12	WO_OR	TPCFSI_OPB_SW_RESET_DC:
13	WO_OR	ROOT_CTRL2_13_SPARE_OPB_CONTROL:
14	WO_OR	ROOT_CTRL2_14_SPARE_OPB_CONTROL:
15	WO_OR	ROOT_CTRL2_15_SPARE_OPB_CONTROL:
16	WO_OR	TPFSI_TP_EDRAM_CTRL_GATE:
17	WO_OR	TP_GLBCK_VSB_NEST_VREGDLY_SHUTOFF_DC:
18	WO_OR	TPFSI_TP_PFET_FORCE_OFF_DC:
19	WO_OR	TPFSI_TP_PFET_OVERRIDE_ON_DC_N:
20	WO_OR	TPFSI_TC_HSSPORWREN_ALLOW:
21	WO_OR	ROOT_CTRL2_21_FREE_USAGE:
22	WO_OR	ROOT_CTRL2_22_FREE_USAGE:
23	WO_OR	ROOT_CTRL2_23_FREE_USAGE:

Bits	SCOM	Field Mnemonic: Description
24	WO_OR	TP_IO_VSB_OP0A_V1P8_EN:
25	WO_OR	TP_IO_VSB_OP0B_V1P8_EN:
26	WO_OR	ROOT_CTRL2_26_FREE_USAGE:
27	WO_OR	ROOT_CTRL2_27_FREE_USAGE:
28	WO_OR	ROOT_CTRL2_28_FREE_USAGE:
29	WO_OR	ROOT_CTRL2_29_FREE_USAGE:
30	WO_OR	TP_IO_VSB_OP3A_V1P8_EN:
31	WO_OR	TP_IO_VSB_OP3B_V1P8_EN:

Register Name	Set Function of Root Control 3 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL3_SET
Address	0000000000050123 (SCOM)
Description	Set Function of Root Control 3 Register

Bits	SCOM	Field Mnemonic: Description
0:15	WO_OR	OSCSWITCH_CNTL0_DC:
16:19	WO_OR	TP_GLBCK_VSB_PCIESW_USEOSC_DC:
20:23	WO_OR	TP_GLBCK_VSB_PCIESW_TWEAK_DC:
24:31	WO_OR	OSCSWITCH_CNTL1_DC:

Register Name	Set Function of Root Control 4 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL4_SET
Address	0000000000050124 (SCOM)
Description	Set Function of Root Control 4 Register

Bits	SCOM	Field Mnemonic: Description
0:31	WO_OR	TP_OSCSWITCH_VSB_ROOT_CTRL4:

Register Name	Set Function of Root Control 5 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL5_SET
Address	0000000000050125 (SCOM)
Description	Set Function of Root Control 5 Register

Bits	SCOM	Field Mnemonic: Description
0:2	WO_OR	TPFSI_OSCSW_ERRINJ0_DC:
3:5	WO_OR	TPFSI_OSCSW_ERRINJ1_DC:
6:7	WO_OR	TPFSI_OSCSW_TWEAK_DC:
8:11	WO_OR	TPFSI_OSCSW_SKEW_ADJUST_DC:
12:14	WO_OR	TPFSI_OSCSW_SNS_CONTENT_SEL_DC:

Bits	SCOM	Field Mnemonic: Description
15	WO_OR	ROOT_CTRL5_15_SPARE_OSC:
16	WO_OR	ROOT_CTRL5_16_SPARE_OSC:
17	WO_OR	ROOT_CTRL5_17_SPARE_OSC:
18	WO_OR	ROOT_CTRL5_18_SPARE_OSC:
19	WO_OR	ROOT_CTRL5_19_SPARE_OSC:
20	WO_OR	ROOT_CTRL5_20_SPARE_OSC:
21	WO_OR	ROOT_CTRL5_21_SPARE_OSC:
22	WO_OR	ROOT_CTRL5_22_SPARE_OSC:
23	WO_OR	ROOT_CTRL5_23_SPARE_OSC:
24	WO_OR	ROOT_CTRL5_24_SPARE_OSC:
25	WO_OR	ROOT_CTRL5_25_SPARE_OSC:
26	WO_OR	ROOT_CTRL5_26_SPARE_OSC:
27	WO_OR	ROOT_CTRL5_27_SPARE_OSC:
28	WO_OR	ROOT_CTRL5_28_SPARE_OSC:
29	WO_OR	ROOT_CTRL5_29_SPARE_OSC:
30	WO_OR	ROOT_CTRL5_30_SPARE_OSC:
31	WO_OR	ROOT_CTRL5_31_SPARE_OSC:

Register Name	Set Function of Root Control 6 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL6_SET
Address	0000000000050126 (SCOM)
Description	Set Function of Root Control 6 Register

Bits	SCOM	Field Mnemonic: Description
0:1	WO_OR	TP_PLLREFCLK_RCVR_TERM_DC:
2:3	WO_OR	TP_PCIREFCLK_RCVR_TERM_DC:
4	WO_OR	REFCLK_0_TERM_DIS_DC:
5	WO_OR	REFCLK_1_TERM_DIS_DC:
6	WO_OR	ROOT_CTRL6_6_SPARE_TERM_DIS:
7	WO_OR	ROOT_CTRL6_7_SPARE_TERM_DIS:
8	WO_OR	TPFSI_OSCSW0_PGOOD_N:
9	WO_OR	TPFSI_OSCSW1_PGOOD:
10	WO_OR	ROOT_CTRL6_10_SPARE_REFCLOCK:
11	WO_OR	ROOT_CTRL6_11_SPARE_REFCLOCK:
12:23	WO_OR	TPFSI_OFFCHIP_REFCLK_EN_DC:
24	WO_OR	GP_TP_GLBCK_VSB_NEST_MESH_SEL_DC:
25	WO_OR	ROOT_CTRL6_25_SPARE_REFCLOCK_CONTROL:
26	WO_OR	ROOT_CTRL6_26_SPARE_REFCLOCK_CONTROL:
27	WO_OR	TPFSI_ALTREFCLK_SEL:

Bits	SCOM	Field Mnemonic: Description
28	WO_OR	TPFSI_ALTREFCLK_SE1:
29	WO_OR	ROOT_CTRL6_29_SPARE_REFCLOCK_CONTROL:
30	WO_OR	ROOT_CTRL6_30_SPARE_REFCLOCK_CONTROL:
31	WO_OR	ROOT_CTRL6_31_SPARE_REFCLOCK_CONTROL:

Register Name	Set Function of Root Control 7 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL7_SET
Address	0000000000050127 (SCOM)
Description	Set Function of Root Control 7 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_OR	ROOT_CTRL7_0_SPARE_SECTOR_BUFFER_CONTROL:
1	WO_OR	ROOT_CTRL7_1_SPARE_SECTOR_BUFFER_CONTROL:
2	WO_OR	ROOT_CTRL7_2_SPARE_SECTOR_BUFFER_CONTROL:
3	WO_OR	ROOT_CTRL7_3_SPARE_SECTOR_BUFFER_CONTROL:
4	WO_OR	ROOT_CTRL7_4_SPARE_SECTOR_BUFFER_CONTROL:
5	WO_OR	ROOT_CTRL7_5_SPARE_SECTOR_BUFFER_CONTROL:
6	WO_OR	ROOT_CTRL7_6_SPARE_SECTOR_BUFFER_CONTROL:
7	WO_OR	ROOT_CTRL7_7_SPARE_SECTOR_BUFFER_CONTROL:
8	WO_OR	ROOT_CTRL7_8_SPARE_SECTOR_BUFFER_CONTROL:
9	WO_OR	ROOT_CTRL7_9_SPARE_SECTOR_BUFFER_CONTROL:
10	WO_OR	ROOT_CTRL7_10_SPARE_SECTOR_BUFFER_CONTROL:
11	WO_OR	ROOT_CTRL7_11_SPARE_SECTOR_BUFFER_CONTROL:
12	WO_OR	ROOT_CTRL7_12_SPARE_SECTOR_BUFFER_CONTROL:
13	WO_OR	ROOT_CTRL7_13_SPARE_SECTOR_BUFFER_CONTROL:
14	WO_OR	ROOT_CTRL7_14_SPARE_SECTOR_BUFFER_CONTROL:
15	WO_OR	ROOT_CTRL7_15_SPARE_SECTOR_BUFFER_CONTROL:
16	WO_OR	ROOT_CTRL7_16_SPARE_RESONANT_CLOCKING_CONTROL:
17	WO_OR	ROOT_CTRL7_17_SPARE_RESONANT_CLOCKING_CONTROL:
18	WO_OR	ROOT_CTRL7_18_SPARE_RESONANT_CLOCKING_CONTROL:
19	WO_OR	ROOT_CTRL7_19_SPARE_RESONANT_CLOCKING_CONTROL:
20	WO_OR	ROOT_CTRL7_20_SPARE_RESONANT_CLOCKING_CONTROL:
21	WO_OR	ROOT_CTRL7_21_SPARE_RESONANT_CLOCKING_CONTROL:
22	WO_OR	ROOT_CTRL7_22_SPARE_RESONANT_CLOCKING_CONTROL:
23	WO_OR	ROOT_CTRL7_23_SPARE_RESONANT_CLOCKING_CONTROL:
24	WO_OR	ROOT_CTRL7_24_SPARE_RESONANT_CLOCKING_CONTROL:
25	WO_OR	ROOT_CTRL7_25_SPARE_RESONANT_CLOCKING_CONTROL:
26	WO_OR	ROOT_CTRL7_26_SPARE_RESONANT_CLOCKING_CONTROL:
27	WO_OR	ROOT_CTRL7_27_SPARE_RESONANT_CLOCKING_CONTROL:

Bits	SCOM	Field Mnemonic: Description
28	WO_OR	ROOT_CTRL7_28_SPARE_RESONANT_CLOCKING_CONTROL:
29	WO_OR	ROOT_CTRL7_29_SPARE_RESONANT_CLOCKING_CONTROL:
30	WO_OR	ROOT_CTRL7_30_SPARE_RESONANT_CLOCKING_CONTROL:
31	WO_OR	ROOT_CTRL7_31_SPARE_RESONANT_CLOCKING_CONTROL:

Register Name	Set Function of Root Control 8 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL8_SET
Address	0000000000050128 (SCOM)
Description	Set Function of Root Control 8 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_OR	TP_SS0_PLL_RESET:
1	WO_OR	TP_SS0_PLL_BYPASS:
2	WO_OR	TP_SS0_PLL_TEST_EN:
3	WO_OR	ROOT_CTRL8_3_SPARE_SS_PLL_CONTROL:
4	WO_OR	TP_FILT0_PLL_RESET:
5	WO_OR	TP_FILT0_PLL_BYPASS:
6	WO_OR	TP_FILT0_PLL_TEST_EN:
7	WO_OR	SPARE_FILT0_PLL:
8	WO_OR	TP_FILT1_PLL_RESET:
9	WO_OR	TP_FILT1_PLL_BYPASS:
10	WO_OR	TP_FILT1_PLL_TEST_EN:
11	WO_OR	SPARE_FILT1_PLL:
12	WO_OR	TP_PLL_TEST_EN:
13	WO_OR	TP_PLL_FORCE_OUT_EN_DC:
14	WO_OR	ROOT_CTRL8_14_SPARE_PLL:
15	WO_OR	ROOT_CTRL8_15_SPARE_PLL:
16	WO_OR	TP_CLK_ASYNC_RESET_DC:
17	WO_OR	TP_CLK_DIV_BYPASS_EN_DC:
18	WO_OR	TP_CLK_PDLY_BYPASS1_EN_DC:
19	WO_OR	TP_CLK_PDLY_BYPASS2_EN_DC:
20	WO_OR	ROOT_CTRL8_20_SPARE_PLL_CONTROL:
21	WO_OR	ROOT_CTRL8_21_SPARE_PLL_CONTROL:
22	WO_OR	ROOT_CTRL8_22_SPARE_PLL_CONTROL:
23	WO_OR	ROOT_CTRL8_23_SPARE_PLL_CONTROL:
24	WO_OR	TP_FSI_CLKIN_SEL_DC:
25	WO_OR	ROOT_CTRL8_25_SPARE_CLKIN_CONTROL:
26	WO_OR	ROOT_CTRL8_26_SPARE_CLKIN_CONTROL:
27	WO_OR	ROOT_CTRL8_27_SPARE_CLKIN_CONTROL:

Bits	SCOM	Field Mnemonic: Description
28	WO_OR	TP_PLL_CLKIN_SEL1_DC:
29	WO_OR	TP_PLL_CLKIN_SEL2_DC:
30	WO_OR	TP_PLL_CLKIN_SEL3_DC:
31	WO_OR	TP_PLL_CLKIN_SEL4_DC:

Register Name	Set Function of PERV Control 0 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL0_SET
Address	000000000005012A (SCOM)
Description	Set Function of PERV Control 0 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_OR	TP_CHIPLET_EN_DC:
1	WO_OR	TP_PCB_EP_RESET_DC:
2	WO_OR	PERV_CTRL0_2_RESERVED:
3	WO_OR	TP_PLL_TEST_EN_DC:
4	WO_OR	TP_PLLRST_DC:
5	WO_OR	TP_PLLBYP_DC:
6	WO_OR	TP_VITL_SCAN_CLK_DC:
7	WO_OR	TP_VITL_SCIN_DC:
8	WO_OR	PERV_CTRL0_8_RESERVED:
9	WO_OR	TP_FLUSH_ALIGN_OVERWRITE:
10	WO_OR	TP_ARRAY_WRITE_ASSIST_EN_DC:
11	WO_OR	TP_VITL_ACT_DIS_DC:
12	WO_OR	TP_VITL_MPW1_DC_N:
13	WO_OR	TP_VITL_MPW2_DC_N:
14	WO_OR	TP_VITL_MPW3_DC_N:
15	WO_OR	TP_VITL_DELAY_LCLKR_DC:
16	WO_OR	TP_VITL_CLKOFF_DC:
17	WO_OR	TP_FLUSH_SCAN_DC_N:
18	WO_OR	TP_FENCE_EN_DC:
19	WO_OR	TP_RI_DC_N:
20	WO_OR	TP_DI1_DC_N:
21	WO_OR	TP_DI2_DC_N:
22	WO_OR	PERV_CTRL0_22_RESERVED:
23	WO_OR	PERV_CTRL0_23_RESERVED:
24	WO_OR	PERV_CTRL0_24_RESERVED:
25	WO_OR	TP_FENCE_PCB_DC:
26	WO_OR	TP_LVLTRANS_FENCE_DC:
27	WO_OR	TP_EDRAM_ENABLE_DC:

Bits	SCOM	Field Mnemonic: Description
28	WO_OR	PERV_CTRL0_28_RESERVED_FOR_HTB:
29	WO_OR	PERV_CTRL0_29_RESERVED_FOR_HTB:
30	WO_OR	PERV_CTRL0_30_RESERVED_FOR_HTB:
31	WO_OR	PERV_CTRL0_31_RESERVED_FOR_HTB:

Register Name	Set Function of PERV Control 1 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL1_SET
Address	000000000005012B (SCOM)
Description	Set Function of PERV Control 1 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_OR	UNUSED1:
1	WO_OR	UNUSED2:
2	WO_OR	UNUSED3:
3	WO_OR	PERV_CTRL1_3_RESERVED:
4	WO_OR	PERV_CTRL1_4_RESERVED:
5	WO_OR	PERV_CTRL1_5_RESERVED:
6	WO_OR	PERV_CTRL1_6_RESERVED:
7	WO_OR	PERV_CTRL1_7_RESERVED:
8	WO_OR	PERV_CTRL1_8_RESERVED:
9	WO_OR	PERV_CTRL1_9_RESERVED:
10	WO_OR	PERV_CTRL1_10_RESERVED:
11	WO_OR	PERV_CTRL1_11_RESERVED:
12	WO_OR	PERV_CTRL1_12_RESERVED:
13	WO_OR	PERV_CTRL1_13_RESERVED:
14	WO_OR	PERV_CTRL1_14_RESERVED:
15	WO_OR	PERV_CTRL1_15_RESERVED:
16:19	WO_OR	TP_SEC_BUF_DRV_STRENGTH_DC:
20	WO_OR	PERV_CTRL1_20_RESERVED:
21	WO_OR	PERV_CTRL1_21_RESERVED:
22	WO_OR	PERV_CTRL1_22_RESERVED:
23	WO_OR	PERV_CTRL1_23_RESERVED:
24	WO_OR	PERV_CTRL1_24_RESERVED:
25	WO_OR	TP_CLK_PULSE_ENABLE_DC:
26:27	WO_OR	TP_CLK_PULSE_MODE_DC:
28	WO_OR	TP_RESCLK_DIS_DC:
29	WO_OR	TP_CPM_CAL_SET:
30	WO_OR	PERV_CTRL1_30_RESERVED:
31	WO_OR	TP_PCB_PM_MUX_SEL_DC:

Register Name	Clear Function of Root Control 0 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL0_CLEAR
Address	0000000000050130 (SCOM)
Description	Clear Function of Root Control 0 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_CLEAR	FENCE0_DC: Dedicated fence for observing OSC switch.
1	WO_CLEAR	TPFSI_TP_FENCE_VTLIO_DC:
2	WO_CLEAR	TPFSI_TPI2C_BUS_FENCE_DC:
3:5	WO_CLEAR	TPCFSI_OPB_SW0_FENCE_DC:
6:7	WO_CLEAR	TPCFSI_OPB_SW1_FENCE_DC:
8	WO_CLEAR	FENCE1_DC:
9	WO_CLEAR	FENCE2_DC:
10	WO_CLEAR	FENCE3_DC:
11	WO_CLEAR	FENCE4_DC:
12	WO_CLEAR	FENCE5_DC:
13	WO_CLEAR	FENCE6_DC:
14	WO_CLEAR	SPARE_FENCE_CONTROL:
15	WO_CLEAR	VDD2VIO_LVL_FENCE_DC:
16	WO_CLEAR	PIB2PCB_DC:
17	WO_CLEAR	OOB_MUX:
18	WO_CLEAR	ROOT_CTRL0_18_SPARE_MUX_CONTROL:
19	WO_CLEAR	ROOT_CTRL0_19_SPARE_MUX_CONTROL:
20	WO_CLEAR	FSI_CC_VSB_CBS_REQ:
21:23	WO_CLEAR	FSI_CC_VSB_CBS_CMD:
24	WO_CLEAR	ROOT_CTRL0_24_SPARE_CBS_CONTROL:
25	WO_CLEAR	ROOT_CTRL0_25_SPARE_CBS_CONTROL:
26	WO_CLEAR	ROOT_CTRL0_26_SPARE_CBS_CONTROL:
27	WO_CLEAR	ROOT_CTRL0_27_SPARE_CBS_CONTROL:
28	WO_CLEAR	ROOT_CTRL0_28_SPARE_RESET:
29	WO_CLEAR	ROOT_CTRL0_29_SPARE_RESET:
30	WO_CLEAR	PCB_RESET_DC:
31	WO_CLEAR	GLOBAL_EP_RESET_DC:

Register Name	Clear Function of Root Control 1 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL1_CLEAR
Address	0000000000050131 (SCOM)
Description	Clear Function of Root Control 1 Register

Bits	SCOM	Field Mnemonic: Description
0:3	WO_CLEAR	TP_PROBE0_SEL_DC:
4:7	WO_CLEAR	TP_PROBE1_SEL_DC:
8	WO_CLEAR	TP_PROBE_MESH_SEL_DC:
9	WO_CLEAR	TP_PROBE_DRV_EN_DC:
10	WO_CLEAR	TP_PROBE_HIGHDRIVE_DC:
11:12	WO_CLEAR	TP_FSI_PROBE_SEL_DC:
13	WO_CLEAR	ROOT_CTRL1_13_SPARE_PROBE:
14	WO_CLEAR	ROOT_CTRL1_14_SPARE_PROBE:
15	WO_CLEAR	ROOT_CTRL1_15_SPARE_PROBE:
16	WO_CLEAR	TP_IDDQ_DC:
17	WO_CLEAR	SPARE_RI_CONTROL:
18	WO_CLEAR	SPARE_DI_CONTROL:
19	WO_CLEAR	TP_RI_DC_B:
20	WO_CLEAR	TP_DI1_DC_B:
21	WO_CLEAR	TP_DI2_DC_B:
22	WO_CLEAR	ROOT_CTRL1_22_SPARE_TEST:
23	WO_CLEAR	ROOT_CTRL1_23_SPARE_TEST:
24	WO_CLEAR	TP_TEST_BURNIN_MODE_DC:
25	WO_CLEAR	TPFSI_ARRAY_SET_VBL_TO_VDD_DC:
26	WO_CLEAR	TPFSI_TP_LOWFREQTEST_REFCLK_DC_UNUSED:
27	WO_CLEAR	TP_GLBCK_MEM_TESTCLK_SEL_DC:
28	WO_CLEAR	ROOT_CTRL1_28_SPARE_TEST_CONTROL:
29	WO_CLEAR	ROOT_CTRL1_29_SPARE_TEST_CONTROL:
30	WO_CLEAR	ROOT_CTRL1_30_SPARE_TEST_CONTROL:
31	WO_CLEAR	ROOT_CTRL1_31_SPARE_TEST_CONTROL:

Register Name	Clear Function of Root Control 2 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL2_CLEAR
Address	0000000000050132 (SCOM)
Description	Clear Function of Root Control 2 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_CLEAR	TPFSI_TP_VSB_DBG_PCB_ASYNC_EN_DC:
1	WO_CLEAR	TPFSI_TP_VSB_DBG_PCB_DATA_PAR_DIS_DC:
2	WO_CLEAR	TPFSI_TP_VSB_DBG_PCB_TYPE_PAR_DIS_DC:
3	WO_CLEAR	TPFSI_TP_VSB_PCB_GSD_LATCHED_MODE_DC:
4	WO_CLEAR	TP_PIB_VSB_DISABLE_PARITY_DC:
5	WO_CLEAR	TP_PIB_TRACE_MODE_DATA_DC: Trace mode to PIB.
6	WO_CLEAR	TP_PIB_VSB_SBE_TRACE_MODE: Trace mode to SBE.

Bits	SCOM	Field Mnemonic: Description
7	WO_CLEAR	TP_TPCPERV_VSB_TRACE_STOP: Trace stop signal to DBG macro.
8:10	WO_CLEAR	TP_GPIO_PIB_TIMEOUT:
11	WO_CLEAR	SPARE_PIB_CONTROL:
12	WO_CLEAR	TPCFSI_OPB_SW_RESET_DC:
13	WO_CLEAR	ROOT_CTRL2_13_SPARE_OPB_CONTROL:
14	WO_CLEAR	ROOT_CTRL2_14_SPARE_OPB_CONTROL:
15	WO_CLEAR	ROOT_CTRL2_15_SPARE_OPB_CONTROL:
16	WO_CLEAR	TPFSI_TP_EDRAM_CTRL_GATE:
17	WO_CLEAR	TP_GLBCK_VSB_NEST_VREGDLY_SHUTOFF_DC:
18	WO_CLEAR	TPFSI_TP_PFET_FORCE_OFF_DC:
19	WO_CLEAR	TPFSI_TP_PFET_OVERRIDE_ON_DC_N:
20	WO_CLEAR	TPFSI_TC_HSSPORWREN_ALLOW:
21	WO_CLEAR	ROOT_CTRL2_21_FREE_USAGE:
22	WO_CLEAR	ROOT_CTRL2_22_FREE_USAGE:
23	WO_CLEAR	ROOT_CTRL2_23_FREE_USAGE:
24	WO_CLEAR	TP_IO_VSB_OP0A_V1P8_EN:
25	WO_CLEAR	TP_IO_VSB_OP0B_V1P8_EN:
26	WO_CLEAR	ROOT_CTRL2_26_FREE_USAGE:
27	WO_CLEAR	ROOT_CTRL2_27_FREE_USAGE:
28	WO_CLEAR	ROOT_CTRL2_28_FREE_USAGE:
29	WO_CLEAR	ROOT_CTRL2_29_FREE_USAGE:
30	WO_CLEAR	TP_IO_VSB_OP3A_V1P8_EN:
31	WO_CLEAR	TP_IO_VSB_OP3B_V1P8_EN:

Register Name	Clear Function of Root Control 3 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL3_CLEAR
Address	0000000000050133 (SCOM)
Description	Clear Function of Root Control 3 Register

Bits	SCOM	Field Mnemonic: Description
0:15	WO_CLEAR	OSCSWITCH_CNTL0_DC:
16:19	WO_CLEAR	TP_GLBCK_VSB_PCIESW_USEOSC_DC:
20:23	WO_CLEAR	TP_GLBCK_VSB_PCIESW_TWEAK_DC:
24:31	WO_CLEAR	OSCSWITCH_CNTL1_DC:

Register Name	Clear Function of Root Control 4 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL4_CLEAR
Address	0000000000050134 (SCOM)
Description	Clear Function of Root Control 4 Register

Bits	SCOM	Field Mnemonic: Description
0:31	WO_CLEAR	TP_OSCSWITCH_VSB_ROOT_CTRL4:

Register Name	Clear Function of Root Control 5 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL5_CLEAR
Address	0000000000050135 (SCOM)
Description	Clear Function of Root Control 5 Register

Bits	SCOM	Field Mnemonic: Description
0:2	WO_CLEAR	TPFSI_OSCSW_ERRINJ0_DC:
3:5	WO_CLEAR	TPFSI_OSCSW_ERRINJ1_DC:
6:7	WO_CLEAR	TPFSI_OSCSW_TWEAK_DC:
8:11	WO_CLEAR	TPFSI_OSCSW_SKEW_ADJUST_DC:
12:14	WO_CLEAR	TPFSI_OSCSW_SNS_CONTENT_SEL_DC:
15	WO_CLEAR	ROOT_CTRL5_15_SPARE_OSC:
16	WO_CLEAR	ROOT_CTRL5_16_SPARE_OSC:
17	WO_CLEAR	ROOT_CTRL5_17_SPARE_OSC:
18	WO_CLEAR	ROOT_CTRL5_18_SPARE_OSC:
19	WO_CLEAR	ROOT_CTRL5_19_SPARE_OSC:
20	WO_CLEAR	ROOT_CTRL5_20_SPARE_OSC:
21	WO_CLEAR	ROOT_CTRL5_21_SPARE_OSC:
22	WO_CLEAR	ROOT_CTRL5_22_SPARE_OSC:
23	WO_CLEAR	ROOT_CTRL5_23_SPARE_OSC:
24	WO_CLEAR	ROOT_CTRL5_24_SPARE_OSC:
25	WO_CLEAR	ROOT_CTRL5_25_SPARE_OSC:
26	WO_CLEAR	ROOT_CTRL5_26_SPARE_OSC:
27	WO_CLEAR	ROOT_CTRL5_27_SPARE_OSC:
28	WO_CLEAR	ROOT_CTRL5_28_SPARE_OSC:
29	WO_CLEAR	ROOT_CTRL5_29_SPARE_OSC:
30	WO_CLEAR	ROOT_CTRL5_30_SPARE_OSC:
31	WO_CLEAR	ROOT_CTRL5_31_SPARE_OSC:

Register Name	Clear Function of Root Control 6 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL6_CLEAR
Address	0000000000050136 (SCOM)
Description	Clear Function of Root Control 6 Register

Bits	SCOM	Field Mnemonic: Description
0:1	WO_CLEAR	TP_PLLREFCLK_RCVR_TERM_DC:
2:3	WO_CLEAR	TP_PCIREFCLK_RCVR_TERM_DC:
4	WO_CLEAR	REFCLK_0_TERM_DIS_DC:
5	WO_CLEAR	REFCLK_1_TERM_DIS_DC:
6	WO_CLEAR	ROOT_CTRL6_6_SPARE_TERM_DIS:
7	WO_CLEAR	ROOT_CTRL6_7_SPARE_TERM_DIS:
8	WO_CLEAR	TPFSI_OSCSW0_PGOOD_N:
9	WO_CLEAR	TPFSI_OSCSW1_PGOOD:
10	WO_CLEAR	ROOT_CTRL6_10_SPARE_REFCLOCK:
11	WO_CLEAR	ROOT_CTRL6_11_SPARE_REFCLOCK:
12:23	WO_CLEAR	TPFSI_OFFCHIP_REFCLK_EN_DC:
24	WO_CLEAR	GP_TP_GLBCK_VSB_NEST_MESH_SEL_DC:
25	WO_CLEAR	ROOT_CTRL6_25_SPARE_REFCLOCK_CONTROL:
26	WO_CLEAR	ROOT_CTRL6_26_SPARE_REFCLOCK_CONTROL:
27	WO_CLEAR	TPFSI_ALTREFCLK_SEL:
28	WO_CLEAR	TPFSI_ALTREFCLK_SE1:
29	WO_CLEAR	ROOT_CTRL6_29_SPARE_REFCLOCK_CONTROL:
30	WO_CLEAR	ROOT_CTRL6_30_SPARE_REFCLOCK_CONTROL:
31	WO_CLEAR	ROOT_CTRL6_31_SPARE_REFCLOCK_CONTROL:

Register Name	Clear Function of Root Control 7 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL7_CLEAR
Address	0000000000050137 (SCOM)
Description	Clear Function of Root Control 7 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_CLEAR	ROOT_CTRL7_0_SPARE_SECTOR_BUFFER_CONTROL:
1	WO_CLEAR	ROOT_CTRL7_1_SPARE_SECTOR_BUFFER_CONTROL:
2	WO_CLEAR	ROOT_CTRL7_2_SPARE_SECTOR_BUFFER_CONTROL:
3	WO_CLEAR	ROOT_CTRL7_3_SPARE_SECTOR_BUFFER_CONTROL:
4	WO_CLEAR	ROOT_CTRL7_4_SPARE_SECTOR_BUFFER_CONTROL:
5	WO_CLEAR	ROOT_CTRL7_5_SPARE_SECTOR_BUFFER_CONTROL:
6	WO_CLEAR	ROOT_CTRL7_6_SPARE_SECTOR_BUFFER_CONTROL:
7	WO_CLEAR	ROOT_CTRL7_7_SPARE_SECTOR_BUFFER_CONTROL:

Bits	SCOM	Field Mnemonic: Description
8	WO_CLEAR	ROOT_CTRL7_8_SPARE_SECTOR_BUFFER_CONTROL:
9	WO_CLEAR	ROOT_CTRL7_9_SPARE_SECTOR_BUFFER_CONTROL:
10	WO_CLEAR	ROOT_CTRL7_10_SPARE_SECTOR_BUFFER_CONTROL:
11	WO_CLEAR	ROOT_CTRL7_11_SPARE_SECTOR_BUFFER_CONTROL:
12	WO_CLEAR	ROOT_CTRL7_12_SPARE_SECTOR_BUFFER_CONTROL:
13	WO_CLEAR	ROOT_CTRL7_13_SPARE_SECTOR_BUFFER_CONTROL:
14	WO_CLEAR	ROOT_CTRL7_14_SPARE_SECTOR_BUFFER_CONTROL:
15	WO_CLEAR	ROOT_CTRL7_15_SPARE_SECTOR_BUFFER_CONTROL:
16	WO_CLEAR	ROOT_CTRL7_16_SPARE_RESONANT_CLOCKING_CONTROL:
17	WO_CLEAR	ROOT_CTRL7_17_SPARE_RESONANT_CLOCKING_CONTROL:
18	WO_CLEAR	ROOT_CTRL7_18_SPARE_RESONANT_CLOCKING_CONTROL:
19	WO_CLEAR	ROOT_CTRL7_19_SPARE_RESONANT_CLOCKING_CONTROL:
20	WO_CLEAR	ROOT_CTRL7_20_SPARE_RESONANT_CLOCKING_CONTROL:
21	WO_CLEAR	ROOT_CTRL7_21_SPARE_RESONANT_CLOCKING_CONTROL:
22	WO_CLEAR	ROOT_CTRL7_22_SPARE_RESONANT_CLOCKING_CONTROL:
23	WO_CLEAR	ROOT_CTRL7_23_SPARE_RESONANT_CLOCKING_CONTROL:
24	WO_CLEAR	ROOT_CTRL7_24_SPARE_RESONANT_CLOCKING_CONTROL:
25	WO_CLEAR	ROOT_CTRL7_25_SPARE_RESONANT_CLOCKING_CONTROL:
26	WO_CLEAR	ROOT_CTRL7_26_SPARE_RESONANT_CLOCKING_CONTROL:
27	WO_CLEAR	ROOT_CTRL7_27_SPARE_RESONANT_CLOCKING_CONTROL:
28	WO_CLEAR	ROOT_CTRL7_28_SPARE_RESONANT_CLOCKING_CONTROL:
29	WO_CLEAR	ROOT_CTRL7_29_SPARE_RESONANT_CLOCKING_CONTROL:
30	WO_CLEAR	ROOT_CTRL7_30_SPARE_RESONANT_CLOCKING_CONTROL:
31	WO_CLEAR	ROOT_CTRL7_31_SPARE_RESONANT_CLOCKING_CONTROL:

Register Name	Clear Function of Root Control 8 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.ROOT_CTRL8_CLEAR
Address	0000000000050138 (SCOM)
Description	Clear Function of Root Control 8 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_CLEAR	TP_SS0_PLL_RESET:
1	WO_CLEAR	TP_SS0_PLL_BYPASS:
2	WO_CLEAR	TP_SS0_PLL_TEST_EN:
3	WO_CLEAR	ROOT_CTRL8_3_SPARE_SS_PLL_CONTROL:
4	WO_CLEAR	TP_FILT0_PLL_RESET:
5	WO_CLEAR	TP_FILT0_PLL_BYPASS:
6	WO_CLEAR	TP_FILT0_PLL_TEST_EN:
7	WO_CLEAR	SPARE_FILT0_PLL:

Bits	SCOM	Field Mnemonic: Description
8	WO_CLEAR	TP_FILT1_PLL_RESET:
9	WO_CLEAR	TP_FILT1_PLL_BYPASS:
10	WO_CLEAR	TP_FILT1_PLL_TEST_EN:
11	WO_CLEAR	SPARE_FILT1_PLL:
12	WO_CLEAR	TP_PLL_TEST_EN:
13	WO_CLEAR	TP_PLL_FORCE_OUT_EN_DC:
14	WO_CLEAR	ROOT_CTRL8_14_SPARE_PLL:
15	WO_CLEAR	ROOT_CTRL8_15_SPARE_PLL:
16	WO_CLEAR	TP_CLK_ASYNC_RESET_DC:
17	WO_CLEAR	TP_CLK_DIV_BYPASS_EN_DC:
18	WO_CLEAR	TP_CLK_PDLY_BYPASS1_EN_DC:
19	WO_CLEAR	TP_CLK_PDLY_BYPASS2_EN_DC:
20	WO_CLEAR	ROOT_CTRL8_20_SPARE_PLL_CONTROL:
21	WO_CLEAR	ROOT_CTRL8_21_SPARE_PLL_CONTROL:
22	WO_CLEAR	ROOT_CTRL8_22_SPARE_PLL_CONTROL:
23	WO_CLEAR	ROOT_CTRL8_23_SPARE_PLL_CONTROL:
24	WO_CLEAR	TP_FSI_CLKIN_SEL_DC:
25	WO_CLEAR	ROOT_CTRL8_25_SPARE_CLKIN_CONTROL:
26	WO_CLEAR	ROOT_CTRL8_26_SPARE_CLKIN_CONTROL:
27	WO_CLEAR	ROOT_CTRL8_27_SPARE_CLKIN_CONTROL:
28	WO_CLEAR	TP_PLL_CLKIN_SEL1_DC:
29	WO_CLEAR	TP_PLL_CLKIN_SEL2_DC:
30	WO_CLEAR	TP_PLL_CLKIN_SEL3_DC:
31	WO_CLEAR	TP_PLL_CLKIN_SEL4_DC:

Register Name	Clear Function of PERV Control 0 Register
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL0_CLEAR
Address	000000000005013A (SCOM)
Description	CLEAR function of PERV Control 0 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_CLEAR	TP_CHIPLET_EN_DC:
1	WO_CLEAR	TP_PCB_EP_RESET_DC:
2	WO_CLEAR	PERV_CTRL0_2_RESERVED:
3	WO_CLEAR	TP_PLL_TEST_EN_DC:
4	WO_CLEAR	TP_PLLRST_DC:
5	WO_CLEAR	TP_PLLBYP_DC:
6	WO_CLEAR	TP_VITL_SCAN_CLK_DC:
7	WO_CLEAR	TP_VITL_SCIN_DC:

Bits	SCOM	Field Mnemonic: Description
8	WO_CLEAR	PERV_CTRL0_8_RESERVED:
9	WO_CLEAR	TP_FLUSH_ALIGN_OVERWRITE:
10	WO_CLEAR	TP_ARRAY_WRITE_ASSIST_EN_DC:
11	WO_CLEAR	TP_VITL_ACT_DIS_DC:
12	WO_CLEAR	TP_VITL_MPW1_DC_N:
13	WO_CLEAR	TP_VITL_MPW2_DC_N:
14	WO_CLEAR	TP_VITL_MPW3_DC_N:
15	WO_CLEAR	TP_VITL_DELAY_LCLKR_DC:
16	WO_CLEAR	TP_VITL_CLKOFF_DC:
17	WO_CLEAR	TP_FLUSH_SCAN_DC_N:
18	WO_CLEAR	TP_FENCE_EN_DC:
19	WO_CLEAR	TP_RI_DC_N:
20	WO_CLEAR	TP_DI1_DC_N:
21	WO_CLEAR	TP_DI2_DC_N:
22	WO_CLEAR	PERV_CTRL0_22_RESERVED:
23	WO_CLEAR	PERV_CTRL0_23_RESERVED:
24	WO_CLEAR	PERV_CTRL0_24_RESERVED:
25	WO_CLEAR	TP_FENCE_PCB_DC:
26	WO_CLEAR	TP_LVLTRANS_FENCE_DC:
27	WO_CLEAR	TP_EDRAM_ENABLE_DC:
28	WO_CLEAR	PERV_CTRL0_28_RESERVED_FOR_HTB:
29	WO_CLEAR	PERV_CTRL0_29_RESERVED_FOR_HTB:
30	WO_CLEAR	PERV_CTRL0_30_RESERVED_FOR_HTB:
31	WO_CLEAR	PERV_CTRL0_31_RESERVED_FOR_HTB:

Register Name	**Clear Function of PERV Control 1 Register**
Mnemonic	TP.TPVSB.FSI.W.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_CTRL1_CLEAR
Address	000000000005013B (SCOM)
Description	Clear Function of PERV Control 1 Register

Bits	SCOM	Field Mnemonic: Description
0	WO_CLEAR	UNUSED1:
1	WO_CLEAR	UNUSED2:
2	WO_CLEAR	UNUSED3:
3	WO_CLEAR	PERV_CTRL1_3_RESERVED:
4	WO_CLEAR	PERV_CTRL1_4_RESERVED:
5	WO_CLEAR	PERV_CTRL1_5_RESERVED:
6	WO_CLEAR	PERV_CTRL1_6_RESERVED:
7	WO_CLEAR	PERV_CTRL1_7_RESERVED:

Bits	SCOM	Field Mnemonic: Description
8	WO_CLEAR	PERV_CTRL1_8_RESERVED:
9	WO_CLEAR	PERV_CTRL1_9_RESERVED:
10	WO_CLEAR	PERV_CTRL1_10_RESERVED:
11	WO_CLEAR	PERV_CTRL1_11_RESERVED:
12	WO_CLEAR	PERV_CTRL1_12_RESERVED:
13	WO_CLEAR	PERV_CTRL1_13_RESERVED:
14	WO_CLEAR	PERV_CTRL1_14_RESERVED:
15	WO_CLEAR	PERV_CTRL1_15_RESERVED:
16:19	WO_CLEAR	TP_SEC_BUF_DRV_STRENGTH_DC:
20	WO_CLEAR	PERV_CTRL1_20_RESERVED:
21	WO_CLEAR	PERV_CTRL1_21_RESERVED:
22	WO_CLEAR	PERV_CTRL1_22_RESERVED:
23	WO_CLEAR	PERV_CTRL1_23_RESERVED:
24	WO_CLEAR	PERV_CTRL1_24_RESERVED:
25	WO_CLEAR	TP_CLK_PULSE_ENABLE_DC:
26:27	WO_CLEAR	TP_CLK_PULSE_MODE_DC:
28	WO_CLEAR	TP_RESCLK_DIS_DC:
29	WO_CLEAR	TP_CPM_CAL_SET:
30	WO_CLEAR	PERV_CTRL1_30_RESERVED:
31	WO_CLEAR	TP_PCB_PM_MUX_SEL_DC:

Register Name	GPE Timer Select Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPETSEL
Address	0000000000060000 (SCOM)
Description	GPE Timer Select Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	GPETSEL_FIT_SEL: Selects the fixed interval timer rate.
4:7	RW	GPETSEL_WATCHDOG_SEL: Selects the watchdog timer rate
8:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	GPE Interrupt Vector Prefix Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPEIVPR
Address	0000000000060001 (SCOM)
Description	GPE Interrupt Vector Prefix Register

Bits	SCOM	Field Mnemonic: Description
0:22	RW	GPEIVPR_IVPR: Interrupt Prefix Vector Register (Resets to 0xFFFFFE left justified).
23	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	GPE Debug Mode Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPEDBG
Address	0000000000060002 (SCOM)
Description	GPE Debug Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GPEDBG_EN_DBG: Enables debug trace. This bit is the switch that enables clocks to the trace. This bit also causes RISCTrace to start on the Rising edge and stop on the falling edge when RISCTrace is enabled. (TRACE_DATA_SEL[0] = 0).
1	RW	GPEDBG_HALT_ON_XSTOP: Enable halt on checkstop input.
2	RW	GPEDBG_HALT_ON_TRIG: Enable halt on trigger input.
3	RW	GPEDBG_RESERVED3: Implemented but not used.
4	RW	GPEDBG_EN_INTR_ADDR: When RISCTrace is enabled, trace the full interrupt vector address; otherwise, trace ONLY the lower byte of the address.
5	RW	GPEDBG_EN_TRACE_EXTRA: When RISCTrace is enabled and this bit is set, extra trace data is recorded. This is not needed for 405 RISCTrace specification. When this bit is not set, MTMSR or MTSPRG0 data is not recorded and a new MSR on an RFI is not recorded.
6	RW	GPEDBG_EN_TRACE_STALL: When RISCTrace is enabled and this bit is set, cycles are stalled when the processor is not actively executing. Also, any instruction that is not already included in the previous event is recorded unless it is halted or in wait state. When this bit is not set, the RISCTrace is smaller but not time accurate.
7	RW	GPEDBG_EN_WAIT_CYCLES: When RISCTrace is enabled and this bit is set, stall events are used to record the number of cycles in the PPE that are in wait state. Otherwise, the cycles in wait state are ignored. When this bit is set, EN_TRACE_STALL must also be set.
8	RW	GPEDBG_EN_FULL_SPEED: When this bit is set, the trace valid is pulsed at 1:1 (4x faster than the debug data, which changes at PPE clock speed). This is required for CHTM and NHTM (in-memory trace). When this mode is not set, the trace valid is held constant for a full PPE cycle (four 1:1 cycles). When connected to a trace array this value should match the corresponding sampling speed of the array.
9	RW	GPEDBG_RESERVED9: Implemented but not used.
10:11	RW	GPEDBG_TRACE_MODE_SEL: Bit GPEDBG_EN_DBG (bit 0) chooses between 0 (PPE Core Debug Mode A) and 1 (Mode B). When bit GPEDBG_HALT_ON_XSTOP (bit 1) is set, it ORs in the secondary valid corresponding lower bits of the trace data when they are from a different source than bits 0:23. **Note:** When bit 1 = ‘0’ it is likely for HTM tracing.
12:15	RW	GPEDBG_RESERVED12_15: Implemented but not used.
16	RW	GPEDBG_FIR_TRIGGER: Programmatically asserts a FIR bit to inject a checkstop or send an attention to the service element.
17:19	RW	GPEDBG_SPARE: Spare (used for GPIO on other instances).

Bits	SCOM	Field Mnemonic: Description
20:23	RW	GPEDBG_TRACE_DATA_SEL: MUX select to choose debug data content on the trace bus. All 16 encodes are defined as per the table in the Debug Bolt-on chapter of the Power Management Specification. 0x0 chooses an 88-bit PPE-RISCTrace by default. b00XX enables RISCTrace records to be generated in the upper 64-bits of trace data. 0bXX00 selects the remaining 24 bits to form 88-bit trace packets to be generated on the debug bus to be sent to the hardware trace array. Otherwise, PPE, MIB, or EXT data is used. The other 12 encodes contain permutations of the PPE core, memory interface, and external debug buses instead of RISCTrace records.
24:63	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	GPE SRAM Translation Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPESTR
Address	0000000000060003 (SCOM)
Description	GPE SRAM Translation Register

Bits	SCOM	Field Mnemonic: Description
0:11	RO	constant=0b000000000000
12:21	RW	GPESTR_PBASE: Specifies the physical base address for effective addresses starting at 0xFFFF8000 and extending upwards for the range indicated by GSTR[size]. GSTR[pbase] must imply a correctly aligned physical base address for any legal value of GSTR[size] detailed as follows: Size = 0b000 (1 KB) : pbase = 0bxxxxxxxxxx Size = 0b001 (2 KB) : pbase = 0bxxxxxxxxx0 Size = 0b010 (4 KB) : pbase = 0bxxxxxxxx00 Size = 0b011 (8 KB) : pbase = 0bxxxxxxx000 Size = 0b100 (16 KB) : pbase = 0bxxxxxx0000 Size = 0b101 (32 KB) : pbase = 0bxxxxx00000 **Note:** The reset value represents an illegal OCI address, which results in a machine check exception if a translatable effective address is accessed.
22:28	RO	constant =0b0000000
29:31	RW	GPESTR_SIZE: Specifies the size of the translated region : 0b000: 1 KB 0b001: 2 KB 0b010: 4 KB 0b011: 8 KB 0b100: 16 KB 0b101: 32 KB Other values are illegal and result in data or instruction storage exceptions as appropriate.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE Memory Access Configuration Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPEMACR
Address	0000000000060004 (SCOM)
Description	GPE Memory Access Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	GPEMACR_MEM_LOW_PRIORITY: OCI priority to use for accessing main memory when address[0:1] = 10 and the PPE high priority output is ‘0’.

Bits	SCOM	Field Mnemonic: Description
2:3	RW	GPEMACR_MEM_HIGH_PRIORITY: OCI priority to use for accessing main memory when address[0:1] = 10 and the PPE high priority output is ‘1’.
4:5	RW	GPEMACR_LOCAL_LOW_PRIORITY: OCI priority to use for accessing local registers when address[0:2] = 110 and the PPE high priority output is ‘0’.
6:7	RW	GPEMACR_LOCAL_HIGH_PRIORITY: OCI priority to use for accessing local registers when address[0:2] = 110 and the PPE high priority output is ‘1’.
8:9	RW	GPEMACR_SRAM_LOW_PRIORITY: OCI priority to use for accessing SRAM tank when Address(0:2) = 111 and the PPE high priority output is ‘0’.
10:11	RW	GPEMACR_SRAM_HIGH_PRIORITY: OCI priority to use for accessing SRAM tank when Address(0:2) = 111 and the PPE high priority output is ‘1’.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface XCR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIXCR
Address	0000000000060010 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 Force = Halt.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface XCR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPENXIXCR
Address	0000000000060010 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface RAMRA
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIRAMRA
Address	0000000000060011 (SCOM)
Description	PPE External Interface RAMRA

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:31	RO	constant = 0b00000000000000000000000000000
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMGA
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIRAMGA
Address	0000000000060012 (SCOM)
Description	PPE External Interface RAMGA

Bits	SCOM	Field Mnemonic: Description
0:31	WOX	PPE_XIRAMGA_IR: PPE Instruction Register. Writes cause a RAM operation. It can be written when only the processor is halted (XSR[HS] = ‘1’). Provides the requested PPE Instruction to execute.
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMDBG
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIRAMDBG
Address	0000000000060013 (SCOM)
Description	PPE External Interface RAMDBG

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMEDR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIRAMEDR
Address	0000000000060014 (SCOM)
Description	PPE External Interface RAMEDR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	ROX	PPE_XIRAMEDR_EDR: Error Data Register. This field is set on PPE interrupts that are caused by an error. See the PPE Specification for a definition.

Register Name	PPE External Interface DBGPRO
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPE.PPE.PPE_XIDBGPRO
Address	0000000000060015 (SCOM)
Description	PPE External Interface DBGPRO

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:61	RWX	Reserved field.
62:63	RO	constant = 0b00

Register Name	MIB External Interface MEM Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPE.MIB.MIB_XIMEM
Address	0000000000060017 (SCOM)
Description	MIB External Interface MEM Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XIMEM_MEM_ADDR: MEM transaction buffer: current or previous transaction byte address.
32	ROX	MIB_XIMEM_MEM_R_NW: MEM transaction buffer: current or previous transaction type. 0 = Write. 1 = Read.
33	ROX	MIB_XIMEM_MEM_BUSY: Indicates if the transaction buffer is occupied with an ongoing transaction. Busy is cleared when the transaction is completed.
34	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. It is cleared when it is reported back to the PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
35:42	ROX	MIB_XIMEM_MEM_BYTE_ENABLE: MEM transaction buffer: current or previous transaction byte enables.
43	ROX	MIB_XIMEM_MEM_LINE_MODE: MEM transaction buffer: current or previous transaction line mode. Indicates a 32 B read request when set to ‘1’.
44:48	RO	constant = 0b00000
49:51	ROX	MIB_XIMEM_MEM_ERROR: MEM transaction buffer error code. A current or previous transaction received an error on the memory interface when non-zero.
52:61	RO	constant = 0b0000000000

Bits	SCOM	Field Mnemonic: Description
62	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to ‘1’, indicates that an instruction fetch is pending on the MEM interface.
63	ROX	MIB_XIMEM_MEM_DATAOP_PENDING: When set to ‘1’, indicates that a data transaction is pending on the MEM interface.

Register Name	MIB External Interface Store Gather Buffer Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPE.MIB.MIB_XISGB
Address	0000000000060018 (SCOM)
Description	MIB External Interface Store Gather Buffer Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XISGB_STORE_ADDRESS: Contains either the SGB address 4-byte tag or the address of an imprecise store error that occurred when a previous data transaction was done.
32:34	RO	constant = 0b000
35	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. It is cleared when it is reported back to the PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
36:39	ROX	MIB_XISGB_SGB_BYTE_VALID: Byte valid bits within the 4 B tag. Cleared when the SGB contents are committed, that is, when the SGB contents are either flushed to memory or copied into the transaction buffer. **Note:** These bits can never be set if a MEM IMPRECISE ERROR is pending.
40:62	RO	constant = 0b00000000000000000000000
63	ROX	MIB_XISGB_SGB_FLUSH_PENDING: When set to ‘1’, indicates that a store gather buffer flush to memory is pending on the MEM interface. This can happen only if MEM_BUSY in the MEM transaction buffer is ‘0’.

Register Name	MIB External Interface I-cache Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPE.MIB.MIB_XIICAC
Address	0000000000060019 (SCOM)
Description	MIB External Interface I-cache Information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:31	RO	constant = 0b00000
32	ROX	Reserved field.
33	RO	constant = 0b0
34	ROX	Reserved field.
35	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to ‘1’, indicates that an instruction fetch is pending on the MEM interface.
36:39	ROX	Reserved field.
40:43	ROX	Reserved field.
44	RO	constant = 0b0
45	ROX	Reserved field.
46	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
47	ROX	Reserved field.
48:63	RO	constant = 0b0000000000000000

Register Name	MIB External Interface D-cache Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.MIB_XIDCAC
Address	000000000006001A (SCOM)
Description	MIB External Interface D-cache Information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	MIB_XIDCAC_DCACHE_TAG_ADDR: 32 B data address tag for the current or previous cache content.
27:31	RO	constant = 0b00000
32	ROX	MIB_XIDCAC_DCACHE_ERR: Indicates the current or previous content of the cache is bad due to an interface error during populate.
33:34	RO	constant = 0b00
35	ROX	Reserved field.
36:37	ROX	Reserved field.
38:63	RO	constant = 0b00000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPEXIXCR
Address	0000000000060020 (SCOM)
Description	Word XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPEXIXSR
Address	0000000000060021 (SCOM)
Description	Word XSR

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:

Bits	SCOM	Field Mnemonic: Description
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPEXISPRG0
Address	0000000000060022 (SCOM)
Description	Word SPRG0

Bits	SCOM	Field Mnemonic: Description
0:31	RW	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPEXIEDR
Address	0000000000060023 (SCOM)
Description	Word EDR

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	PPE_XIRAMEDR_EDR: Error Data Register. Set on PPE interrupts that are caused by an error. See the PPE Specification for a definition.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPEXIIR
Address	0000000000060024 (SCOM)
Description	Word IR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE0.GPEXIIAR
Address	0000000000060025 (SCOM)
Description	Word IAR

Bits	SCOM	Field Mnemonic: Description
0:29	RWX	Reserved field.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE Timer Select Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPETSEL
Address	0000000000062000 (SCOM)
Description	GPE Timer Select Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	GPETSEL_FIT_SEL: Selects the fixed interval timer rate.
4:7	RW	GPETSEL_WATCHDOG_SEL: Selects the watchdog timer rate.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	GPE Interrupt Vector Prefix Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPEIVPR
Address	0000000000062001 (SCOM)
Description	GPE Interrupt Vector Prefix Register

Bits	SCOM	Field Mnemonic: Description
0:22	RW	GPEIVPR_IVPR: Interrupt Prefix Vector Register (Resets to 0xFFFFFE left justified).
23	RW	Reserved.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	GPE Debug Mode Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPEDBG
Address	0000000000062002 (SCOM)
Description	GPE Debug Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GPEDBG_EN_DBG: Enable Debug Trace. Master switch that enables clocks to the trace. Also causes RISCTrace to start on the rising edge and stop on the falling edge when RISCTrace is enabled (TRACE_DATA_SEL[0] = 0).
1	RW	GPEDBG_HALT_ON_XSTOP: Enable halt on checkstop input.
2	RW	GPEDBG_HALT_ON_TRIG: Enable halt on trigger input.
3	RW	GPEDBG_RESERVED3: Implemented but not used.

Bits	SCOM	Field Mnemonic: Description
4	RW	GPEDBG_EN_INTR_ADDR: When RISCTrace is enabled, trace the full interrupt vector address. Otherwise trace only the lower byte of the address.
5	RW	GPEDBG_EN_TRACE_EXTRA: When RISCTrace is enabled and this bit is set, records extra trace data not needed for the 405 RISCTrace specification. When this bit is not set: Does not record MTMSR or MTSPRG0 data Does not record new MSR on an RFI.
6	RW	GPEDBG_EN_TRACE_STALL: When RISCTrace is enabled and this bit is set, stalls cycles when the processor is not actively executing instructions. Cycles that are not already included in the previous event and cycles that are recorded unless they are halt or in wait state are also stalled. When this mode is not set, the RISCTrace is smaller but not time accurate.
7	RW	GPEDBG_EN_WAIT_CYCLES: When RISCTrace is enabled and this bit is set, stall events are used to record the number of cycles the PPE is in wait state. Otherwise, cycles in wait state are ignored. When this bit is set, EN_TRACE_STALL must also be set.
8	RW	GPEDBG_EN_FULL_SPEED: When set, the trace valid is pulsed at 1:1 (4x faster than the debug data, which changes at PPE clock speed). This is required for CHTM and NHTM (in-memory trace). When this mode is not set, trace valid is held constant for a full PPE cycle (four 1:1 cycles). When connected to a trace array, this value must match the corresponding sampling speed of the array.
9	RW	GPEDBG_RESERVED9: Implemented but not used.
10:11	RW	GPEDBG_TRACE_MODE_SEL: Bit GPEDBG_EN_DBG (bit 0) chooses between 0 (PPE Core Debug Mode A) and 1 (Mode B). When bit GPEDBG_HALT_ON_XSTOP (bit 1) is set, it ORs in the secondary valid corresponding lower bits of the trace data when they are from a different source than bits 0:23. **Note:** When bit 1 = ‘0’ it is likely for HTM tracing.
12:15	RW	GPEDBG_RESERVED12_15: Implemented but not used.
16	RW	GPEDBG_FIR_TRIGGER: Programmatically asserts a FIR bit to inject a checkstop or send an attention to the service element.
17:19	RW	GPEDBG_SPARE: Spare (used for GPIO on other instances).
20:23	RW	GPEDBG_TRACE_DATA_SEL: Mux select to choose debug data content on the trace bus. All 16 encodes are defined as per the table in the Debug Bolt-on chapter of the Power Management Specification. 0x0 chooses an 88-bit PPE-RISCTrace by default. b00XX enables RISCTrace records to be generated in the upper 64-bits of trace data. 0bXX00 selects the remaining 24 bits to form 88-bit Trace Packets to be generated on the debug bus to be sent to the hardware trace array (otherwise PPE, MIB, or EXT data will be used). The other 12 encodes contain permutations of the PPE Core, Memory Interface, and External debug buses instead of RISCTrace records.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	GPE SRAM Translation Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPESTR
Address	0000000000062003 (SCOM)
Description	GPE SRAM Translation Register

Bits	SCOM	Field Mnemonic: Description
0:11	RO	constant = 0b000000000000

Bits	SCOM	Field Mnemonic: Description
12:21	RW	GPESTR_PBASE: Specifies the physical base address for effective addresses starting at 0xFFFF8000, and extending upwards for the range indicated by GSTR[size]. GSTR[pbase] must imply a correctly aligned physical base address for any legal value of GSTR[size] as detailed follows: Size = 0b000 (1 KB) pbase = 0bxxxxxxxxxx Size = 0b001 (2 KB) pbase = 0bxxxxxxxxx0 Size = 0b010 (4 KB) pbase = 0bxxxxxxxx00 Size = 0b011 (8 KB) pbase = 0bxxxxxxx000 Size = 0b100 (16 KB) pbase = 0bxxxxxx0000 Size = 0b101 (32 KB) pbase = 0bxxxxx00000 **Note:** The reset value represents an illegal OCI address, which results in a machine check exception if a translatable effective address is accessed.
22:28	RO	constant = 0b0000000
29:31	RW	GPESTR_SIZE: Specifies the size of the translated region: 0b000 = 1 KB 0b001 = 2 KB 0b010 = 4 KB 0b011 = 8 KB 0b100 = 16 KB 0b101 = 32 KB Other values are illegal and results in data or instruction storage exceptions as appropriate.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**GPE Memory Access Configuration Register**
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPEMACR
Address	0000000000062004 (SCOM)
Description	GPE Memory Access Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	GPEMACR_MEM_LOW_PRIORITY: OCI priority to use for accessing main memory when address[0:1] = 10 and the PPE high priority output is ‘0’.
2:3	RW	GPEMACR_MEM_HIGH_PRIORITY: OCI priority to use for accessing main memory when address[0:1] = 10 and the PPE high priority output is ‘1’.
4:5	RW	GPEMACR_LOCAL_LOW_PRIORITY: OCI priority to use for accessing local registers when address[0:2] = 110 and the PPE high priority output is ‘0’.
6:7	RW	GPEMACR_LOCAL_HIGH_PRIORITY: OCI priority to use for accessing local registers when address[0:2] = 110 and the PPE high priority output is ‘1’.
8:9	RW	GPEMACR_SRAM_LOW_PRIORITY: OCI priority to use for accessing SRAM tank when address(0:2) = 111 and the PPE high priority output is ‘0’.
10:11	RW	GPEMACR_SRAM_HIGH_PRIORITY: OCI priority to use for accessing SRAM tank when address(0:2) = 111 and the PPE high priority output is ‘1’.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface XCR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIXCR
Address	0000000000062010 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface XCR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPENXIXCR
Address	0000000000062010 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface RAMRA
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIRAMRA
Address	0000000000062011 (SCOM)
Description	PPE External Interface RAMRA

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:31	RO	constant = 0b00000000000000000000000000000
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMGA
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIRAMGA
Address	0000000000062012 (SCOM)
Description	PPE External Interface RAMGA

Bits	SCOM	Field Mnemonic: Description
0:31	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMDBG
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIRAMDBG
Address	0000000000062013 (SCOM)
Description	PPE External Interface RAMDBG

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAMEDR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIRAMEDR
Address	0000000000062014 (SCOM)
Description	PPE External Interface RAMEDR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = '1').
32:63	ROX	PPE_XIRAMEDR_EDR: Error Data Register. Set on PPE interrupts that are caused by an error. See the PPE Specification for a definition.

Register Name	PPE External Interface DBGPRO
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPE.PPE.PPE_XIDBGPRO
Address	0000000000062015 (SCOM)
Description	PPE External Interface DBGPRO

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:61	RWX	Reserved field.
62:63	RO	constant = 0b00

Register Name	MIB External Interface MEM Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPE.MIB.MIB_XIMEM
Address	0000000000062017 (SCOM)
Description	MIB External Interface MEM Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XIMEM_MEM_ADDR: MEM transaction buffer: current or previous transaction byte address.
32	ROX	MIB_XIMEM_MEM_R_NW: MEM transaction buffer: current or previous transaction type. 0 = Write. 1 = Read.
33	ROX	MIB_XIMEM_MEM_BUSY: Indicates if the transaction buffer is occupied with an ongoing transaction. Busy is cleared when the transaction is completed.
34	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. It is cleared when it is reported back to the PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
35:42	ROX	MIB_XIMEM_MEM_BYTE_ENABLE: MEM transaction buffer: current or previous transaction byte enables.
43	ROX	MIB_XIMEM_MEM_LINE_MODE: MEM transaction buffer: current or previous transaction line mode. Indicates a 32 B read request when set to ‘1’.
44:48	RO	constant = 0b00000
49:51	ROX	MIB_XIMEM_MEM_ERROR: MEM transaction buffer error code. A current or previous transaction received an error on the memory interface when non-zero.
52:61	RO	constant = 0b0000000000
62	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to ‘1’, indicates that an instruction fetch is pending on the MEM interface.
63	ROX	MIB_XIMEM_MEM_DATAOP_PENDING: When set to ‘1’, indicates that a data transaction is pending on the MEM interface.

Register Name	MIB External Interface Store Gather Buffer Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPE.MIB.MIB_XISGB
Address	0000000000062018 (SCOM)
Description	MIB External Interface Store Gather Buffer Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XISGB_STORE_ADDRESS: Contains either the SGB address 4-byte tag or the address of an imprecise store error that occurred when a previous data transaction was done.
32:34	RO	constant = 0b000
35	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. It is cleared when it is reported back to the PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
36:39	ROX	MIB_XISGB_SGB_BYTE_VALID: Byte valid bits within the 4 B tag. Cleared when the SGB contents are committed, that is, when the SGB contents are either flushed to memory or copied into the transaction buffer. **Note:** These bits can never be set if a MEM IMPRECISE ERROR is pending.
40:62	RO	constant = 0b00000000000000000000000
63	ROX	MIB_XISGB_SGB_FLUSH_PENDING: When set to ‘1’, indicates that a store gather buffer flush to memory is pending on the MEM interface. This can happen only if MEM_BUSY in the MEM transaction buffer is ‘0’.

Register Name	MIB External Interface I-cache Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPE.MIB.MIB_XIICAC
Address	0000000000062019 (SCOM)
Description	MIB External Interface I-cache Information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:31	RO	constant = 0b00000
32	ROX	Reserved field.
33	RO	constant = 0b0
34	ROX	Reserved field.
35	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to ‘1’, indicates that an instruction fetch is pending on the MEM interface.
36:39	ROX	Reserved field.
40:43	ROX	Reserved field.
44	RO	constant = 0b0
45	ROX	Reserved field.
46	ROX	Reserved field.
47	ROX	Reserved field.
48:63	RO	constant = 0b0000000000000000

Register Name	MIB External Interface D-cache Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.MIB_XIDCAC
Address	000000000006201A (SCOM)
Description	MIB External Interface D-cache Information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	MIB_XIDCAC_DCACHE_TAG_ADDR: 32 B data address tag for the current or previous cache content.
27:31	RO	constant = 0b00000
32	ROX	MIB_XIDCAC_DCACHE_ERR: Indicates the current or previous content of the cache is bad due to an interface error during populate.
33:34	RO	constant = 0b00
35	ROX	Reserved field.
36:37	ROX	Reserved field.
38:63	RO	constant = 0b00000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPEXIXCR
Address	0000000000062020 (SCOM)
Description	Word XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPEXIXSR
Address	0000000000062021 (SCOM)
Description	Word XSR

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPEXISPRG0
Address	0000000000062022 (SCOM)
Description	Word SPRG0

Bits	SCOM	Field Mnemonic: Description
0:31	RW	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPEXIEDR
Address	0000000000062023 (SCOM)
Description	Word EDR

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	PPE_XIRAMEDR_EDR: Error Data Register. Set on PPE interrupts that are caused by an error. See the PPE Specification for a definition.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPEXIIR
Address	0000000000062024 (SCOM)
Description	Word IR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE1.GPEXIIAR
Address	0000000000062025 (SCOM)
Description	Word IAR

Bits	SCOM	Field Mnemonic: Description
0:29	RWX	Reserved field.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE Timer Select Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPETSEL
Address	0000000000064000 (SCOM)
Description	GPE Timer Select Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	GPETSEL_FIT_SEL: Selects the fixed interval timer rate.
4:7	RW	GPETSEL_WATCHDOG_SEL: Selects the watchdog timer rate.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	GPE Interrupt Vector Prefix Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPEIVPR
Address	0000000000064001 (SCOM)
Description	GPE Interrupt Vector Prefix Register

Bits	SCOM	Field Mnemonic: Description
0:22	RW	GPEIVPR_IVPR: Interrupt Prefix Vector Register (Resets to 0xFFFFFE left justified).
23	RW	Reserved.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	GPE Debug Mode Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPEDBG
Address	0000000000064002 (SCOM)
Description	GPE Debug Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GPEDBG_EN_DBG: Enable Debug Trace. Master switch that enables clocks to the trace. Also causes RISCTrace to start on the rising edge and stop on the falling edge when RISCTrace is enabled (TRACE_DATA_SEL(0) = 0).
1	RW	GPEDBG_HALT_ON_XSTOP: Enable halt on checkstop input.
2	RW	GPEDBG_HALT_ON_TRIG: Enable halt on trigger input.
3	RW	GPEDBG_RESERVED3: Implemented but not used.
4	RW	GPEDBG_EN_INTR_ADDR: When RISCTrace is enabled, trace the full interrupt vector address. Otherwise, trace only the lower byte of the address.
5	RW	GPEDBG_EN_TRACE_EXTRA: When RISCTrace is enabled and this bit is set, records extra trace data not needed for 405 RISCTrace specification. When this bit is NOT set: Do not record MTMSR or MTSPRG0 data Do not record new MSR on an RFI
6	RW	GPEDBG_EN_TRACE_STALL: When RISCTrace is enabled and this bit is set, stalls cycles when the processor is not actively executing instructions, cycles that are not already included in the previous event, and cycles that are recorded unless they are halt or in wait state. When this mode is not set, the RISCTrace is smaller but not time accurate.
7	RW	GPEDBG_EN_WAIT_CYCLES: When RISCTrace is enabled and this bit is set, stall events are used to record the number of cycles the PPE is in wait state otherwise cycles in wait state are ignored. When this bit is set, EN_TRACE_STALL must also be set.
8	RW	GPEDBG_EN_FULL_SPEED: When set, the trace valid is pulsed at 1:1 (4x faster than the debug data, which changes at PPE clock speed). This is required for CHTM and NHTM (in-memory trace). When this mode is NOT set, trace valid is held constant for a full PPE cycle (four 1:1 cycles). When connected to a trace array this value should match the corresponding sampling speed of the array.
9	RW	GPEDBG_RESERVED9: Implemented but not used.
10:11	RW	GPEDBG_TRACE_MODE_SEL: Bit GPEDBG_EN_DBG (bit 0) chooses between 0 (PPE Core Debug Mode A) and 1 (Mode B). When bit GPEDBG_HALT_ON_XSTOP (bit 1) is set, it ORs in the secondary valid corresponding lower bits of the trace data when they are from a different source than bits 0:23. **Note:** When bit 1 = '0' it is likely for HTM tracing.
12:15	RW	GPEDBG_RESERVED12_15: Implemented but not used.
16	RW	GPEDBG_FIR_TRIGGER: Programmatically asserts a FIR bit to inject a checkstop or send an attention to the service element.
17:19	RW	GPEDBG_SPARE: Spare (used for GPIO on other instances).
20:23	RW	GPEDBG_TRACE_DATA_SEL: Mux select to choose debug data content on the trace bus. All 16 encodes are defined as per the table in the Debug Bolt-on chapter of the Power Management Specification. 0x0 chooses an 88-bit PPE-RISCTrace by default. b00XX enables RISCTrace records to be generated in the upper 64-bits of trace data. 0bXX00 selects the remaining 24 bits to form 88-bit Trace Packets to be generated on the debug bus to be sent to the hardware trace array (otherwise PPE, MIB, or EXT data is used). The other 12 encodes contain permutations of the PPE core, memory interface, and external debug buses instead of RISCTrace records.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	GPE SRAM Translation Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPESTR
Address	0000000000064003 (SCOM)
Description	GPE SRAM Translation Register

Bits	SCOM	Field Mnemonic: Description
0:11	RO	constant = 0b000000000000
12:21	RW	GPESTR_PBASE: Specifies the physical base address for effective addresses starting at 0xFFFF8000, and extending upwards for the range indicated by GSTR[size]. GSTR[pbase] must imply a correctly aligned physical base address for any legal value of GSTR[size] detailed as follows: Size = 0b000 (1 KB) pbase = 0bxxxxxxxxxx Size = 0b001 (2 KB) pbase = 0bxxxxxxxxx0 Size = 0b010 (4 KB) pbase = 0bxxxxxxxx00 Size = 0b011 (8 KB) pbase = 0bxxxxxxx000 Size = 0b100 (16 KB) pbase = 0bxxxxxx0000 Size = 0b101 (32 KB) pbase = 0bxxxxx00000 The reset value represents an illegal OCI address, which results in a machine check exception if a translatable effective address be accessed.
22:28	RO	constant = 0b0000000
29:31	RW	GPESTR_SIZE: Specifies the size of the translated region. 0b000 = 1 KB 0b001 = 2 KB 0b010 = 4 KB 0b011 = 8 KB 0b100 = 16 KB 0b101 = 32 KB Other values are illegal and result in data or instruction storage exceptions as appropriate.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE Memory Access Configuration Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPEMACR
Address	0000000000064004 (SCOM)
Description	GPE Memory Access Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	GPEMACR_MEM_LOW_PRIORITY: OCI priority to use for accessing main memory when address[0:1] = 10 and the PPE high priority output is ‘0’.
2:3	RW	GPEMACR_MEM_HIGH_PRIORITY: OCI priority to use for accessing main memory when address[0:1] = 10 and the PPE high priority output is ‘1’.
4:5	RW	GPEMACR_LOCAL_LOW_PRIORITY: OCI priority to use for accessing local registers when address[0:2] = 110 and the PPE high priority output is ‘0’.
6:7	RW	GPEMACR_LOCAL_HIGH_PRIORITY: OCI priority to use for accessing local registers when address[0:2] = 110 and the PPE high priority output is ‘1’.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	GPEMACR_SRAM_LOW_PRIORITY: OCI priority to use for accessing SRAM tank when address[0:2] = 111 and the PPE high priority output is ‘0’.
10:11	RW	GPEMACR_SRAM_HIGH_PRIORITY: OCI priority to use for accessing SRAM tank when address[0:2] = 111 and the PPE high priority output is ‘1’.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface XCR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIXCR
Address	0000000000064010 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command. 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface XCR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPENXIXCR
Address	0000000000064010 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command. 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface RAMRA
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIRAMRA
Address	0000000000064011 (SCOM)
Description	PPE External Interface RAMRA

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command. 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt.
4:31	RO	constant = 0b00000000000000000000000000000
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMGA
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIRAMGA
Address	0000000000064012 (SCOM)
Description	PPE External Interface RAMGA

Bits	SCOM	Field Mnemonic: Description
0:31	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMDBG
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIRAMDBG
Address	0000000000064013 (SCOM)
Description	PPE External Interface RAMDBG

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMEDR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIRAMEDR
Address	0000000000064014 (SCOM)
Description	PPE External Interface RAMEDR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	ROX	PPE_XIRAMEDR_EDR: Error Data Register. This field is set on PPE interrupts that are caused by an error. See the PPE Specification for a definition.

Register Name	PPE External Interface DBGPRO
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPE.PPE.PPE_XIDBGPRO
Address	0000000000064015 (SCOM)
Description	PPE External Interface DBGPRO

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:61	RWX	Reserved field.
62:63	RO	constant = 0b00

Register Name	MIB External Interface MEM Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPE.MIB.MIB_XIMEM
Address	0000000000064017 (SCOM)
Description	MIB External Interface MEM Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XIMEM_MEM_ADDR: MEM transaction buffer: current or previous transaction byte address.
32	ROX	MIB_XIMEM_MEM_R_NW: MEM transaction buffer: current or previous transaction type. 0 = Write. 1 = Read.
33	ROX	MIB_XIMEM_MEM_BUSY: Indicates if the transaction buffer is occupied with an ongoing transaction. Busy is cleared when the transaction is completed.
34	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. It is cleared when it is reported back to the PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
35:42	ROX	MIB_XIMEM_MEM_BYTE_ENABLE: MEM transaction buffer: current or previous transaction byte enables.
43	ROX	MIB_XIMEM_MEM_LINE_MODE: MEM transaction buffer: current or previous transaction line mode. Indicates a 32 B read request when set to ‘1’.
44:48	RO	constant = 0b00000
49:51	ROX	MIB_XIMEM_MEM_ERROR: MEM transaction buffer error code. Current or previous transaction got an error on the memory interface when nonzero.
52:61	RO	constant = 0b0000000000

Bits	SCOM	Field Mnemonic: Description
62	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: Indicates an instruction fetch is pending on the MEM interface when set to ‘1’.
63	ROX	MIB_XIMEM_MEM_DATAOP_PENDING: When set to ‘1’, indicates that a data transaction is pending on the MEM interface.

Register Name	MIB External Interface Store Gather Buffer Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPE.MIB.MIB_XISGB
Address	0000000000064018 (SCOM)
Description	MIB External Interface Store Gather Buffer Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XISGB_STORE_ADDRESS: Contains either the SGB address 4-byte tag or the address of an imprecise store error that occurred when a previous data transaction was done.
32:34	RO	constant = 0b000
35	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. This bit is cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
36:39	ROX	MIB_XISGB_SGB_BYTE_VALID: Byte valid bits within the 4 B tag. This field is cleared when the SGB contents are committed, meaning that it is either flushed to memory or it is copied into the transaction buffer. **Note:** These bits can never be set if a MEM IMPRECISE ERROR is pending.
40:62	RO	constant = 0b000000000000000000000000
63	ROX	MIB_XISGB_SGB_FLUSH_PENDING: When set to ‘1’, indicates that a store gather buffer flush to memory is pending on the MEM interface. This can happen only if MEM_BUSY in the MEM transaction buffer is ‘0’.

Register Name	MIB External Interface I-cache Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPE.MIB.MIB_XIICAC
Address	0000000000064019 (SCOM)
Description	MIB External Interface I-cache Information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:31	RO	constant = 0b00000
32	ROX	Reserved field.
33	RO	constant = 0b0
34	ROX	Reserved field.
35	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to ‘1’, indicates that an instruction fetch is pending on the MEM interface.
36:39	ROX	Reserved field.
40:43	ROX	Reserved field.
44	RO	constant = 0b0
45	ROX	Reserved field.
46	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
47	ROX	Reserved field.
48:63	RO	constant = 0b0000000000000000

Register Name	MIB External Interface D-cache Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.MIB_XIDCAC
Address	000000000006401A (SCOM)
Description	MIB External Interface D-cache Information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	MIB_XIDCAC_DCACHE_TAG_ADDR: 32 B data address tag for the current or previous cache content.
27:31	RO	constant = 0b00000
32	ROX	MIB_XIDCAC_DCACHE_ERR: Indicates the current or previous content of the cache is bad from an interface error during populate.
33:34	RO	constant = 0b00
35	ROX	Reserved field.
36:37	ROX	Reserved field.
38:63	RO	constant = 0b00000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPEXIXCR
Address	0000000000064020 (SCOM)
Description	Word XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPEXIXSR
Address	0000000000064021 (SCOM)
Description	Word XSR

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:

Bits	SCOM	Field Mnemonic: Description
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPEXISPRG0
Address	0000000000064022 (SCOM)
Description	Word SPRG0

Bits	SCOM	Field Mnemonic: Description
0:31	RW	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPEXIEDR
Address	0000000000064023 (SCOM)
Description	Word EDR

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	PPE_XIRAMEDR_EDR: Error Data Register. This field is set on PPE interrupts that are caused by an error. See the PPE Specification for a definition.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPEXIIR
Address	0000000000064024 (SCOM)
Description	Word IR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE2.GPEXIIAR
Address	0000000000064025 (SCOM)
Description	Word IAR

Bits	SCOM	Field Mnemonic: Description
0:29	RWX	Reserved field.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE Timer Select Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPETSEL
Address	0000000000066000 (SCOM)
Description	GPE Timer Select Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	GPETSEL_FIT_SEL: Selects the fixed interval timer rate.
4:7	RW	GPETSEL_WATCHDOG_SEL: Selects the watchdog timer rate.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	GPE Interrupt Vector Prefix Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPEIVPR
Address	0000000000066001 (SCOM)
Description	GPE Interrupt Vector Prefix Register

Bits	SCOM	Field Mnemonic: Description
0:22	RW	GPEIVPR_IVPR: Interrupt Prefix Vector Register (Resets to 0xFFFFFE left justified).
23	RW	Reserved.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	GPE Debug Mode Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPEDBG
Address	0000000000066002 (SCOM)
Description	GPE Debug Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GPEDBG_EN_DBG: Enable Debug Trace. Master switch that enables clocks to the trace. Also causes RISCTrace to start on the rising edge and stop on the falling edge when RISCTrace is enabled (TRACE_DATA_SEL[0] = 0).
1	RW	GPEDBG_HALT_ON_XSTOP: Enable halt on checkstop input.
2	RW	GPEDBG_HALT_ON_TRIG: Enable halt on trigger input.
3	RW	GPEDBG_RESERVED3: Implemented but not used.

Bits	SCOM	Field Mnemonic: Description
4	RW	GPEDBG_EN_INTR_ADDR: When RISCTrace is enabled, trace the full interrupt vector address. Otherwise, only trace the lower byte of the address.
5	RW	GPEDBG_EN_TRACE_EXTRA: When RISCTrace is enabled and this bit is set, records extra trace data not needed for 405 RISCTrace specification. When this bit is NOT set: Do not record MTMSR or MTSPRG0 data Do not record new MSR on an RFI.
6	RW	GPEDBG_EN_TRACE_STALL: When RISCTrace is enabled and this bit is set, stall cycles when the processor is not actively executing and instruction that are not already included in the previous event and are recorded unless it is halted or in wait state. When this mode is not set, the RISCTrace is smaller but not time accurate.
7	RW	GPEDBG_EN_WAIT_CYCLES: When RISCTrace is enabled and this bit is set, stall events are used to record the number of cycles the PPE is in wait state. Otherwise, cycles in wait state are ignored. When this bit is set, EN_TRACE_STALL must also be set.
8	RW	GPEDBG_EN_FULL_SPEED: When set, the trace valid is pulsed at 1:1 (4x faster than the debug data, which changes at PPE clock speed). This is required for CHTM and NHTM (in-memory trace). When this mode is not set, trace valid is held constant for a full PPE cycle (four 1:1 cycles). When connected to a trace array this value should match the corresponding sampling speed of the array.
9	RW	GPEDBG_RESERVED9: Implemented but not used.
10:11	RW	GPEDBG_TRACE_MODE_SEL: Bit GPEDBG_EN_DBG (bit 0) chooses between 0 (PPE Core Debug Mode A) and 1 (Mode B). When bit GPEDBG_HALT_ON_XSTOP (bit 1) is set, it ORs in the secondary valid corresponding lower bits of the trace data when they are from a different source than bits 0:23. **Note:** When bit 1 = '0' it is likely for HTM tracing.
12:15	RW	GPEDBG_RESERVED12_15: Implemented but not used.
16	RW	GPEDBG_FIR_TRIGGER: Programmatically asserts a FIR bit to inject a checkstop or send an attention to the service element.
17:19	RW	GPEDBG_SPARE: Spare (used for GPIO on other instances).
20:23	RW	GPEDBG_TRACE_DATA_SEL: Mux select to choose debug data content on the trace bus. All 16 encodes are defined as per the table in the Debug Bolt-on chapter of the Power Management Spec. 0x0 chooses an 88-bit PPE-RISCTrace by default. - b00XX enables RISCTrace records to be generated in the upper 64-bits of trace data. - 0bXX00 selects the remaining 24 bits to form 88-bit Trace Packets to be generated on the debug bus to be sent to the hardware trace array (otherwise PPE, MIB, or EXT data will be used) The other 12 encodes contain permutations of the PPE Core, Memory Interface, and External debug buses instead of RISCTrace records.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	GPE SRAM Translation Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPESTR
Address	0000000000066003 (SCOM)
Description	GPE SRAM Translation Register

Bits	SCOM	Field Mnemonic: Description
0:11	RO	constant = 0b000000000000

Bits	SCOM	Field Mnemonic: Description
12:21	RW	GPESTR_PBASE: Specifies the physical base address for effective addresses starting at 0xFFFF8000, and extending upwards for the range indicated by GSTR[size]. GSTR[pbase] must imply a correctly aligned physical base address for any legal value of GSTR[size] are detailed as follow: Size = 0b000 (1 KB) pbase = 0bxxxxxxxxxx Size = 0b001 (2 KB) pbase = 0bxxxxxxxxx0 Size = 0b010 (4 KB) pbase = 0bxxxxxxxx00 Size = 0b011 (8 KB) pbase = 0bxxxxxxx000 Size = 0b100 (16 KB) pbase = 0bxxxxxx0000 Size = 0b101 (32 KB) pbase = 0bxxxxx00000 The reset value represents an illegal OCI address, which results in a machine check exception if a translatable effective address be accessed.
22:28	RO	constant = 0b0000000
29:31	RW	GPESTR_SIZE: Specifies the size of the translated region. 0b000 = 1 KB 0b001 = 2 KB 0b010 = 4 KB 0b011 = 8 KB 0b100 = 16 KB 0b101 = 32 KB Other values are illegal and result in data or instruction storage exceptions as appropriate.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE Memory Access Configuration Register
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPEMACR
Address	0000000000066004 (SCOM)
Description	GPE Memory Access Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	GPEMACR_MEM_LOW_PRIORITY: OCI priority to use for accessing main memory when address[0:1] = 10 and the PPE high priority output is ‘0’.
2:3	RW	GPEMACR_MEM_HIGH_PRIORITY: OCI priority to use for accessing main memory when address[0:1] = 10 and the PPE high priority output is ‘1’.
4:5	RW	GPEMACR_LOCAL_LOW_PRIORITY: OCI priority to use for accessing local registers when address[0:2] = 110 and the PPE high priority output is ‘0’.
6:7	RW	GPEMACR_LOCAL_HIGH_PRIORITY: OCI priority to use for accessing local registers when address[0:2] = 110 and the PPE high priority output is ‘1’.
8:9	RW	GPEMACR_SRAM_LOW_PRIORITY: OCI priority to use for accessing SRAM tank when Address(0:2) = 111 and the PPE high priority output is ‘0’.
10:11	RW	GPEMACR_SRAM_HIGH_PRIORITY: OCI priority to use for accessing SRAM tank when Address(0:2) = 111 and the PPE high priority output is ‘1’.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface XCR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIXCR
Address	0000000000066010 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface XCR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPENXIXCR
Address	0000000000066010 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface RAMRA
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIRAMRA
Address	0000000000066011 (SCOM)
Description	PPE External Interface RAMRA

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:31	RO	constant = 0b00000000000000000000000000000
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMGA
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIRAMGA
Address	0000000000066012 (SCOM)
Description	PPE External Interface RAMGA

Bits	SCOM	Field Mnemonic: Description
0:31	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMDBG
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIRAMDBG
Address	0000000000066013 (SCOM)
Description	PPE External Interface RAMDBG

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMEDR
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIRAMEDR
Address	0000000000066014 (SCOM)
Description	PPE External Interface RAMEDR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	ROX	PPE_XIRAMEDR_EDR: Error Data Register. Set on PPE interrupts that are caused by an error. See the PPE Specification for a definition.

Register Name	PPE External Interface DBGPRO
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPE.PPE.PPE_XIDBGPRO
Address	0000000000066015 (SCOM)
Description	PPE External Interface DBGPRO

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:61	RWX	Reserved field.
62:63	RO	constant = 0b00

Register Name	MIB External Interface MEM Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPE.MIB.MIB_XIMEM
Address	0000000000066017 (SCOM)
Description	MIB External Interface MEM Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XIMEM_MEM_ADDR: MEM transaction buffer: current or previous transaction byte address.
32	ROX	MIB_XIMEM_MEM_R_NW: MEM transaction buffer: current or previous transaction type. 0 = Write. 1 = Read.
33	ROX	MIB_XIMEM_MEM_BUSY: Indicates if the transaction buffer is occupied with an ongoing transaction. Busy is cleared when the transaction is completed.
34	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. Cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
35:42	ROX	MIB_XIMEM_MEM_BYTE_ENABLE: MEM transaction buffer: current or previous transaction byte enables.
43	ROX	MIB_XIMEM_MEM_LINE_MODE: MEM transaction buffer: current or previous transaction line mode. Indicates a 32 B read request when set to ‘1’.
44:48	RO	constant = 0b00000
49:51	ROX	MIB_XIMEM_MEM_ERROR: MEM transaction buffer error code. A current or previous transaction received an error on the memory interface when non-zero.
52:61	RO	constant = 0b0000000000
62	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to ‘1’, indicates that an instruction fetch is pending on the MEM interface.
63	ROX	MIB_XIMEM_MEM_DATAOP_PENDING: When set to ‘1’, indicates that a data transaction is pending on the MEM interface.

Register Name	MIB External Interface Store Gather Buffer Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPE.MIB.MIB_XISGB
Address	0000000000066018 (SCOM)
Description	MIB External Interface Store Gather Buffer Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XISGB_STORE_ADDRESS: Contains either the SGB address 4-byte tag or the address of an imprecise store error that occurred when a previous data transaction was done.
32:34	RO	constant = 0b000
35	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. Cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory I interface can continue to service I-fetches.
36:39	ROX	MIB_XISGB_SGB_BYTE_VALID: Byte valid bits within the 4 B tag. Cleared when the SGB contents are committed, that is, when the SGB contents are either flushed to memory or copied into the transaction buffer. **Note:** These bits can never be set if a MEM IMPRECISE ERROR is pending.
40:62	RO	constant = 0b00000000000000000000000
63	ROX	MIB_XISGB_SGB_FLUSH_PENDING: When set to ‘1’, indicates that a store gather buffer flush to memory is pending on the MEM interface. This can happen only if MEM_BUSY in the MEM transaction buffer is ‘0’.

Register Name	MIB External Interface I-cache Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPE.MIB.MIB_XIICAC
Address	0000000000066019 (SCOM)
Description	MIB External Interface I-cache Information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:31	RO	constant = 0b00000
32	ROX	Reserved field.
33	RO	constant = 0b0
34	ROX	Reserved field.
35	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to ‘1’, indicates that an instruction fetch is pending on the MEM interface.
36:39	ROX	Reserved field.
40:43	ROX	Reserved field.
44	RO	constant = 0b0
45	ROX	Reserved field.
46	ROX	Reserved field.
47	ROX	Reserved field.
48:63	RO	constant = 0b0000000000000000

Register Name	MIB External Interface D-cache Information
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.MIB_XIDCAC
Address	000000000006601A (SCOM)
Description	MIB External Interface D-cache Information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	MIB_XIDCAC_DCACHE_TAG_ADDR: 32 B data address tag for the current or previous cache content.
27:31	RO	constant = 0b00000
32	ROX	MIB_XIDCAC_DCACHE_ERR: Indicates the current or previous content of the cache is bad due to an interface error during populate.
33:34	RO	constant = 0b00
35	ROX	Reserved field.
36:37	ROX	Reserved field.
38:63	RO	constant = 0b00000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPEXIXCR
Address	0000000000066020 (SCOM)
Description	Word XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPEXIXSR
Address	0000000000066021 (SCOM)
Description	Word XSR

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPEXISPRG0
Address	0000000000066022 (SCOM)
Description	Word SPRG0

Bits	SCOM	Field Mnemonic: Description
0:31	RW	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPEXIEDR
Address	0000000000066023 (SCOM)
Description	Word EDR

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	PPE_XIRAMEDR_EDR: Error Data Register. Set on PPE interrupts that are caused by an error. See the PPE Specification for a definition.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPEXIIR
Address	0000000000066024 (SCOM)
Description	Word IR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	GPE External Interface OCI
Mnemonic	TP.TPCHIP.OCC.OCI.GPE3.GPEXIIAR
Address	0000000000066025 (SCOM)
Description	Word IAR

Bits	SCOM	Field Mnemonic: Description
0:29	RWX	Reserved field.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	SRAM SRAM Mode Register
Mnemonic	TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRMR
Address	000000000006A001 (SCOM)
Description	SRAM SRAM Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SRAM_SRMR_SRAM_ENABLE_REMAP: SRAM Enable Remap. When this bit is set, the SRAM remaps an OCI request that targets within the 64-byte address in the SRMAP [sram_remap_source] to the address defined in the SRMAP [sram_remap_dest].
1	RW	SRAM_SRMR_SRAM_ARB_EN_SEND_ALL_WRITES: SRAM Arbiter Send all Writes. 0 = The internal SRAM arbiter prioritizes one pending write-over-read operation when the dispatch logic indicated writes must be prioritized. 1 = The internal SRAM arbiter prioritizes all pending write operations over read operations when the dispatch logic indicated writes must be prioritized.
2	RW	SRAM_SRMR_SRAM_DISABLE_LFSR: SRAM Dispatcher LFSR Disable. 0 = Allows the LFSR in the dispatcher to pseudo randomly rearbitrate instead of address acknowledge a PLB request. 1 = Disables LFSR in dispatcher.
3:7	RW	SRAM_SRMR_SRAM_LFSR_FAIRNESS_MASK: LFSR Fairness Mask. This is a 5-bit mask for the LFSR prematch. Mask bits control probability from 2:1 to 64:1. (That is, all bits set in the mask and only one bit needs to match).
8	RW	SRAM_SRMR_SRAM_ERROR_INJECT_ENABLE: Error Injection Enable. 0 = Disable error inject logic in the SRAM tanks. 1 = Enables error inject logic in the SRAM tanks.
9	RW	SRAM_SRMR_SRAM_CTL_TRACE_EN: SRAM trace bus enable. Use this bit to turn on/off trace bus logic for power savings.

Bits	SCOM	Field Mnemonic: Description
10	RW	SRAM_SRMR_SRAM_CTL_TRACE_SEL: SRAM trace bus select. 0 = Select group 0. 1 = Selects group 1.
11:15	RW	SRAM_SRMR_SPARE: Implemented but unused.
16:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	SRAM Remap Register
Mnemonic	TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRMAP
Address	000000000006A002 (SCOM)
Description	SRAM Remap Register

Bits	SCOM	Field Mnemonic: Description
0:13	RW	SRAM_SRMAP_SRAM_REMAP_SOURCE: SRAM source address to remap. A write or read that targets the SRAM and matches OCI address[12:25] is automatically remapped to the SRAM destination address instead. Use of this register must be enabled in SRMOD[sram_enable_remap].
14:15	RO	constant = 0b00
16:29	RW	SRAM_SRMAP_SRAM_REMAP_DEST: SRAM destination address to remap. When a remap match has occurred, the OCI address(12:25) is changed to this destination address when forwarded to the SRAM tanklets.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	SRAM SRAM Error Address Register
Mnemonic	TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SREAR
Address	000000000006A003 (SCOM)
Description	SRAM SRAM Error Address Register

Bits	SCOM	Field Mnemonic: Description
0:16	RWX	SRAM_SREAR_SRAM_ERROR_ADDRESS: SRAM error address. Capture of OCI address bits [12:28]. The first read error encountered causes the address to be stored. Subsequent read errors do not overwrite this initial captured address until this register is written. This register can be written by using an OCI write with any value. Thus, to clear it, an OCI write of all 0's is required.
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	SRAM Boot Vector Word 0 Register
Mnemonic	TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV0
Address	000000000006A004 (SCOM)
Description	SRAM Boot Vector Word 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	SRAM_SRBV0_BOOT_VECTOR_WORD0: Boot vector word 0. Instruction word 0 is returned from SRAM when the PowerPC 405 fetches from the boot vector address. This register corresponds to address 0xFFFFFFF0 of the cache line holding the boot vector.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	SRAM Boot Vector Word1 Register
Mnemonic	TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV1
Address	000000000006A005 (SCOM)
Description	SRAM SRAM Boot Vector Word1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	SRAM_SRBV1_BOOT_VECTOR_WORD1: Boot vector word 1. Instruction word 1 is returned from SRAM when the PowerPC 405 core fetches from the boot vector address. This register corresponds to address 0xFFFFFFF4 of the cache line holding the boot vector.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	SRAM Boot Vector Word 2 Register
Mnemonic	TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV2
Address	000000000006A006 (SCOM)
Description	SRAM SRAM Boot Vector Word 2 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	SRAM_SRBV2_BOOT_VECTOR_WORD2: Boot Vector Word 2. Instruction word 2 returned from SRAM when the PowerPC 405 core fetches from the boot vector address. This register corresponds to address 0xFFFFFFF8 of the cache line holding the boot vector.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	SRAM Boot Vector Word 3 Register
Mnemonic	TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV3
Address	000000000006A007 (SCOM)
Description	SRAM SRAM Boot Vector Word 3 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	SRAM_SRBV3_BOOT_VECTOR_WORD3: Boot Vector Word 3. Instruction word 3 is returned from SRAM when the PowerPC 405 core fetches from the boot vector address. This register corresponds to address 0xFFFFFFFC of the cache line holding the boot vector. The initial value is a branch absolute 0x00000010.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	SRAM Chicken Switch Register
Mnemonic	TP.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRCHSW
Address	000000000006A008 (SCOM)
Description	SRAM SRAM Chicken Switch Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SRAM_SRCHSW_CHKSW_WRFSM_DLY_DIS: Disables the default 3-cycle delay (PLB read request window) of a dispatched write machine's request to arbiter.
1	RW	SRAM_SRCHSW_CHKSW_ALLOW1_RD: Allows one read at a time.

Bits	SCOM	Field Mnemonic: Description
2	RW	SRAM_SRCHSW_CHKSW_ALLOW1_WR: Allows one write at a time.
3	RW	SRAM_SRCHSW_CHKSW_ALLOW1_RDWR: Allows one read or one write at a time.
4	RW	SRAM_SRCHSW_CHKSW_OCI_PARCHK_DIS: Disables parity checking on PLB inputs.
5	RW	SRAM_SRCHSW_CHKSW_TANK_RDDATA_PARCHK_DIS: Disables parity checking on tank read data.
6	RW	SRAM_SRCHSW_CHKSW_SPARE_6: spare.
7	RW	SRAM_SRCHSW_CHKSW_VAL_BE_ADDR_CHK_DIS: Disables valid byte enable and address checking in dispatcher.
8:9	RW	SRAM_SRCHSW_CHKSW_SO_SPARE: Spares.
10:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	OCB OCI OCC Interrupt Source 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OISR0
Address	000000000006C000 (SCOM) 000000000006C001 (SCOM1) 000000000006C002 (SCOM2)
Description	OCB_OCI OCC Interrupt Source 0 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_DEBUGGER: Debugger software on the FSP uses this bit to produce an interrupt. The physical input is tied low. The respective OITR bit must be set to edge so that a WOR to this register will produce an interrupt.
1	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_TRACE_TRIGGER: Asserted if the trace array logic analyzer logic has detected a trigger condition.
2	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_OCC_ERROR: Indicates an unmasked OCC FIR with action01 = 10 has asserted. Typical use is for the PowerPC 405 ICU and DCU uncorrectable errors but is based on the actual OCC mask and action01 settings.
3	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_PBA_ERROR: Indicates that the attached PBA detected an error. This signal is asserted for an error that sets a bit in the PBA_FIR and also has the corresponding bit set in the PBA_OCC_ACTION register. Normally used to report problems detected with the BCE.
4	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_SRT_ERROR: Indicates that an error has occurred in the attached SRAM tank. Errors include address parity, invalid address, and data uncorrectable ECC errors. The SRAM controller holds the address in error.
5	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_GPE0_ERROR: Indicates the GPE0 reported an error that caused it to halt.
6	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_GPE1_ERROR: Indicates the GPE1 reported an error that caused it to halt.
7	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_GPE2_ERROR: Indicates the GPE2 reported an error that caused it to halt.
8	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_GPE3_ERROR: Indicates the GPE3 reported an error that caused it to halt.
9	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_PPC405_HALT: Indicates the PowerPC 405 core hit a halt condition.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
10	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_OCB_ERROR: Indicates the OCB unit had an error.
11	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_SPARE_11: Implemented but unused. The physical input is tied low.
12	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_CHECK_STOP_PPC405: Indicates a system checkstop was detected. Use to interrupt the PowerPC 405 core.
13	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_CHECK_STOP_GPE0: Indicates a system checkstop was detected. Use to interrupt the GPE0.
14	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_CHECK_STOP_GPE1: Indicates a system checkstop was detected. Use to interrupt the GPE1.
15	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_CHECK_STOP_GPE2: Indicates a system checkstop was detected. Use to interrupt the GPE2.
16	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_CHECK_STOP_GPE3: Indicates a system checkstop was detected. Use to interrupt the GPE3.
17	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_OCC_MALF_ALERT: Malfunction alert classified FIR (used to be PMC LFIR).
18	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_ADU_MALF_ALERT: Indicates that a malfunction alert has been raised in the system.
19	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_EXTERNAL_TRAP: Comes from a chip pin to indicated that an external condition occurred in which the OCC FW is to take action, if enabled. This might be used to indicated that the power supplies are in over-subscription mode and that fast action to reduce socket and associated memory power is required.
20	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_IVRM_PVREF_ERROR: Indicates that the precision voltage reference (PVREF) circuit has detected an error and that iVRMs should be taken out of regulation.
21	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_OCC_TIMER0: Indicates that timer0 in the OCB has popped. Timer0 is a 16-bit counter that is incremented with a 1 us input pulse. It is implemented as an autoreload programmable interval timer (PIT).
22	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_OCC_TIMER1: Indicates that timer1 in the OCB has popped. Timer1 is a 16-bit counter incremented with a 1 us input pulse. It is implemented as an autoreload programmable interval timer (PIT).
23	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_AVS_SLAVE0: Indicates that the VRM slave attached to AVS bus 0 has signaled attention.
24	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_AVS_SLAVE1: Indicates that the VRM slave attached to AVS bus 1 has signaled attention.
25	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_IPI0_HI_PRIORITY: Inter-processor interrupt 0. This interrupt is treated as high priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.
26	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_IPI1_HI_PRIORITY: Inter-processor interrupt 1.This interrupt is treated as high priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.
27	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_IPI2_HI_PRIORITY: Inter-processor interrupt 2. This interrupt is treated as high priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
28	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_IPI3_HI_PRIORITY: Inter-processor interrupt 3. This interrupt is treated as high priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.
29	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_IPI4_HI_PRIORITY: Inter-processor interrupt 4. This interrupt is treated as high priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.
30	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_ADCFSM_ONGOING: Indicates the A2D collection state machine in the PSS unit is currently busy.
31	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR0_I2CM_INTER: OR of four incoming I2CM interrupts.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Interrupt Mask 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIMR0
Address	000000000006C004 (SCOM) 000000000006C005 (SCOM1) 000000000006C006 (SCOM2)
Description	OCB_OCI OCC Interrupt Mask 0 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIMR0_INTERRUPT_MASK_N: See the OCC interrupt source [n] for bit definitions. Masks the respective event from producing an interrupt to the OCC complex engines. The events are still captured in the OISR but are not reported through interrupt signals. 0 = Not masked (for example, enabled) 1 = Masked
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Interrupt Type 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OITR0
Address	000000000006C008 (SCOM) 000000000006C009 (SCOM1) 000000000006C00A (SCOM2)
Description	OCB_OCI OCC Interrupt Type 0 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OITR0_INTERRUPT_TYPE_N: See OCC Interrupt Source [n] for bit definitions. Establishes the type of interrupt that is monitored. 0 = Level 1 = Edge When set to level, the respective OISR[n] bit follows the value of the associated input source with the polarity defined by the OIEPR[n]. **Note:** With this setting, direct OCI writes to the OISR[n] bit must never be attempted because the value will not be held and will immediately return to its previous state. When set to edge: the respective OISR[n] bit will be set upon the transition (as defined by the OIEPR[n]) of the associated input source. Specifically, if the respective OIEPR[n] bit is set to rising, a transition from 0 to 1 sets the bit. If the respective OIEPR[n] bit is set to falling, a transition from 1 to 0 sets the bit. In this mode, the only way to clear the OISR[n] bit is from a direct OCI write-CLEAR. Additionally, firmware can inject interrupts by direct OISR write-OR to the bit (where the OIEPR[n] setting is a don't care). **Engineering Note:** For firmware testing, a potential interrupt injection technique for level interrupts is to override their definition to edge and then use the OR register associated with the OISR[n]. This allows the injected transition to stick because logic does not follow the input interrupt signal. However, if the firmware is expecting to find status in the driving unit, this technique might not be appropriate. Therefore, it makes more sense to have the driving unit provide an interrupt inject mechanism itself. Interrupt bits that intended for firmware use, that is, not driven by a hardware source, are typically tied low unless otherwise specified. The preferred mechanism for injecting interrupts is to configure these bits as an edge and use OR and CLEAR write operations to control the value of the interrupt.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_OCI OCC Interrupt Edge/Polarity 0 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIEPR0
Address	000000000006C00C (SCOM) 000000000006C00D (SCOM1) 000000000006C00E (SCOM2)
Description	OCB_OCI OCC Interrupt Edge/Polarity 0 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIEPR0_INTERRUPT_EDGE_POL_N: See OCC Interrupt Source [n] for bit definitions. Establishes the edge or polarity of interrupt. 0 = Falling/Low 1 = Rising/High When set, the respective bit in the OITR[n] is set to level, then the low and high meanings apply as follows: If this bit is set to low, the respective OISR[n] bit follows the inverted input to the OISR from the unit driving the signal. If this bit is set to high, the respective OISR[n] bit follows the direct input to the OISR[n] from the unit driving the signal. When set, the respective bit in the OITR[n] is set to edge, then the falling and rising meanings apply as follows: If this bit is set to falling, a transition from 1 to 0 of the input signal to the OISR[n] sets the respective OISR[n] bit. If this bit is set to rising, a transition from 0 to 1 of the input signal to the OISR[n] sets the respective OISR[n] bit.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Interrupt Source 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OISR1
Address	000000000006C020 (SCOM) 000000000006C021 (SCOM1) 000000000006C022 (SCOM2)
Description	OCB_OCI OCC Interrupt Source 1 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PBAX_OCC_SEND_ATTN: Indicates that the PBAX send engine is busy. Falling edge indicates it is complete.
1	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PBAX_OCC_PUSH0: Indicates that PBA streaming channel 0 push queue has detected interrupt condition.
2	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PBAX_OCC_PUSH1: Indicates that PBA streaming channel 1 push queue has detected interrupt condition.
3	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PBA_BCDE_ATTN: Indicates that BCDE in the attached PBA detected has an attention condition (non error). Typically, this indicates that a block copy download engine has completed a requested activity.
4	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PBA_BCUE_ATTN: Indicates that BCUE in the attached PBA detected has an attention condition (non error). Typically, this indicates that a block copy download engine has completed a requested activity.
5	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_OCC_STRM0_PULL: Indicates that streaming channel 0 pull queue has detected the condition enabled in OCBSLSC0.
6	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_OCC_STRM0_PUSH: Indicates that streaming channel 0 pull queue has detected the condition enabled in OCBSHSC0.
7	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_OCC_STRM1_PULL: Indicates that streaming channel 1 pull queue has detected the condition enabled in OCBSLSC1.
8	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_OCC_STRM1_PUSH: Indicates that streaming channel 1 pull queue has detected the condition enabled in OCBSHSC1.
9	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_OCC_STRM2_PULL: Indicates that streaming channel 2 pull queue has detected the condition enabled in OCBSLSC2.
10	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_OCC_STRM2_PUSH: Indicates that streaming channel 2 pull queue has detected the condition enabled in OCBSHSC2.
11	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_OCC_STRM3_PULL: Indicates that streaming channel 3 pull queue has detected the condition enabled in OCBSLSC3.
12	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_OCC_STRM3_PUSH: Indicates that streaming channel 3 push queue has detected the condition enabled in OCBSHSC3.
13	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_PCB_INTR_TYPE0_PENDING: Indicates that a PCB type 0 interrupt is pending.
14	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_PCB_INTR_TYPE1_PENDING: Indicates that a PCB type 1 interrupt is pending.
15	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_PCB_INTR_TYPE2_PENDING: Indicates that a PCB type 2 interrupt is pending.
16	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_PCB_INTR_TYPE3_PENDING: Indicates that a PCB type 3 interrupt is pending.
17	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_PCB_INTR_TYPE4_PENDING: Indicates that a PCB type 4 interrupt is pending.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_PCB_INTR_TYPE5_PENDING: Indicates that a PCB type 5 interrupt is pending.
19	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_PCB_INTR_TYPE6_PENDING: Indicates that a PCB type 6 interrupt is pending.
20	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_PCB_INTR_TYPE7_PENDING: Indicates that a PCB type 7 interrupt is pending.
21	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_O2S_0A_ONGOING: Indicates the A O2S bridge for AVS interface 0 has an ongoing transaction.
22	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_O2S_0B_ONGOING: Indicates the B O2S bridge for AVS interface 0 has an ongoing transaction.
23	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_O2S_1A_ONGOING: Indicates the A O2S bridge for AVS interface 1 has an ongoing transaction.
24	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PMC_O2S_1B_ONGOING: Indicates the B O2S bridge for AVS interface 1 has an ongoing transaction.
25	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_PSSBRIDGE_ONGOING: The physical input is tied low. The respective OITR bit must be set to edge so that a WOR to this register by hypervisor firmware will produce an interrupt.
26	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_IPI0_LO_PRIORITY: Inter-processor interrupt 0 is treated as low priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.
27	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_IPI1_LO_PRIORITY: Inter-processor interrupt 1 is treated as low priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.
28	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_IPI2_LO_PRIORITY: Inter-processor interrupt 2 is treated as low priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.
29	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_IPI3_LO_PRIORITY: Inter-processor interrupt 3 is treated as low priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.
30	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_IPI4_LO_PRIORITY: Inter-processor interrupt 4 is treated as low priority by firmware. Allows synchronization between critical and non-critical code. The physical input is tied low. To inject an interrupt, see the engineering note in the OITR.
31	ROX	WOX_CLEAR	WOX_OR	OCB_OCI_OISR1_SPARE_31: Implemented but unused. The physical input is tied low.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_OCI OCC Interrupt Mask 1 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIMR1
Address	000000000006C024 (SCOM) 000000000006C025 (SCOM1) 000000000006C026 (SCOM2)
Description	OCB_OCI OCC Interrupt Mask 1 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIMR1_INTERRUPT_MASK_N: See OCC interrupt source [n] for bit definitions. Masks the respective event from producing an interrupt to the OCC complex engines. The events are still captured in the OISR but are not reported through interrupt signals. 0 = Not masked (for example, enabled) 1 = Masked.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Interrupt Type 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OITR1
Address	000000000006C028 (SCOM) 000000000006C029 (SCOM1) 000000000006C02A (SCOM2)
Description	OCB_OCI OCC Interrupt Type 1 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OITR1_INTERRUPT_TYPE_N: See OCC interrupt source [n] for bit definitions. This field establishes the type of interrupt that is monitored. 0 = Level 1 = Edge When set to level, the respective OISR[n] bit follows the value of the associated input source with the polarity defined by the OIEPR[n]. **Note:** With this setting, direct OCI writes to the OISR[n] bit must never be attempted because the value is not held and isl immediately return to its previous state. When set to edge, the respective OISR[n] bit is set upon the transition (as defined by the OIEPR[n]) of the associated input source. Specifically, if the respective OIEPR[n] bit is set to rising, a transition from 0 to 1 sets the bit. If the respective OIEPR[n] bit is set to falling, a transition from 1 to 0 sets the bit. In this mode, the only way to clear the OISR[n] bit is by a direct OCI write-clear. Additionally, firmware can inject interrupts by direct OISR write-OR to the bit (where the OIEPR[n] setting is a don't care). **Engineering Note:** For firmware testing, a potential interrupt injection technique for level interrupts is to override their definition to edge and then use the OR register associated with the OISR[n]. This allows the injected transition to stick because logic does not follow the input interrupt signal. However, if the firmware is expecting to find status in the driving unit, this technique might not be appropriate. Therefore, it makes more sense to have the driving unit provide an interrupt inject mechanism itself. Interrupt bits that intended for firmware use, that is, not driven by a hardware source, are typically tied low unless otherwise specified. The preferred mechanism for injecting interrupts is to configure these bits as an edge and use OR and CLEAR write operations to control the value of the interrupt.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Interrupt Edge/Polarity 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIEPR1
Address	000000000006C02C (SCOM) 000000000006C02D (SCOM1) 000000000006C02E (SCOM2)
Description	OCB_OCI OCC Interrupt Edge/Polarity 1 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIEPR1_INTERRUPT_EDGE_POL_N: See OCC interrupt source [n] for bit definitions. This field establishes the type of interrupt that is monitored. 0 = Falling/Low 1 = Rising/High When set, the respective bit in the OITR[n] is set to level. The Low and high meanings apply as follows: If this bit is set to low, the respective OISR[n] bit follows the inverted input to the OISR from the unit driving the signal. If this bit is set to high, the respective OISR[n] bit follows the direct input to the OISR[n] from the unit driving the signal. When set the respective bit in the OITR[n] is set to edge, the the falling and rising meanings apply as follows: If this bit is set to falling, a transition from 1 to 0 of the input signal to the OISR[n] sets the respective OISR[n] bit. If this bit is set to rising, a transition from 0 to 1 of the input signal to the OISR[n] sets the respective OISR[n] bit.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC Interrupt 0 Route A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIRR0A
Address	000000000006C040 (SCOM) 000000000006C041 (SCOM1) 000000000006C042 (SCOM2)
Description	OCC Interrupt 0 Route A Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIRR0A_INTERRUPT_ROUTE_A_N: See OCC Interrupt Source [a] for bit definitions. 0 = Interrupt is noncritical (for example, external) 1 = Interrupt is critical
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC Interrupt 0 Route B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIRR0B
Address	000000000006C044 (SCOM) 000000000006C045 (SCOM1) 000000000006C046 (SCOM2)
Description	OCC Interrupt 0 Route B Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIRR0B_INTERRUPT_ROUTE_A_N: See OCC Interrupt Source [a] for bit definitions. 0 = Interrupt is noncritical (for example, external) 1 = Interrupt is critical
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC Interrupt 0 Route C Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIRR0C
Address	000000000006C048 (SCOM) 000000000006C049 (SCOM1) 000000000006C04A (SCOM2)
Description	OCC Interrupt 0 Route C Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIRR0C_INTERRUPT_ROUTE_A_N: See OCC Interrupt Source [a] for bit definitions. 0 = Interrupt is noncritical (for example, external) 1 = Interrupt is critical
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC Interrupt 1 Route A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIRR1A
Address	000000000006C050 (SCOM) 000000000006C051 (SCOM1) 000000000006C052 (SCOM2)
Description	OCC Interrupt 1 Route A Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIRR1A_INTERRUPT_ROUTE_A_N: See OCC Interrupt Source [a] for bit definitions. 0 = Interrupt is noncritical (for example, external) 1 = Interrupt is critical
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC Interrupt 1 Route B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIRR1B
Address	000000000006C054 (SCOM) 000000000006C055 (SCOM1) 000000000006C056 (SCOM2)
Description	OCC Interrupt 1 Route B Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIRR1B_INTERRUPT_ROUTE_A_N: See OCC Interrupt Source [a] for bit definitions. 0 = Interrupt is noncritical (for example, external) 1 = Interrupt is critical

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC Interrupt 1 Route C Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIRR1C
Address	000000000006C058 (SCOM) 000000000006C059 (SCOM1) 000000000006C05A (SCOM2)
Description	OCC Interrupt 1 Route C Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OIRR1C_INTERRUPT_ROUTE_A_N: See OCC Interrupt Source [a] for bit definitions. 0 = Interrupt is noncritical (for example, external) 1 = Interrupt is critical
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Critical Interrupt Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_ONISR0
Address	000000000006C060 (SCOM)
Description	Critical Interrupt Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Critical Interrupt Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCISR0
Address	000000000006C061 (SCOM)
Description	OCB_OCI OCC Critical Interrupt Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Unconditional Interrupt Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OUISR0
Address	000000000006C062 (SCOM)
Description	OCB_OCI OCC Unconditional Interrupt Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Debug Interrupt Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_ODISR0
Address	000000000006C063 (SCOM)
Description	OCB_OCI OCC Debug Interrupt Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI GPE0 Interrupt Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G0ISR0
Address	000000000006C064 (SCOM)
Description	OCB_OCI GPE0 Interrupt Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI GPE1 Interrupt Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G1ISR0
Address	000000000006C065 (SCOM)
Description	OCB_OCI GPE1 Interrupt Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI GPE2 Interrupt Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G2ISR0
Address	000000000006C066 (SCOM)
Description	OCB_OCI GPE2 Interrupt Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI GPE3 Interrupt Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G3ISR0
Address	000000000006C067 (SCOM)
Description	OCB_OCI GPE3 Interrupt Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Non
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_ONISR1
Address	000000000006C070 (SCOM)
Description	Critical Interrupt Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Critical Interrupt Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCISR1
Address	000000000006C071 (SCOM)
Description	OCB_OCI OCC Critical Interrupt Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Unconditional Interrupt Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OUISR1
Address	000000000006C072 (SCOM)
Description	OCB_OCI OCC Unconditional Interrupt Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Debug Interrupt Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_ODISR1
Address	000000000006C073 (SCOM)
Description	OCB_OCI OCC Debug Interrupt Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI GPE0 Interrupt Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G0ISR1
Address	000000000006C074 (SCOM)
Description	OCB_OCI GPE0 Interrupt Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI GPE1 Interrupt Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G1ISR1
Address	000000000006C075 (SCOM)
Description	OCB_OCI GPE1 Interrupt Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI GPE2 Interrupt Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G2ISR1
Address	000000000006C076 (SCOM)
Description	OCB_OCI GPE2 Interrupt Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI GPE3 Interrupt Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_G3ISR1
Address	000000000006C077 (SCOM)
Description	OCB_OCI GPE3 Interrupt Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Miscellaneous Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCMISC
Address	000000000006C080 (SCOM) 000000000006C081 (SCOM1) 000000000006C082 (SCOM2)
Description	OCB_OCI OCC Miscellaneous Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	OCB_OCI_OCCMISC_CORE_EXT_INTR: Core External Interrupt. Setting this bit to a 1 causes a wire to pulse to the PSI host bridge, which allows the presentation of an external interrupt to a core thread. The core thread to be interrupted is controlled by the XIVR OCC register, SCOM 02010916. For a subsequent interrupt to be requested, this bit must be reset to '0' and then set to '1' (for example, a rising edge must be created).
1:3	RW	WO_CLEAR	WO_OR	OCB_OCI_OCCMISC_SPARE_1_3: Implemented but not used.
4:5	RW	WO_CLEAR	WO_OR	OCB_OCI_OCCMISC_PVREF_ERROR_EN: Enables the PVREF_ERROR_GROSS and PVREF_ERROR_FINE inputs after they are captured by the next two bits of this register. After applying the respective enables, the two are then ORed to assert the PVREF_FAIL indication. This sets the OISR and is also sent as an output to be delivered unlatched to all VREGs and CMEs on the chip to indicate that on-chip voltage regulation is now suspect.
6	ROX	NCX	NCX	OCB_OCI_OCCMISC_PVREF_ERROR_GROSS: Gross error indication directly from the Precision Voltage Reference.
7	ROX	NCX	NCX	OCB_OCI_OCCMISC_PVREF_ERROR_FINE: Fine error indication directly from the Precision Voltage Reference.
8	RW	WO_CLEAR	WO_OR	OCB_OCI_OCCMISC_FIRMWARE_FAULT: Sets OCCLFIR[occ_complex_fault] to indicate an OCC error occurred.
9	RW	WO_CLEAR	WO_OR	OCB_OCI_OCCMISC_FIRMWARE_NOTIFY: Sets OCCLFIR[occ_complex_notify] to indicate an OCC event occurred that needs attention from another firmware entity.
10:15	RW	WO_CLEAR	WO_OR	OCB_OCI_OCCMISC_SPARE: Implemented but not used.
16:18	ROX	NCX	NCX	OCB_OCI_OCCMISC_I2CM_INTR_STATUS: Interrupt Status from I2CM.
19:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCC HTM Control Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OHTMCR
Address	000000000006C083 (SCOM)
Description	OCB_OCI OCC HTM Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	OCB_OCI_OHTMCR_HTM_SRC_SEL: Select OCC source to drive out HTM data. 00 = HTM off 01 = PLB data 10 = 405 data 11 = Selected GPE from HTM_GPE_SRC_SEL.
2	RW	OCB_OCI_OHTMCR_HTM_STOP: HTM Stop Signal. Setting this bit causes the HTM stop signal to be sent to the NHTM to indicate to stop collecting OCC.

Bits	SCOM	Field Mnemonic: Description
3:5	RW	OCB_OCI_OHTMCR_HTM_MARKER_SLAVE_ADRS: HTM Slave Address Marker. Used to match against the slave address in the PLB HTM stream to generate markers.
6:7	RW	OCB_OCI_OHTMCR_EVENT2HALT_MODE: Event to Halt Mode: 00 = Off 01 = Halt on event 10 = Halt some delay after event 11 = Unused (off)
8:18	RW	OCB_OCI_OHTMCR_EVENT2HALT_EN: Enable Trace Trigger Event(0:10) to cause a halt as programmed by field EVENT2HALT_MODE. 0 = Disabled 1 = Enabled
19	RO	constant = 0b0
20:21	RW	OCB_OCI_OHTMCR_HTM_GPE_SRC_SEL: Select GPE source to drive out HTM data. 00 = GPE0 01 = GPE1 10 = GPE2 11 = GPE3
22	RO	constant = 0b0
23	RW	OCB_OCI_OHTMCR_EVENT2HALT_OCC: Enabled halt event causes the PowerPC 405 core to halt.
24	RW	OCB_OCI_OHTMCR_EVENT2HALT_GPE0: Enabled halt event causes the GPE0 to halt.
25	RW	OCB_OCI_OHTMCR_EVENT2HALT_GPE1: Enabled halt event causes the GPE1 to halt.
26	RW	OCB_OCI_OHTMCR_EVENT2HALT_GPE2: Enabled halt event causes the GPE2 to halt.
27	RW	OCB_OCI_OHTMCR_EVENT2HALT_GPE3: Enabled halt event causes the GPE3 to halt.
28:30	RO	constant = 0b000
31	RWX_WCLRPART	OCB_OCI_OHTMCR_EVENT2HALT_HALT_STATE: Event-driven halt. This bit reflects the value of the event-driven halt condition that is sent to the targets as indicated in bits 23:27. Writing this register clears the event-driven halt condition.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Event Halt Delay Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OEHDR
Address	000000000006C084 (SCOM)
Description	OCB_OCI OCC Event Halt Delay Register

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	OCB_OCI_OEHDR_EVENT2HALT_DELAY: Event to Halt Delay Counter. This field contains the amount of delay to wait between a Trigger Event occurring and Debug Halt being asserted. Only valid if EVENT2HALT_MODE = 10.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCB_OCI OCC OCI Configuration Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCICFG
Address	000000000006C085 (SCOM)
Description	OCB_OCI OCC OCI Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	OCB_OCI_OCICFG_M0_PRIORITY: Set OCI Master0 Arbitration Priority (GPE0). 00 = Lowest 01 = Low 10 = High 11 = Highest
2:3	RW	OCB_OCI_OCICFG_M1_PRIORITY: Set OCI Master1 Arbitration Priority (GPE1). 00 = Lowest 01 = Low 10 = High 11 = Highest
4:5	RW	OCB_OCI_OCICFG_M2_PRIORITY: Set OCI Master2 Arbitration Priority (GPE2). 00 = Lowest 01 = Low 10 = High 11 = Highest
6:7	RW	OCB_OCI_OCICFG_M3_PRIORITY: Set OCI Master3 Arbitration Priority (GPE3). 00 = Lowest 01 = Low 10 = High 11 = Highest
8:9	RW	OCB_OCI_OCICFG_M4_PRIORITY: Set OCI Master4 Arbitration Priority (PBA). 00 = Lowest 01 = Low 10 = High 11 = Highest
10:11	RW	OCB_OCI_OCICFG_M5_PRIORITY: Set OCI Master5 Arbitration Priority (PowerPC 405 core IC). 00 = Lowest 01 = Low 10 = High 11 = Highest
12:13	RW	OCB_OCI_OCICFG_M6_PRIORITY: Set OCI Master6 Arbitration Priority (OCB). 00 = Lowest 01 = Low 10 = High 11 = Highest
14:15	RW	OCB_OCI_OCICFG_M7_PRIORITY: Set OCI Master7 Arbitration Priority (PowerPC 405 core DC). 00 = Lowest 01 = Low 10 = High 11 = Highest
16	RW	OCB_OCI_OCICFG_M0_PRIORITY_SEL: Selects between the M0_PRIORITY register setting and the GPE0 requested priority value. 0 = Select M0_PRIORITY 1 = Select GPE0_OCI_M_PRIORITY
17	RW	OCB_OCI_OCICFG_M1_PRIORITY_SEL: Selects between the M1_PRIORITY register setting and the GPE1 requested priority value. 0 = Select M1_PRIORITY 1 = Select GPE1_OCI_M_PRIORITY
18	RW	OCB_OCI_OCICFG_M2_PRIORITY_SEL: Selects between the M2_PRIORITY register setting and the GPE2 requested priority value. 0 = Select M2_PRIORITY 1 = Select GPE2_OCI_M_PRIORITY

Bits	SCOM	Field Mnemonic: Description
19	RW	OCB_OCI_OCICFG_M3_PRIORITY_SEL: Selects between the M3_PRIORITY register setting and the GPE3 requested priority value. 0 = Select M3_PRIORITY 1 = Select GPE3_OCI_M_PRIORITY
20	RW	OCB_OCI_OCICFG_OCICFG_RESERVED_20: Implemented but not used. Master 4 (PBA) priority always come from the M4_PRIORITY field.
21	RW	OCB_OCI_OCICFG_M5_PRIORITY_SEL: Selects between the M5_PRIORITY register setting and the ICU 405 priority value. 0 = Select M5_PRIORITY 1 = Select C405ICU_OCI_M_PRIORITY.
22	RW	OCB_OCI_OCICFG_OCICFG_RESERVED_23: Implemented but not used. Master 6 (OCB) priority always come from the M6_PRIORITY field.
23	RW	OCB_OCI_OCICFG_M7_PRIORITY_SEL: Selects between the m7_PRIORITY register setting and the DCU 405 priority value. 0 = Select M7_PRIORITY 1 = Select C405DCU_OCI_M_PRIORITY
24	RW	OCB_OCI_OCICFG_PLBARB_LOCKERR: Causes PLB arbiter to lock up and hold the address and masteridof a request that gets a timeout.
25:31	RW	OCB_OCI_OCICFG_SPARE_24_31: Spare debug switches.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Scratch 0
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCS0
Address	000000000006C086 (SCOM)
Description	OCB_OCI OCC Scratch 0

Bits	SCOM	Field Mnemonic: Description
0:31	RW	OCB_OCI_OCCS0_OCC_SCRATCH_N: Scratch Data [n].
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Scratch 1
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCS1
Address	000000000006C087 (SCOM)
Description	OCB_OCI OCC Scratch 1

Bits	SCOM	Field Mnemonic: Description
0:31	RW	OCB_OCI_OCCS1_OCC_SCRATCH_N: Scratch Data [n].
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Scratch 2
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCS2
Address	000000000006C088 (SCOM)
Description	OCB_OCI OCC Scratch 2

Bits	SCOM	Field Mnemonic: Description
0:31	RW	OCB_OCI_OCCS2_OCC_SCRATCH_N: Scratch Data [n].
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Flags
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCFLG
Address	000000000006C08A (SCOM) 000000000006C08B (SCOM1) 000000000006C08C (SCOM2)
Description	OCB_OCI OCC Flags

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	OCB_OCI_OCCFLG_OCC_FLAGS: Flags that are defined by OCC firmware.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB OCC Heartbeat Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCCHBR
Address	000000000006C08F (SCOM)
Description	OCB_OCI OCB OCC Heartbeat Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	OCB_OCI_OCCHBR_OCC_HEARTBEAT_COUNT: When written, this field defines the starting value for a counter that increments at about 1us if OCC_HEARTBEAT_EN = 1 and the counter value is non-zero. If OCC_HEARTBEAT_EN = 0 or the counter value is 0, the counter does not increment. If OCC_HEARTBEAT_EN = 1 and this counter becomes 0 (either from a written value or from the counter wrapping) constitutes the loss of the OCC heartbeat and surfaces an attention through TBD LFIR(TBD). The pulses used for this field come from a free running pervasive hang timer pulse (PM_Hang_Pulse) programmed to be ~ 32 ns that has a 5-bit precounter whose carryout forms a resultant ~ 1us decrement pulse. Upon writing this register with OCC_HEARTBEAT_EN = 1, the precounter is cleared and will begin counting upon the next PM_Hang_Pulse. This PM_Hang_Pulse might arrive immediately or a full duration later. With a (215)-1 range and an ~1 us incrementation time yields a heartbeat range of 1us (+0-32ns) (value 0xFFFF) to 65.535 ms (+0-32ns) (value 0x0001). The value chosen to be written for debug purposes only, writing 0x0000 causes an immediate heartbeat_lost if OCC_HEARTBEAT_EN = 1. Reads return the current value of the counter value.
16	RW	OCB_OCI_OCCHBR_OCC_HEARTBEAT_EN: OCC Heartbeat Timer Enable.
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI Core Configuration Status Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_CCSR
Address	000000000006C090 (SCOM) 000000000006C091 (SCOM1) 000000000006C092 (SCOM2)
Description	OCB_OCI Core Configuration Status Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:23	RW	WO_CLEAR	WO_OR	OCB_OCI_CCSR_CORE_CONFIG: The bit per core chiplet that indicates when it is set to 1, it is configured and therefore available to target. If a core is configured, its associated EX region must also be configured in the QCSR. Likewise, if a pair of cores is deconfigured, the corresponding EX region of the cache chiplet must also be deconfigured with them.
24:30	RW	WO_CLEAR	WO_OR	OCB_OCI_CCSR_RESERVED_24: Reserved Spare bit.
31	RW	WO_CLEAR	WO_OR	OCB_OCI_CCSR_CHANGE_IN_PROGRESS: Configuration change is in progress. When this bit is zero, all multicast groups and chiplet enables are consistent with the contents of this register.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI Quad Configuration Status Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_QCSR
Address	000000000006C094 (SCOM) 000000000006C095 (SCOM1) 000000000006C096 (SCOM2)
Description	OCB_OCI Quad Configuration Status Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:23	RW	WO_CLEAR	WO_OR	OCB_OCI_QCSR_CORE_CONFIG: The bit per core chiplet that indicates when it is set to 1, it is configured and therefore available to target. **Note:** If both core pairs are deconfigured, by definition the L2 is also deconfigured with them. This register enables both core and L2 partial good support. **Note:** A bad L2 results in deconfiguration of both of its associated core chiplets. If a core is configured, its associated L3 must also be configured in the following field.
24:31	RW	WO_CLEAR	WO_OR	OCB_OCI_QCSR_RESERVED_24_31: Reserved Spare bit.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI Quad Stop Status Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_QSSR
Address	000000000006C098 (SCOM) 000000000006C099 (SCOM1) 000000000006C09A (SCOM2)
Description	OCB_OCI Quad Stop Status Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:11	RW	WO_CLEAR	WO_OR	OCB_OCI_QSSR_L2_STOPPED: The bit per L2 cache in the cache chiplet that indicates when it is set to 1, it is stopped by the Stop GPE due to a Core Stop State or partial good condition. **Note:** Two core chiplets share each L2. Therefore, this bit implies that the core pair has also been put into a stop state.
12:23	RW	WO_CLEAR	WO_OR	OCB_OCI_QSSR_L3_STOPPED: The bit per L3 cache region in the cache chiplet that indicates when it is set to 1, it is stopped by the stop GPE from a Core Stop State or partial good condition. If an L3_STOPPED bit is set, the corresponding L2_STOPPED bit must also be set.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24:29	RW	WO_CLEAR	WO_OR	OCB_OCI_QSSR_QUAD_STOPPED: The bit per quad that indicates when it is set to 1, the cache chiplet is stopped by the stop GPE from a Core Stop state. **Note:** If QUAD_STOPPED(X) is set then L3_STOPPED(2 * X : 2 * X + 1) must also be set.
30	RW	WO_CLEAR	WO_OR	OCB_OCI_QSSR_RESERVED_30: Reserved. Spare bit.
31	RW	WO_CLEAR	WO_OR	OCB_OCI_QSSR_CHANGE_IN_PROGRESS: The stop state change is in progress (entry or exit) for one or more quads that rely on the stop GPE.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Timebase Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OTBR
Address	000000000006C09F (SCOM)
Description	OCB_OCI OCB Timebase Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	OCB_OCI_OTBR_TIMEBASE: OCB timebase free-running counter whose least-significant-bit increments every CME timer input pulse, which is configured to run at nest (processor bus) clock64. (At 2 GHz, this rises every 32 ns, and this counter will wrap every 137 seconds). Firmware must perform all delta calculations (including accounting for the wrap condition) to perform elapsed time functions.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Timer Register 0
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OTR0
Address	000000000006C100 (SCOM)
Description	OCB_OCI OCC Timer Register 0

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	OCB_OCI_OTR0_TIMEOUT_N: This bit is set by hardware on any 1 0 transition of the timer. This value of this bit is provided to the interrupt controller as the occ_timer[n] status. The interrupt controller is typically be programmed to recognize occ_timer[n] as an active-high, level sensitive interrupt. This bit is reset by writing the register with a ‘1’ in this bit position. If the hardware timer value transition from 1 0 occurs concurrently with the updating of this register to perform a reset, this bit is reset and the hardware transition is lost.
1	WO	OCB_OCI_OTR0_CONTROL_N: Reading this bit always returns 0. If the register is written with a ‘1’ in this bit position, all other fields other than timeout are updated. Otherwise, the write has no effect other than to clear the timeout_[n] field if the timeout_[n] bit is set in the write data. If the register is written with a ‘1’ in this bit position and a ‘0’ in the timeout bit position which occurs concurrently with the hardware timer value making a 1 0 transition, the timeout_[n] bit is set per the previous timer_[n] settings.
2	RW	OCB_OCI_OTR0_AUTO_RELOAD_N: If set, the timer operates in autoreload mode. In autoreload mode, every timeout of the timer sets the timeout_[n] bit and reinitializes the timer counter from the hidden autoreload value. If clear, a timeout of the timer simply sets the timeout_[n] bit. This field can be written only if the control_[n] bit is set on a write of the register.
3:15	RW	OCB_OCI_OTR0_SPARE_N: Writes store the value only if the control_[n] bit is set on a write of this register. Reads return the last value written.

Bits	SCOM	Field Mnemonic: Description
16:31	RWX	OCB_OCI_OTR0_TIMER_N: When the register is read, this field returns the current value of the hardware timer. When written, the value of the field goes into the hardware timer and the hidden autoreload register, and the hardware timer begins to decrement. This field can only be written if the control_[n] bit is set on a write of the register.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC Timer Register 1
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OTR1
Address	000000000006C101 (SCOM)
Description	OCB_OCI OCC Timer Register 1

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	OCB_OCI_OTR1_TIMEOUT_N: This bit is set by hardware on any 1 0 transition of the timer. This value of this bit is provided to the interrupt controller as the occ_timer[n] status. The interrupt controller is typically programmed to recognize occ_timer[n] as an active-high, level sensitive interrupt. This bit is reset by writing the register with a '1' in this bit position. If the hardware timer value transition from 1 0 occurs concurrently with the updating of this register to perform a reset, this bit is reset and the hardware transition is lost.
1	WO	OCB_OCI_OTR1_CONTROL_N: Reading this bit always returns 0. If the register is written with a '1' in this bit position, all other fields other than timeout are updated. Otherwise, the write has no effect other than to clear the timeout_[n] field if the timeout_[n] bit is set in the write data. If the register is written with a '1' in this bit position and a '0' in the timeout bit position occurs concurrently with the hardware timer value making a 1 0 transition, the timeout_[n] bit will be set per the previous timer_[n] settings.
2	RW	OCB_OCI_OTR1_AUTO_RELOAD_N: If set, the timer operates in autoreload mode. In autoreload mode, every timeout of the timer sets the timeout_[n] bit and reinitializes the timer counter from the hidden autoreload value. If clear, a timeout of the timer simply sets the timeout_[n] bit. This field can be written only if the control_[n] bit is set on a write of the register.
3:15	RW	OCB_OCI_OTR1_SPARE_N: Writes store the value only if the control_[n] bit is set on a write of this register. Reads return the last value written.
16:31	RWX	OCB_OCI_OTR1_TIMER_N: When the register is read, this field returns the current value of the hardware timer. When written, the value of the field goes into the hardware timer and the hidden autoreload register, and the hardware timer begins to decrement. This field can only be written if the control_[n] bit is set on a write of the register.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Pull Base 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR0
Address	000000000006C200 (SCOM)
Description	OCB_OCI OCB Stream Pull Base 0 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBSLBR0_PULL_OCI_REGION: Pull OCI Region Allowed values: 10X = Processor bus memory 111 = SRAM. Others are reserved.
3:28	RW	OCB_OCI_OCBSLBR0_PULL_START: Starting address of pull queue (8 B alignment).
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Pull Control/Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS0
Address	000000000006C201 (SCOM)
Description	OCB_OCI OCB Stream Pull Control/Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	OCB_OCI_OCBSLCS0_PULL_FULL: Reads indicate the pull queue is full condition. Any write to this register clears this indicator and clears PULL_WRITE_PTR and PULL_READ_PTR to 0s. (This is a means for resetting the queue hardware) RWX_WCLRPART.
1	RWX_WSETPART	OCB_OCI_OCBSLCS0_PULL_EMPTY: Reads indicate the pull queue empty condition. Any write to this register sets this indicator and clears PULL_WRITE_PTR and PULL_READ_PTR to 0s. (This is a means for resetting the queue hardware) RWX_WSETPART.
2:3	RW	OCB_OCI_OCBSLCS0_SPARE: Implemented but not used. Writes store the value. Reads return the last value written.
4:5	RW	OCB_OCI_OCBSLCS0_PULL_INTR_ACTION_0_1: Pull Interrupt Action This field controls the condition which will assert the pull interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware initialization) b01 = Nonfull b10 = Empty (the more useful firmware default) b11 = Not empty.
6:10	RW	OCB_OCI_OCBSLCS0_PULL_LENGTH: Pull queue length in (pull_length + 1) * 8 B Value mapping: 0b00000 = 8 B 0b00001 = 16 B 0b00010 = 24 B 0b00011 = 32 B 0b00100 = 40 B 0b00101 = 48 B 0b00110 = 56 B 0b00111 = 64 B 0b01000 = 72 B 0b01001 = 80 B 0b01010 = 88 B 0b01011 = 96 B 0b01100 = 104 B 0b01101 = 112 B 0b01110 = 120 B 0b01111 = 128 B 0b10000 = 136 B 0b10001 = 144 B 0b10010 = 152 B 0b10011 = 160 B 0b10100 = 168 B 0b10101 = 176 B 0b10110 = 184 B 0b10111 = 192 B 0b11000 = 200 B 0b11001 = 208 B 0b11010 = 216 B 0b11011 = 224 B 0b11100 = 232 B 0b11101 = 240 B 0b11110 = 248 B 0b11111 = 256 B
11:12	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
13:17	RWX_WCLRPART	OCB_OCI_OCBSLCS0_PULL_WRITE_PTR: Pull write pointer Reads indicate the current pull queue write pointer in increments of 8 B. The actual address used is PULL_OCI_REGION || PULL_START + PULL_WRITE_PTR || 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register.
18:20	RO	constant = 0b000
21:25	RWX_WCLRPART	OCB_OCI_OCBSLCS0_PULL_READ_PTR: Pull read pointer Reads indicate the current pull queue read pointer in increments of 8 B. The actual address used is PULL_OCI_REGION || PULL_START + PULL_WRITE_PTR || 00000. This field is cleared upon a write to this register.
26:30	RO	constant = 0b00000
31	RW	OCB_OCI_OCBSLCS0_PULL_ENABLE: Enables the pull queue function If Disabled, PIB Reads to OCB Data [n] Register to perform a pull will result in an offline PIB error back to the PIB Master. **Note:** OCI Reads to OCB Stream Pull Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full or empty conditions might still arise to the OCC even if this bit indicates disabled.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Pull Increment 0 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLI0
Address	000000000006C202 (SCOM)
Description	OCB_OCI OCB Stream Pull Increment 0 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Push Base 0 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR0
Address	000000000006C203 (SCOM)
Description	OCB_OCI OCB Stream Push Base 0 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBSHBR0_PUSH_OCI_REGION: Push OCI Region Allowed values: 10X = Processor bus memory 111 = SRAM Others are reserved.
3:28	RW	OCB_OCI_OCBSHBR0_PUSH_START: Starting address of Push Queue (8 B alignment).
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Push Control/Status 0 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS0
Address	000000000006C204 (SCOM)
Description	OCB_OCI OCB Stream Push Control/Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	OCB_OCI_OCBSHCS0_PUSH_FULL: Reads indicate the push queue is full condition. Any write to this register clears this indicator and clears PUSH_WRITE_PTR and PUSH_READ_PTR to 0s. This is a means for resetting the queue hardware.
1	RWX_WSETPART	OCB_OCI_OCBSHCS0_PUSH_EMPTY: Read indicate the push queue empty condition. Any write to this register sets this indicator and clears PUSH_WRITE_PTR and PUSH_READ_PTR to 0s. This is a means for resetting the queue hardware.
2:3	RW	OCB_OCI_OCBSHCS0_SPARE: Implemented by not used. Writes store the value. Reads return the last value written.
4:5	RW	OCB_OCI_OCBSHCS0_PUSH_INTR_ACTION_0_1: Push Interrupt Action. This field controls the condition that will assert the push interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware init) b01 = Not full b10 = Empty b11 = Not empty.

Bits	SCOM	Field Mnemonic: Description
6:10	RW	OCB_OCI_OCBSHCS0_PUSH_LENGTH: Push queue length in (PUSH_LENGTH + 1) * 8 B Value mapping: 0b00000 = 8 B 0b00001 = 16 B 0b00010 = 24 B 0b00011 = 32 B 0b00100 = 40 B 0b00101 = 48 B 0b00110 = 56 B 0b00111 = 64 B 0b01000 = 72 B 0b01001 = 80 B 0b01010 = 88 B 0b01011 = 96 B 0b01100 = 104 B 0b01101 = 112 B 0b01110 = 120 B 0b01111 = 128 B 0b10000 = 136 B 0b10001 = 144 B 0b10010 = 152 B 0b10011 = 160 B 0b10100 = 168 B 0b10101 = 176 B 0b10110 = 184 B 0b10111 = 192 B 0b11000 = 200 B 0b11001 = 208 B 0b11010 = 216 B 0b11011 = 224 B 0b11100 = 232 B 0b11101 = 240 B 0b11110 = 248 B 0b11111 = 256 B
11:12	RO	constant = 0b00
13:17	RWX_WCLRPART	OCB_OCI_OCBSHCS0_PUSH_WRITE_PTR: Push write pointer. Reads indicate the current push queue write pointer in increments of 8 B. The actual address used is PUSH_OCI_REGION || PUSH_START + PUSH_WRITE_PTR || 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register.
18:20	RO	constant = 0b000
21:25	RWX_WCLRPART	OCB_OCI_OCBSHCS0_PUSH_READ_PTR: Push read pointer reads indicate the current push queue read pointer in increments of 8 B. The actual address used is PUSH_OCI_REGION || PUSH_START + PUSH_READ_PTR || 00000. This field is cleared upon a write to this register.
26:30	RO	constant = 0b00000
31	RW	OCB_OCI_OCBSHCS0_PUSH_ENABLE: Enables the push queue function if disabled, PIB writes to OCB Data [n] Register to perform a push will result in an offline PIB error back to the PIB master. **Note:** OCI Writes to OCB Stream Push Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full or empty conditions might still arise to the OCC even if this bit indicates disabled.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Push Increment 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHI0
Address	000000000006C205 (SCOM)
Description	OCB_OCI OCB Stream Push Increment 0 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Error Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES0
Address	000000000006C206 (SCOM)
Description	OCB_OCI OCB Stream Error Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	OCB_OCI_OCBSES0_PUSH_READ_UNDERFLOW: Push Queue Read Underflow. Underflow is defined as a store to the PUSH_READ_INCR facility is done and the PUSH_EMPTY facility is already set. This bit is cleared only by a firmware write of this bit to 0.
1	RWX	OCB_OCI_OCBSES0_PULL_WRITE_OVERFLOW: Pull Queue Write Overflow. Overflow is defined as a load to the PULL_WRITE_INCR facility is done and the PULL_FULL facility is already set. This bit is cleared only by a firmware write of this bit to 0.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Write Window Control 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR0
Address	000000000006C208 (SCOM)
Description	OCB_OCI OCB Linear Write Window Control 0 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_OCBLWCR0_LINEAR_WINDOW_ENABLE: Linear Window Enable 0 = Window facility disabled. See the the Power Management Specification, section Indirect Bridge Operation for the effects of this bit for a write operation as it is dependent on the setting of trusted mode. 1 = Window facility enabled. If OCBCSR[n]. OCB_STREAM_TYPE = linear. Linear Window BAR and Mask are valid and operations are to be honored. SC_RESP codes are the same as for the OCB indirect facility to reflect the status of the OCI operation.
1:2	RW	OCB_OCI_OCBLWCR0_SPARE_0: Implemented by not used. Writes store the value. Reads return the last value written.
3:19	RW	OCB_OCI_OCBLWCR0_LINEAR_WINDOW_BAR: Linear Window Base Address Register Defines OCI address(12:28). 17 bits to define the starting offset within the region addressed.
20:31	RW	OCB_OCI_OCBLWCR0_LINEAR_WINDOW_MASK: Linear Window Address Mask Register Masks OCI address (17:28). 12 bits to define the window size.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Write Window Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSR0
Address	000000000006C20A (SCOM)
Description	OCB_OCI OCB Linear Write Window Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	OCB_OCI_OCBLWSR0_LINEAR_WINDOW_SCRESP: Linear Window PIB SC Response If OCBLWCR.linear_window_enable = 1, this field contains the last PIB response code sent (potentially allowing OCC FW to tell if attempts were made to use the window.
3:7	RO	OCB_OCI_OCBLWSR0_SPARE0: Implemented but not used.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Window Write Base 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR0
Address	000000000006C20C (SCOM)
Description	OCB_OCI OCB Linear Window Write Base 0 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBLWSBR0_LINEAR_WINDOW_REGION: Linear Window Region. If LINEAR_WINDOW_ENABLE = 1, this field defines the OCI region (OCI Address[0:2]) that is enabled for accessing the linear window. If the value written into OCBAR[n] does not match this value and the OCBDR[n] is accessed, a PIB scresp error is produced. Only the SRAM region (0b111) is supported.
3:9	RW	OCB_OCI_OCBLWSBR0_LINEAR_WINDOW_BASE: Linear Window Base. If LINEAR_WINDOW_ENABLE = 1, establishes OCI Address(5:11); 128 B aliases still apply (for example, OCI Address[3:4]).
10:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Pull Base 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR1
Address	000000000006C210 (SCOM)
Description	OCB_OCI OCB Stream Pull Base 1 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBSLBR1_PULL_OCI_REGION: Pull OCI Region Allowed values: 10X = Processor bus memory 111 = SRAM. Others are reserved.
3:28	RW	OCB_OCI_OCBSLBR1_PULL_START: Starting address of pull queue (8 B alignment).
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Pull Control/Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS1
Address	000000000006C211 (SCOM)
Description	OCB_OCI OCB Stream Pull Control/Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	OCB_OCI_OCBSLCS1_PULL_FULL: Reads indicate the pull queue is full condition. Any write to this register clears this indicator and clears PULL_WRITE_PTR and PULL_READ_PTR to 0s. (This is a means for resetting the queue hardware) RWX_WCLRPART.
1	RWX_WSETPART	OCB_OCI_OCBSLCS1_PULL_EMPTY: Reads indicate the pull queue empty condition. Any write to this register sets this indicator and clears PULL_WRITE_PTR and PULL_READ_PTR to 0s. This is a means for resetting the queue hardware RWX_WSETPART.
2:3	RW	OCB_OCI_OCBSLCS1_SPARE: Implemented but not used. Writes store the value. Reads return the last value written.
4:5	RW	OCB_OCI_OCBSLCS1_PULL_INTR_ACTION_0_1: Pull Interrupt Action. This field controls the condition the will assert the pull interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware init) b01 = Not full b10 = Empty (the more useful firmware default) b11 = Not Empty.
6:10	RW	OCB_OCI_OCBSLCS1_PULL_LENGTH: Pull queue length in (pull_length + 1) * 8 B Value mapping: 0b00000 = 8 B 0b00001 = 16 B 0b00010 = 24 B 0b00011 = 32 B 0b00100 = 40 B 0b00101 = 48 B 0b00110 = 56 B 0b00111 = 64 B 0b01000 = 72 B 0b01001 = 80 B 0b01010 = 88 B 0b01011 = 96 B 0b01100 = 104 B 0b01101 = 112 B 0b01110 = 120 B 0b01111 = 128 B 0b10000 = 136 B 0b10001 = 144 B 0b10010 = 152 B 0b10011 = 160 B 0b10100 = 168 B 0b10101 = 176 B 0b10110 = 184 B 0b10111 = 192 B 0b11000 = 200 B 0b11001 = 208 B 0b11010 = 216 B 0b11011 = 224 B 0b11100 = 232 B 0b11101 = 240 B 0b11110 = 248 B 0b11111 = 256 B
11:12	RO	constant = 0b00
13:17	RWX_WCLRPART	OCB_OCI_OCBSLCS1_PULL_WRITE_PTR: Pull write pointer. Reads indicate the current pull queue write pointer in increments of 8 B. The actual address used is PULL_OCI_REGION || PULL_START + PULL_WRITE_PTR || 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register.
18:20	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
21:25	RWX_WCLRPART	OCB_OCI_OCBSLCS1_PULL_READ_PTR: Pull read pointer Reads indicate the current pull queue read pointer in increments of 8 B. The actual address used is PULL_OCI_REGION || PULL_START + PULL_WRITE_PTR || 00000. This field is cleared upon a write to this register.
26:30	RO	constant = 0b00000
31	RW	OCB_OCI_OCBSLCS1_PULL_ENABLE: Enables the Pull Queue Function. If disabled, PIB reads to the OCB Data [n] Register to perform a pull will result in an offline PIB error back to the PIB Master. **Note:** OCI reads to OCB Stream Pull Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full or empty conditions might still arise to the OCC even if this bit indicates disabled.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Pull Increment 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLI1
Address	000000000006C212 (SCOM)
Description	OCB_OCI OCB Stream Pull Increment 1 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Push Base 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR1
Address	000000000006C213 (SCOM)
Description	OCB_OCI OCB Stream Push Base 1 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBSHBR1_PUSH_OCI_REGION: Push OCI Region Allowed values: 10X = processor bus memory 111 = SRAM Others are reserved.
3:28	RW	OCB_OCI_OCBSHBR1_PUSH_START: Starting address of push queue (8 B alignment).
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Push Control/Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS1
Address	000000000006C214 (SCOM)
Description	OCB_OCI OCB Stream Push Control/Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	OCB_OCI_OCBSHCS1_PUSH_FULL: Reads indicate the push queue is full condition. Any write to this register clears this indicator and clears PUSH_WRITE_PTR and PUSH_READ_PTR to 0s. This is a means for resetting the queue hardware.
1	RWX_WSETPART	OCB_OCI_OCBSHCS1_PUSH_EMPTY: Read indicate the push queue empty condition. Any write to this register sets this indicator and clears PUSH_WRITE_PTR and PUSH_READ_PTR to 0s. This is a means for resetting the queue hardware.

Bits	SCOM	Field Mnemonic: Description
2:3	RW	OCB_OCI_OCBSHCS1_SPARE: Implemented by not used. Writes store the value. Reads return the last value written.
4:5	RW	OCB_OCI_OCBSHCS1_PUSH_INTR_ACTION_0_1: Push Interrupt Action This field controls the condition which will assert the push interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware init) b01 = Non Full b10 = Empty b11 = Not Empty.
6:10	RW	OCB_OCI_OCBSHCS1_PUSH_LENGTH: Push queue length in (PUSH_LENGTH + 1) * 8 B Value mapping: 0b00000 = 8 B 0b00001 = 16 B 0b00010 = 24 B 0b00011 = 32 B 0b00100 = 40 B 0b00101 = 48 B 0b00110 = 56 B 0b00111 = 64 B 0b01000 = 72 B 0b01001 = 80 B 0b01010 = 88 B 0b01011 = 96 B 0b01100 = 104 B 0b01101 = 112 B 0b01110 = 120 B 0b01111 = 128 B 0b10000 = 136 B 0b10001 = 144 B 0b10010 = 152 B 0b10011 = 160 B 0b10100 = 168 B 0b10101 = 176 B 0b10110 = 184 B 0b10111 = 192 B 0b11000 = 200 B 0b11001 = 208 B 0b11010 = 216 B 0b11011 = 224 B 0b11100 = 232 B 0b11101 = 240 B 0b11110 = 248 B 0b11111 = 256 B
11:12	RO	constant = 0b00
13:17	RWX_WCLRPART	OCB_OCI_OCBSHCS1_PUSH_WRITE_PTR: Push write pointer Reads indicate the current Push Queue write pointer in increments of 8 B. The actual address used is push_oci_region || push_start + push_write_ptr || 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register. ROX_WCLRPART.
18:20	RO	constant = 0b000
21:25	RWX_WCLRPART	OCB_OCI_OCBSHCS1_PUSH_READ_PTR: Push read pointer Reads indicate the current Push Queue read pointer in increments of 8 B. The actual address used is push_oci_region || push_start + push_read_ptr || 00000. This field is cleared upon a write to this register. ROX_WCLRPART.
26:30	RO	constant = 0b00000
31	RW	OCB_OCI_OCBSHCS1_PUSH_ENABLE: Enables the Push Queue function If Disabled, PIB Writes to OCB Data [n] Register to perform a push will result in an offline PIB error back to the PIB Master. **Note:** OCI Writes to OCB Stream Push Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full or empty conditions might still arise to the OCC even if this bit indicates disabled.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Push Increment 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHI1
Address	000000000006C215 (SCOM)
Description	OCB_OCI OCB Stream Push Increment 1 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Error Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES1
Address	000000000006C216 (SCOM)
Description	OCB_OCI OCB Stream Error Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	OCB_OCI_OCBSES1_PUSH_READ_UNDERFLOW: Push Queue Read Underflow. Underflow is defined as a store to the push_read_incr facility is done and the PUSH_EMPTY facility is already set. This bit is cleared only by a firmware write of this bit to 0.
1	RWX	OCB_OCI_OCBSES1_PULL_WRITE_OVERFLOW: Pull Queue Write Overflow. Overflow is defined as a load to the PULL_WRITE_INCR facility is done and the PULL_FULL facility is already set. This bit is cleared only by a firmware write of this bit to 0.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Write Window Control 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR1
Address	000000000006C218 (SCOM)
Description	OCB_OCI OCB Linear Write Window Control 1 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_OCBLWCR1_LINEAR_WINDOW_ENABLE: Linear Window Enable 0: Window facility disabled. See Power Management Specification, section Indirect Bridge Operation for the effects of this bit for a write operation as it is dependent on the setting of trusted mode. 1: Window facility enabled. If OCBCSR[n]. OCB_STREAM_TYPE = linear, Linear Window BAR and Mask are valid and operations are to be honored. SC_RESP codes are the same as for the OCB indirect facility to reflect the status of the OCI operation.
1:2	RW	OCB_OCI_OCBLWCR1_SPARE_0: Implemented by not used. Writes store the value. Reads return the last value written.
3:19	RW	OCB_OCI_OCBLWCR1_LINEAR_WINDOW_BAR: Linear Window Base Address Register Defines OCI address(12:28) - 17 bits to define the starting offset within the region addressed.
20:31	RW	OCB_OCI_OCBLWCR1_LINEAR_WINDOW_MASK: Linear Window Address Mask Register Masks OCI address (17:28) - 12 bits to define the window size.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Write Window Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSR1
Address	000000000006C21A (SCOM)
Description	OCB_OCI OCB Linear Write Window Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	OCB_OCI_OCBLWSR1_LINEAR_WINDOW_SCRESP: Linear Window PIB SC Response If OCBLWCR.linear_window_enable=1, this field contains the last PIB response code sent (potentially allowing OCC FW to tell if attempts were made to use the window.
3:7	RO	OCB_OCI_OCBLWSR1_SPARE0: Implemented but not used.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Window Write Base 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR1
Address	000000000006C21C (SCOM)
Description	OCB_OCI OCB Linear Window Write Base 1 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBLWSBR1_LINEAR_WINDOW_REGION: Linear Window Region If linear_window_enable = 1, this field defines the OCI region (OCI Address[0:2] that is enabled for accessing the Linear Window). If the value written into OCBAR[n] does not match this value and the OCBDR[n] is accessed, a PIB scresp error is produced. Only the SRAM region (0b111) is supported.
3:9	RW	OCB_OCI_OCBLWSBR1_LINEAR_WINDOW_BASE: Linear Window Base If linear_window_enable = 1, establishes OCI Address(5:11); 128 B aliases still apply (for example, OCI Address(3:4).
10:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Pull Base 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR2
Address	000000000006C220 (SCOM)
Description	OCB_OCI OCB Stream Pull Base 2 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBSLBR2_PULL_OCI_REGION: Pull OCI Region Allowed values: 10X = Processor bus memory 111 = SRAM Others are reserved
3:28	RW	OCB_OCI_OCBSLBR2_PULL_START: Starting address of pull queue (8 B alignment).
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Pull Control/Status 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS2
Address	000000000006C221 (SCOM)
Description	OCB_OCI OCB Stream Pull Control/Status 2 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	OCB_OCI_OCBSLCS2_PULL_FULL: Reads indicate the pull queue is full condition Any write to this register clears this indicator and clears PULL_WRITE_PTR and PULL_READ_PTR to 0s. (this is a means for resetting the queue hardware) RWX_WCLRPART.
1	RWX_WSETPART	OCB_OCI_OCBSLCS2_PULL_EMPTY: Reads indicate the pull queue empty condition Any write to this register sets this indicator and clears PULL_WRITE_PTR and PULL_READ_PTR to 0s. (this is a means for resetting the queue hardware) RWX_WSETPART.
2:3	RW	OCB_OCI_OCBSLCS2_SPARE: Implemented but not used. Writes store the value. Reads return the last value written.
4:5	RW	OCB_OCI_OCBSLCS2_PULL_INTR_ACTION_0_1: Pull Interrupt Action This field controls the condition which will assert the pull interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware init) b01 = Non Full b10 = Empty (the more useful firmware default) b11 = Not Empty.
6:10	RW	OCB_OCI_OCBSLCS2_PULL_LENGTH: Pull queue length in (pull_length + 1) * 8 B Value mapping: 0b00000 = 8 B 0b00001 = 16 B 0b00010 = 24 B 0b00011 = 32 B 0b00100 = 40 B 0b00101 = 48 B 0b00110 = 56 B 0b00111 = 64 B 0b01000 = 72 B 0b01001 = 80 B 0b01010 = 88 B 0b01011 = 96 B 0b01100 = 104 B 0b01101 = 112 B 0b01110 = 120 B 0b01111 = 128 B 0b10000 = 136 B 0b10001 = 144 B 0b10010 = 152 B 0b10011 = 160 B 0b10100 = 168 B 0b10101 = 176 B 0b10110 = 184 B 0b10111 = 192 B 0b11000 = 200 B 0b11001 = 208 B 0b11010 = 216 B 0b11011 = 224 B 0b11100 = 232 B 0b11101 = 240 B 0b11110 = 248 B 0b11111 = 256 B
11:12	RO	constant = 0b00
13:17	RWX_WCLRPART	OCB_OCI_OCBSLCS2_PULL_WRITE_PTR: Pull write pointer Reads indicate the current pull queue write pointer in increments of 8 B. The actual address used is PULL_OCI_REGION || PULL_START + PULL_WRITE_PTR || 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register. ROX_WCLRPART.
18:20	RO	constant = 0b000
21:25	RWX_WCLRPART	OCB_OCI_OCBSLCS2_PULL_READ_PTR: Pull read pointer Reads indicate the current pull queue read pointer in increments of 8 B. The actual address used is PULL_OCI_REGION || PULL_START + PULL_WRITE_PTR || 00000. This field is cleared upon a write to this register. ROX_WCLRPART.
26:30	RO	constant = 0b00000

Bits	SCOM	Field Mnemonic: Description
31	RW	OCB_OCI_OCBSLCS2_PULL_ENABLE: Enables the Pull Queue Function. If disabled, PIB reads to the OCB Data [n] Register to perform a pull will result in an offline PIB error back to the PIB Master. **Note:** OCI reads to OCB Stream Pull Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full or empty conditions might still arise to the OCC even if this bit indicates disabled.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Pull Increment 2 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLI2
Address	000000000006C222 (SCOM)
Description	OCB_OCI OCB Stream Pull Increment 2 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Push Base 2 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR2
Address	000000000006C223 (SCOM)
Description	OCB_OCI OCB Stream Push Base 2 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBSHBR2_PUSH_OCI_REGION: Push OCI Region Allowed values: 10X - processor bus memory 111 - SRAM Others are reserved.
3:28	RW	OCB_OCI_OCBSHBR2_PUSH_START: Starting address of Push Queue (8 B alignment).
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Push Control/Status 2 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS2
Address	000000000006C224 (SCOM)
Description	OCB_OCI OCB Stream Push Control/Status 2 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	OCB_OCI_OCBSHCS2_PUSH_FULL: Reads indicate the push queue is full condition. Any write to this register clears this indicator and clears PUSH_WRITE_PTR and PUSH_READ_PTR to 0s. This is a means for resetting the queue hardware.
1	RWX_WSETPART	OCB_OCI_OCBSHCS2_PUSH_EMPTY: Read indicate the push queue empty condition. Any write to this register sets this indicator and clears PUSH_WRITE_PTR and PUSH_READ_PTR to 0s. This is a means for resetting the queue hardware.
2:3	RW	OCB_OCI_OCBSHCS2_SPARE: Implemented by not used. Writes store the value. Reads return the last value written.
4:5	RW	OCB_OCI_OCBSHCS2_PUSH_INTR_ACTION_0_1: Push Interrupt Action This field controls the condition which will assert the push interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware init) b01 = Non Full b10 = Empty b11 = Not Empty.

Bits	SCOM	Field Mnemonic: Description
6:10	RW	OCB_OCI_OCBSHCS2_PUSH_LENGTH: Push queue length in (PUSH_LENGTH + 1) * 8 B Value mapping: 0b00000 = 8 B 0b00001 = 16 B 0b00010 = 24 B 0b00011 = 32 B 0b00100 = 40 B 0b00101 = 48 B 0b00110 = 56 B 0b00111 = 64 B 0b01000 = 72 B 0b01001 = 80 B 0b01010 = 88 B 0b01011 = 96 B 0b01100 = 104 B 0b01101 = 112 B 0b01110 = 120 B 0b01111 = 128 B 0b10000 = 136 B 0b10001 = 144 B 0b10010 = 152 B 0b10011 = 160 B 0b10100 = 168 B 0b10101 = 176 B 0b10110 = 184 B 0b10111 = 192 B 0b11000 = 200 B 0b11001 = 208 B 0b11010 = 216 B 0b11011 = 224 B 0b11100 = 232 B 0b11101 = 240 B 0b11110 = 248 B 0b11111 = 256 B
11:12	RO	constant = 0b00
13:17	RWX_WCLRPART	OCB_OCI_OCBSHCS2_PUSH_WRITE_PTR: Push write pointer Reads indicate the current Push Queue write pointer in increments of 8 B. The actual address used is push_oci_region || push_start + push_write_ptr || 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register. ROX_WCLRPART.
18:20	RO	constant = 0b000
21:25	RWX_WCLRPART	OCB_OCI_OCBSHCS2_PUSH_READ_PTR: Push read pointer Reads indicate the current Push Queue read pointer in increments of 8 B. The actual address used is push_oci_region || push_start + push_read_ptr || 00000. This field is cleared upon a write to this register. ROX_WCLRPART.
26:30	RO	constant = 0b00000
31	RW	OCB_OCI_OCBSHCS2_PUSH_ENABLE: Enables the Push Queue function If Disabled, PIB Writes to OCB Data [n] Register to perform a push will result in an offline PIB error back to the PIB Master. **Note:** OCI Writes to OCB Stream Push Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full or empty conditions might still arise to the OCC even if this bit indicates disabled.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Push Increment 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHI2
Address	000000000006C225 (SCOM)
Description	OCB_OCI OCB Stream Push Increment 2 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Error Status 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES2
Address	000000000006C226 (SCOM)
Description	OCB_OCI OCB Stream Error Status 2 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	OCB_OCI_OCBSES2_PUSH_READ_UNDERFLOW: Push Queue Read Underflow. Underflow is defined as a store to the push_read_incr facility is done and the PUSH_EMPTY facility is already set. This bit is cleared only by a firmware write of this bit to 0.
1	RWX	OCB_OCI_OCBSES2_PULL_WRITE_OVERFLOW: Pull Queue Write Overflow. Overflow is defined as a load to the PULL_WRITE_INCR facility is done and the PULL_FULL facility is already set. This bit is cleared only by a firmware write of this bit to 0.
2:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Write Window Control 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR2
Address	000000000006C228 (SCOM)
Description	OCB_OCI OCB Linear Write Window Control 2 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_OCBLWCR2_LINEAR_WINDOW_ENABLE: Linear Window Enable 0: Window facility disabled. See Power Management Specification, section Indirect Bridge Operation for the effects of this bit for a write operation as it is dependent on the setting of trusted mode. 1: Window facility enabled. If OCBCSR[n]. OCB_STREAM_TYPE = linear, Linear Window BAR and Mask are valid and operations are to be honored. SC_RESP codes are the same as for the OCB indirect facility to reflect the status of the OCI operation.
1:2	RW	OCB_OCI_OCBLWCR2_SPARE_0: Implemented by not used. Writes store the value. Reads return the last value written.
3:19	RW	OCB_OCI_OCBLWCR2_LINEAR_WINDOW_BAR: Linear Window Base Address Register Defines OCI address(12:28) - 17 bits to define the starting offset within the region addressed.
20:31	RW	OCB_OCI_OCBLWCR2_LINEAR_WINDOW_MASK: Linear Window Address Mask Register Masks OCI address (17:28) - 12 bits to define the window size.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Write Window Status 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSR2
Address	000000000006C22A (SCOM)
Description	OCB_OCI OCB Linear Write Window Status 2 Register

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	OCB_OCI_OCBLWSR2_LINEAR_WINDOW_SCRESP: Linear Window PIB SC Response If OCBLWCR.linear_window_enable=1, this field contains the last PIB response code sent (potentially allowing OCC FW to tell if attempts were made to use the window.
3:7	RO	OCB_OCI_OCBLWSR2_SPARE0: Implemented but not used.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Window Write Base 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR2
Address	000000000006C22C (SCOM)
Description	OCB_OCI OCB Linear Window Write Base 2 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBLWSBR2_LINEAR_WINDOW_REGION: Linear Window Region If linear_window_enable=1, this field defines the OCI region (OCI Address(0:2) that is enabled for accessing the Linear Window. If the value written into OCBAR[n] does not match this value and the OCBDR[n] is accessed, a PIB scresp error is produced. Only the SRAM region (0b111) is supported.
3:9	RW	OCB_OCI_OCBLWSBR2_LINEAR_WINDOW_BASE: Linear Window Base If linear_window_enable = 1, establishes OCI Address(5:11); 128 B aliases still apply (for example, OCI Address[3:4]).
10:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Pull Base 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR3
Address	000000000006C230 (SCOM)
Description	OCB_OCI OCB Stream Pull Base 3 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBSLBR3_PULL_OCI_REGION: Pull OCI Region Allowed values: 10X = Processor bus memory 111=- SRAM Others are reserved
3:28	RW	OCB_OCI_OCBSLBR3_PULL_START: Starting address of pull queue. (8 B alignment).
29:63	RO	constant = 0b00000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Stream Pull Control/Status 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS3
Address	000000000006C231 (SCOM)
Description	OCB_OCI OCB Stream Pull Control/Status 3 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	OCB_OCI_OCBSLCS3_PULL_FULL: Reads indicate the pull queue is full condition. Any write to this register clears this indicator and clears PULL_WRITE_PTR and PULL_READ_PTR to 0s. (This is a means for resetting the queue hardware) RWX_WCLRPART.
1	RWX_WSETPART	OCB_OCI_OCBSLCS3_PULL_EMPTY: Reads indicate the pull queue empty condition Any write to this register sets this indicator and clears PULL_WRITE_PTR and PULL_READ_PTR to 0s. (This is a means for resetting the queue hardware) RWX_WSETPART.
2:3	RW	OCB_OCI_OCBSLCS3_SPARE: Implemented but not used writes store the value. Reads return the last value written.
4:5	RW	OCB_OCI_OCBSLCS3_PULL_INTR_ACTION_0_1: Pull Interrupt Action. This field controls the condition that will assert the pull interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware init) b01 = Nonfull b10 = Empty (the more useful firmware default) b11 = Not empty.
6:10	RW	OCB_OCI_OC BSLCS3_PULL_LENGTH: Pull queue length in (pull_length + 1) * 8 B value mapping: 0b00000: 8 B 0b00001: 16 B 0b00010: 24 B 0b00011: 32 B 0b00100: 40 B 0b00101: 48 B 0b00110: 56 B 0b00111: 64 B 0b01000: 72 B 0b01001: 80 B 0b01010: 88 B 0b01011: 96 B 0b01100: 104 B 0b01101: 112 B 0b01110: 120 B 0b01111: 128 B 0b10000: 136 B 0b10001: 144 B 0b10010: 152 B 0b10011: 160 B 0b10100: 168 B 0b10101: 176 B 0b10110: 184 B 0b10111: 192 B 0b11000: 200 B 0b11001: 208 B 0b11010: 216 B 0b11011: 224 B 0b11100: 232 B 0b11101: 240 B 0b11110: 248 B 0b11111: 256 B.
11:12	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
13:17	RWX_WCLRPART	OCB_OCI_OCBSLCS3_PULL_WRITE_PTR: Pull Write Pointer. Reads indicate the current pull queue write pointer in increments of 8 B. The actual address used is PULL_OCI_REGION || PULL_START + PULL_WRITE_PTR || 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register. ROX_WCLRPART.
18:20	RO	constant = 0b000
21:25	RWX_WCLRPART	OCB_OCI_OCBSLCS3_PULL_READ_PTR: Pull read pointer reads indicate the current pull queue read pointer in increments of 8 B. The actual address used is PULL_OCI_REGION || PULL_START + PULL_WRITE_PTR || 00000. This field is cleared upon a write to this register. ROX_WCLRPART.
26:30	RO	constant = 0b00000
31	RW	OCB_OCI_OCBSLCS3_PULL_ENABLE: Enables the Pull Queue Function. If disabled, PIB reads to the OCB Data [n] Register to perform a pull will result in an offline PIB error back to the PIB Master. **Note:** OCI reads to OCB Stream Pull Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full or empty conditions might still arise to the OCC even if this bit indicates disabled.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Pull Increment 3 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLI3
Address	000000000006C232 (SCOM)
Description	OCB_OCI OCB Stream Pull Increment 3 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Push Base 3 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR3
Address	000000000006C233 (SCOM)
Description	OCB_OCI OCB Stream Push Base 3 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBSHBR3_PUSH_OCI_REGION: Push OCI Region Allowed values: 10X - processor bus memory 111 - SRAM Others are reserved.
3:28	RW	OCB_OCI_OCBSHBR3_PUSH_START: Starting address of Push Queue (8 B alignment).
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Push Control/Status 3 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS3
Address	000000000006C234 (SCOM)
Description	OCB_OCI OCB Stream Push Control/Status 3 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	OCB_OCI_OCBSHCS3_PUSH_FULL: Reads indicate the push queue is full condition. Any write to this register clears this indicator and clears PUSH_WRITE_PTR and PUSH_READ_PTR to 0s. This is a means for resetting the queue hardware.

Bits	SCOM	Field Mnemonic: Description
1	RWX_WSETPART	OCB_OCI_OCBSHCS3_PUSH_EMPTY: Read indicate the push queue empty condition. Any write to this register sets this indicator and clears PUSH_WRITE_PTR and PUSH_READ_PTR to 0s. This is a means for resetting the queue hardware.
2:3	RW	OCB_OCI_OCBSHCS3_SPARE: Implemented by not used writes store the value. Reads return the last value written.
4:5	RW	OCB_OCI_OCBSHCS3_PUSH_INTR_ACTION_0_1: Push Interrupt Action. This field controls the condition that asserts the push interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware init) b01 = Nonfull b10 = Empty b11 = Not empty.
6:10	RW	OCB_OCI_OC BSHCS3_PUSH_LENGTH: Push Queue length in (PUSH_LENGTH + 1) * 8 B Value mapping: 0b00000 = 8 B 0b00001 = 16 B 0b00010 = 24 B 0b00011 = 32 B 0b00100 = 40 B 0b00101 = 48 B 0b00110 = 56 B 0b00111 = 64 B 0b01000 = 72 B 0b01001 = 80 B 0b01010 = 88 B 0b01011 = 96 B 0b01100 = 104 B 0b01101 = 112 B 0b01110 = 120 B 0b01111 = 128 B 0b10000 = 136 B 0b10001 = 144 B 0b10010 = 152 B 0b10011 = 160 B 0b10100 = 168 B 0b10101 = 176 B 0b10110 = 184 B 0b10111 = 192 B 0b11000 = 200 B 0b11001 = 208 B 0b11010 = 216 B 0b11011 = 224 B 0b11100 = 232 B 0b11101 = 240 B 0b11110 = 248 B 0b11111 = 256 B.
11:12	RO	constant = 0b00
13:17	RWX_WCLRPART	OCB_OCI_OCBSHCS3_PUSH_WRITE_PTR: Push write pointer. Reads indicate the current push queue write pointer in increments of 8 B. The actual address used is PUSH_OCI_REGION || PUSH_START + PUSH_WRITE_PTR || 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register. ROX_WCLRPART.
18:20	RO	constant = 0b000
21:25	RWX_WCLRPART	OCB_OCI_OCBSHCS3_PUSH_READ_PTR: Push read pointer reads indicate the current push queue read pointer in increments of 8 B. The actual address used is PUSH_OCI_REGION || PUSH_START + PUSH_READ_PTR || 00000. This field is cleared upon a write to this register. ROX_WCLRPART.
26:30	RO	constant = 0b00000

Bits	SCOM	Field Mnemonic: Description
31	RW	OCB_OCI_OCBSHCS3_PUSH_ENABLE: Enables the push queue function. If disabled, PIB writes to OCB Data [n] Register to perform a push results in an offline PIB error back to the PIB master. **Note:** OCI writes to OCB Stream Push Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full or empty conditions might still arise to the OCC even if this bit indicates disabled.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Push Increment 3 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHI3
Address	000000000006C235 (SCOM)
Description	OCB_OCI OCB Stream Push Increment 3 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	**OCB_OCI OCB Stream Error Status 3 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES3
Address	000000000006C236 (SCOM)
Description	OCB_OCI OCB Stream Error Status 3 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	OCB_OCI_OCBSES3_PUSH_READ_UNDERFLOW: Push Queue Read Underflow. Underflow is defined as a store to the PUSH_READ_INCR facility is done and the PUSH_EMPTY facility is already set. This bit is cleared only by a firmware write of this bit to 0.
1	RWX	OCB_OCI_OCBSES3_PULL_WRITE_OVERFLOW: Pull Queue Write Overflow. Overflow is defined as a load to the PULL_WRITE_INCR facility is done and the PULL_FULL facility is already set. This bit is cleared only by a firmware write of this bit to 0.
2:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	**OCB_OCI OCB Linear Write Window Control 3 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR3
Address	000000000006C238 (SCOM)
Description	OCB_OCI OCB Linear Write Window Control 3 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_OCBLWCR3_LINEAR_WINDOW_ENABLE: Linear Window Enable 0 = Window facility disabled. See the Power Management Specification, section Indirect Bridge Operation for the effects of this bit for a write operation as it is dependent on the setting of trusted mode. 1 = Window facility enabled. If OCBCSR[n], OCB_STREAM_TYPE = linear. Linear window bar and mask are valid and operations are to be honored. SC_RESP codes are the same as for the OCB indirect facility to reflect the status of the OCI operation.
1:2	RW	OCB_OCI_OCBLWCR3_SPARE_0: Implemented by not used writes store the value. Reads return the last value written.
3:19	RW	OCB_OCI_OCBLWCR3_LINEAR_WINDOW_BAR: Linear Window Base Address Register. Defines OCI address(12:28) 17 bits to define the starting offset within the region addressed.

Bits	SCOM	Field Mnemonic: Description
20:31	RW	OCB_OCI_OCBLWCR3_LINEAR_WINDOW_MASK: Linear Window Address Mask Register. Masks OCI address (17:28), 12 bits to define the window size.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Write Window Status 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSR3
Address	000000000006C23A (SCOM)
Description	OCB_OCI OCB Linear Write Window Status 3 Register

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	OCB_OCI_OCBLWSR3_LINEAR_WINDOW_SCRESP: Linear Window PIB SC Response. If OCBLWCR.linear_window_enable = 1, this field contains the last PIB response code sent (potentially allowing OCC FW to tell if attempts were made to use the window).
3:7	RO	OCB_OCI_OCBLWSR3_SPARE0: Implemented but not used.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCB Linear Window Write Base 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR3
Address	000000000006C23C (SCOM)
Description	OCB_OCI OCB Linear Window Write Base 3 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_OCI_OCBLWSBR3_LINEAR_WINDOW_REGION: Linear Window Region. If linear_window_enable = 1, this field defines the OCI region (OCI Address(0:2) that is enabled for accessing the linear window. If the value written into OCBAR[n] does not match this value and the OCBDR[n] is accessed, a PIB scresp error is produced. Only the SRAM region (0b111) is supported.
3:9	RW	OCB_OCI_OCBLWSBR3_LINEAR_WINDOW_BASE: Linear Window Base. If linear_window_enable = 1, establishes OCI Address(5:11). 128 B aliases still apply (for example, OCI Address[3:4]).
10:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C0
Address	000000000006C400 (SCOM) 000000000006C500 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 0 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C0_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C1
Address	000000000006C401 (SCOM) 000000000006C501 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 1 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C1_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C2
Address	000000000006C402 (SCOM) 000000000006C502 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 2 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C2_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C3
Address	000000000006C403 (SCOM) 000000000006C503 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 3 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C3_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 4 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C4
Address	000000000006C404 (SCOM) 000000000006C504 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 4 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C4_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 5 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C5
Address	000000000006C405 (SCOM) 000000000006C505 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 5 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C5_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 6 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C6
Address	000000000006C406 (SCOM) 000000000006C506 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 6 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C6_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 7 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C7
Address	000000000006C407 (SCOM) 000000000006C507 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 7 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C7_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 8 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C8
Address	000000000006C408 (SCOM) 000000000006C508 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 8 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C8_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 9 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C9
Address	000000000006C409 (SCOM) 000000000006C509 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 9 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C9_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 10 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C10
Address	000000000006C40A (SCOM) 000000000006C50A (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 10 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C10_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 11 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C11
Address	000000000006C40B (SCOM) 000000000006C50B (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 11 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C11_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 12 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C12
Address	000000000006C40C (SCOM) 000000000006C50C (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 12 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C12_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 13 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C13
Address	000000000006C40D (SCOM) 000000000006C50D (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 13 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C13_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 14 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C14
Address	000000000006C40E (SCOM) 000000000006C50E (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 14 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C14_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 15 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C15
Address	000000000006C40F (SCOM) 000000000006C50F (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 15 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C15_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 16 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C16
Address	000000000006C410 (SCOM) 000000000006C510 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 16 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C16_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 17 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C17
Address	000000000006C411 (SCOM) 000000000006C511 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 17 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C17_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 18 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C18
Address	000000000006C412 (SCOM) 000000000006C512 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 18 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C18_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 19 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C19
Address	000000000006C413 (SCOM) 000000000006C513 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 19 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C19_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 20 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C20
Address	000000000006C414 (SCOM) 000000000006C514 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 20 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C20_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 21 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C21
Address	000000000006C415 (SCOM) 000000000006C515 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 21 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C21_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 22 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C22
Address	000000000006C416 (SCOM) 000000000006C516 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 22 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C22_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 0 Core 23 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0C23
Address	000000000006C417 (SCOM) 000000000006C517 (SCOM1)
Description	OCC PCB Interrupt Type 0 Core 23 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT0C23_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C0
Address	000000000006C420 (SCOM) 000000000006C520 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 0 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C0_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C1
Address	000000000006C421 (SCOM) 000000000006C521 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 1 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C1_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C2
Address	000000000006C422 (SCOM) 000000000006C522 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 2 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C2_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C3
Address	000000000006C423 (SCOM) 000000000006C523 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 3 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C3_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 4 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C4
Address	000000000006C424 (SCOM) 000000000006C524 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 4 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C4_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 5 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C5
Address	000000000006C425 (SCOM) 000000000006C525 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 5 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C5_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 6 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C6
Address	000000000006C426 (SCOM) 000000000006C526 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 6 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C6_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 7 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C7
Address	000000000006C427 (SCOM) 000000000006C527 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 7 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C7_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 8 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C8
Address	000000000006C428 (SCOM) 000000000006C528 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 8 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C8_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 9 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C9
Address	000000000006C429 (SCOM) 000000000006C529 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 9 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C9_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 10 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C10
Address	000000000006C42A (SCOM) 000000000006C52A (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 10 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C10_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 11 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C11
Address	000000000006C42B (SCOM) 000000000006C52B (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 11 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C11_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 12 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C12
Address	000000000006C42C (SCOM) 000000000006C52C (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 12 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C12_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 13 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C13
Address	000000000006C42D (SCOM) 000000000006C52D (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 13 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C13_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 14 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C14
Address	000000000006C42E (SCOM) 000000000006C52E (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 14 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C14_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 15 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C15
Address	000000000006C42F (SCOM) 000000000006C52F (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 15 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C15_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 16 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C16
Address	000000000006C430 (SCOM) 000000000006C530 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 16 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C16_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 17 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C17
Address	000000000006C431 (SCOM) 000000000006C531 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 17 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C17_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 18 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C18
Address	000000000006C432 (SCOM) 000000000006C532 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 18 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C18_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 19 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C19
Address	000000000006C433 (SCOM) 000000000006C533 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 19 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C19_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 20 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C20
Address	000000000006C434 (SCOM) 000000000006C534 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 20 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C20_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 21 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C21
Address	000000000006C435 (SCOM) 000000000006C535 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 21 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C21_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 22 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C22
Address	000000000006C436 (SCOM) 000000000006C536 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 22 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C22_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 1 Core 23 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1C23
Address	000000000006C437 (SCOM) 000000000006C537 (SCOM1)
Description	OCC PCB Interrupt Type 1 Core 23 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT1C23_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C0
Address	000000000006C440 (SCOM) 000000000006C540 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 0 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C0_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C1
Address	000000000006C441 (SCOM) 000000000006C541 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 1 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C1_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C2
Address	000000000006C442 (SCOM) 000000000006C542 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 2 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C2_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C3
Address	000000000006C443 (SCOM) 000000000006C543 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 3 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C3_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 4 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C4
Address	000000000006C444 (SCOM) 000000000006C544 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 4 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C4_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 5 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C5
Address	000000000006C445 (SCOM) 000000000006C545 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 5 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C5_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 6 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C6
Address	000000000006C446 (SCOM) 000000000006C546 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 6 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C6_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 7 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C7
Address	000000000006C447 (SCOM) 000000000006C547 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 7 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C7_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 8 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C8
Address	000000000006C448 (SCOM) 000000000006C548 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 8 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C8_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 9 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C9
Address	000000000006C449 (SCOM) 000000000006C549 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 9 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C9_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 10 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C10
Address	000000000006C44A (SCOM) 000000000006C54A (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 10 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C10_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 11 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C11
Address	000000000006C44B (SCOM) 000000000006C54B (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 11 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C11_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 12 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C12
Address	000000000006C44C (SCOM) 000000000006C54C (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 12 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C12_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 13 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C13
Address	000000000006C44D (SCOM) 000000000006C54D (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 13 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C13_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 14 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C14
Address	000000000006C44E (SCOM) 000000000006C54E (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 14 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C14_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 15 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C15
Address	000000000006C44F (SCOM) 000000000006C54F (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 15 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C15_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 16 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C16
Address	000000000006C450 (SCOM) 000000000006C550 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 16 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C16_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 17 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C17
Address	000000000006C451 (SCOM) 000000000006C551 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 17 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C17_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 18 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C18
Address	000000000006C452 (SCOM) 000000000006C552 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 18 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C18_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 19 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C19
Address	000000000006C453 (SCOM) 000000000006C553 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 19 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C19_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 20 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C20
Address	000000000006C454 (SCOM) 000000000006C554 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 20 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C20_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 21 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C21
Address	000000000006C455 (SCOM) 000000000006C555 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 21 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C21_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 22 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C22
Address	000000000006C456 (SCOM) 000000000006C556 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 22 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C22_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 2 Core 23 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2C23
Address	000000000006C457 (SCOM) 000000000006C557 (SCOM1)
Description	OCC PCB Interrupt Type 2 Core 23 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT2C23_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C0
Address	000000000006C460 (SCOM) 000000000006C560 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 0 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C0_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C1
Address	000000000006C461 (SCOM) 000000000006C561 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 1 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C1_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C2
Address	000000000006C462 (SCOM) 000000000006C562 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 2 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C2_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C3
Address	000000000006C463 (SCOM) 000000000006C563 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 3 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C3_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 4 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C4
Address	000000000006C464 (SCOM) 000000000006C564 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 4 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C4_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 5 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C5
Address	000000000006C465 (SCOM) 000000000006C565 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 5 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C5_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 6 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C6
Address	000000000006C466 (SCOM) 000000000006C566 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 6 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C6_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 7 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C7
Address	000000000006C467 (SCOM) 000000000006C567 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 7 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C7_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 8 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C8
Address	000000000006C468 (SCOM) 000000000006C568 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 8 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C8_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 9 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C9
Address	000000000006C469 (SCOM) 000000000006C569 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 9 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C9_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 10 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C10
Address	000000000006C46A (SCOM) 000000000006C56A (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 10 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C10_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 11 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C11
Address	000000000006C46B (SCOM) 000000000006C56B (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 11 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C11_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 12 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C12
Address	000000000006C46C (SCOM) 000000000006C56C (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 12 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C12_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 13 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C13
Address	000000000006C46D (SCOM) 000000000006C56D (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 13 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C13_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 14 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C14
Address	000000000006C46E (SCOM) 000000000006C56E (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 14 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C14_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 15 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C15
Address	000000000006C46F (SCOM) 000000000006C56F (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 15 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C15_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 16 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C16
Address	000000000006C470 (SCOM) 000000000006C570 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 16 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C16_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 17 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C17
Address	000000000006C471 (SCOM) 000000000006C571 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 17 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C17_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 18 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C18
Address	000000000006C472 (SCOM) 000000000006C572 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 18 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C18_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 19 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C19
Address	000000000006C473 (SCOM) 000000000006C573 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 19 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C19_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 20 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C20
Address	000000000006C474 (SCOM) 000000000006C574 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 20 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C20_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 21 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C21
Address	000000000006C475 (SCOM) 000000000006C575 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 21 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C21_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 22 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C22
Address	000000000006C476 (SCOM) 000000000006C576 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 22 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C22_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 3 Core 23 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3C23
Address	000000000006C477 (SCOM) 000000000006C577 (SCOM1)
Description	OCC PCB Interrupt Type 3 Core 23 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT3C23_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C0
Address	000000000006C480 (SCOM) 000000000006C580 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 0 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C0_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C1
Address	000000000006C481 (SCOM) 000000000006C581 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 1 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C1_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C2
Address	000000000006C482 (SCOM) 000000000006C582 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 2 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C2_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C3
Address	000000000006C483 (SCOM) 000000000006C583 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 3 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C3_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 4 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C4
Address	000000000006C484 (SCOM) 000000000006C584 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 4 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C4_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 5 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C5
Address	000000000006C485 (SCOM) 000000000006C585 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 5 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C5_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 6 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C6
Address	000000000006C486 (SCOM) 000000000006C586 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 6 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C6_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 7 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C7
Address	000000000006C487 (SCOM) 000000000006C587 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 7 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C7_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 8 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C8
Address	000000000006C488 (SCOM) 000000000006C588 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 8 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C8_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 9 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C9
Address	000000000006C489 (SCOM) 000000000006C589 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 9 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C9_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 10 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C10
Address	000000000006C48A (SCOM) 000000000006C58A (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 10 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C10_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 11 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C11
Address	000000000006C48B (SCOM) 000000000006C58B (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 11 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C11_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 12 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C12
Address	000000000006C48C (SCOM) 000000000006C58C (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 12 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C12_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 13 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C13
Address	000000000006C48D (SCOM) 000000000006C58D (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 13 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C13_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 14 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C14
Address	000000000006C48E (SCOM) 000000000006C58E (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 14 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C14_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 15 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C15
Address	000000000006C48F (SCOM) 000000000006C58F (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 15 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C15_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 16 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C16
Address	000000000006C490 (SCOM) 000000000006C590 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 16 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C16_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 17 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C17
Address	000000000006C491 (SCOM) 000000000006C591 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 17 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C17_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 18 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C18
Address	000000000006C492 (SCOM) 000000000006C592 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 18 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C18_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 19 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C19
Address	000000000006C493 (SCOM) 000000000006C593 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 19 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C19_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 20 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C20
Address	000000000006C494 (SCOM) 000000000006C594 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 20 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C20_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 21 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C21
Address	000000000006C495 (SCOM) 000000000006C595 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 21 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C21_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 22 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C22
Address	000000000006C496 (SCOM) 000000000006C596 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 22 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C22_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 4 Core 23 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4C23
Address	000000000006C497 (SCOM) 000000000006C597 (SCOM1)
Description	OCC PCB Interrupt Type 4 Core 23 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT4C23_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C0
Address	000000000006C4A0 (SCOM) 000000000006C5A0 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 0 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C0_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C1
Address	000000000006C4A1 (SCOM) 000000000006C5A1 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 1 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C1_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C2
Address	000000000006C4A2 (SCOM) 000000000006C5A2 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 2 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C2_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C3
Address	000000000006C4A3 (SCOM) 000000000006C5A3 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 3 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C3_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 4 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C4
Address	000000000006C4A4 (SCOM) 000000000006C5A4 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 4 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C4_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 5 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C5
Address	000000000006C4A5 (SCOM) 000000000006C5A5 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 5 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C5_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 6 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C6
Address	000000000006C4A6 (SCOM) 000000000006C5A6 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 6 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C6_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 7 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C7
Address	000000000006C4A7 (SCOM) 000000000006C5A7 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 7 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C7_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 8 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C8
Address	000000000006C4A8 (SCOM) 000000000006C5A8 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 8 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C8_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 9 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C9
Address	000000000006C4A9 (SCOM) 000000000006C5A9 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 9 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C9_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 10 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C10
Address	000000000006C4AA (SCOM) 000000000006C5AA (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 10 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C10_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 11 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C11
Address	000000000006C4AB (SCOM) 000000000006C5AB (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 11 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C11_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 12 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C12
Address	000000000006C4AC (SCOM) 000000000006C5AC (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 12 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C12_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 13 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C13
Address	000000000006C4AD (SCOM) 000000000006C5AD (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 13 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C13_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 14 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C14
Address	000000000006C4AE (SCOM) 000000000006C5AE (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 14 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C14_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 15 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C15
Address	000000000006C4AF (SCOM) 000000000006C5AF (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 15 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C15_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 16 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C16
Address	000000000006C4B0 (SCOM) 000000000006C5B0 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 16 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C16_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 17 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C17
Address	000000000006C4B1 (SCOM) 000000000006C5B1 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 17 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C17_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 18 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C18
Address	000000000006C4B2 (SCOM) 000000000006C5B2 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 18 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C18_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 19 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C19
Address	000000000006C4B3 (SCOM) 000000000006C5B3 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 19 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C19_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 20 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C20
Address	000000000006C4B4 (SCOM) 000000000006C5B4 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 20 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C20_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 21 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C21
Address	000000000006C4B5 (SCOM) 000000000006C5B5 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 21 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C21_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 22 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C22
Address	000000000006C4B6 (SCOM) 000000000006C5B6 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 22 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C22_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC PCB Interrupt Type 5 Core 23 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5C23
Address	000000000006C4B7 (SCOM) 000000000006C5B7 (SCOM1)
Description	OCC PCB Interrupt Type 5 Core 23 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:19	RO	RO	constant = 0b00000000000000000000
20:31	ROX	ROX	OCB_OCI_OPIT5C23_PCB_INTR_TYPE_A_CORE_N: Type [a] PCB interrupt packet content from core [n].
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 6 Quad 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT6Q0
Address	000000000006C4C0 (SCOM) 000000000006C5C0 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 6 Quad 0 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT6Q0_PCB_INTR_TYPE_A_QUAD_N: Type 6 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_OCI OCC PCB Interrupt Type 6 Quad 1 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT6Q1
Address	000000000006C4C1 (SCOM) 000000000006C5C1 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 6 Quad 1 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT6Q1_PCB_INTR_TYPE_A_QUAD_N: Type 6 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_OCI OCC PCB Interrupt Type 6 Quad 2 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT6Q2
Address	000000000006C4C2 (SCOM) 000000000006C5C2 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 6 Quad 2 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT6Q2_PCB_INTR_TYPE_A_QUAD_N: Type 6 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_OCI OCC PCB Interrupt Type 6 Quad 3 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT6Q3
Address	000000000006C4C3 (SCOM) 000000000006C5C3 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 6 Quad 3 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT6Q3_PCB_INTR_TYPE_A_QUAD_N: Type 6 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 6 Quad 4 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT6Q4
Address	000000000006C4C4 (SCOM) 000000000006C5C4 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 6 Quad 4 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT6Q4_PCB_INTR_TYPE_A_QUAD_N: Type 6 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 6 Quad 5 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT6Q5
Address	000000000006C4C5 (SCOM) 000000000006C5C5 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 6 Quad 5 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT6Q5_PCB_INTR_TYPE_A_QUAD_N: Type 6 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type Quad 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT7Q0
Address	000000000006C4E0 (SCOM) 000000000006C5E0 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type Quad 0 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT7Q0_PCB_INTR_TYPE_A_QUAD_N: Type 7 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type Quad 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT7Q1
Address	000000000006C4E1 (SCOM) 000000000006C5E1 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type Quad 1 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT7Q1_PCB_INTR_TYPE_A_QUAD_N: Type 7 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type Quad 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT7Q2
Address	000000000006C4E2 (SCOM) 000000000006C5E2 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type Quad 2 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT7Q2_PCB_INTR_TYPE_A_QUAD_N: Type 7 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type Quad 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT7Q3
Address	000000000006C4E3 (SCOM) 000000000006C5E3 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type Quad 3 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT7Q3_PCB_INTR_TYPE_A_QUAD_N: Type 7 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type Quad 4 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT7Q4
Address	000000000006C4E4 (SCOM) 000000000006C5E4 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type Quad 4 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT7Q4_PCB_INTR_TYPE_A_QUAD_N: Type 7 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type Quad 5 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT7Q5
Address	000000000006C4E5 (SCOM) 000000000006C5E5 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type Quad 5 Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0:27	RO	RO	constant = 0b00000000000000000000000000000
28:31	ROX	ROX	OCB_OCI_OPIT7Q5_PCB_INTR_TYPE_A_QUAD_N: Type 7 PCB interrupt packet content from quad [n]. **Note:** Unlike the core types, only four bits are implemented.
32:63	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 0 Pending Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT0PRA
Address	000000000006C600 (SCOM) 000000000006C601 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 0 Pending Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_0: PCB interrupt type [n] pending: core 0.
1	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_1: PCB interrupt type [n] pending: core 1.
2	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_2: PCB interrupt type [n] pending: core 2.
3	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_3: PCB interrupt type [n] pending: core 3.
4	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_4: PCB interrupt type [n] pending: core 4.
5	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_5: PCB interrupt type [n] pending: core 5.
6	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_6: PCB interrupt type [n] pending: core 6.
7	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_7: PCB interrupt type [n] pending: core 7.
8	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_8: PCB interrupt type [n] pending: core 8.
9	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_9: PCB interrupt type [n] pending: core 9.
10	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_10: PCB interrupt type [n] pending: core 10.
11	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_11: PCB interrupt type [n] pending: core 11.
12	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_12: PCB interrupt type [n] pending: core 12.
13	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_13: PCB interrupt type [n] pending: core 13.

Bits	SCOM	SCOM1	Field Mnemonic: Description
14	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_14: PCB interrupt type [n] pending: core 14.
15	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_15: PCB interrupt type [n] pending: core 15.
16	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_16: PCB interrupt type [n] pending: core 16.
17	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_17: PCB interrupt type [n] pending: core 17.
18	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_18: PCB interrupt type [n] pending: core 18.
19	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_19: PCB interrupt type [n] pending: core 19.
20	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_20: PCB interrupt type [n] pending: core 20.
21	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_21: PCB interrupt type [n] pending: core 21.
22	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_22: PCB interrupt type [n] pending: core 22.
23	ROX	WOX_CLEAR	OCB_OCI_OPIT0PRA_PCB_INTR_TYPE_N_PENDING_23: PCB interrupt type [n] pending: core 23.
24:63	RO	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 1 Pending Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT1PRA
Address	000000000006C620 (SCOM) 000000000006C621 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 1 Pending Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_0: PCB interrupt type [n] pending: core 0.
1	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_1: PCB interrupt type [n] pending: core 1.
2	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_2: PCB interrupt type [n] pending: core 2.
3	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_3: PCB interrupt type [n] pending: core 3.
4	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_4: PCB interrupt type [n] pending: core 4.
5	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_5: PCB interrupt type [n] pending: core 5.
6	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_6: PCB interrupt type [n] pending: core 6.
7	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_7: PCB interrupt type [n] pending: core 7.

Bits	SCOM	SCOM1	Field Mnemonic: Description
8	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_8: PCB interrupt type [n] pending: core 8.
9	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_9: PCB interrupt type [n] pending: core 9.
10	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_10: PCB interrupt type [n] pending: core 10.
11	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_11: PCB interrupt type [n] pending: core 11.
12	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_12: PCB interrupt type [n] pending: core 12.
13	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_13: PCB interrupt type [n] pending: core 13.
14	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_14: PCB interrupt type [n] pending: core 14.
15	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_15: PCB interrupt type [n] pending: core 15.
16	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_16: PCB interrupt type [n] pending: core 16.
17	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_17: PCB interrupt type [n] pending: core 17.
18	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_18: PCB interrupt type [n] pending: core 18.
19	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_19: PCB interrupt type [n] pending: core 19.
20	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_20: PCB interrupt type [n] pending: core 20.
21	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_21: PCB interrupt type [n] pending: core 21.
22	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_22: PCB interrupt type [n] pending: core 22.
23	ROX	WOX_CLEAR	OCB_OCI_OPIT1PRA_PCB_INTR_TYPE_N_PENDING_23: PCB interrupt type [n] pending: core 23.
24:63	RO	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 2 Pending Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT2PRA
Address	000000000006C640 (SCOM) 000000000006C641 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 2 Pending Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_0: PCB interrupt type [n] pending: core 0.
1	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_1: PCB interrupt type [n] pending: core 1.

Bits	SCOM	SCOM1	Field Mnemonic: Description
2	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_2: PCB interrupt type [n] pending: core 2.
3	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_3: PCB interrupt type [n] pending: core 3.
4	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_4: PCB interrupt type [n] pending: core 4.
5	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_5: PCB interrupt type [n] pending: core 5.
6	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_6: PCB interrupt type [n] pending: core 6.
7	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_7: PCB interrupt type [n] pending: core 7.
8	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_8: PCB interrupt type [n] pending: core 8.
9	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_9: PCB interrupt type [n] pending: core 9.
10	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_10: PCB interrupt type [n] pending: core 10.
11	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_11: PCB interrupt type [n] pending: core 11.
12	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_12: PCB interrupt type [n] pending: core 12.
13	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_13: PCB interrupt type [n] pending: core 13.
14	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_14: PCB interrupt type [n] pending: core 14.
15	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_15: PCB interrupt type [n] pending: core 15.
16	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_16: PCB interrupt type [n] pending: core 16.
17	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_17: PCB interrupt type [n] pending: core 17.
18	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_18: PCB interrupt type [n] pending: core 18.
19	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_19: PCB interrupt type [n] pending: core 19.
20	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_20: PCB interrupt type [n] pending: core 20.
21	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_21: PCB interrupt type [n] pending: core 21.
22	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_22: PCB interrupt type [n] pending: core 22.
23	ROX	WOX_CLEAR	OCB_OCI_OPIT2PRA_PCB_INTR_TYPE_N_PENDING_23: PCB interrupt type [n] pending: core 23.
24:63	RO	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 3 Pending Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT3PRA
Address	000000000006C660 (SCOM) 000000000006C661 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 3 Pending Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_0: PCB interrupt type [n] pending: core 0.
1	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_1: PCB interrupt type [n] pending: core 1.
2	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_2: PCB interrupt type [n] pending: core 2.
3	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_3: PCB interrupt type [n] pending: core 3.
4	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_4: PCB interrupt type [n] pending: core 4.
5	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_5: PCB interrupt type [n] pending: core 5.
6	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_6: PCB interrupt type [n] pending: core 6.
7	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_7: PCB interrupt type [n] pending: core 7.
8	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_8: PCB interrupt type [n] pending: core 8.
9	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_9: PCB interrupt type [n] pending: core 9.
10	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_10: PCB interrupt type [n] pending: core 10.
11	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_11: PCB interrupt type [n] pending: core 11.
12	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_12: PCB interrupt type [n] pending: core 12.
13	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_13: PCB interrupt type [n] pending: core 13.
14	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_14: PCB interrupt type [n] pending: core 14.
15	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_15: PCB interrupt type [n] pending: core 15.
16	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_16: PCB interrupt type [n] pending: core 16.
17	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_17: PCB interrupt type [n] pending: core 17.
18	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_18: PCB interrupt type [n] pending: core 18.
19	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_19: PCB interrupt type [n] pending: core 19.

Bits	SCOM	SCOM1	Field Mnemonic: Description
20	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_20: PCB interrupt type [n] pending: core 20.
21	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_21: PCB interrupt type [n] pending: core 21.
22	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_22: PCB interrupt type [n] pending: core 22.
23	ROX	WOX_CLEAR	OCB_OCI_OPIT3PRA_PCB_INTR_TYPE_N_PENDING_23: PCB interrupt type [n] pending: core 23.
24:63	RO	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 4 Pending Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT4PRA
Address	000000000006C680 (SCOM) 000000000006C681 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 4 Pending Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_0: PCB interrupt type [n] pending: core 0.
1	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_1: PCB interrupt type [n] pending: core 1.
2	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_2: PCB interrupt type [n] pending: core 2.
3	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_3: PCB interrupt type [n] pending: core 3.
4	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_4: PCB interrupt type [n] pending: core 4.
5	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_5: PCB interrupt type [n] pending: core 5.
6	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_6: PCB interrupt type [n] pending: core 6.
7	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_7: PCB interrupt type [n] pending: core 7.
8	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_8: PCB interrupt type [n] pending: core 8.
9	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_9: PCB interrupt type [n] pending: core 9.
10	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_10: PCB interrupt type [n] pending: core 10.
11	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_11: PCB interrupt type [n] pending: core 11.
12	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_12: PCB interrupt type [n] pending: core 12.
13	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_13: PCB interrupt type [n] pending: core 13.

Bits	SCOM	SCOM1	Field Mnemonic: Description
14	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_14: PCB interrupt type [n] pending: core 14.
15	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_15: PCB interrupt type [n] pending: core 15.
16	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_16: PCB interrupt type [n] pending: core 16.
17	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_17: PCB interrupt type [n] pending: core 17.
18	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_18: PCB interrupt type [n] pending: core 18.
19	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_19: PCB interrupt type [n] pending: core 19.
20	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_20: PCB interrupt type [n] pending: core 20.
21	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_21: PCB interrupt type [n] pending: core 21.
22	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_22: PCB interrupt type [n] pending: core 22.
23	ROX	WOX_CLEAR	OCB_OCI_OPIT4PRA_PCB_INTR_TYPE_N_PENDING_23: PCB interrupt type [n] pending: core 23.
24:63	RO	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 5 Pending Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT5PRA
Address	000000000006C6A0 (SCOM) 000000000006C6A1 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 5 Pending Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_0: PCB interrupt type [n] pending: core 0.
1	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_1: PCB interrupt type [n] pending: core 1.
2	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_2: PCB interrupt type [n] pending: core 2.
3	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_3: PCB interrupt type [n] pending: core 3.
4	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_4: PCB interrupt type [n] pending: core 4.
5	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_5: PCB interrupt type [n] pending: core 5.
6	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_6: PCB interrupt type [n] pending: core 6.
7	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_7: PCB interrupt type [n] pending: core 7.

Bits	SCOM	SCOM1	Field Mnemonic: Description
8	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_8: PCB interrupt type [n] pending: core 8.
9	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_9: PCB interrupt type [n] pending: core 9.
10	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_10: PCB interrupt type [n] pending: core 10.
11	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_11: PCB interrupt type [n] pending: core 11.
12	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_12: PCB interrupt type [n] pending: core 12.
13	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_13: PCB interrupt type [n] pending: core 13.
14	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_14: PCB interrupt type [n] pending: core 14.
15	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_15: PCB interrupt type [n] pending: core 15.
16	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_16: PCB interrupt type [n] pending: core 16.
17	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_17: PCB interrupt type [n] pending: core 17.
18	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_18: PCB interrupt type [n] pending: core 18.
19	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_19: PCB interrupt type [n] pending: core 19.
20	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_20: PCB interrupt type [n] pending: core 20.
21	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_21: PCB interrupt type [n] pending: core 21.
22	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_22: PCB interrupt type [n] pending: core 22.
23	ROX	WOX_CLEAR	OCB_OCI_OPIT5PRA_PCB_INTR_TYPE_N_PENDING_23: PCB interrupt type [n] pending: core 23.
24:63	RO	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 6 Pending Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT6PRB
Address	000000000006C6C0 (SCOM) 000000000006C6C1 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 6 Pending Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	ROX	WOX_CLEAR	OCB_OCI_OPIT6PRB_PCB_INTR_TYPE_N_PENDING_0: PCB interrupt type [n] pending: quad 0.
1	ROX	WOX_CLEAR	OCB_OCI_OPIT6PRB_PCB_INTR_TYPE_N_PENDING_1: PCB interrupt type [n] pending: quad 1.

Bits	SCOM	SCOM1	Field Mnemonic: Description
2	ROX	WOX_CLEAR	OCB_OCI_OPIT6PRB_PCB_INTR_TYPE_N_PENDING_2: PCB interrupt type [n] pending: quad 2.
3	ROX	WOX_CLEAR	OCB_OCI_OPIT6PRB_PCB_INTR_TYPE_N_PENDING_3: PCB interrupt type [n] pending: quad 3.
4	ROX	WOX_CLEAR	OCB_OCI_OPIT6PRB_PCB_INTR_TYPE_N_PENDING_4: PCB interrupt type [n] pending: quad 4.
5	ROX	WOX_CLEAR	OCB_OCI_OPIT6PRB_PCB_INTR_TYPE_N_PENDING_5: PCB interrupt type [n] pending: quad 5.
6:63	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCB_OCI OCC PCB Interrupt Type 7 Pending Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_OPIT7PRB
Address	000000000006C6E0 (SCOM) 000000000006C6E1 (SCOM1)
Description	OCB_OCI OCC PCB Interrupt Type 7 Pending Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	ROX	WOX_CLEAR	OCB_OCI_OPIT7PRB_PCB_INTR_TYPE_N_PENDING_0: PCB interrupt type [n] pending: quad 0.
1	ROX	WOX_CLEAR	OCB_OCI_OPIT7PRB_PCB_INTR_TYPE_N_PENDING_1: PCB interrupt type [n] pending: quad 1.
2	ROX	WOX_CLEAR	OCB_OCI_OPIT7PRB_PCB_INTR_TYPE_N_PENDING_2: PCB interrupt type [n] pending: quad 2.
3	ROX	WOX_CLEAR	OCB_OCI_OPIT7PRB_PCB_INTR_TYPE_N_PENDING_3: PCB interrupt type [n] pending: quad 3.
4	ROX	WOX_CLEAR	OCB_OCI_OPIT7PRB_PCB_INTR_TYPE_N_PENDING_4: PCB interrupt type [n] pending: quad 4.
5	ROX	WOX_CLEAR	OCB_OCI_OPIT7PRB_PCB_INTR_TYPE_N_PENDING_5: PCB interrupt type [n] pending: quad 5.
6:63	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCC O2S Control First Frame 0A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLF0A
Address	000000000006C700 (SCOM)
Description	OCC O2S Control First Frame 0A Register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	OCB_OCI_O2SCTRLF0A_O2S_FRAME_SIZE_A_N: Number of data bits per individual SPI transaction (also referred to as a frame) during virtual chip select assertion. Supported values: 0x20 (32d) (virtual). Chip select assertion duration is O2S_FRAME_SIZE + 2.
6:11	RW	OCB_OCI_O2SCTRLF0A_O2S_OUT_COUNT1_A_N: Number of bits sent out AVS_MDATA in frame 1 of a 2 frame set (the arbitration unit). Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] are ignored.

Bits	SCOM	Field Mnemonic: Description
12:17	RW	OCB_OCI_O2SCTRLF0A_O2S_IN_DELAY1_A_N: Number of SPI clocks to wait before capturing AVS_SDATA input in frame 1 Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] result in the input never being captured.
18:23	RW	OCB_OCI_O2SCTRLF0A_O2S_IN_COUNT1_A_N: Number of bits captured on AVS_SDATA input in frame 1 Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. The actual number of bits captured is O2S_FRAME_SIZE_[a][n] - O2S_IN_DELAY1_[a][n].
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCC O2S Control Second Frame 0A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLS0A
Address	000000000006C701 (SCOM)
Description	OCC O2S Control Second Frame 0A Register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	OCB_OCI_O2SCTRLS0A_O2S_OUT_COUNT2_A_N: Number of bits sent out AVS_MDATA in frame 2 of a 2 frame set (the arbitration unit) Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] are ignored.
6:11	RW	OCB_OCI_O2SCTRLS0A_O2S_IN_DELAY2_A_N: Number of SPI clocks to wait before capturing AVS_SDATA input in subframe 2 Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] result in the input never being captured.
12:17	RW	OCB_OCI_O2SCTRLS0A_O2S_IN_COUNT2_A_N: Number of bits captured on AVS_SDATA input in subframe 2 Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. The actual number of bits captured is O2S_FRAME_SIZE_[a][n] - O2S_IN_DELAY2_[a][n].
18:63	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	OCC O2S Control1 0A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL10A
Address	000000000006C702 (SCOM)
Description	OCC O2S Control1 0A Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_O2SCTRL10A_O2S_BRIDGE_ENABLE_A_N: If set to 1, the OCI2SPI bridge can be used to control the SPI interface If set to 0, the OCI2SPI is forced to the reset state. **Note:** If the bridge is presently active (OS2_IN_PROGRESS + E147 = 1), the hard reset can truncate on-going operations and leave the SPIVID in an indeterminate state.
1	RW	OCB_OCI_O2SCTRL10A_O2SCTRL1_A_N_RESERVED_1: Implemented but not used.
2	RW	OCB_OCI_O2SCTRL10A_O2S_CPOL_A_N: SPI clock polarity. If CPOL = 0, CLK IDLE is deasserted. If CPOL = 1, CLK IDLE is asserted.
3	RW	OCB_OCI_O2SCTRL10A_O2S_CPHA_A_N: SPI clock phase. If CPHA = 0, change the sample values of data signals on the first edge. Otherwise, change the sample values of data signals on the second edge.
4:13	RW	OCB_OCI_O2SCTRL10A_O2S_CLOCK_DIVIDER_A_N: A SPI clock speed divider that is used to divide the NEST_NCLK4 mesh clock, which results in a divider = (NEST_FREQ [SPI_FREQ * 8]) – 1. For a 2.4 GHz nest clock, this means that the SPI clock can be theoretically adjusted between 600 MHz and 0.29 MHz (cycle time 1.66 ns…3.41 us, in 1.66 ns steps). However, a practical range is 0.5…25 MHz.
14:16	RW	OCB_OCI_O2SCTRL10A_O2SCTRL1_A_N_RESERVED_14_16: Reserved for number of frames.

Bits	SCOM	Field Mnemonic: Description
17	RW	OCB_OCI_O2SCTRL10A_O2S_NR_OF_FRAMES_A_N: Specifies the number of frames sent in the frame set (the number of frames before the arbitration unit rearbitrates). 0 = 1 frame 1 = 2 frames
18:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	OCC O2S Control2 0A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL20A
Address	000000000006C703 (SCOM)
Description	OCC O2S Control2 0A Register

Bits	SCOM	Field Mnemonic: Description
0:16	RW	OCB_OCI_O2SCTRL20A_O2S_INTER_FRAME_DELAY_A_N: Delay between two frames of a two-command set as measured from the end of the last bit of the first frame until the chip select of the second frame is asserted. Delay is computed as: (value * ~100 ns_hang_pulse) + 0 - ~100 ns_hang_pulse time. 0x00000 = Wait 1 SPI clock. 0x00001 - 0x1FFFF: value = number of ~10 0ns_hang_pulses. For values greater than 0x00000, the actual delay is 1 SPI clock + the time delay designated by the value defined. Maximum delay at 0x1FFFF: 13.1 ms + 1 SPI clock cycle.
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	OCC O2S Status 0A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SST0A
Address	000000000006C706 (SCOM)
Description	OCC O2S STATUS 0A Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	OCB_OCI_O2SST0A_O2S_ONGOING_A_N: Indicates that a bridge transaction is in progress of being executed. This bit is set by hardware while an operation is in progress and will be be reset by hardware when the operation is complete.
1:4	RO	OCB_OCI_O2SST0A_O2SST_A_N_RESERVED_1_4: Implemented but not used.
5	ROX	OCB_OCI_O2SST0A_O2S_WRITE_WHILE_BRIDGE_BUSY_ERR_A_N: Indicates that firmware attempted to perform an write to either the O2S_RWDATA_REG while the O2S bridge is busy. This causes undefined bridge behavior. This bit is sticky and is cleared with O2S_CLEAR_STICKY_BITS_[a][n].
6	RO	OCB_OCI_O2SST0A_O2SST_A_N_RESERVED_6: Implemented but not used.
7	ROX	OCB_OCI_O2SST0A_O2S_FSM_ERR_A_N: Indicates a catastrophic FSM error in the OCI2SPI control FSM. This bit is sticky and is cleared with O2S_CLEAR_STICKY_BITS_[a][n].
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	OCC O2S Command Reg 0A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCMD0A
Address	000000000006C707 (SCOM)
Description	OCC O2S Command Reg 0A Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_O2SCMD0A_O2SCMD_A_N_RESERVED_0: Implemented but not used.
1	RWX	OCB_OCI_O2SCMD0A_O2S_CLEAR_STICKY_BITS_A_N: If set to 1, all sticky bits in O2S_STATUS_REG_[a][n] are cleared.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCC O2S WDATA 0A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SWD0A
Address	000000000006C708 (SCOM)
Description	OCC O2S WDATA 0A Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	OCB_OCI_O2SWD0A_O2S_WDATA_A_N: SPI send data packet.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC O2S RDATA 0A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SRD0A
Address	000000000006C709 (SCOM)
Description	OCC O2S RDATA 0A Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	OCB_OCI_O2SRD0A_O2S_RDATA_A_N: 8-bit SPI receive data packet, duplicated in bits 8…15 and 16…23, plus 8-bit CRC. CRC is checked in SPI master if SPIVID_CRC_CHECK_EN = 1. If SPIVID_MAJORITY_VOTE_EN = 1, bits 0…7, contain the corrected result. Duplicated in bits 8…15 and 16…23.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC O2S Control First Frame 0B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLF0B
Address	000000000006C710 (SCOM)
Description	OCC O2S Control First Frame 0B Register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	OCB_OCI_O2SCTRLF0B_O2S_FRAME_SIZE_A_N: Number of data bits per individual SPI transaction (also referred to as frame) during (virtual) chip select assertion. Supported values: 0x20 (32 d) (virtual). Chip select assertion duration is O2S_FRAME_SIZE + 2.
6:11	RW	OCB_OCI_O2SCTRLF0B_O2S_OUT_COUNT1_A_N: Number of bits sent out AVS_MDATA in frame 1 of a 2 frame set (the arbitration unit). Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] are ignored.
12:17	RW	OCB_OCI_O2SCTRLF0B_O2S_IN_DELAY1_A_N: Number of SPI clocks to wait before capturing AVS_SDATA input in frame 1. Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] result in the input never being captured.

Bits	SCOM	Field Mnemonic: Description
18:23	RW	OCB_OCI_O2SCTRLF0B_O2S_IN_COUNT1_A_N: Number of bits captured on AVS_SDATA input in frame 1 Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. The actual number of bits captured is O2S_FRAME_SIZE_[a][n] - O2S_IN_DELAY1_[a][n].
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCC O2S Control Second Frame 0B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLS0B
Address	000000000006C711 (SCOM)
Description	OCC O2S Control Second Frame 0B Register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	OCB_OCI_O2SCTRLS0B_O2S_OUT_COUNT2_A_N: Number of bits sent out AVS_MDATA in frame 2 of a 2 frame set (the arbitration unit). Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] are ignored.
6:11	RW	OCB_OCI_O2SCTRLS0B_O2S_IN_DELAY2_A_N: Number of SPI clocks to wait before capturing AVS_SDATA input in subframe 2. Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] result in the input never being captured.
12:17	RW	OCB_OCI_O2SCTRLS0B_O2S_IN_COUNT2_A_N: Number of bits captured on AVS_SDATA input in subframe 2. Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. The actual number of bits captured is O2S_FRAME_SIZE_[a][n] - O2S_IN_DELAY2_[a][n].
18:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCC O2S Control1 0B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL10B
Address	000000000006C712 (SCOM)
Description	OCC O2S Control1 0B Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_O2SCTRL10B_O2S_BRIDGE_ENABLE_A_N: If set to 1, the OCI2SPI bridge can be used to control the SPI interface. If set to 0, the OCI2SPI is forced to the reset state. **Note:** If the bridge is presently active (OS2_IN_PROGRESS + E147 = 1), the hard reset can truncate on-going operations and leave the SPIVID in an indeterminate state.
1	RW	OCB_OCI_O2SCTRL10B_O2SCTRL1_A_N_RESERVED_1: Implemented but not used.
2	RW	OCB_OCI_O2SCTRL10B_O2S_CPOL_A_N: SPI clock polarity. If CPOL = 0, CLK IDLE is deasserted. If CPOL = 1, CLK IDLE is asserted.
3	RW	OCB_OCI_O2SCTRL10B_O2S_CPHA_A_N: SPI clock phase. If CPHA = 0, change sample values of data signals on the first edge. Otherwise, change sample values of data signals on the second edge.
4:13	RW	OCB_OCI_O2SCTRL10B_O2S_CLOCK_DIVIDER_A_N: SPI clock speed divider to divide the NEST_NCLK4 mesh clock, which results in a divider = (NEST_FREQ [SPI_freq * 8]) - 1. For a 2.4 GHz nest clock, this means that the SPI clock can be theoretically adjusted between 600 MHz and 0.29 MHz (cycle time 1.66 ns…3.41us, in 1.66 ns steps). However, a practical range is 0.5…25 MHz.
14:16	RW	OCB_OCI_O2SCTRL10B_O2SCTRL1_A_N_RESERVED_14_16: Reserved for number of frames.
17	RW	OCB_OCI_O2SCTRL10B_O2S_NR_OF_FRAMES_A_N: Specifies the number of frames sent in the frame set (# of frames before the arbitration unit rearbitrates). 0 = 1 frame 1 = 2 frames

Bits	SCOM	Field Mnemonic: Description
18:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	OCC O2S Control2 0B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL20B
Address	000000000006C713 (SCOM)
Description	OCC O2S Control2 0B Register

Bits	SCOM	Field Mnemonic: Description
0:16	RW	OCB_OCI_O2SCTRL20B_O2S_INTER_FRAME_DELAY_A_N: Delay between two frames of a two command set as measured from the end of the last bit of the first frame until the chip select of the second frame is asserted. Delay is computed as: (value * ~100 ns_hang_pulse) + 0 - ~100 ns_hang_pulse time. 0x00000 = Wait 1 SPI clock 0x00001 0x1FFFF = value = number of ~100 ns_hang_pulses For values greater than 0x00000, the actual delay is 1. SPI clock + the time delay designated by the value defined. Maximum delay at 0x1FFFF: 13.1 ms + 1 SPI clock cycle.
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	OCC O2S Status 0B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SST0B
Address	000000000006C716 (SCOM)
Description	OCC O2S STATUS 0B Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	OCB_OCI_O2SST0B_O2S_ONGOING_A_N: Indicates that a bridge transaction is in progress of being executed. This bit is set by hardware while an operation is in progress and will be be reset by hardware when the operation is complete.
1:4	RO	OCB_OCI_O2SST0B_O2SST_A_N_RESERVED_1_4: Implemented but not used.
5	ROX	OCB_OCI_O2SST0B_O2S_WRITE_WHILE_BRIDGE_BUSY_ERR_A_N: Indicates that firmware attempted to perform an write to either the O2S_RWDATA_REG while the O2S bridge is busy. This causes undefined bridge behavior. This bit is sticky and is cleared with O2S_CLEAR_STICKY_BITS_[a][n].
6	RO	OCB_OCI_O2SST0B_O2SST_A_N_RESERVED_6: Implemented but not used.
7	ROX	OCB_OCI_O2SST0B_O2S_FSM_ERR_A_N: Indicates a catastrophic FSM error in the OCI2SPI control FSM. This bit is sticky and is cleared with O2S_CLEAR_STICKY_BITS_[a][n].
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCC O2S Command Reg 0B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCMD0B
Address	000000000006C717 (SCOM)
Description	OCC O2S Command Reg 0B Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_O2SCMD0B_O2SCMD_A_N_RESERVED_0: Implemented but not used.

Bits	SCOM	Field Mnemonic: Description
1	RWX	OCB_OCI_O2SCMD0B_O2S_CLEAR_STICKY_BITS_A_N: If set to 1, all sticky bits in O2S_STATUS_REG_[a][n] are cleared.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCC O2S WDATA 0B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SWD0B
Address	000000000006C718 (SCOM)
Description	OCC O2S WDATA 0B Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	OCB_OCI_O2SWD0B_O2S_WDATA_A_N: SPI send data packet.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC O2S RDATA 0B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SRD0B
Address	000000000006C719 (SCOM)
Description	OCC O2S RDATA 0B Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	OCB_OCI_O2SRD0B_O2S_RDATA_A_N: 8-bit SPI receive data packet, duplicated in bits 8…15 and 16…23, plus 8-bit CRC. CRC is checked in SPI master if SPIVID_CRC_CHECK_EN = 1. If SPIVID_MAJORITY_VOTE_EN = 1, bits 0…7, contain the corrected result. Duplicated in bits 8…15 and 16…23.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC O2S Control First Frame 1A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLF1A
Address	000000000006C720 (SCOM)
Description	OCC O2S Control First Frame 1A Register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	OCB_OCI_O2SCTRLF1A_O2S_FRAME_SIZE_A_N: Number of data bits per individual SPI transaction (also referred to as frame) during (virtual) chip select assertion. Supported values: 0x20 (32 d) (virtual) chip select assertion duration is O2S_FRAME_SIZE + 2.
6:11	RW	OCB_OCI_O2SCTRLF1A_O2S_OUT_COUNT1_A_N: Number of bits sent out AVS_MDATA in frame 1 of a 2 frame set (the arbitration unit). Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] are ignored.
12:17	RW	OCB_OCI_O2SCTRLF1A_O2S_IN_DELAY1_A_N: Number of SPI clocks to wait before capturing AVS_SDATA input in frame 1. Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] result in the input never being captured.
18:23	RW	OCB_OCI_O2SCTRLF1A_O2S_IN_COUNT1_A_N: Number of bits captured on AVS_SDATA input in frame 1. Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. The actual number of bits captured is O2S_FRAME_SIZE_[a][n] - O2S_IN_DELAY1_[a][n].

Bits	SCOM	Field Mnemonic: Description
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCC O2S Control Second Frame 1A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLS1A
Address	000000000006C721 (SCOM)
Description	OCC O2S Control Second Frame 1A Register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	OCB_OCI_O2SCTRLS1A_O2S_OUT_COUNT2_A_N: Number of bits sent out AVS_MDATA in frame 2 of a 2-frame set (the arbitration unit). Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] are ignored.
6:11	RW	OCB_OCI_O2SCTRLS1A_O2S_IN_DELAY2_A_N: Number of SPI clocks to wait before capturing AVS_SDATA input in subframe 2. Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] result in the input never being captured.
12:17	RW	OCB_OCI_O2SCTRLS1A_O2S_IN_COUNT2_A_N: Number of bits captured on AVS_SDATA input in subframe 2. Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. The actual number of bits captured is O2S_FRAME_SIZE_[a][n] - O2S_IN_DELAY2_[a][n].
18:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCC O2S Control1 1A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL11A
Address	000000000006C722 (SCOM)
Description	OCC O2S Control1 1A Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_O2SCTRL11A_O2S_BRIDGE_ENABLE_A_N: If set to 1, the OCI2SPI bridge can be used to control the SPI interface. If set to 0, the OCI2SPI is forced to the reset state. **Note:** If the bridge is presently active (OS2_IN_PROGRESS + E147 = 1), the hard reset can truncate on-going operations and leave the SPIVID in an indeterminate state.
1	RW	OCB_OCI_O2SCTRL11A_O2SCTRL1_A_N_RESERVED_1: Implemented but not used.
2	RW	OCB_OCI_O2SCTRL11A_O2S_CPOL_A_N: SPI clock polarity. If CPOL = 0, CLK IDLE is deasserted. If CPOL = 1, CLK IDLE is asserted.
3	RW	OCB_OCI_O2SCTRL11A_O2S_CPHA_A_N: SPI clock phase. If CPHA = 0, change sample values of data signals on the first edge. Otherwise, change sample values of data signals on the second edge.
4:13	RW	OCB_OCI_O2SCTRL11A_O2S_CLOCK_DIVIDER_A_N: SPI clock speed divider to divide the NEST_NCLK4 mesh clock, which results in a divider = (NEST_FREQ [SPI_FREQ * 8]) – 1. For a 2.4 GHz nest clock, this means that the SPI clock can be theoretically adjusted between 600 MHz and 0.29 MHz. (Cycle time is 1.66 ns…3.41 us in 1.66 ns steps). However, a practical range is 0.5…25MHz.
14:16	RW	OCB_OCI_O2SCTRL11A_O2SCTRL1_A_N_RESERVED_14_16: Reserved for number of frames.
17	RW	OCB_OCI_O2SCTRL11A_O2S_NR_OF_FRAMES_A_N: Specifies the number of frames sent in the frame set (number of frames before the arbitration unit rearbitrates). 0 = 1 frame 1 = 2 frames
18:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCC O2S Control2 1A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL21A
Address	000000000006C723 (SCOM)
Description	OCC O2S Control2 1A Register

Bits	SCOM	Field Mnemonic: Description
0:16	RW	OCB_OCI_O2SCTRL21A_O2S_INTER_FRAME_DELAY_A_N: Delay between two frames of a two command set as measured from the end of the last bit of the first frame until the chip select of the second frame is asserted. Delay is computed as: (value * ~100 NS_HANG_PULSE) + 0 - ~100 NS_HANG_PULSE time. 0X00000 = Wait 1 SPI clock 0x00001 – 0x1FFFF = value = number of ~100 NS_HANG_PULSES. For values greater than 0x00000, the actual delay is 1 SPI clock + the time delay designated by the value defined. The maximum delay at 0x1FFFF = 13.1 ms + 1 SPI clock cycle.
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	OCC O2S STATUS 1A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SST1A
Address	000000000006C726 (SCOM)
Description	OCC O2S STATUS 1A Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	OCB_OCI_O2SST1A_O2S_ONGOING_A_N: Indicates that a bridge transaction is in progress of being executed. This bit is set by hardware while an operation is in progress and will be be reset by hardware when the operation is complete.
1:4	RO	OCB_OCI_O2SST1A_O2SST_A_N_RESERVED_1_4: Implemented but not used.
5	ROX	OCB_OCI_O2SST1A_O2S_WRITE_WHILE_BRIDGE_BUSY_ERR_A_N: Indicates that firmware attempted to perform an write to either the O2S_RWDATA_REG while the O2S bridge is busy. This causes undefined bridge behavior. This bit is sticky and is cleared with O2S_CLEAR_STICKY_BITS_[a][n].
6	RO	OCB_OCI_O2SST1A_O2SST_A_N_RESERVED_6: Implemented but not used.
7	ROX	OCB_OCI_O2SST1A_O2S_FSM_ERR_A_N: Indicates a catastrophic FSM error in the OCI2SPI control FSM. This bit is sticky and is cleared with O2S_CLEAR_STICKY_BITS_[a][n].
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCC O2S Command Reg 1A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCMD1A
Address	000000000006C727 (SCOM)
Description	OCC O2S Command Reg 1A Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_O2SCMD1A_O2SCMD_A_N_RESERVED_0: Implemented but not used.
1	RWX	OCB_OCI_O2SCMD1A_O2S_CLEAR_STICKY_BITS_A_N: If set to 1, all sticky bits in O2S_STATUS_REG_[a][n] are cleared.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCC O2S WDATA 1A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SWD1A
Address	000000000006C728 (SCOM)
Description	OCC O2S WDATA 1A Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	OCB_OCI_O2SWD1A_O2S_WDATA_A_N: SPI send data packet.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC O2S RDATA 1A Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SRD1A
Address	000000000006C729 (SCOM)
Description	OCC O2S RDATA 1A Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	OCB_OCI_O2SRD1A_O2S_RDATA_A_N: 8-bit SPI receive data packet. Duplicated in bits 8…15 and 16…23, plus 8-bit CRC. CRC is checked in SPI master if SPIVID_CRC_CHECK_EN = 1. If SPIVID_MAJORITY_VOTE_EN = 1, bits 0…7, contain the corrected result, duplicated in bits 8…15 and 16…23.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC O2S Control First Frame 1B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLF1B
Address	000000000006C730 (SCOM)
Description	OCC O2S Control First Frame 1B Register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	OCB_OCI_O2SCTRLF1B_O2S_FRAME_SIZE_A_N: Number of data bits per individual SPI transaction (also referred to as frame) during (virtual) chip select assertion. Supported values: 0x20 (32d) (virtual). Chip select assertion duration is O2S_FRAME_SIZE + 2.
6:11	RW	OCB_OCI_O2SCTRLF1B_O2S_OUT_COUNT1_A_N: Number of bits sent out AVS_MDATA in frame 1 of a 2 frame set (the arbitration unit) Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] are ignored.
12:17	RW	OCB_OCI_O2SCTRLF1B_O2S_IN_DELAY1_A_N: Number of SPI clocks to wait before capturing AVS_SDATA input in frame 1 Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] result in the input never being captured.
18:23	RW	OCB_OCI_O2SCTRLF1B_O2S_IN_COUNT1_A_N: Number of bits captured on AVS_SDATA input in frame 1 Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. The actual number of bits captured is O2S_FRAME_SIZE_[a][n] - O2S_IN_DELAY1_[a][n].
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	OCC O2S Control Second Frame 1B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRLS1B
Address	000000000006C731 (SCOM)
Description	OCC O2S Control Second Frame 1B Register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	OCB_OCI_O2SCTRLS1B_O2S_OUT_COUNT2_A_N: Number of bits sent out AVS_MDATA in frame 2 of a 2 frame set (the arbitration unit). Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] are ignored.
6:11	RW	OCB_OCI_O2SCTRLS1B_O2S_IN_DELAY2_A_N: Number of SPI clocks to wait before capturing AVS_SDATA input in subframe 2. Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. Values beyond O2S_FRAME_SIZE_[a][n] result in the input never being captured.
12:17	RW	OCB_OCI_O2SCTRLS1B_O2S_IN_COUNT2_A_N: Number of bits captured on AVS_SDATA input in subframe 2. Supported values: 0x00 to O2S_FRAME_SIZE_[a][n]. The actual number of bits captured is O2S_FRAME_SIZE_[a][n] - O2S_IN_DELAY2_[a][n].
18:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	OCC O2S Control1 1B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL11B
Address	000000000006C732 (SCOM)
Description	OCC O2S Control1 1B Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_O2SCTRL11B_O2S_BRIDGE_ENABLE_A_N: If set to 1, the OCI2SPI bridge can be used to control the SPI interface. If set to 0, the OCI2SPI is forced to the reset state. **Note:** If the bridge is presently active (OS2_IN_PROGRESS + E147 = 1), the hard reset can truncate on-going operations and leave the SPIVID in an indeterminate state.
1	RW	OCB_OCI_O2SCTRL11B_O2SCTRL1_A_N_RESERVED_1: Implemented but not used.
2	RW	OCB_OCI_O2SCTRL11B_O2S_CPOL_A_N: SPI clock polarity. If CPOL = 0, CLK IDLE is deasserted. If CPOL = 1, CLK IDLE is asserted.
3	RW	OCB_OCI_O2SCTRL11B_O2S_CPHA_A_N: SPI clock phase. If CPHA = 0, change sample values of data signals on first edge. Otherwise change the sample values of data signals on the second edge.
4:13	RW	OCB_OCI_O2SCTRL11B_O2S_CLOCK_DIVIDER_A_N: SPI clock speed divider to divide the NEST_NCLK4 mesh clock, which results in a divider = (NEST_FREQ [SPI_freq * 8]) -1. For a 2.4GHz nest clock, this means that the SPI clock can be theoretically adjusted between 600 MHz and 0.29 MHz (cycle time 1.66ns…3.41us, in 1.66 ns steps). However, a practical range is 0.5…25MHz.
14:16	RW	OCB_OCI_O2SCTRL11B_O2SCTRL1_A_N_RESERVED_14_16: Reserved for number of frames.
17	RW	OCB_OCI_O2SCTRL11B_O2S_NR_OF_FRAMES_A_N: Specifies the number of frames sent in the frame set (number of frames before the arbitration unit rearbitrates). 0 = 1 frame 1 = 2 frames
18:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	OCC O2S Control2 1B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCTRL21B
Address	000000000006C733 (SCOM)
Description	OCC O2S Control2 1B Register

Bits	SCOM	Field Mnemonic: Description
0:16	RW	OCB_OCI_O2SCTRL21B_O2S_INTER_FRAME_DELAY_A_N: Delay between two frames of a two-command set as measured from the end of the last bit of the first frame until the chip select of the second frame is asserted. Delay is computed as: (value * ~100 ns_hang_pulse) + 0 -~100 ns_hang_pulse time. 0x00000 = Wait 1 SPI clock 0x00001 = 0x1FFFF = value = number of ~100 ns_hang_pulses For values greater than 0x00000, the actual delay is 1 SPI Clock + the time delay designated by the value defined. Maximum delay is at 0x1FFFF = 13.1 ms + 1 SPI clock cycle.
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	OCC O2S Status 1B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SST1B
Address	000000000006C736 (SCOM)
Description	OCC O2S STATUS 1B Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	OCB_OCI_O2SST1B_O2S_ONGOING_A_N: Indicates that a bridge transaction is in progress of being executed. This bit is set by hardware while an operation is in progress and will be reset by hardware when the operation is complete.
1:4	RO	OCB_OCI_O2SST1B_O2SST_A_N_RESERVED_1_4: Implemented but not used.
5	ROX	OCB_OCI_O2SST1B_O2S_WRITE_WHILE_BRIDGE_BUSY_ERR_A_N: Indicates that firmware attempted to perform an write to either the O2S_RWDATA_REG while the O2S bridge is busy. This causes undefined bridge behavior. This bit is sticky and is cleared with O2S_CLEAR_STICKY_BITS_[a][n].
6	RO	OCB_OCI_O2SST1B_O2SST_A_N_RESERVED_6: Implemented but not used.
7	ROX	OCB_OCI_O2SST1B_O2S_FSM_ERR_A_N: Indicates a catastrophic FSM error in the OCI2SPI control FSM. This bit is sticky and is cleared with O2S_CLEAR_STICKY_BITS_[a][n].
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCC O2S Command Reg 1B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SCMD1B
Address	000000000006C737 (SCOM)
Description	OCC O2S Command Reg 1B Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_OCI_O2SCMD1B_O2SCMD_A_N_RESERVED_0: Implemented but not used.
1	RWX	OCB_OCI_O2SCMD1B_O2S_CLEAR_STICKY_BITS_A_N: If set to 1, all sticky bits in O2S_STATUS_REG_[a][n] are cleared.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCC O2S WDATA 1B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SWD1B
Address	000000000006C738 (SCOM)
Description	OCC O2S WDATA 1B Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	OCB_OCI_O2SWD1B_O2S_WDATA_A_N: SPI send data packet.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCC O2S RDATA 1B Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_OCI_O2SRD1B
Address	000000000006C739 (SCOM)
Description	OCC O2S RDATA 1B Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	OCB_OCI_O2SRD1B_O2S_RDATA_A_N: An 8-bit SPI receive data packet, duplicated in bits 8…15 and 16…23 plus and 8-bit CRC. The CRC is checked in the SPI master if SPIVID_CRC_CHECK_EN = 1. If SPIVID_MAJORITY_VOTE_EN = 1, bits 0…7, contain the corrected result, duplicated in bits 8…15 and 16…23.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_PIB OCC Control Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCR
Address	000000000006D000 (SCOM) 000000000006D001 (SCOM1) 000000000006D002 (SCOM2)
Description	OCB_PIB OCC Control Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCR_CORE_RESET: Controls the core_reset pin to the PowerPC 405 core. **Note:** The reset value puts the PowerPC 405 core into reset. A PIB slave reset might or might not set this bit as well. See bit 9 (PIB_SLAVE_RESET_TO_405_ENABLE), which controls this behavior.
1	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_CHIP_RESET: Controls the chip_reset pin to the PowerPC 405 core.
2	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_SYSTEM_RESET: Controls the system_reset pin to the PowerPC 405 core.
3	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_OCI_ARB_RESET: Controls the reset pin to the OCI arbiter.
4	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_TRACE_DISABLE: Disables the PowerPC 405 core trace function when set.
5	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_TRACE_EVENT: Asserts a trigger event to the PowerPC 405 core.
6	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_DBG_UNCONDITIONAL_EVENT: Asserted the unconditional debug event (UDE) and sets the UDE bit of the debug status register (DBSR) if enabled.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
7	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_EXT_INTERRUPT: Asserts an external interrupt to the PowerPC 405 core.
8	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_CRITICAL_INTERRUPT: Asserts a critical interrupt to the PowerPC 405 core.
9	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_PIB_SLAVE_RESET_TO_405_ENABLE: Controls whether a PIB slave reset puts the PowerPC 405 core into reset. 0 = PIB slave reset does not cause PowerPC 405 core reset(default) 1 = PIB slave reset causes PowerPC 405 core reset (sets bit 0)
10	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_OCC_DBG_HALT: Halts the PowerPC 405 core execution. This bit is ORed with OCC JTAG Configuration Register(dbg_HALT), which is used by RISCWatch code for debug operations. This bit is intended to be used by OCC reset code to gracefully halt the PowerPC 405 core without colliding with RISCWatch firmware.
11:15	RO	WO_CLEAR	WO_OR	OCB_PIB_OCR_SPARE: Implemented but unused.
16:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_PIB OCC Debug Mode Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCDBG
Address	000000000006D003 (SCOM)
Description	OCB_PIB OCC Debug Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_PIB_OCDBG_MST_DIS_ABUSPAREN: Disable ADBUS_PAREN. Disables address parity generation for all GPE OCI Masters.
1	RW	OCB_PIB_OCDBG_MST_DIS_BEPAREN: Disable BE_PAREN. Disables byte enable parity generation for all GPE OCI Masters.
2	RW	OCB_PIB_OCDBG_MST_DIS_WRDBUSPAREN: Disable WRDATA_PAREN. Disables write data parity generation for all GPE OCI Masters.
3	RW	OCB_PIB_OCDBG_MST_DIS_RDDBUSPAR: Disable read data parity checking. Parity checking on read data will be disabled and data will be forwarded to unit for all GPE OCI masters.
4	RW	OCB_PIB_OCDBG_MST_SPARE: Spare debug signal for OCI Master for all GPE OCI masters.
5	RW	OCB_PIB_OCDBG_SLV_DIS_SACK: Disable acknowledge of secondary requests. Savalid will be ignored and interface component will respond only to pavalid.
6	RW	OCB_PIB_OCDBG_SLV_DIS_ABUSPAR: Disable address parity checking. Address parity error will be ignored by all GPE OCI Slaves.
7	RW	OCB_PIB_OCDBG_SLV_DIS_BEPAR: Disable byte enable parity checking. Byte enable parity error will be ignored by all GPE OCI Slaves.
8	RW	OCB_PIB_OCDBG_SLV_DIS_BE: Disable byte enable correctness checking. Invalid combinations of byte enable will be ignored by all GPE OCI slaves. Transfers will be allowed to progress to unit with all ‘1’ byte_enable.
9	RW	OCB_PIB_OCDBG_SLV_DIS_WRDBUSPAR: Disable write data parity checking. Parity checking on write data will be disabled and data will be forwarded to unit.
10	RW	OCB_PIB_OCDBG_SLV_DIS_RDDBUSPAREN: Disable RDDBUS_PAREN. Disable read data parity generation by all GPE OCI slaves.
11	RW	OCB_PIB_OCDBG_SLV_SPARE: Spare debug signal for all GPE OCI slaves.
12:15	RW	OCB_PIB_OCDBG_SPARE: Implemented but unused.

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	JTG_PIB OCC JTAG Configuration Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJCFG
Address	000000000006D004 (SCOM) 000000000006D005 (SCOM1) 000000000006D006 (SCOM2)
Description	JTG_PIB OCC JTAG Configuration Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	JTG_PIB_OJCFG_JTAG_SRC_SEL: Select source to drive the 405 JTAG pins. 0 = OCC FSM 1 = FSI (toad mode)
1	RW	WO_AND	WO_OR	JTG_PIB_OJCFG_RUN_TCK: Control TCK clock (also used as act to enable all associated JTAG driver latches) 0 = Off 1 = On
2:4	RW	WO_AND	WO_OR	JTG_PIB_OJCFG_TCK_WIDTH: This field is used to compute the number of clock cycles before transitioning TCK. The actual TCK width is (TCK_WIDTH + 1) * 2. For example : if TCK_WIDTH is 000, the actual width will be two clock cycles. TCK will be ‘1’ for two cycles and ‘0’ for two cycles and repeat. The possible values of the actual TCK width are even numbers from 2 to 16.
5	RW	WO_AND	WO_OR	JTG_PIB_OJCFG_JTAG_TRST_B: **Note:** This is a low active signal and the reset value puts the PowerPC 405 core JTAG logic into reset.
6	RW	WO_AND	WO_OR	JTG_PIB_OJCFG_DBG_HALT: Halts the PowerPC 405 core execution. This bit is ORed with OCC Control Register(OCC_DBG_HALT), which is used by OCC reset code. This bit is intended to be used by RISCWatch firmware without colliding with reset firmware.
7:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	JTG_PIB OCC JTAG FSM Reset Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJFRST
Address	000000000006D007 (SCOM)
Description	JTG_PIB OCC JTAG FSM Reset Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000000000000

Register Name	JTG_PIB OCC JTAG Instruction and Control Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJIC
Address	000000000006D008 (SCOM) 000000000006D009 (SCOM1) 000000000006D00A (SCOM2)
Description	JTG_PIB OCC JTAG Instruction and Control Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	WOX	WOX_AND	WOX_OR	JTG_PIB_OJIC_START_JTAG_CMD: Self-clearing bit. When written to a '1' initiates the FSM to perform the specified JTAG command. Clears to '0' on next cycle after being written.
1	RW	WO_AND	WO_OR	JTG_PIB_OJIC_DO_IR: IR control 0 = Do not execute IR path 1 = Execute IR path
2	RW	WO_AND	WO_OR	JTG_PIB_OJIC_DO_DR: DR control 0 = Do not execute DR path 1 = Execute DR path
3	RW	WO_AND	WO_OR	JTG_PIB_OJIC_DO_TAP_RESET: 405 TAP reset control 0 = Do not perform TAP controller reset before IR 1 = Perform TAP controller reset before IR. (That is, issue TMS for 5 TCK clocks to force TAP controller state machine reset) **Note:** DO_TAP_RESET is only valid when DO_IR = 1. Otherwise, its value is ignored.
4	RW	WO_AND	WO_OR	JTG_PIB_OJIC_WR_VALID: The 33rd bit placed on TDI when performing a 33-bit JTAG register access.
5:11	RO	RO	RO	constant = 0b0000000
12:15	RW	WO_AND	WO_OR	JTG_PIB_OJIC_JTAG_INSTR: 4-bit 405 JTAG instruction.
16:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	JTG_PIB OCC JTAG Status Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJSTAT
Address	000000000006D00B (SCOM)
Description	JTG_PIB OCC JTAG Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	JTG_PIB_OJSTAT_JTAG_INPROG: Status bit to indicate that a current JTAG operation is in progress. (That is, FSM is not idle).
1	RWX_WCLEAR	JTG_PIB_OJSTAT_SRC_SEL_EQ1_ERR: Status to indicate that a JTAG operation was attempted, but the SRC_SEL bit in OJCFG was set to FSI as source of JTAG instead of the JTAG accelerator.
2	RWX_WCLEAR	JTG_PIB_OJSTAT_RUN_TCK_EQ0_ERR: Status to indicate that a JTAG operation was attempted, but the RUN_TCK bit in OJCFG was set to '0'. (That is, TCK is not running).
3	RWX_WCLEAR	JTG_PIB_OJSTAT_TRST_B_EQ0_ERR: Status to indicate that a JTAG operation was attempted, but the JTAG_TRST_B bit in OJCFG was set to '0'. (That is, PowerPC 405 JTAG is in reset).
4	RWX_WCLEAR	JTG_PIB_OJSTAT_IR_DR_EQ0_ERR: Status to indicate that a JTAG operation was attempted, but DO_IR and DO_DR bits in OJIC were both set to '0'. (That is, no operation is selected).
5	RWX_WCLEAR	JTG_PIB_OJSTAT_INPROG_WR_ERR: Status to indicate that a PIB register write was attempted to either OJCFG, OJIC, or OJTDI while jtag_inprog = '1'. (That is, JTAG operation still in progress).

Bits	SCOM	Field Mnemonic: Description
6	RWX_WCLEAR	JTG_PIB_OJSTAT_FSM_ERROR: Status to indicate that the JTAG FSM went to an illegal state. (That is, odd parity check on one-hot state machine bits).
7:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	JTG_PIB OCC JTAG TDI Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJTDI
Address	000000000006D00C (SCOM)
Description	JTG_PIB OCC JTAG TDI Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	JTG_PIB_OJTDI_JTAG_TDI: 32 bits of data to write into 405 JTAG registers.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	JTG_PIB OCC JTAG TDO Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJTDO
Address	000000000006D00D (SCOM)
Description	JTG_PIB OCC JTAG TDO Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	JTG_PIB_OJTDO_JTAG_TDO: 32 bits of data read from 405 JTAG registers.
32	ROX	JTG_PIB_OJCFG_JTAG_SRC_SEL: Select source to drive the 405 JTAG pins 0 = OCC FSM 1 = FSI (toad mode)
33	ROX	JTG_PIB_OJCFG_RUN_TCK: Control TCK clock (also used as act to enable all associated JTAG driver latches) 0 = Off 1 = On
34:36	ROX	JTG_PIB_OJCFG_TCK_WIDTH: This field is used to compute the number of clock cycles before transitioning TCK. The actual TCK width is (TCK_WIDTH + 1) * 2. For example, if TCK_WIDTH is 000, the actual width will be 2 clock cycles. TCK will be ‘1’ for two cycles and ‘0’ for two cycles and repeat. The possible values of the actual TCK width are even numbers from 2 to 16.
37	ROX	JTG_PIB_OJCFG_JTAG_TRST_B: **Note:** This is a low active signal and the reset value puts the PowerPC 405 JTAG logic into reset.
38	ROX	JTG_PIB_OJCFG_DBG_HALT: Halts the PowerPC 405 execution. This bit is ORed with OCC Control Register(OCC_DBG_HALT), which is used by OCC Reset code. This bit is intended to be used by RISCWatch firmware without colliding with reset firmware.
39	RO	constant = 0b0
40	ROX	JTG_PIB_OJSTAT_JTAG_INPROG: Status bit to indicate that a current JTAG operation is in progress. (That is, FSM not idle).
41	ROX	JTG_PIB_OJSTAT_SRC_SEL_EQ1_ERR: Status to indicate that a JTAG operation was attempted, but the SRC_SEL bit in OJCFG was set to FSI as source of JTAG instead of the JTAG accelerator.
42	ROX	JTG_PIB_OJSTAT_RUN_TCK_EQ0_ERR: Status to indicate that a JTAG operation was attempted, but RUN_TCK bit in OJCFG was set to ‘0’. (That is, TCK is not running).
43	ROX	JTG_PIB_OJSTAT_TRST_B_EQ0_ERR: Status to indicate that a JTAG operation was attempted, but the JTAG_TRST_B bit in OJCFG was set to ‘0’. (That is, PowerPC 405 JTAG is in reset).

Bits	SCOM	Field Mnemonic: Description
44	ROX	JTG_PIB_OJSTAT_IR_DR_EQ0_ERR: Status to indicate that a JTAG operation was attempted, but do_ir and DO_DR bits in OJIC were both set to ‘0’. (That is, no operation is selected).
45	ROX	JTG_PIB_OJSTAT_INPROG_WR_ERR: Status to indicate that a PIB register write was attempted to either OJCFG, OJIC, or OJTDI while JTAG_INPROG = ‘1’. (That is, JTAG operation still in progress).
46	ROX	JTG_PIB_OJSTAT_FSM_ERROR: Status to indicate that the JTAG FSM went to an illegal state. (That is, odd parity check on one-hot state machine bits).
47:48	RO	constant = 0b00
49	ROX	JTG_PIB_OJIC_DO_IR: IR control 0 = Do not execute IR path 1 = Execute IR path
50	ROX	JTG_PIB_OJIC_DO_DR: DR control 0 = Do not execute DR path 1 = Execute DR path
51	ROX	JTG_PIB_OJIC_DO_TAP_RESET: 405 TAP reset control 0 = Do not perform TAP controller reset before IR 1 = Perform TAP controller reset before IR. (That is, issue TMS for 5 TCK clocks to force TAP controller state machine reset.) **Note:** DO_TAP_RESET is only valid when DO_IR =1. Otherwise, its value is ignored.
52	ROX	JTG_PIB_OJIC_WR_VALID: 33rd bit placed on TDI when performing a 33 bit JTAG register access.
53:59	RO	constant = 0b0000000
60:63	ROX	JTG_PIB_OJIC_JTAG_INSTR: 4-bit 405 JTAG instruction.

Register Name	OCB_PIB OCB Address 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR0
Address	000000000006D010 (SCOM)
Description	OCB_PIB OCB Address 0 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_PIB_OCBAR0_OCI_REGION: OCI Address Space Region 0XX = Reserved 10X = Processor bus memory 110 = Register space 111 = SRAM
3:28	RW	OCB_PIB_OCBAR0_OCB_ADDRESS: Address of 8 B quantity the OCI for this channel. The field contents depends on accessed OCI_REGION processor bus. Bits 3:11 = Maskable alignment (see the PBA specification). Bits 12:28 = Offset SRAM. Bits 3:4 = 128 MB alias. Bits are not compared. Bits 5:11 = 0b1111111. Bits 12:28 = Offset.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	**OCB_PIB OCB Control/Status 0 Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR0
Address	000000000006D011 (SCOM) 000000000006D012 (SCOM1) 000000000006D013 (SCOM2)
Description	OCB_PIB OCB Control/Status 0 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR0_PULL_READ_UNDERFLOW: Pull queue read underflow underflow is defined as a read to the OCB Data [n] Register and the PULL_EMPTY facility is already set. This bit is cleared only by a firmware write of this bit to 0. Writes store the value.
1	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR0_PUSH_WRITE_OVERFLOW: Push Queue Write Overflow. Overflow is defined as a store to the OCB Data [n] Register and the PUSH_FULL facility is already set. This bit is cleared only by a firmware write of this bit to 0.
2	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR0_PULL_READ_UNDERFLOW_EN: Enable the setting of pull_read_underflow by hardware. 0 = Underflow detection disabled 1 = Underflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
3	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR0_PUSH_WRITE_OVERFLOW_EN: Enable the setting of push_write_overflow by hardware. 0 = Overflow detection disabled 1 = Overflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
4	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR0_OCB_STREAM_MODE: Put the bridge channel in streaming mode with the behavior further defined by the setting of OCB_STREAM_TYPE. 0 = Stream mode disabled 1 = Stream mode enabled This bit is set using the OR mask register and cleared using the AND mask register.
5	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR0_OCB_STREAM_TYPE: Type of streaming enabled by OCB_STREAM_MODE = 1 0 = Linear 1 = Circular For linear type, the OCB_ADDRESS field is incremented by 8 with each access to the OCB Data [n] Register. In circular type, the address manipulation is through access to OCB Stream [Push-Pull] Increment registers. This bit is set using the OR mask register and cleared using the AND mask register.
6:7	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR0_SPARE0: Implemented but not used.
8	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR0_OCB_OCI_TIMEOUT: Indicates the MnTimeout signal on the OCI for the OCB master was asserted to a flag, but no OCI slave acknowledged the request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
9	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR0_OCB_OCI_READ_DATA_PARITY: Indicates the OCI read data parity was in error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
10	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR0_OCB_OCI_SLAVE_ERROR: Indicates the SlvError signal on the OCI for the OCB master was asserted. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
11	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR0_OCB_PIB_ADDR_PARITY_ERR: Indicates the PIB address parity was in error (PIB read or write operation). This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
12	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR0_OCB_PIB_DATA_PARITY_ERR: Indicates the PIB data parity was in error for a PIB write operation. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
13	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR0_SPARE1: Implemented but not used.
14	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR0_OCB_FSM_ERR: Catastrophic state machine error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
15	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR0_SPARE2: Implemented but not used. Writes store the value. Reads return the last value written.
16:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_PIB OCB Error Status 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR0
Address	000000000006D014 (SCOM)
Description	OCB_PIB OCB Error Status 0 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RWX_WCLRREG	OCB_PIB_OCBESR0_OCB_ERROR_ADDR: OCI address being accessed when the first channel error is detected. This register is cleared upon writing any value.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_PIB OCB Data 0 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR0
Address	000000000006D015 (SCOM)
Description	OCB_PIB OCB Data 0 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	OCB_PIB_OCBDR0_OCB_DATA: Data to and from the OCI for this channel.

Register Name	OCB_PIB OCB Address 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR1
Address	000000000006D030 (SCOM)
Description	OCB_PIB OCB Address 1 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_PIB_OCBAR1_OCI_REGION: OCI Address Space Region 0XX = Reserved 10X = Processor bus memory 110 = Register space 111 = SRAM.
3:28	RW	OCB_PIB_OCBAR1_OCB_ADDRESS: Address of 8 B quantity the OCI for this channel. The field contents depends on accessed OCI_REGION processor bus Bits 3:4 = 128 MB alias. Bits are not compared. Bits 3:11 = Maskable alignment. See the PBA specification. Bits 5:11 = 0b1111111. Bits 12:28 = Offset SRAM. Bits 12:28 = Offset.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	OCB_PIB OCB Control/Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR1
Address	000000000006D031 (SCOM) 000000000006D032 (SCOM1) 000000000006D033 (SCOM2)
Description	OCB_PIB OCB Control/Status 1 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR1_PULL_READ_UNDERFLOW: Pull queue read underflow. Underflow is defined as a read to the OCB Data [n] Register and the PULL_EMPTY facility is already set. This bit is cleared only by a firmware write of this bit to 0. Writes store the value.
1	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR1_PUSH_WRITE_OVERFLOW: Push Queue Write Overflow. Overflow is defined as a store to the OCB Data [n] Register and the PUSH_FULL facility is already set. This bit is cleared only by a firmware write of this bit to 0.
2	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR1_PULL_READ_UNDERFLOW_EN: Enable the setting of pull_read_underflow by hardware. 0 = Underflow detection disabled 1 = Underflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
3	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR1_PUSH_WRITE_OVERFLOW_EN: Enable the setting of push_write_overflow by hardware. 0 = Overflow detection disabled 1 =Overflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
4	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR1_OCB_STREAM_MODE: Put the bridge channel in streaming mode with the behavior further defined by the setting of OCB_STREAM_TYPE. 0 = Stream Mode Disabled 1 =Stream Mode Enabled This bit is set using the OR mask register and cleared using the AND mask register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR1_OCB_STREAM_TYPE: The type of streaming enabled by OCB_STREAM_MODE = 1. 0 = Linear 1 = Circular For linear type, the OCB_ADDRESS field is incremented by 8 with each access to the OCB Data [n] Register. In circular type, the address manipulation is through access to OCB Stream [Push-Pull] Increment registers. This bit is set using the OR mask register and cleared using the AND mask register.
6:7	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR1_SPARE0: Implemented but not used.
8	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR1_OCB_OCI_TIMEOUT: Indicates the MnTimeout signal on the OCI for the OCB master was asserted to flag that no OCI slave acknowledged the request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
9	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR1_OCB_OCI_READ_DATA_PARITY: Indicates the OCI read data parity was in error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
10	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR1_OCB_OCI_SLAVE_ERROR: Indicates the SlvError signal on the OCI for the OCB master was asserted. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
11	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR1_OCB_PIB_ADDR_PARITY_ERR: Indicates the PIB address parity was in error (PIB read or write operation). This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
12	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR1_OCB_PIB_DATA_PARITY_ERR: Indicates the PIB data parity was in error for a PIB write operation. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
13	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR1_SPARE1: Implemented but not used.
14	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR1_OCB_FSM_ERR: Catastrophic state machine error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
15	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR1_SPARE2: Implemented but not used. Writes store the value. Reads return the last value written.
16:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_PIB OCB Error Status 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR1
Address	000000000006D034 (SCOM)
Description	OCB_PIB OCB Error Status 1 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RWX_WCLRREG	OCB_PIB_OCBESR1_OCB_ERROR_ADDR: OCI address being accessed when the first channel error is detected. This register is cleared upon writing any value.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_PIB OCB Data 1 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR1
Address	000000000006D035 (SCOM)
Description	OCB_PIB OCB Data 1 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	OCB_PIB_OCBDR1_OCB_DATA: Data to and from OCI for this channel.

Register Name	OCB_PIB OCB Address 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR2
Address	000000000006D050 (SCOM)
Description	OCB_PIB OCB Address 2 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_PIB_OCBAR2_OCI_REGION: OCI Address Space Region 0XX = Reserved 10X = processor bus memory 110 = Register space 111 = SRAM
3:28	RW	OCB_PIB_OCBAR2_OCB_ADDRESS: Address of 8 B quantity the OCI for this channel. The field contents depends on accessed OCI_REGION processor bus. Bits 3:4 = 128 MB alias. Bits are not compared. Bits 3:11 = Maskable alignment. (See the PBA specification.) Bits 5:11 = 0b1111111. Bits 12:28 = Offset SRAM. Bits 12:28 = Offset.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	OCB_PIB OCB Control/Status 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR2
Address	000000000006D051 (SCOM) 000000000006D052 (SCOM1) 000000000006D053 (SCOM2)
Description	OCB_PIB OCB Control/Status 2 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR2_PULL_READ_UNDERFLOW: Pull Queue Read Underflow. Underflow is defined as a read to the OCB Data [n] Register and the PULL_EMPTY facility is already set. This bit is cleared only by a firmware write of this bit to 0. Writes store the value.
1	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR2_PUSH_WRITE_OVERFLOW: Push Queue Write Overflow. Overflow is defined as a store to the OCB Data [n] Register and the push_full facility is already set. This bit is cleared only by a firmware write of this bit to 0.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR2_PULL_READ_UNDERFLOW_EN: Enable the setting of pull_read_underflow by hardware. 0 = Underflow detection disabled 1 = Underflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
3	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR2_PUSH_WRITE_OVERFLOW_EN: Enable the setting of push_write_overflow by hardware. 0 = Overflow detection disabled 1 = Overflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
4	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR2_OCB_STREAM_MODE: Put the bridge channel in streaming mode with the behavior further defined by the setting of OCB_STREAM_TYPE. 0 = Stream mode disabled 1 = Stream mode enabled This bit is set using the OR mask register and cleared using the AND mask register.
5	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR2_OCB_STREAM_TYPE: Type of streaming enabled by OCB_STREAM_MODE = 1 0 = Linear 1 = Circular For linear type, the OCB_ADDRESS field is incremented by 8 with each access to the OCB Data [n] Register. In circular type, the address manipulation is through access to OCB Stream [Push-Pull] Increment registers. This bit is set using the OR mask register and cleared using the AND mask register.
6:7	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR2_SPARE0: Implemented but not used.
8	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR2_OCB_OCI_TIMEOUT: Indicates the MnTimeout signal on the OCI for the OCB master was asserted to flag that no OCI slave acknowledged the request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
9	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR2_OCB_OCI_READ_DATA_PARITY: Indicates the OCI read data parity was in error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
10	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR2_OCB_OCI_SLAVE_ERROR: Indicates the SlvError signal on the OCI for the OCB master was asserted. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
11	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR2_OCB_PIB_ADDR_PARITY_ERR: Indicates the PIB address parity was in error (PIB read or write operation). This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
12	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR2_OCB_PIB_DATA_PARITY_ERR: Indicates the PIB data parity was in error for a PIB write operation. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
13	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR2_SPARE1: Implemented but not used.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
14	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR2_OCB_FSM_ERR: Catastrophic state machine error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
15	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR2_SPARE2: Implemented but not used. Writes store the value. Reads return the last value written.
16:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_PIB OCB Error Status 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR2
Address	000000000006D054 (SCOM)
Description	OCB_PIB OCB Error Status 2 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RWX_WCLRREG	OCB_PIB_OCBESR2_OCB_ERROR_ADDR: OCI address being accessed when the first channel error is detected. This register is cleared upon writing any value.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_PIB OCB Data 2 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR2
Address	000000000006D055 (SCOM)
Description	OCB_PIB OCB Data 2 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	OCB_PIB_OCBDR2_OCB_DATA: Data to and from the OCI for this channel.

Register Name	OCB_PIB OCB Address 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR3
Address	000000000006D070 (SCOM)
Description	OCB_PIB OCB Address 3 Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	OCB_PIB_OCBAR3_OCI_REGION: OCI Address Space Region 0XX = Reserved 10X = Processor bus memory 110 = Register space 111 = SRAM
3:28	RW	OCB_PIB_OCBAR3_OCB_ADDRESS: Address of 8 B quantity the OCI for this channel. The field contents depends on accessed OCI_REGION processor bus. Bits 3:4 = 128 MB alias. Bits are not compared. Bits 3:11 = Maskable alignment (see PBA the specification). Bits 5:11 = 0b1111111. Bits 12:28 = Offset SRAM. Bits 12:28 = Offset.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	OCB_PIB OCB Control/Status 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR3
Address	000000000006D071 (SCOM) 000000000006D072 (SCOM1) 000000000006D073 (SCOM2)
Description	OCB_PIB OCB Control/Status 3 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR3_PULL_READ_UNDERFLOW: Pull Queue Read Underflow. Underflow is defined as a read to the OCB Data [n] Register and the PULL_EMPTY facility is already set. This bit is cleared only by a firmware write of this bit to 0. Writes store the value.
1	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR3_PUSH_WRITE_OVERFLOW: Push Queue Write Overflow. Overflow is defined as a store to the OCB Data [n] Register and the push_full facility is already set. This bit is cleared only by a firmware write of this bit to 0.
2	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR3_PULL_READ_UNDERFLOW_EN: Enable the setting of pull_read_underflow by hardware. 0 = Underflow detection disabled 1 = Underflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
3	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR3_PUSH_WRITE_OVERFLOW_EN: Enable the setting of push_write_overflow by hardware. 0 = Overflow detection disabled 1 = Overflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
4	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR3_OCB_STREAM_MODE: Put the bridge channel in streaming mode with the behavior further defined by the setting of OCB_STREAM_TYPE. 0 = Stream Mode Disabled 1 = Stream Mode Enabled. This bit is set using the OR mask register and cleared using the AND mask register.
5	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR3_OCB_STREAM_TYPE: Type of streaming enabled by OCB_STREAM_MODE = 1 0 = Linear 1 = Circular For linear type, the OCB_ADDRESS field is incremented by 8 with each access to the OCB Data [n] Register. In circular type, the address manipulation is through access to OCB Stream [Push-Pull] Increment registers. This bit is set using the OR mask register and cleared using the AND mask register.
6:7	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR3_SPARE0: Implemented but not used.
8	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR3_OCB_OCI_TIMEOUT: Indicates the MnTimeout signal on the OCI for the OCB master was asserted to flag that no OCI slave acknowledged the request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
9	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR3_OCB_OCI_READ_DATA_PARITY: Indicates the OCI read data parity was in error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
10	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR3_OCB_OCI_SLAVE_ERROR: Indicates the SlvError signal on the OCI for the OCB master was asserted. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
11	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR3_OCB_PIB_ADDR_PARITY_ERR: Indicates the PIB address parity was in error (PIB read or write operation). This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
12	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR3_OCB_PIB_DATA_PARITY_ERR: Indicates the PIB data parity was in error for a PIB write operation. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
13	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR3_SPARE1: Implemented but not used.
14	ROX	WOX_CLEAR	WOX_OR	OCB_PIB_OCBCSR3_OCB_FSM_ERR: Catastrophic state machine error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
15	RO	WO_CLEAR	WO_OR	OCB_PIB_OCBCSR3_SPARE2: Implemented but not used. Writes store the value. Reads return the last value written.
16:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_PIB OCB Error Status 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR3
Address	000000000006D074 (SCOM)
Description	OCB_PIB OCB Error Status 3 Register

Bits	SCOM	Field Mnemonic: Description
0:31	RWX_WCLRREG	OCB_PIB_OCBESR3_OCB_ERROR_ADDR: OCI address being accessed when the first channel error is detected. This register is cleared upon writing any value.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_PIB OCB Data 3 Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR3
Address	000000000006D075 (SCOM)
Description	OCB_PIB OCB Data 3 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	OCB_PIB_OCBDR3_OCB_DATA: Data to and from the OCI for this channel.

Register Name	OCB_PIB OCC Trace Debug Control Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OTDCR
Address	000000000006D110 (SCOM)
Description	OCB_PIB OCC Trace Debug Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_PIB_OTDCR_TRACE_BUS_EN: Trace Bus Enable.
1	RW	OCB_PIB_OTDCR_OCB_TRACE_MUX_SEL: OCB Trace Bus Mux_Select 0 = Select OCB group 1 1 = Select OCB group 2
2:3	RW	OCB_PIB_OTDCR_OCC_TRACE_MUX_SEL: OCC Trace Bus Mux Select. Connects to TRACE_MUX4 macro in OCC_TOP. 00 = Select PMC trace bus 01 = Unused 10 = Select SRAM trace bus 11 = Overview mode: SRAM(0:11) and PMC(0:11).
4:7	RW	OCB_PIB_OTDCR_OCI_TRACE_MUX_SEL: OCC Trace Bus Mux Select 0000 = Select OCB trace bus 0001 = Select TRACE_MUX4 trace data 0010 = Select PLB trace data 0011 = Reserved 0100 = Select GPE0 trace data 0101 = Select GPE1 trace data 0110 = Select GPE2 trace data 0111 = Select GPE3 trace data 1000 = Select OCC Overview Mode1 trace data 1001 = Select OCC Overview Mode2 trace data 1010:1111 = Unused.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_PIB OCC PowerPC 405 Cache Error Injection Control Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OPPCINJ
Address	000000000006D111 (SCOM)
Description	OCB_PIB OCC PowerPC 405 Cache Error Injection Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	OCB_PIB_OPPCINJ_OCI_ERR_INJ_DCU: Enable PowerPC 405 data cache error injection.
1	RW	OCB_PIB_OPPCINJ_OCI_ERR_INJ_ICU: Enable PowerPC 405 instruction cache error injection.
2	RW	OCB_PIB_OPPCINJ_OCI_ERR_INJ_CE_UE: Select CE or UE injection 0 = Inject CE 1 = Inject UE
3	RW	OCB_PIB_OPPCINJ_OCI_ERR_INJ_SINGL_CONT: Select single or continuous injection 0 = Inject until first error is detected 1 = Inject continuously
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_PIB OCC Special Timeout Error Address Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB_PIB_OSTOEAR
Address	000000000006D200 (SCOM)
Description	OCB_PIB OCC Special Timeout Error Address Register

Bits	SCOM	Field Mnemonic: Description
0:31	RO	OCB_PIB_OSTOEAR_OCC_SPCL_TIMEOUT_ADDR: OCC Special Timeout Address from PowerPC 405 access.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	OCB_PIB OCC Special Timeout Error Status Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB_PIB_OSTOESR
Address	000000000006D201 (SCOM)
Description	OCB_PIB OCC Special Timeout Error Status Register

Bits	SCOM	Field Mnemonic: Description
0	RW_WCLEAR	OCB_PIB_OSTOESR_ICU_TIMEOUT_ERROR: Indicates that a PowerPC 405 Instruction Cache operation encountered an OCI timeout.
1	RW_WCLEAR	OCB_PIB_OSTOESR_ICU_RNW: Indicates the type of PowerPC 405 Instruction Cache operation being performed that timed out.
2:3	RW_WCLEAR	OCB_PIB_OSTOESR_RESERVED_2_3: Reserved bits.
4	RW_WCLEAR	OCB_PIB_OSTOESR_DCU_TIMEOUT_ERROR: Status bit to indicate that a PowerPC 405 Data Cache operation encountered an OCI timeout.
5	RW_WCLEAR	OCB_PIB_OSTOESR_DCU_RNW: Indicates the type of PowerPC 405 Data Cache operation being performed that timed out.
6:7	RW_WCLEAR	OCB_PIB_OSTOESR_RESERVED_6_7: Reserved bits.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	OCB_PIB OCI Arbiter Revision ID
Mnemonic	TP.TPCHIP.OCC.OCI.OCB_PIB_OREV
Address	000000000006D202 (SCOM)
Description	OCB_PIB OCI Arbiter Revision ID

Bits	SCOM	Field Mnemonic: Description
0:63	RO	constant = 0b0000000000000000000000110000001000000000000000000000000000000000

Register Name	OCB_PIB OCI Error Status Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB_PIB_OESR
Address	000000000006D204 (SCOM)
Description	OCB_PIB OCI Error Status Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	OCB_PIB_OESR_OCI_M0_TIMEOUT_ERROR: Master 0 OCI timeout error status.
1	RWX_WCLEAR	OCB_PIB_OESR_OCI_M0_RW_STATUS: Master 0 read/write status.
2	RWX_WCLEAR	OCB_PIB_OESR_OCI_M0_OESR_FLCK: Master 0 OESR field lock.

Bits	SCOM	Field Mnemonic: Description
3	RWX_WCLEAR	OCB_PIB_OESR_OCI_M0_OEAR_LOCK: Master 0 OEAR address lock.
4	RWX_WCLEAR	OCB_PIB_OESR_OCI_M1_TIMEOUT_ERROR: Master 1 OCI timeout error status.
5	RWX_WCLEAR	2: Master 1 read/write status.
6	RWX_WCLEAR	OCB_PIB_OESR_OCI_M1_OESR_FLCK: Master 1 OESR field lock.
7	RWX_WCLEAR	OCB_PIB_OESR_OCI_M1_OEAR_LOCK: Master 0 OEAR address lock.
8	RWX_WCLEAR	OCB_PIB_OESR_OCI_M2_TIMEOUT_ERROR: Master 2 OCI timeout error status.
9	RWX_WCLEAR	OCB_PIB_OESR_OCI_M2_RW_STATUS: Master 2 read/write status.
10	RWX_WCLEAR	OCB_PIB_OESR_OCI_M2_OESR_FLCK: Master 2 OESR field lock.
11	RWX_WCLEAR	OCB_PIB_OESR_OCI_M2_OEAR_LOCK: Master 2 OEAR address lock.
12	RWX_WCLEAR	OCB_PIB_OESR_OCI_M3_TIMEOUT_ERROR: Master 3 OCI timeout error status.
13	RWX_WCLEAR	OCB_PIB_OESR_OCI_M3_RW_STATUS: Master 3 read/write status.
14	RWX_WCLEAR	OCB_PIB_OESR_OCI_M3_OESR_FLCK: Master 3 OESR field lock.
15	RWX_WCLEAR	OCB_PIB_OESR_OCI_M3_OEAR_LOCK: Master 3 OEAR address lock.
16	RWX_WCLEAR	OCB_PIB_OESR_OCI_M4_TIMEOUT_ERROR: Master 4 OCI timeout error status.
17	RWX_WCLEAR	OCB_PIB_OESR_OCI_M4_RW_STATUS: Master 4 read/write status.
18	RWX_WCLEAR	OCB_PIB_OESR_OCI_M4_OESR_FLCK: Master 4 OESR field lock.
19	RWX_WCLEAR	OCB_PIB_OESR_OCI_M4_OEAR_LOCK: Master 4 OEAR address lock.
20	RWX_WCLEAR	OCB_PIB_OESR_OCI_M5_TIMEOUT_ERROR: Master 5 OCI timeout error status.
21	RWX_WCLEAR	OCB_PIB_OESR_OCI_M5_RW_STATUS: Master 5 read/write status.
22	RWX_WCLEAR	OCB_PIB_OESR_OCI_M5_OESR_FLCK: Master 5 OESR field lock.
23	RWX_WCLEAR	OCB_PIB_OESR_OCI_M5_OEAR_LOCK: Master 5 OEAR address lock.
24	RWX_WCLEAR	OCB_PIB_OESR_OCI_M6_TIMEOUT_ERROR: Master 6 OCI timeout error status.
25	RWX_WCLEAR	OCB_PIB_OESR_OCI_M6_RW_STATUS: Master 6 read/write status.
26	RWX_WCLEAR	OCB_PIB_OESR_OCI_M6_OESR_FLCK: Master 6 OESR field lock.

Bits	SCOM	Field Mnemonic: Description
27	RWX_WCLEAR	OCB_PIB_OESR_OCI_M6_OEAR_LOCK: Master 6 OEAR address lock.
28	RWX_WCLEAR	OCB_PIB_OESR_OCI_M7_TIMEOUT_ERROR: Master 7 OCI timeout error status.
29	RWX_WCLEAR	OCB_PIB_OESR_OCI_M7_RW_STATUS: Master 7 read/write status.
30	RWX_WCLEAR	OCB_PIB_OESR_OCI_M7_OESR_FLCK: Master 7 OESR field lock.
31	RWX_WCLEAR	OCB_PIB_OESR_OCI_M7_OEAR_LOCK: Master 7 OEAR address lock.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_PIB OCI Error Address Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB_PIB_OEAR
Address	000000000006D206 (SCOM)
Description	OCB_PIB OCI Error Address Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	OCB_PIB_OEAR_OCI_TIMEOUT_ADDR: OCI timeout address.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**OCB_PIB OCI Arbiter Control Register**
Mnemonic	TP.TPCHIP.OCC.OCI.OCB_PIB_OACR
Address	000000000006D207 (SCOM)
Description	OCB_PIB OCI Arbiter Control Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	OCB_PIB_OACR_OCI_PRIORITY_MODE: OCI priority mode.
1:3	RWX	OCB_PIB_OACR_OCI_PRIORITY_ORDER: OCI priority order 000 = Masters 0, 1, 2, 3, 4, 5, 6, 7 001 = Masters 1, 2, 3, 4, 5, 6, 7, 0 010 = Masters 2, 3, 4, 5, 6, 7, 0, 1 011 = Masters 3, 4, 5, 6, 7, 0, 1, 2 100 = Masters 4, 5, 6, 7, 0, 1, 2, 3 101 = Masters 5, 6, 7, 0, 1, 2, 3, 4 110 = Masters 6, 7, 0, 1, 2, 3, 4, 5 111 = Masters 7, 0, 1, 2, 3, 4, 5, 6
4	RW	OCB_PIB_OACR_OCI_HI_BUS_MODE: High bus utilization (see the OCI arbiter documentation for description).
5:6	RW	OCB_PIB_OACR_OCI_READ_PIPELINE_CONTROL: Read pipeline control 00 = Read pipe lining disabled 01 = 2-deep read pipe 10 = 3-deep read pipe 11 = 4-deep read pipe

Bits	SCOM	Field Mnemonic: Description
7	RW	OCB_PIB_OACR_OCI_WRITE_PIPELINE_CONTROL: Write pipeline control 0 = Write pipe lining disabled 1 = 2-deep write pipe
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	OCB_PIB OCB Error Address Register
Mnemonic	TP.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBEAR
Address	000000000006D210 (SCOM)
Description	OCB_PIB OCB Error Address Register

Bits	SCOM	Field Mnemonic: Description
0:31	RWX_WCLRPART	OCB_PIB_OCBEAR_OCB_ERROR_ADDRESS: Captured address upon OCI errors.
32:34	RWX_WCLRPART	OCB_PIB_OCBEAR_RESERVED_32_34: Reserved bits.
35	RWX_WCLRPART	OCB_PIB_OCBEAR_DIRECT_BRIDGE_SOURCE: Address was source from the direct bridge.
36	RWX_WCLRPART	OCB_PIB_OCBEAR_INDIRECT_BRIDGE_0_SOURCE: Address was source from the indirect bridge 0.
37	RWX_WCLRPART	OCB_PIB_OCBEAR_INDIRECT_BRIDGE_1_SOURCE: Address was source from the indirect bridge 1.
38	RWX_WCLRPART	OCB_PIB_OCBEAR_INDIRECT_BRIDGE_2_SOURCE: Address was source from the indirect bridge 2.
39	RWX_WCLRPART	OCB_PIB_OCBEAR_INDIRECT_BRIDGE_3_SOURCE: Address was source from the indirect bridge 3.
40:63	RO	constant = 0b000000000000000000000000

Register Name	The SSCR0 Provides the Length Control Information for the P2S Frames
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIMPSS_ADC_CTRL_REG0
Address	0000000000070000 (SCOM)
Description	The SSCR0 provides the length control information for the P2S frames.

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	HWCTRL_FRAME_SIZE: Number of data bits per individual SPI transaction (also referred to as frame) during chip select assertion. Supported values: 0x10 (16d) Chip select assertion duration is SPI_FRAME_SIZE + 2.
6:11	RWX	HWCTRL_OUT_COUNT: Number of bits sent out MOSI of the frame. Supported values: 0x000 to SPI_FRAME_SIZE. Values beyond SPI_FRAME_SIZE are ignored.
12:17	RWX	HWCTRL_IN_DELAY: Number of SPI clocks after chip select to wait before capturing MISO input. Supported values: 0x000 to SPI_FRAME_SIZE. Values beyond SPI_FRAME_SIZE result in the input never being captured.
18:23	RWX	HWCTRL_IN_COUNT: Number of bits captured on MISO input. Supported values: 0x000 to SPI_FRAME_SIZE. The actual number of bits captured is SPI_FRAME_SIZE - SPI_IN_DELAY.

Register Name	The SSCR1 Provides All Control Bits for the SPI ADC Interface
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_CTRL_REG1
Address	0000000000070001 (SCOM)
Description	The SSCR1 provides all control bits for the SPI ADC interface. This interface does not support CRC.

Bits	SCOM	Field Mnemonic: Description
0	RWX	HWCTRL_FSM_ENABLE: If set to 1 the ADC FSM can be used to control the SPI interface.
1	RWX	HWCTRL_DEVICE: Select the device on the ADC bus to target: 0 = Chip select 0. 1 = Chip select 1.
2	RWX	HWCTRL_CPOL: SPI clock polarity. If CPOL = 0, CLK IDLE is deasserted. If CPOL = 1, CLK IDLE is asserted.
3	RWX	HWCTRL_CPHA: SPI clock phase. If CPHA = 0, first edge sample , second_edge change If CPHA = 1, first edge change, second_edge sample
4:13	RWX	HWCTRL_CLOCK_DIVIDER: SPI clock speed divider to divide the NEST_NCLK/4 mesh clock, which results in a SPI frequency SPI_freq = NEST_FREQ/(8 * [clock_divider + 1]). Therefore, for a 2.4 GHz nest clock, the interchip clock can be theoretically adjusted between 300 MHz and 0.29MHz (cycle time 1.66ns…3.41 us, in 1.66 ns steps). However, because of some constraints, a practical range is 0.5…75 MHz. Allowed values: 0x003…0x3FF. Because of metastability constraints, only use values > 2 for INTERCHIP_CLOCK_DIVIDER. Otherwise, data will not be sampled correctly.
14:17	RWX	HWCTRL_NR_OF_FRAMES: Specifies the number of frames for each iteration of ADC sampling (legal values are 0,1, 2, …, 15).
18	RWX	HWCTRL_WRITE_WHILE_BRIDGE_BUSY_SCRESP_EN: If this bit is ‘1’ (enabled), if a write into the registers of HWCTRL in the middle of operation is attempted, it sends the BUSY_RESPONSE code, which is given in bits [19:21].
19:21	RWX	BUSY_RESPONSE_CODE: Busy response code for the bit 18.

Register Name	The SSCR2 Provides all Control Bits for the SPI ADC Interface
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_CTRL_REG2
Address	0000000000070002 (SCOM)
Description	The SSCR2 provides all control bits for the SPI ADC interface. This interface does not support ECC.

Bits	SCOM	Field Mnemonic: Description
0:16	RWX	HWCTRL_INTER_FRAME_DELAY: A delay between two frames of a two-command set as measured from the end of the last bit of the first frame until the chip select of the second frame, which contains the status, is asserted. This delay allows for the ADC chip to acquire the next value… Delay is computed as: (value * ~100 ns_hang_pulse) +0/-~100 ns_hang_pulse time. 0x00000: Wait 1 SPI clock. 0x00001 = 0x1FFFF: value = number of ~100ns_hang_pulses. The maximum delay at 0x1FFFF: 131071* 100 ns = 13.1 ms. Firmware must ensure that the delay is at least one SPI clock. In the case of of APSS with analog-to-digital converter (ADC), this delay allows for acquisition of the next reading when using a continuous acquisition mode. (TI specs indicate 325ns).

Register Name	The SSSR Displays the Current Status about SPI
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_STATUS_REG
Address	0000000000070003 (SCOM)
Description	Related activities.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HWCTRL_ONGOING: The SPI interface is in progress of shifting data. This bit is provided, as a wire, to the OCC interrupt controller. The FW can poll on this bit to wait for valid data.
1	ROX	ADC_RESERVED_1: Implemented but not used.
2	ROX	ADC_RESERVED_2: Implemented but not used.
3	ROX	ADC_RESERVED_3: Implemented but not used.
4	ROX	HWCTRL_INVALID_NUMBER_OF_FRAMES: if this bit is asserted, a nonsupported number of frames was set in SPIPSS_ADC_CTRL_REG1. This bit is cleared upon the next enabled command that has a legal number of frames.
5	NCX	HWCTRL_WRITE_WHILE_FSM_BUSY_ERR: Indicates that firmware attempted to perform an PIB write to the any writable register while the ADC FSM is busy (ADC_ONGOING = 1), which causes undefined bridge behavior. This bit can only be reset by doing proper reset operation using reset register.
6	ROX	ADC_RESERVED_6: Implemented but not used.
7	ROX	HWCTRL_FSM_ERR: Indicates a catastrophic FSM error in the PIB2SPI control FSM.

Register Name	The SSCR Provided a way to Start the ADC Sampling
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_CMD_REG
Address	0000000000070004 (SCOM)
Description	The SSCR provided a way to start the ADC sampling.

Bits	SCOM	Field Mnemonic: Description
0	RWX	HWCTRL_START_SAMPLING: If bit set to 1 this register immediately resets itself and starts the ADC sampling only if ADC_FSM_ENABLE is enabled otherwise it will not trigger the sampling.

Register Name	Reset Complete HWCTRL SPIPSS
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RESET_REGISTER
Address	0000000000070005 (SCOM)
Description	Writes into this register with a proper value resets complete HWCTRL SPIPSS.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	HWCTRL_RESET: Writing value 01 on this will reset.

Register Name	Configure SPI Data
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_WDATA_REG
Address	0000000000070010 (SCOM)
Description	The SSWDR register is used to configure the SPI data that is shifted out for each frame to the SPIADC.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX	HWCTRL_WDATA: These 16bits are shifted out of the SPI interface to the ADC every time a frame is read.

Register Name	**The SRDR0 Displays the Read Data for Frames 0 - 3**
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RDATA_REG0
Address	0000000000070020 (SCOM)
Description	The SRDR0 displays the read data for frames 0 to 3. Note to FW: This register should be read last, if the dial ENABLE_RESTART_ADC_SAMPLING_AFTER_LAST_READ is enabled.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HWCTRL_RDATA0: Bits 0:15 = Frame 0 read data Bits 16:31 = Frame 1 read data Bits 32:47 = Frame 2 read data Bits 48:63 = Frame 3 read data

Register Name	**The SRDR1 Displays the Read Data for Frames 4 - 7**
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RDATA_REG1
Address	0000000000070021 (SCOM)
Description	The SRDR1 displays the read data for frames 4 to 7.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HWCTRL_RDATA1: Bits 0:15 = Frame 4 read data Bits 16:31 = Frame 5 read data Bits 32:47 = Frame 6 read data Bits 48:63 = Frame 7 read data

Register Name	**The SRDR2 Displays the Read Data for Frames 8 - 11**
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RDATA_REG2
Address	0000000000070022 (SCOM)
Description	The SRDR2 displays the read data for frames 8 to 11.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HWCTRL_RDATA2: Bits 0:15 = Frame 8 read data Bits 16:31 = Frame 9 read data Bits 32:47 = Frame 10 read data Bits 48:63 = Frame 11 read data

Register Name	**The SRDR2 Displays the Read Data for Frames 8 - 11**
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RDATA_REG3
Address	0000000000070023 (SCOM)
Description	The SRDR2 displays the read data for frames 8 to 11.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HWCTRL_RDATA3: Bits 0:15 = Frame 12 read data Bits 16:31 = Frame 13 read data Bits 32:47 = Frame 14 read data Bits 48:63 = Frame 15 read data

Register Name	**The S100R Register Defines the Number of Nest/4 Cycles**
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_100NS_REG
Address	0000000000070028 (SCOM)
Description	The S100R register defines the number of nest/4 cycles approximately every 100 ns as the decrementer is reloaded with this value until reaching 0. At the 0 value, a pulse is generated to represent an approximate 100 ns interval.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	REG_100NS_OUT: The value should correspond to 100 ns.

Register Name	**The PPCR0A Provides the Length Control Information for the P2S Frames**
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_P2S_CTRL_REG0
Address	0000000000070040 (SCOM)
Description	The PPCR0A provides the length control information for the P2S frames

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	P2S_FRAME_SIZE: Number of data bits per individual SPI transaction (also referred to as frame) during chip select assertion. Supported values: 0x10 (16d), Chip Select assertion duration is SPI_FRAME_SIZE + 2.
6:11	RWX	P2S_OUT_COUNT1: Number of bits sent out MOSI in frame 1 of a 2 frame set (the arbitration unit). Supported values: 0x000 to SPI_FRAME_SIZE. Values beyond SPI_FRAME_SIZE are ignored.
12:17	RWX	P2S_IN_DELAY1: Number of SPI clocks after chip select to wait before capturing MISO input in frame 1. Supported values: 0x000 to SPI_FRAME_SIZE. Values beyond SPI_FRAME_SIZE result in the input never being captured.
18:23	RWX	P2S_IN_COUNT1: Number of bits captured on MISO input in frame 1. Supported values: 0x000 to SPI_FRAME_SIZE. The actual number of bits captured is SPI_FRAME_SIZE - SPI_IN_DELAY.
24:29	RWX	P2S_OUT_COUNT2: Number of bits sent out MOSI in frame 2 of a 2 frame set (the arbitration unit). Supported values: 0x000 to SPI_FRAME_SIZE. Values beyond SPI_FRAME_SIZE are ignored.
30:35	RWX	P2S_IN_DELAY2: Number of SPI clocks after chip select to wait before capturing MISO input in frame 2. Supported values: 0x000 to SPI_FRAME_SIZE. Values beyond SPI_FRAME_SIZE result in the input never being captured.
36:41	RWX	P2S_IN_COUNT2: Number of bits captured on MISO input in frame 2. Supported values: 0x000 to SPI_FRAME_SIZE. The actual number of bits captured is SPI_FRAME_SIZE - SPI_IN_DELAY.

Register Name	The SSCR1 provides control bits for the P2S Bridge interface
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_P2S_CTRL_REG1
Address	0000000000070041 (SCOM)
Description	The SSCR1 provides control bits for the P2S bridge interface. This interface does not support CRC.

Bits	SCOM	Field Mnemonic: Description
0	RWX	P2S_BRIDGE_ENABLE: If set to 1 the PIB2SPI bridge can be used to control the SPI interface. If set to 0, the PIB2SPI bridge is disabled.
1	RWX	P2S_DEVICE: Select the device on the ADC bus to target: 0 = Chip select 0 1 = Chip select 1
2	RWX	P2S_CPOL: SPI clock polarity. If CPOL = 0, CLK IDLE is deasserted. If CPOL = 1, CLK IDLE is asserted.
3	RWX	P2S_CPHA: SPI clock phase. If CPHA = 0, change or sample values of data signals on the first edge. Otherwise, change or sample values of data signals on the second edge.
4:13	RWX	P2S_CLOCK_DIVIDER: SPI clock speed divider to divide the NEST_NCLK/4 mesh clock, which results in a SPI frequency SPI_freq = NEST_FREQ/(8 * [clock_divider + 1]). For a 2.4 GHz nest clock, the interchip clock can be theoretically adjusted between 300 MHz and 0.29 MHz (cycle time 1.66 ns…3.41 us, in 1.66 ns steps). However, because of some constraints, a practical range is 0.5…75MHz. Allowed values: 0x003…0x3FF. Because of metastability constraints, only use values > 2 for INTERCHIP_CLOCK_DIVIDER. Otherwise data will not be sampled correctly.
14:16	RWX	RESERVED: Implemented but not used.
17	RWX	P2S_NR_OF_FRAMES: Specifies the number of frames sent in the frame set (number of frames before the arbitration unit rearbitrates). 0 = 1 frame 1 = 2 frames
18	RWX	P2S_WRITE_WHILE_BRIDGE_BUSY_SCRESP_EN: If this bit is ‘1’ (enabled), if somebody tries to write into the registers of P2S bridge in the middle of operation, it sends out the BUSY_RESPONSE code, which is given in the bit [19:21].
19:21	RWX	BUSY_RESPONSE_CODE_NO_1: Busy response code for the bit 18.

Register Name	The SSCR2 Provides all Control Bits for the SPI ADC Interface
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_P2S_CTRL_REG2
Address	0000000000070042 (SCOM)
Description	The SSCR2 provides all control bits for the SPI ADC interface. This interface does not support ECC.

Bits	SCOM	Field Mnemonic: Description
0:16	RWX	P2S_INTER_FRAME_DELAY: Delay between two frames of a two command set as measured from the end of the last bit of the first frame until the chip select of the second frame, which contains the status, is asserted. This delay allows for the checking and status data the production in the addressed chip. Delay is computed as: (value * ~100 ns_hang_pulse) +0/-~100 ns_hang_pulse time. 0x00000: Wait 1 SPI Clock. 0x00001 - 0x1FFFF: value = number of ~100ns_hang_pulses. Maximum delay at 0x1FFFF: 131071* 100 ns = 13.1 ms. Firmware has to make sure that the delay is at least one SPI clock.

Register Name	The SSSR Displays the Current Status about SPI
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_P2S_STATUS_REG
Address	0000000000070043 (SCOM)
Description	Related activities.

Bits	SCOM	Field Mnemonic: Description
0	ROX	P2S_ONGOING: Indicates that a bridge transaction is queued or in progress of being executed. This bit is set by hardware while an operation is queued or in progress and will be be reset by hardware when the operation is complete.
1	ROX	P2S_RESERVED_1: Implemented but not used.
2	ROX	P2S_RESERVED_2: Implemented but not used.
3	ROX	P2S_RESERVED_3: Implemented but not used.
4	ROX	P2S_RESERVED_4: Implemented but not used.
5	NCX	P2S_WRITE_WHILE_BRIDGE_BUSY_ERR: Indicates that firmware attempted to perform a PIB write to the any register while the P2S bridge is busy, which causes undefined bridge behavior. This bit can only be reset by doing proper reset operation using reset register.
6	ROX	RESERVED6: Implemented but not used.
7	ROX	P2S_FSM_ERR: Indicates a catastrophic FSM error in the PIB2SPI control FSM.

Register Name	The SSCR Provides the Means to Start the P2S Bridge
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_P2S_COMMAND_REG
Address	0000000000070044 (SCOM)
Description	The SSCR provides the means to start the P2S bridge

Bits	SCOM	Field Mnemonic: Description
0	RWX	P2S_START_COMMAND: If set to ‘1’ and ENABLE_PIB2SPI_BRIDGE = ‘1’, this register immediately resets itself and starts the P2S operation. If ENABLE_PIB2SPI_BRIDGE = ‘0’. This register immediately resets itself but no operation is started.

Register Name	Write into this Register with the Proper Value Resets P2S_ SPIPSS
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_P2S_RESET_REGISTER
Address	0000000000070045 (SCOM)
Description	Write into this register with proper value will reset P2S_ SPIPSS

Bits	SCOM	Field Mnemonic: Description
0:1	RW	P2S_RESET: Writing value 01 on this will reset.

Register Name	The SPW Register is used for the Most Significant 4 B of Write Data through the P2S Bridge
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_P2S_WDATA_REG
Address	0000000000070050 (SCOM)
Description	The SPW register is used for the most significant 4 B of write data through the p2s bridge. A write to this register starts the SPI transaction (read or write), if the switch ENABLE_PIB2P2S_BRIDGE is set.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	P2S_WDATA: Bits 0 to 31 of SPI data packet.

Register Name	The SPR Register Is used for the Most-Significant 4 B Of Read Data of the P2S Bridge
Mnemonic	TP.TPCHIP.PIB.SPIADC.SPIPSS_P2S_RDATA_REG
Address	0000000000070060 (SCOM)
Description	The SPR register is used for the most significant 4 B of read data of the P2S bridge. After the P2S_ONGOING bit has dropped, the read values are available in SPR.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	P2S_RDATA: Bits 0:31 of SPI data packet.

Register Name	Provides the controllability in Handling the Auto Increment/Decrement Address Pointer In Indirect Mode from both Access
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.PIBMEM_CONTROL_REGISTER
Address	0000000000088000 (SCOM)
Description	Provides the controllablity in handling the auto increment/decrement address pointer in indirect mode from both access.

Bits	SCOM	Field Mnemonic: Description
0	RWX	AUTO_PRE_INCREMENT_PIB: 1 = When AUTO_INCREMENT_REGISTER is read/written from the PIB side, data is read/written into the array after the address pointer is incremented. 0 = When AUTO_INCREMENT_REGISTER is read/written, data is read/written into array before address pointer is incremented. Default_value = 0.
1	RWX	AUTO_POST_DECREMENT_PIB: 1 = When AUTO_DECREMENT_REGISTER is read or written from the PIB side, data will be read or written into the array before the address pointer is decremented. 0 = When AUTO_DECREMENT_REGISTER is read/written, data will be read or written into the array after address pointer is decremented. Default_value = 0.
2	RWX	DISABLE_ECC: 1 = Disables the ECC checking and calculating. 0 = Sends ECC and checks the ECC for the array data.
3	RWX	AUTO_PRE_INCREMENT_FACES: 1 = When the AUTO_INCREMENT_REGISTER is read or written from fast access side, data will be read/written into the array after the address pointer is incremented. 0 = When the AUTO_INCREMENT_REGISTER is read or written, data will be read or written into the array before address pointer is incremented. Default_value = 0.
4	RWX	AUTO_POST_DECREMENT_FACES: 1 = When AUTO_DECREMENT_REGISTER is read/written from fast access side, data will be read/written into array before the address pointer is decremented. 0 = When AUTO_DECREMENT_REGISTER is read/written, data will be read/written into array after address pointer is decremented. Default_value:0.
5	RWX	CHKSW_AR012: Debug switch to disable the enhanced PIB error handling.

Register Name	Indirect Address Pointer
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.PIBMEM_ADDRESS_REGISTER
Address	0000000000088001 (SCOM)
Description	Indirect address pointer

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	ADDRESS_POINTER: 0x0000 = Accesses location 0 of the array. 0x0001 = Accesses the first location of the array.

Register Name	Status of PIBMEM Controller
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.PIBMEM_STATUS_REG
Address	0000000000088005 (SCOM)
Description	Status of PIBMEM controller

Bits	SCOM	Field Mnemonic: Description
0	ROX	ADDR_INVALID_PIB: The address that the PIB is trying to access in the PIBMEM is not the valid.
1	ROX	WRITE_INVALID_PIB: The address for which the PIB is trying to write is not writable.
2	ROX	READ_INVALID_PIB: The address for which the PIB is trying to read is not readable.
3	ROX	ECC_UNCORRECTED_ERROR_PIB: Uncorrectable error occurred while PIB memory read. This also go out as FIR error.
4	ROX	ECC_CORRECTED_ERROR_PIB: Corrected error in PIB MEM read. Data can still be considered as good. This is an error O/P of the ECC_CHECK_CORRECTION block.
5	ROX	Reserved field.
6	ROX	WRITE_RST_INTERRUPT_PIB: This bit gets set, when a reset occurred during write operation to PIBMEM from PIB side. It is sticky status bit.
7	ROX	READ_RST_INTERRUPT_PIB: This bit gets set, when a reset occurred during read operation to PIBMEM from PIB side. It is sticky status bit.
8:11	RO	constant = 0b0000
12:18	ROX	FSM_PRESENT_STATE: State machines present state. 0000001 = ECC_CHK. Performs ECC checking in this state. 0000010 = READ_ARRAY. Performs read operation to array in this state. 0000100 = READ_SETUP. Checks for errors in this state. 0001000 = ACK. Gives out the acknowledgment to the PIB. 0010000 = WRITE_ARRAY. Writes data into the array. 0100000 = ECC_GEN. ECC generation happens for the write operation. 1000000 = IDLE. Default state.
19	ROX	ADDR_INVALID_FACES: The address that is given by the fast access interface. To access in PIBMEM is not valid.
20	ROX	WRITE_INVALID_FACES: The address that is given by the fast access interface. To access in PIBMEM is not valid one in PIBMEM or not writable.
21	ROX	READ_INVALID_FACES: The address that is given by the fast access interface. To access is not readable.
22	ROX	ECC_UNCORRECTED_ERROR_FACES: Uncorrectable error occurred while fast access interface was read.

Bits	SCOM	Field Mnemonic: Description
23	ROX	ECC_CORRECTED_ERROR_FACES: Corrected error in fast access read operation. Data can still be considered as good. This is an error O/P of the ECC_CHECK_CORRECTION block.
24	ROX	BAD_ARRAY_ADDRESS_FACES: Wrong address accessed in indirect mode of operation from fast access interface. It is a sticky status bit.
25	ROX	WRITE_RST_INTERRUPT_FACES: This bit is set when a reset occurred during a write operation to PIBMEM from fast access side. It is a sticky status bit.
26	ROX	READ_RST_INTERRUPT_FACES: This bit is set when a reset occurred during a read operation to PIBMEM from fast access side. It is sticky status bit.
27:31	RO	constant = 0b00000
32:47	ROX	ADDR_RESET_INTR_PIB: Address information of reset interrupted transaction from the PIB side.
48:63	ROX	ADDR_RESET_INTR_FACES: Address information of reset interrupted transaction from the FAST ACESS side.

Register Name	Write into this Register with Proper the Value will Reset Complete PIBMEM Controller Except Array
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.PIBMEM_RESET_REGISTER
Address	0000000000088006 (SCOM)
Description	A write into this register with the proper value will reset complete PIBMEM controller except array.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	RESET: Writing value 10 on this will reset PIBMEM.

Register Name	Indirect Address Pointer
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.PIBMEM_ADDRESS_REGISTER_FA
Address	0000000000088007 (SCOM)
Description	Indirect Address Pointer

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	ADDRESS_POINTER_FA: If the value on this is. 0x0000 = Accesses location 0 of the array. 0x0001 = Accesses the first location of the array.

Register Name	FIR Error Mask Register
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.FIR_MASK_REGISTER
Address	0000000000088008 (SCOM)
Description	FIR Error Mask Register

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b000
3	RWX	MASK_ECC_UNCORRECTED_ERR_PIB: Bit allows to mask ECC uncorrected error for PIB transaction in generation of the FIR error.
4	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
5	RWX	MASK_BAD_ARRAY_ADDR_PIB: Bit allows masking of a bad array address error for PIB transactions in the generation of a FIR error.
6	RWX	MASK_WRT_RST_INTRPT_PIB: Bit allows masking of write reset interrupts for PIB transactions in the generation of a FIR error.
7	RWX	MASK_RD_RST_INTRPT_PIB: Bit allows masking of read reset interrupts for PIB transactions in the generation of a FIR error.
8:21	RO	constant = 0b00000000000000
22	RWX	MASK_ECC_UNCORRECTED_ERR_FACES: Bit allows masking of ECC uncorrected errors for fast access transaction in the generation of the FIR error.
23	RO	constant = 0b0
24	RWX	MASK_BAD_ARRAY_ADDR_FACES: Bit allows masking of bad array address errors for fast access transactions in the generation of the FIR error.
25	RWX	MASK_WRT_RST_INTRPT_FACES: Bit allows masking of a write reset interrupt errors for fast access transaction in the generation of the FIR error.
26	RWX	MASK_RD_RST_INTRPT_FACES: Bit allows masking read reset interrupt errors for fast access transactions in the generation of the FIR error.
27	RO	constant = 0b0

Register Name	Holds Repair Data for the Array
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.PIBMEM_REPAIR_REGISTER_0
Address	000000000008800B (SCOM)
Description	Holds repair data for the array

Bits	SCOM	Field Mnemonic: Description
0:1	RW	REPAIR_DATA_0: Repair Data Load Control Register. 0 = Enables the MUX selecting repair data from this register. 1 = Fence ABIST_START_TEST to PIBMEM ABIST engine. 2:63 = Reserved.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Holds Repair Data for the Array
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.PIBMEM_REPAIR_REGISTER_1
Address	000000000008800C (SCOM)
Description	Holds repair data for the array.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	REPAIR_DATA_1: Parallel register through which repair data can be loaded directly on to the repair chain of the array. 0:7 = Repair data for array-1. 8:15 = Repair data for array-2. 16:23 = Repair data for array-3. 24:31 = Repair data for array-4. 32:39 = Repair data for array-5. 40:47 = Repair data for array-6. 48:55 = Repair data for array-7. 56:63 = Repair data for array-8.

Register Name	Holds repair data for the array
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.PIBMEM_REPAIR_REGISTER_2
Address	000000000008800D (SCOM)
Description	Holds repair data for the array

Bits	SCOM	Field Mnemonic: Description
0:63	RW	REPAIR_DATA_2: Parallel register through which repair data can be loaded directly on to the repair chain of the array. 0:7 = Repair data for array-9. 8:15 = Repair data for array-10. 16:23 = Repair data for array-11. 24:31 = Repair data for array-12. 32:39 = Repair data for array-13. 40:47 = Repair data for array-14. 48:55 = Repair data for array-15. 56:63 = Repair data for array-16.

Register Name	Holds Repair Data for the Array
Mnemonic	TP.TPCHIP.PIB.POREMEM.PIBMEM.CTRL_MAC.PIBMEM_REPAIR_REGISTER_3
Address	000000000008800E (SCOM)
Description	Holds repair data for the array

Bits	SCOM	Field Mnemonic: Description
0:63	RW	REPAIR_DATA_3: Parallel register through which repair data can be loaded directly on to the repair chain of the array. 0:7 = Repair data for array-17. 8:15 = Repair data for array-18. 16:23 = Repair data for array-19. 24:31 = Repair data for array-20. 32:39 = Repair data for array-21. 40:47 = Repair data for array-22. 48:55 = Repair data for array-23. 56:63 = Repair data for array-24.

Register Name	Alter/Display Control Register
Mnemonic	BRIDGE.AD.ALTD_ADDR_REG
Address	0000000000090000 (SCOM)
Description	Alter/Display Control Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:63	RWX	FBC_ALTD_ADDRESS: The address bits [8:63] to use with the Alter/Display command.

Register Name	Alter/Display Command Register
Mnemonic	BRIDGE.AD.ALTD_CMD_REG
Address	0000000000090001 (SCOM)
Description	Alter/Display Command Register

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant = 0b00
2	NCX	FBC_ALTD_START_OP: Start the fabric alter/display operation (latch resets after arbitration passed).
3	NCX	FBC_ALTD_CLEAR_STATUS: Clear the Fabric Alter/Display Status Register.
4	NCX	FBC_ALTD_RESET_FSM: Reset the Fabric Alter/Display State Machine and Status Registers. For exceptional use only.
5	RW	FBC_ALTD_RNW: The read or write control for the fabric alter/display command. Read = 1 Write = 0 Setting must match FBC_ALTD_TTYPE.
6	RWX	FBC_ALTD_AXTYPE: Address only type command. No data transfer will be done.
7	RW	FBC_ALTD_DATA_ONLY: Skip the CMD-CRESP part and only send a data packet with FBC_ALTD_ADDRESS(0:13) as TTAG. The address bits [57:59] are sent to the HT-Data ramp too.
8:9	RO	constant = 0b00
10	NCX	Reserved field.
11	RWX	FBC_LOCKED: Set when the locked the ALTD_CMD_REG, ALTD_ADDRESS_REG, and ALTD_DATA_REG.
12:15	ROX	FBC_LOCK_ID: Reading current lock owner (only valid when locked). Writing current owner when overwrite the lock.
16:18	RWX	FBC_ALTD_SCOPE: The broadcast scope of the command.
19	RW	FBC_ALTD_AUTO_INC: The Fabric Alter/Display will autoincrement the address and issue the next command. Auto Increment = 1. Address will increment by 8, and the next command will be issued after current command is completed. Regular = 0. Alter/Display will issue one command and stop.
20	RWX	FBC_ALTD_DROP_PRIORITY: Initial command drop priority. Specifying which commands are dropped because of Processor bus congestion first.
21	RW	FBC_ALTD_DROP_PRIORITY_MAX: Maximal value the command drop priority can increase to (if not already bigger).
22	RW	FBC_ALTD_OVERWRITE_PBINIT: Start this command even when PBINIT is low.
23	RW	FBC_ALTD_PIB_DIRECT:Copy ALTD_ADRESS_REG to PIB_DIRECT_CMD and ALTD_DATA_REG to the PIB_DIRECT_DATA register instruction. Must not use the XSCOM of this ADU until done.
24	RW	FBC_ALTD_WITH_TM_QUIESCE: Set and wait for the local token manager quiesce before the processor bus QUIESCE or ALTD command.
25:31	RW	FBC_ALTD_TTYPE: The TTYPE used in the Alter/Display command. Supported values are: CI partial write DMA partial write CI partial read DMA read PB operation (AXTYPE)

Bits	SCOM	Field Mnemonic: Description
32:39	RW	FBC_ALTD_TSIZE: The TSIZE used in the Alter/Display command. Supported values: 1, 2, 4 and 8 bytes. Important: The encoding of this is the processor bus secondary encode. Thus, it is defined differently for each TTYPE.

Register Name	Alter/Display Special Option Register
Mnemonic	BRIDGE.AD.ALTD_OPTION_REG
Address	0000000000090002 (SCOM)
Description	All bits are reset when used.

Bits	SCOM	Field Mnemonic: Description
0:21	RO	constant = 0b00000000000000000000
22	RWX	FBC_ALTD_WITH_PBINIT_LOW_WAIT: Wait for the PBINIT signal to be dropped before continuing.
23	RWX	FBC_ALTD_WITH_PRE_QUIESCE: Sent out a processor bus quiesce command before executing the ALTD command.
24:27	RO	constant = 0b0000
28:47	RWX	FBC_ALTD_AFTER_QUIESCE_WAIT_COUNT: Time to wait between QUIESCE and ALTD command.
48:50	RO	constant = 0b000
51	RWX	FBC_ALTD_WITH_POST_INIT: Sent out a processor bus INIT command after executing the command.
52:53	RO	constant = 0b00
54:63	RWX	FBC_ALTD_BEFORE_INIT_WAIT_COUNT: Time to wait between ALTD command and INIT.

Register Name	Alter/Display Status Register
Mnemonic	BRIDGE.AD.ALTD_STATUS_REG
Address	0000000000090003 (SCOM)
Description	Alter/Display Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	FBC_ALTD_WAIT_CMD_ARBIT: Waiting for arbiter to send the command out.
2	ROX	FBC_ALTD_ADDR_DONE: The address portion of the fabric alter/display operation is complete.
3	ROX	FBC_ALTD_DATA_DONE: The data portion of the fabric alter/display operation is complete.
4	ROX	FBC_ALTD_WAIT_RESP: Waiting on a clean combined response.
5	RWX_WCLRREG	FBC_ALTD_OVERRUN_ERROR: Overrun error indicates new data was written before the previous data was used or a read was performed without new data arrived.
6	RWX_WCLRREG	FBC_ALTD_AUTOINC_ERROR: Autoincrement Error indicates internal address counter rolled over the 0.5 M boundary.
7	RWX_WCLRREG	FBC_ALTD_COMMAND_ERROR: Command Error indicates a new command was issued before the previous one finished.
8	RWX_WCLRREG	FBC_ALTD_ADDRESS_ERROR: Invalid Address Error: Processor bus response with address error combined response.

Bits	SCOM	Field Mnemonic: Description
9	RWX_WCLRREG	FBC_ALTD_PB_OP_HANG_ERR: Processor bus Timeout while waiting for combined response.
10	RWX_WCLRREG	FBC_ALTD_PB_DATA_HANG_ERR: Processor bus Timeout while waiting for data.
11	RWX_WCLRREG	FBC_ALTD_PB_UNEXPECT_CRESP_ERR: Combined response from Processor bus received at a time it is not expected by FSM.
12	RWX_WCLRREG	FBC_ALTD_PB_UNEXPECT_DATA_ERR: Data from Processor bus received at a time it is not expected by FSM.
13:15	RO	constant = 0b000
16	ROX	FBC_ALTD_WAIT_PIB_DIRECT: Waiting on XSCOM state machine to complete a direct PIB (write) command.
17	ROX	FBC_ALTD_PIB_DIRECT_DONE: Completed a direct to PIB (write) command.
18	ROX	FBC_ALTD_PBINIT_MISSING: Attempt to start a command without PB_INIT active. It stays blocked until PB_INIT is set or overridden. A reset or clear both aborts the pending operation.
19:32	RO	constant = 0b00000000000000
33:37	ROX	FBC_ALTD_PIB_ERROR: PIB slave error indicates what kind of PIB slave error occurred.
38:47	RO	constant = 0b0000000000
48	RWX_WCLRREG	FBC_ALTD_ECC_CE: Correctable ECC error detected and corrected during an FBC_ALTD transaction (read).
49	RWX_WCLRREG	FBC_ALTD_ECC_UE: Uncorrectable ECC error detected during an FBC_ALTD transaction (read).
50	RWX_WCLRREG	FBC_ALTD_ECC_SUE: Special uncorrectable ECC error detected during FBC_ALTD transaction (read).
51:58	RO	constant = 0b00000000
59:63	ROX	FBC_ALTD_CRESP_VALUE: The combined response value. Not cleared. It might contain old or invalid value until combined response arrived.

Register Name	Alter/Display Data Register
Mnemonic	BRIDGE.AD.ALTD_DATA_REG
Address	0000000000090004 (SCOM)
Description	Alter/Display Data Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	FBC_ALTD_DATA: The data to use with the alter/display command.

Register Name	Force ECC Register
Mnemonic	BRIDGE.AD.FORCE_ECC_REG
Address	000000000009000D (SCOM)
Description	Force ECC Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	ALTD_DATA_ITAG: the sixty-fourth bit of the ITAG of a fabric alter/display operation.
1:16	RWX	ALTD_DATA_TX_ECC: The two ECC values of a PCB/XSCOM/LPC Processor bus data transfer.

Bits	SCOM	Field Mnemonic: Description
17	RWX	ALTD_DATA_TX_ECC_OVERWRITE: Override (equals suppress update of) ECC value of a PCB Processor bus operation data transfer. Be careful. There must be no XSCOM or LPC data read data transfer. For example, an XSCOM read will modify the ECC value.

Register Name	**Alter/Display XSCOM Base Address Register**
Mnemonic	BRIDGE.AD.XSCOM_BASE_REG
Address	0000000000090010 (SCOM)
Description	Alter/Display XSCOM Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:29	RW	FBC_XSCOM_BASE: Base Address for XSCOM logic in Alter/Display.
30:60	RO	constant = 0b00000000000000000000000000000000
61	WOX	FBC_XSCOM_RESET: Used to reset the XSCOM State Machine logic in Alter/Display.
62	RW	FBC_XSCOM_DISABLE: Used to disable the XSCOM State Machine logic in Alter/Display.
63	RW	FBC_XSCOM_DISABLE_LOCAL_SHORTCUT: Used to disable the shortcut for local ADU internal registers.

Register Name	**XSCOM Mode Register**
Mnemonic	BRIDGE.AD.XSCOM_MODE_REG
Address	0000000000090011 (SCOM)
Description	XSCOM Mode Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	XSCOM_MODE_SPARE: Spare.
4	RW	XSCOM_MODE_BAR_PIB_ON_ERROR1: Prohibit XSCOM through the PIB after an error 001. Accessing ADU registers and the PIB register is still allowed.
5	RW	XSCOM_MODE_BAR_PIB_ON_ERROR2: Prohibit XSCOM through the PIB after an error 010. Accessing ADU registers and the PIB register is still allowed.
6	RW	XSCOM_MODE_BAR_PIB_ON_ERROR3: Prohibit XSCOM through the PIB after an error 011. Accessing ADU registers and the PIB register is still allowed.
7	RW	XSCOM_MODE_BAR_PIB_ON_ERROR4: Prohibit XSCOM through the PIB after an error 100. Accessing ADU registers and the PIB register is still allowed.
8	RW	XSCOM_MODE_BAR_PIB_ON_ERROR5: Prohibit XSCOM through the PIB after an error 101. Accessing ADU registers and the PIB register is still allowed.
9	RW	XSCOM_MODE_BAR_PIB_ON_ERROR6: Prohibit XSCOM through the PIB after an error 110. Accessing ADU registers and the PIB register is still allowed.
10	RW	XSCOM_MODE_BAR_PIB_ON_ERROR7: Prohibit XSCOM through the PIB after an error 111. Accessing ADU registers and the PIB register is still allowed.
11	RW	XSCOM_MODE_HANG_PIB_RESET: Reset the XSCOM state machine when a PIB hang was detected.
12	RW	XSCOM_MODE_HANG_RESET: Reset the XSCOM state machine when another a hang was detected.
13	RW	XSCOM_MODE_RESET_ON_PARITY: Reset the XSCOM state machine when a parity error was detected.
14	RW	XSCOM_MODE_FREEZE_LOG_ON_ERROR1: Freeze XSCOM log register after an error 001.

Bits	SCOM	Field Mnemonic: Description
15	RW	XSCOM_MODE_FREEZE_LOG_ON_ERROR2: Freeze XSCOM log register after an error 010.
16	RW	XSCOM_MODE_FREEZE_LOG_ON_ERROR3: Freeze XSCOM log register after an error 011.
17	RW	XSCOM_MODE_FREEZE_LOG_ON_ERROR4: Freeze XSCOM log register after an error 100.
18	RW	XSCOM_MODE_FREEZE_LOG_ON_ERROR5: Freeze XSCOM log register after an error 101.
19	RW	XSCOM_MODE_FREEZE_LOG_ON_ERROR6: Freeze XSCOM log register after an error 110.
20	RW	XSCOM_MODE_FREEZE_LOG_ON_ERROR7: Freeze XSCOM log register after an error 111.

Register Name	**XSCOM Status Log Register**
Mnemonic	BRIDGE.AD.XSCOM_LOG_REG
Address	0000000000090012 (SCOM)
Description	XSCOM Status Log Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	XSCOM_CMD_IN_PROG: XSCOM command in progress. Read-only status bit does not freeze on an error.
1:3	RWX_WCLRREG	XSCOM_CMD_STATUS: XSCOM command returned status.
4	RWX_WCLRREG	XSCOM_WRITE_CMD: XSCOM was a write command.
5:26	RWX_WCLRREG	XSCOM_ADDR_TAG: XSCOM command fabric address tag. Indicates master of command.
27:29	RWX_WCLRREG	XSCOM_THR_ID: XSCOM Command fabric thread ID, indicates master thread of command.
30	RO	constant = 0b0
31	ROX	XSCOM_PIB_COMPONENT_BUSY: PIB transaction ongoing, if set.
32	RO	constant = 0b0
33:63	RWX_WCLRREG	XSCOM_PIB_ADDR: XSCOM PIB address of failing command.

Register Name	**XSCOM Error Register**
Mnemonic	BRIDGE.AD.XSCOM_ERR_REG
Address	0000000000090013 (SCOM)
Description	XSCOM error register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	XSCOM_ADDRESS_ERR: XSCOM command error: invalid address.
1	RWX_WCLRREG	XSCOM_TSIZE_ERR: XSCOM command error: invalid TSIZE.
2	RWX_WCLRREG	XSCOM_RC_TTAG_PAR_ERR: Processor bus reflected command TTAG parity error.
3	RWX_WCLRREG	XSCOM_CR_TTAG_PAR_ERR: Processor bus combined response TTAG parity error.
4	RWX_WCLRREG	XSCOM_CR_ATAG_PAR_ERR: Processor bus combined response ATAG parity error.
5	RWX_WCLRREG	XSCOM_RC_ADDR_PAR_ERR: Processor bus reflected command ADDR parity error.

Bits	SCOM	Field Mnemonic: Description
6:7	RO	constant = 0b00
8	RWX_WCLRREG	PB_ECC_CE_ERR: Processor bus received correctable ECC error.
9	RWX_WCLRREG	PB_ECC_UE_ERR: Processor bus received uncorrectable ECC error.
10	RWX_WCLRREG	PB_ECC_SUE_ERR: Processor bus received special uncorrectable ECC error.
11	RWX_WCLRREG	RTAG_PARITY_ERR: Error: the data received came with an RTAG that has a parity error, thus it might also be not XSCOM related.
12	RWX_WCLRREG	CRESP_HANG_ERR: Hang detected waiting for combined response.
13	RWX_WCLRREG	PIB_HANG_ERR: Hang detected waiting for PIB.
14	RWX_WCLRREG	PBDATA_HANG_ERR: Hang detected waiting for data from PB.
15	RWX_WCLRREG	ADS_HANG_ERR: Hang detected waiting for internal ADU bus to complete.
16	RWX_WCLRREG	XSCOM_FSM_PERR: XSCOM command state machine parity error.
17	RWX_WCLRREG	SPARE0_ERR: This spare is a placeholder.
18	RWX_WCLRREG	SPARE1_ERR: This spare is a placeholder.
19	RWX_WCLRREG	UNEXPECT_DATA_ERR: Unexpected processor bus data error: state machine was idle while data arrived.
20	RWX_WCLRREG	ILL_CRESP_ERR: Error illegal combined response received.
21:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	XSCOM Received Remote Status pMisc and Source Register
Mnemonic	BRIDGE.AD.XSCOM_RCVED_STAT_REG
Address	0000000000090018 (SCOM)
Description	XSCOM Received Remote Status pMisc and Source Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	XSCOM_DONE: XSCOM command done. An XSCOM command sourced from this chip has completed. This bit needs to be cleared before an XSCOM operation to be accurate.
1:3	RWX_WCLRREG	XSCOM_RESULT: XSCOM Result code 000 = Okay 001 = Retry required, other error.
4:9	RWX_WCLRREG	XSCOM_COREID: UNITID of the command source (which NCU started this operation).
10:12	RWX_WCLRREG	XSCOM_STAT_THRID: THREADID of the command source (which thread started this operation).
13:16	RWX_WCLRREG	DEST_GROUPID: GROUPID of XSCOM command destination (pointing to the ADU that executed the command).

Bits	SCOM	Field Mnemonic: Description
17:19	RWX_WCLRREG	DEST_CHIPID: CHIPID of XSCOM command destination (pointing to the ADU that executed the command).

Register Name	XSCOM Access Address Register
Mnemonic	BRIDGE.AD.ADS_XSCOM_CMD_REG
Address	000000000009001C (SCOM)
Description	XSCOM Access Address Register (ADU internal command transfer use only)

Bits	SCOM	Field Mnemonic: Description
0	ROX	ADS_XSCOM_CMD_REG_RNW: Internal register. Indicate read operation of current XSCOM/LPC access (otherwise, it is a write).
1:4	RO	constant = 0b0000
5:11	ROX	ADS_XSCOM_CMD_REG_SIZE: Internal register. The size of the current XSCOM/LPC access.
12:29	RO	constant = 0b000000000000000000
30:63	ROX	ADS_XSCOM_CMD_REG_ADR: Internal register. byte address of current XSCOM/LPC access.

Register Name	XSCOM Data Ramp Register (Internal use only)
Mnemonic	BRIDGE.AD.XSCOM_DAT0_REG
Address	000000000009001E (SCOM)
Description	XSCOM Data Ramp Register (internal use only)

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	XSCOM_DAT0: Internal register. Left data in the data ramp (to be transferred to and from the PIB and LPC).

Register Name	XSCOM Data Ramp Register (Internal use only)
Mnemonic	BRIDGE.AD.XSCOM_DAT1_REG
Address	000000000009001F (SCOM)
Description	XSCOM Data Ramp Register (internal use only)

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	XSCOM_DAT1: Internal register. Right data in the data ramp (to be transferred to and from PIB and LPC).

Register Name	pMisc Status Register
Mnemonic	BRIDGE.AD.SND_STAT_REG
Address	0000000000090020 (SCOM)
Description	pMisc Status Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	ERR_CMD_OVERRUN: Error command dropped from a queue overrun.

Bits	SCOM	Field Mnemonic: Description
1	RWX_WCLRREG	TRC_CMD_OVERRUN: Trace command dropped from a queue overrun.
2	RWX_WCLRREG	XSC_CMD_OVERRUN: XSCOM status command dropped from a queue overrun.
3	RWX_WCLRREG	HTM_CMD_OVERRUN: HTM command dropped from a queue overrun.
4	RWX_WCLRREG	TOD_CMD_OVERRUN: TOD Command dropped due to queue overrun.
5	RWX_WCLRREG	CMD_COUNT_ERR: Attempt to send but too much commands at a time (causes short stall to prevent tag reuse).
6	RWX_WCLRREG	SND_PB_OP_HANG_ERR: pMisc SND waiting for outstanding combined response much too long.
7:15	RO	constant = 0b000000000
16	RWX_WCLRREG	SND_INVALID_CRESP_ERR: pMisc send received an invalid combined response.
17:31	RO	constant = 0b0000000000000000
32	RWX_WCLRREG	RCV_TTAG_PARITY_ERR: Parity error of TTAG in RCV macro.
33	RWX_WCLRREG	RCV_PB_OP_HANG_ERR: pMisc RCV waiting for outstanding combined response much too long.
34	RWX_WCLRREG	TOD_HANG_ERR: pMisc RCV waiting for second TOD packet much too long.
35:47	RO	constant = 0b0000000000000
48:51	ROX	RCV_TOD_STATE: Reflects what parts of a pMisc TOD package has been received. CRESPAB means all but waiting for XCSM doing the PIB operation.
52:60	RO	constant = 0b000000000

Register Name	pMisc Mode Register
Mnemonic	BRIDGE.AD.SND_MODE_REG
Address	0000000000090021 (SCOM)
Description	pMisc Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_TRC_GLB_TRIG0: Enable broadcast of trace global trigger 0.
1	RW	ENABLE_TRC_GLB_TRIG1: Enable broadcast of trace global trigger 1.
2	RW	ENABLE_GLB_PULSE_MODE: On rising edge, send a trace global trigger toggle command.
3	RW	SINGLE_OUTSTANDING_CMD: Wait for the clean combined response on every command before the next can be posted. This can cause big delays if a command gets retried for a long time. Do not use with ENABLE_RECEIVE_OWN_TOD to prevent deadlock. This is because the receive part depends on XSCOM-RESULT-pMisc going out before XCSM accepts the next TOD command. The deadlock will be TOD-retrying forever, and XSCOM FSM will not finish sending the resulting pMisc.
4:7	RW	PROG_REQ_DELAY: Program amount of delay between fabric address requests. Matches 4 MSB of 12-bit counter. Allows delay from 0 cycles to 3840 cycles in steps of 256 cycles. Defaulted to no delay (0000) in the design.
8	RW	DISABLE_ERR_CMD: Block error commands from being broadcast (malfunction alert, rising edge only).

Bits	SCOM	Field Mnemonic: Description
9	RW	DISABLE_HTM_CMD: Block HTM commands from being broadcast.
10	RW	DISABLE_TRACE_CMD: Block trace commands from being broadcast.
11	RW	DISABLE_TOD_CMD: Block frequency changing commands from being broadcast.
12	RW	DISABLE_XSCOM_CMD: Block XSCOM commands from being broadcast.
13	RW	ENABLE_CLR_ERR_CMD: Enable sending of error reset when a malfunction alert goes away. Do Not Use: Sequence ordering cannot be guaranteed.
14	RW	OVERRIDE_PBINIT_ERR_CMD: Allow error commands to being broadcast on quiesced the processor bus.
15	RW	OVERRIDE_PBINIT_HTM_CMD: Allow HTM commands to being broadcast on quiesced the processor bus.
16	RW	OVERRIDE_PBINIT_TRACE_CMD: Allow trace commands to being broadcast on quiesced the processor bus.
17	RW	OVERRIDE_PBINIT_TOD_CMD: Allow FREQCHNG commands to being broadcast on quiesced the processor bus.
18	RW	OVERRIDE_PBINIT_XSCOM_CMD: Allow XSCOM commands to being broadcast on quiesced the processor bus.
19	RW	DISABLE_CHECKSTOP: Disable forwarding checkstop to stop the processor bus.
20	WOX	MANUAL_SET_PB_STOP: Manual set and overwrite state of Stop the Power Bus Signal (requires disabling forwarding first).
21	WOX	MANUAL_CLR_PB_STOP: Manual clear and overwrite state of Stop the Power Bus Signal (requires disabling forwarding first).
22	ROX	PB_STOP: State of the power bus PB_stop signal.
23:24	RO	constant = 0b00
25	WOX	MANUAL_PB_SWITCH_ABCD: Force a local (not broadcasted) processor bus AB or CD register switch.
26:27	RW	ENABLE_RECEIVE_OWN_TRIGGER: Enables receiving debug trigger pMisc from the same ADU (with the same NODEID, CHIPID).
28	RW	ENABLE_RECEIVE_OWN_TOD: Enables receiving TOD pMisc from the same ADU (with same NODEID, CHIPID). Do not use with SINGLE_OUTSTANDING_CMD to prevent deadlock (see there for reason why).
29	WOX	RESET_TOD_STATE: Reset state machine of incomplete TOD pMisc receive.
30	RW	ENABLE_PB_SWITCH_AB: Enable generation of a processor bus AB Register Switch event pulse.
31	RW	ENABLE_PB_SWITCH_CD: Enable generation of a processor bus CD Register Switch event pulse.

Register Name	pMisc Receive Malfunction Alert Register (First)
Mnemonic	BRIDGE.AD.RCV_ERRLOG0_REG
Address	0000000000090022 (SCOM)
Description	pMisc Receive Malfunction Alert Register (first)

Bits	SCOM	Field Mnemonic: Description
0:7	RW_WAND	MALF_ERR_FROM_GROUP0: There was a malfunction alert error from group 0 (one bit for each chip).
8:15	RW_WAND	MALF_ERR_FROM_GROUP1: There was a malfunction alert error from group 1 (one bit for each chip).
16:23	RW_WAND	MALF_ERR_FROM_GROUP2: There was a malfunction alert error from group 2 (one bit for each chip).
24:31	RW_WAND	MALF_ERR_FROM_GROUP3: There was a malfunction alert error from group 3 (one bit for each chip).
32:39	RW_WAND	MALF_ERR_FROM_GROUP4: There was a malfunction alert error from group 4 (one bit for each chip).

Bits	SCOM	Field Mnemonic: Description
40:47	RW_WAND	MALF_ERR_FROM_GROUP5: There was a malfunction alert error from group 5 (one bit for each chip).
48:55	RW_WAND	MALF_ERR_FROM_GROUP6: There was a malfunction alert error from group 6 (one bit for each chip).
56:63	RW_WAND	MALF_ERR_FROM_GROUP7: There was a malfunction alert error from group 7 (one bit for each chip).

Register Name	pMisc Receive Malfunction Alert Register (last)
Mnemonic	BRIDGE.AD.RCV_ERRLOG1_REG
Address	0000000000090023 (SCOM)
Description	pMisc Receive Malfunction Alert Register (last)

Bits	SCOM	Field Mnemonic: Description
0:7	RW_WAND	MALF_ERR_FROM_GROUP8: There was a malfunction alert error from group 8 (one bit for each chip).
8:15	RW_WAND	MALF_ERR_FROM_GROUP9: There was a malfunction alert error from group 9 (one bit for each chip).
16:23	RW_WAND	MALF_ERR_FROM_GROUP10: There was a malfunction alert error from group 10 (one bit for each chip).
24:31	RW_WAND	MALF_ERR_FROM_GROUP11: There was a malfunction alert error from group 11 (one bit for each chip).
32:39	RW_WAND	MALF_ERR_FROM_GROUP12: There was a malfunction alert error from group 12 (one bit for each chip).
40:47	RW_WAND	MALF_ERR_FROM_GROUP13: There was a malfunction alert error from group 13 (one bit for each chip).
48:55	RW_WAND	MALF_ERR_FROM_GROUP14: There was a malfunction alert error from group 14 (one bit for each chip).
56:63	RW_WAND	MALF_ERR_FROM_GROUP15: There was a malfunction alert error from group 15 (one bit for each chip).

Register Name	TOD: pMisc Data Send Register
Mnemonic	BRIDGE.AD.TOD_DATA_SND_REG
Address	0000000000090028 (SCOM)
Description	TOD: pMisc Data Send Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PCB_TOD_DATA_SND: TOD command value to be sent.

Register Name	TOD: pMisc Data Receive Register
Mnemonic	BRIDGE.AD.TOD_DATA_RCV_REG
Address	0000000000090029 (SCOM)
Description	TOD: pMisc Data Receive Register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	PCB_TOD_DATA_RCV: TOD command value received before forwarded to PIB.

Register Name	TOD: Command Receive PIB Address Register
Mnemonic	BRIDGE.AD.TOD_CMD_REG
Address	000000000009002A (SCOM)
Description	TOD: Command Receive PIB Address Register

Bits	SCOM	Field Mnemonic: Description
0:29	RO	constant = 0b00000000100000000000000000000000
30:60	RW	TOD_CMD_REG_ADR: The constant PIB address of a TOD register to store received TOD command in: 0x00040029
61:63	RO	constant = 0b000

Register Name	PIB Slave Data Register (internal use only)
Mnemonic	BRIDGE.AD.IO_DATA_REG
Address	0000000000090030 (SCOM)
Description	PIB Slave Data Register (internal use only)

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	PCB_IO_TMP_DATA: Internal only data to be transferred between ADS and PIB.

Register Name	Data for access to PIB from XSCOM
Mnemonic	BRIDGE.AD.PIB_CMD_REG
Address	0000000000090031 (SCOM)
Description	Data for access to PIB from XSCOM

Bits	SCOM	Field Mnemonic: Description
0	ROX	PIB_CMD_REG_RNW: Internal register. Setting this bit causes a PIB read and resulting data stored in the PIB_DATA_REG.
1:29	RO	constant = 0b00000000000000000000000000000
30:60	ROX	PIB_CMD_REG_ADR: Internal register. PIB address.
61:63	RO	constant = 0b000

Register Name	Data for access to PIB from Alt
Mnemonic	BRIDGE.AD.PIB_DATA_REG
Address	0000000000090032 (SCOM)
Description	Display. Writing this register with PIB_READ_NOT_WRITE = 0 causes a PIB write.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	PIB_DATA: Data from and to PIB.

Register Name	Reset pulse for PIB
Mnemonic	BRIDGE.AD.PIB_RESET_REG
Address	0000000000090033 (SCOM)
Description	Reset pulse for PIB

Bits	SCOM	Field Mnemonic: Description
0	WOX	PIB_RESET: Writing this to 1 causes a PIB reset. Do not use this unless there was an error.
1	ROX	PIB_RESET_STATE: PIB reset state.
2	RWX_WAND	PIB_RESET_ABORTED_CMD: A former PIB reset aborted a command of this master.

Register Name	LPC Base Address Register
Mnemonic	BRIDGE.AD.LPC_BASE_REG
Address	0000000000090040 (SCOM)
Description	LPC Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:31	RW	LPC_BASE: Base address for LPC unit.
32:62	RO	constant = 0b00000000000000000000000000000000
63	RW	LPC_DISABLE: Used to disable the LPC.

Register Name	Data for Access to LPC from XSCOM
Mnemonic	BRIDGE.AD.LPC_CMD_REG
Address	0000000000090041 (SCOM)
Description	Data for access to LPC from XSCOM

Bits	SCOM	Field Mnemonic: Description
0	ROX	LPC_CMD_REG_RNW: Internal register. Setting this bit causes an LPC read. The resulting data is stored in LPC_DATA_REG.
1:4	RO	constant = 0b0000
5:11	ROX	LPC_CMD_REG_SIZE: Internal register. Size of current XSCOM/LPC access.
12:31	RO	constant = 0b00000000000000000000
32:63	ROX	LPC_CMD_REG_ADR: Internal register. LPC address. **Note:** This field is updated after execution.

Register Name	Data for Access to LPC from Alt
Mnemonic	BRIDGE.AD.LPC_DATA_REG
Address	0000000000090042 (SCOM)
Description	Display. Writing this register with LPC_READ_NOT_WRITE = 0 causes an LPC write

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	LPC_DATA: Data from and to LPC.

Register Name	Status/Debug Register for LPC Operation
Mnemonic	BRIDGE.AD.LPC_STATUS_REG
Address	0000000000090043 (SCOM)
Description	Status/Debug Register for LPC Operation

Bits	SCOM	Field Mnemonic: Description
0	ROX	LPC_DONE_STATUS: Status of LPC transaction.
1:9	RO	constant = 0b000000000
10	ROX	LPC_VALID_STATUS: Status of LPC handshake. Status of LP_OPB_VALID.
11	ROX	LPC_ACK_STATUS: Status of LPC handshake. State of LP_OPB_ACK.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Divider Values for ADU PowerBus Hang
Mnemonic	BRIDGE.AD.ADU_HANG_DIV_REG
Address	0000000000090050 (SCOM)
Description	Divider values for ADU processor bus hang

Bits	SCOM	Field Mnemonic: Description
0:4	RW	ADU_DATA_HANG_DIV: Divider value for ADU processor bus data hang.
5:9	RW	ADU_OPER_HANG_DIV: Divider value for ADU processor bus operational hang.
10:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Control Register Fast Mode B
Mnemonic	TP.TPCHIP.PIB.I2CM.CONTROL_REGISTER_B
Address	00000000000A0000 (SCOM)
Description	Control Register Fast Mode B

Bits	SCOM	Field Mnemonic: Description
0	RWX	PIB_CNTR_REG_BIT_WITHSTART_0: For command register of i2c engine.
1	RWX	PIB_CNTR_REG_BIT_WITHADDR_0: For command register of i2c engine.
2	RWX	PIB_CNTR_REG_BIT_READCONT_0: For command register of i2c engine.
3	RWX	PIB_CNTR_REG_BIT_WITHSTOP_0: For command register of i2c engine.
4:7	RWX	PIB_CNTR_REG_LENGTH_0: Maximum_write = 4 , Maximum_read = 8.
8:14	RWX	PIB_CNTR_REG_ADDR_0: For command register of i2c engine.
15	RWX	PIB_CNTR_REG_BIT_RNW_0: For command register of i2c engine.
16:17	RWX	PIB_CNTR_REG_SPEED_0: 00 = 100 K 01 = 400 K 10 = 3400 K 11 = 50 K
18:22	RWX	PIB_CNTR_REG_PORT_NUMBER_0: For the mode register of the I2C engine.

Bits	SCOM	Field Mnemonic: Description
23:25	RWX	REG_ADDR_LEN_0: 00 = No register address in FIFO 01= 1 byte of the FIFO data is the register address 10 = 2 byte of FIFO data are the register address 11 = 3 byte of FIFO data are are the register address
26	RWX	ENH_MODE_0: Enable enhanced mode in the mode register of the I2C engine.
27	RWX	ECC_ENABLE_0: Enables ECC for the current operation.
28	RWX	ECCCHK_DISABLE_0: Disables ECC checking for read operation when ECC is enabled.
29	RWX	UNUSED_0: Reserved. Not used.
30:31	RWX	FAST_MODE_INTERRUPT_STERRING_BITS_0: Decides which master should see the done interrupt of FAST_MODE.
32:39	RWX	PIB_CNTR_REG_DATA_1_0: Data for I2C FIFO.
40:47	RWX	PIB_CNTR_REG_DATA_2_0: Data for I2C FIFO.
48:55	RWX	PIB_CNTR_REG_DATA_3_0: Data for I2C FIFO.
56:63	RWX	PIB_CNTR_REG_DATA_4_0: Data for I2C FIFO.

Register Name	**DATA8to15 Register Read Only Fast Mode**
Mnemonic	TP.TPCHIP.PIB.I2CM.DATA8TO15_REGISTER_B
Address	00000000000A0001 (SCOM)
Description	DATA8to15 Register Read Only Fast Mode

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	PIB_DATA8TO15_0: The last 8 bytes of data for read. It is not available for write operation.

Register Name	**Reset Register Fast Mode**
Mnemonic	TP.TPCHIP.PIB.I2CM.RESET_REGISTER_B
Address	00000000000A0001 (SCOM)
Description	Reset Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0	WOX	OVERALL_RESET_0. One bit register resets all registers and the I2C engine.
1	WOX	CHKSW_AR012_0: Debug switch to disable the enhanced PIB error handling.

Register Name	**Status Register Fast Mode**
Mnemonic	TP.TPCHIP.PIB.I2CM.STATUS_REGISTER_B
Address	00000000000A0002 (SCOM)
Description	STATUS REGISTER_FAST_MODE

Bits	SCOM	Field Mnemonic: Description
0	ROX	BUS_STATUS_ADDR_NVLD_0: Address invalid.
1	ROX	BUS_STATUS_WRITE_NVLD_0: Write invalid.

Bits	SCOM	Field Mnemonic: Description
2	ROX	BUS_STATUS_READ_NVLD_0: Read invalid.
3	ROX	BUS_STATUS_ADDR_P_ERR_0: Address parity error.
4	ROX	BUS_STATUS_PAR_ERR_0: data parity error.
5	ROX	BUS_STATUS_LB_PARITY_ERROR_0: local bus parity error.
6:37	ROX	PIB_DATA0TO7_0: First eight bytes of data for read and for write, the 5th byte to 12th byte.
38:40	RO	constant = 0b000
41	ROX	ECC_CORRECTED_ERROR_0: This warning indicates that one bit flip was in data and has been corrected.
42	ROX	ECC_UNCORRECTED_ERROR_0: This error indicates that there are two bit flips in read data that cannot be corrected.
43	ROX	ECC_CONFIG_ERROR_0: This the error indicates that the control register is ECC_ENABLED for DATA_LENGTH not equal to eight. OR ECC is enabled for the engine where the ECC block is not at all instantiated.
44	ROX	BUS_STATUS_BUSY_0: Local bus busy.
45	ROX	BUS_STATUS_INVALID_COMMAND_0: invalid command.
46	ROX	BUS_STATUS_PARITY_ERROR_0: parity error.
47	ROX	BUS_STATUS_BACK_END_OVERRUN_ERROR_0: Back end overrun error.
48	ROX	BUS_STATUS_BACK_END_ACCESS_ERROR_0: Back end access error.
49	ROX	BUS_STATUS_ARBITRATION_LOST_ERROR_0: Arbitration lost error.
50	ROX	BUS_STATUS_NACK_RECEIVED_ERROR_0: NACK received error.
51	ROX	BUS_STATUS_DATA_REQUEST_0: Data request.
52	ROX	BUS_STATUS_COMMAND_COMPLETE_0: Command complete.
53	ROX	BUS_STATUS_STOP_ERROR_0: Stop error.
54	ROX	BUS_STATUS_I2C_PORT_BUSY_0: I2C port busy.
55	ROX	BUS_STATUS_I2C_INTERFACE_BUSY_0: I2C interface busy.
56:63	ROX	BUS_STATUS_FIFO_ENTRY_COUNT_0: FIFO entry count.

Register Name	**DATA0to7 Register Fast Mode**
Mnemonic	TP.TPCHIP.PIB.I2CM.DATA0TO7_REGISTER_B
Address	00000000000A0003 (SCOM)
Description	DATA0to7 Register FAST_MODE

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	PIB_DATA0TO7_0: First 8 bytes of data for read and for write the fifth byte to twelfth byte.

Register Name	**FIFO1 Register Read B**
Mnemonic	TP.TPCHIP.PIB.I2CM.FIFO1_REGISTER_READ_B
Address	00000000000A0004 (SCOM)
Description	FIFO1 Register Read B

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_0: Because FIFO is not a normal register, it cannot be completely verified in REGCHK. Thus, this register is a dummy register that is used to maintain the address in HTML FIFO data byte 0. It should be able to read or write 1 byte.
8:31	RO	constant = 0b00000000000000000000000000
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	COMMAND Register B
Mnemonic	TP.TPCHIP.PIB.I2CM.COMMAND_REGISTER_B
Address	00000000000A0005 (SCOM)
Description	COMMAND Register B

Bits	SCOM	Field Mnemonic: Description
0	RWX	WITH_START_0: Decides if the start command is issued during the beginning of the operation.
1	RWX	WITH_ADDRESS_0: Decides if the device address is sent during the beginning of the operation.
2	RWX	READ_CONTINUE_0: Decides if the next read operation is continuation of present operation.
3	RWX	WITH_STOP_0: Decides if the stop command is issued during the end of the operation.
4:7	RWX	NOT_USED_0: Not used.
8:14	RWX	DEVICE_ADDRESS_0: The device address of the slave on the I2C bus.
15	RWX	READ_NOT_WRITE_0: I2C read or write.
16:31	RWX	LENGTH_IN_BYTES_0: The length of bytes to be accessed through the I2C bus.
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Mode Register B
Mnemonic	TP.TPCHIP.PIB.I2CM.MODE_REGISTER_B
Address	00000000000A0006 (SCOM)
Description	Mode Register B

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus.
8:9	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus.
10:15	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus.
16:21	RWX	PORT_NUMBER_0: Port number.
22:25	RO	constant = 0b0000
26	RWX	CHKSW_CMDQUEUEING_0: Debug switch to switch the command queuing option off.
27	RWX	CHKSW_I2C_BUSY_0: A debug switch to switch between the Port Busy Register and I2C busy muxing logic. **Note:** If you do not enable the chicken switch, the older logic behavior occurs.
28	RWX	FGAT_MODE_0: FGAT mode.
29	RWX	DIAG_MODE_0: Diagnostic mode.
30	RWX	PACING_ALLOW_MODE_0: Pacing allow mode.
31	RWX	WRAP_MODE_0: WRAP_MODE.
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Water Mark Register B
Mnemonic	TP.TPCHIP.PIB.I2CM.WATER_MARK_REGISTER_B
Address	00000000000A0007 (SCOM)
Description	Water Mark Register B

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	RWX	WATERMARK_REG_0: Water mark register.

Bits	SCOM	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupt Mask Register B
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_MASK_REGISTER_B
Address	00000000000A0008 (SCOM) 00000000000A0009 (SCOM1) 00000000000A000A (SCOM2)
Description	Interrupt Mask Register B

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:15	RO	RO	RO	constant = 0b0000000000000000
16:31	WOX	WOX_OR	WOX_AND	INT_MASK_0: Interrupt mask register.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	Interrupt Mask Register Read B
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_MASK_REGISTER_READ_B
Address	00000000000A0008 (SCOM)
Description	Interrupt Mask Register Read B

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	ROX	INT_MASK_0: Interrupt mask register.
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupt Condition B
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_COND_B
Address	00000000000A0009 (SCOM)
Description	Interrupt Condition B

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16	ROX	INVALID_CMD_0: Invalid command. A new command was given when the old command was not yet completed.
17	ROX	LBUS_PARITY_ERROR_0: Local bus parity error.
18	ROX	BE_OV_ERROR_0: Back end overrun error. Writing or reading into full or empty FIFO reply.
19	ROX	BE_ACC_ERROR_0: Back end access error. Writing/Reading more data than requested.
20	ROX	ARBITRATION_LOST_ERROR_0: Arbitration lost error. I2C bus is held by some other master when trying to access.
21	ROX	NACK_RECEIVED_ERROR_0: NACK received error. The slave does not respond with the acknowledgment.
22	ROX	DATA_REQUEST_0: Data request: The FIFO must be accessed more to fulfill the expectation.
23	ROX	INT_CONDS_CMD_COMPLETE_0.
24	ROX	STOP_ERROR_0: Stop error: Cannot send the stop condition to the bus.
25	ROX	INT_CONDS_I2C_BUSY_0
26	ROX	INT_CONDS_NOT_I2C_BUSY_0
27	RO	constant = 0b0
28	ROX	INT_CONDS_SCL_EQ_1_0
29	ROX	INT_CONDS_SCL_EQ_0_0
30	ROX	INT_CONDS_SDA_EQ_1_0
31	ROX	INT_CONDS_SDA_EQ_0_0
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupts Register B
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPTS_B
Address	00000000000A000A (SCOM)
Description	Interrupts Register B

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	INTS_0
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	**IMM Reset I2C B**
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_I2C_B
Address	00000000000A000B (SCOM)
Description	IIMM Reset I2C B

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_I2C_0. Resets command, mode, watermark, interrupt mask, and status registers.

Register Name	**Status Register Engine B**
Mnemonic	TP.TPCHIP.PIB.I2CM.STATUS_REGISTER_ENGINE_B
Address	00000000000A000B (SCOM)
Description	STATUS Register ENGINE_B

Bits	SCOM	Field Mnemonic: Description
0	ROX	INVALID_CMD_0: Invalid command. A new command was given when the old command was not yet completed.
1	ROX	LBUS_PARITY_ERROR_0: Local bus parity error.
2	ROX	BE_OV_ERROR_0: Back end overrun error: Writing or reading into full or empty FIFO reply.
3	ROX	BE_ACC_ERROR_0: Back end access error: Writing/Reading more data than requested.
4	ROX	ARBITRATION_LOST_ERROR_0: Arbitration lost error: I2C bus is held by some other master when trying to access.
5	ROX	NACK_RECEIVED_ERROR_0: NACK received error: The slave does not respond with the acknowledgment.
6	ROX	DATA_REQUEST_0: Data request: The FIFO must be accessed more to fulfill the expectation.
7	ROX	CMD_COMPLETE_0. Command complete: Indicates the completion of command.
8	ROX	STOP_ERROR_0: Stop error: Cannot send the stop condition to the bus.
9:15	ROX	MAX_NUM_OF_PORTS_0. Maximum number of ports defined for this engine.
16	ROX	ANY_I2C_INT_0
17:18	RO	constant = 0b00
19	ROX	I2C_PORT_HISTORY_BUSY_0

Bits	SCOM	Field Mnemonic: Description
20	ROX	SCL_SYN_0
21	ROX	SDA_SYN_0
22	ROX	I2C_BUSY_0. I2C bus is occupied.
23	ROX	SELF_BUSY_0: Self busy: I2C bus is occupied by itself.
24:27	RO	constant = 0b0000
28:31	ROX	FIFO_ENTRY_COUNT_0: The number of bytes that are present in the FIFO.
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:43	RO	constant = 0b000
44:47	ROX	I2CM_STEERED_INTERRUPTS_0: Steered I2CM_INTERRUPT either for fast mode or legacy mode.
48:63	RO	constant = 0b0000000000000000

Register Name	Extended Status B
Mnemonic	TP.TPCHIP.PIB.I2CM.EXTENDED_STATUS_B
Address	00000000000A000C (SCOM)
Description	Extended Status B

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_SIZE_0. Total FIFO size.
8:10	RO	constant = 0b000
11:15	ROX	MSM_CURR_STATE_0: Current state.
16	ROX	SCL_SYN_EXT_0
17	ROX	SDA_SYN_EXT_0
18	ROX	S_SCL_0. Clock input for wrap mode.
19	ROX	S_SDA_0. Data input for wrap mode.
20	ROX	M_SCL_0. Clock output for wrap mode.
21	ROX	M_SDA_0. Data output for wrap mode.
22	ROX	HIGH_WATER_0. High water mark: FIFO reached highest water level.
23	ROX	LOW_WATER_0. Low water mark: FIFO reached lowest water level.
24	ROX	I2C_BUSY_EXT_0. I2C bus is busy.
25	ROX	SELF_BUSY_0: I2C bus is occupied by itself.
26:31	RO	constant = 0b010111

Bits	SCOM	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Reset Error B
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_ERR_B
Address	00000000000A000C (SCOM)
Description	IMM Reset Error B

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_ERRORS_0. Resets FIFO, some status bits, and state machine.

Register Name	IMM Sets SCL_B
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_SET_S_SCL_B
Address	00000000000A000D (SCOM)
Description	IMM Sets SCL_B

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SCL_0. Sets output S_SCL.

Register Name	Residual Front End Back End Length B
Mnemonic	TP.TPCHIP.PIB.I2CM.RESIDUAL_FRONT_END_BACK_END_LENGTH_B
Address	00000000000A000D (SCOM)
Description	Residual Front End Back End Length B

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	RESID_FE_LEN_0. Residual front end length register.
16:31	ROX	RESID_BE_LEN_0. Residual back end length register.
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.

Bits	SCOM	Field Mnemonic: Description
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	I2C Busy Register B
Mnemonic	TP.TPCHIP.PIB.I2CM.I2C_BUSY_REGISTER_B
Address	00000000000A000E (SCOM)
Description	I2C Busy Register B

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PORT_BUSY_0. Corresponding port is busy. If it is ‘1’, no one should access. If ‘0’ can be accessed.
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Resets SCL_B
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_S_SCL_B
Address	00000000000A000F (SCOM)
Description	IMM Resets SCL_B

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SCL_0. Resets output S_SCL.

Register Name	IMM Sets SDA_B
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_SET_S_SDA_B
Address	00000000000A0010 (SCOM)
Description	IMM Sets SDA_B

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SDA_0. Sets output S_SDA.

Register Name	IMM Resets SDA_B
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_S_SDA_B
Address	00000000000A0011 (SCOM)
Description	IMM Resets SDA_B

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SDA_0. Resets output S_SDA.

Register Name	FIFO4 Register READ_0
Mnemonic	TP.TPCHIP.PIB.I2CM.FIFO4_REGISTER_READ_B
Address	00000000000A0012 (SCOM)
Description	FIFO4 Register READ_0

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_0: Because FIFO is not a normal register, it cannot be completely verified in REGCHK. Thus, this register is a dummy register that is used to maintain the address in HTML FIFO data byte 0. It should be able to read or write 1 byte.
8:15	ROX	Reserved field.
16:23	ROX	Reserved field.
24:31	ROX	Reserved field.
32:39	ROX	PEEK_DATA1_0: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	CC Protect Mode Register
Mnemonic	TP.TPCHIP.PIB.I2CM.PIBI2CM_PROTECT_MODE_REG_B
Address	00000000000A03FE (SCOM)
Description	CC Protect Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE_0: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE_0: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.PIB.I2CM.PIBI2CM_ATOMIC_LOCK_REG_B
Address	00000000000A03FF (SCOM)
Description	Atomic Lock Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE_0: Enable atomic lock.
1:4	ROX	CC_ATOMIC_ID_0: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY_0: Atomic lock counter.

Register Name	Control Register Fast Mode 1
Mnemonic	TP.TPCHIP.PIB.I2CM.CONTROL_REGISTER_C
Address	00000000000A1000 (SCOM)
Description	Control Register Fast Mode 1

Bits	SCOM	Field Mnemonic: Description
0	RWX	PIB_CNTR_REG_BIT_WITHSTART_1: For command register of the I2C engine.
1	RWX	PIB_CNTR_REG_BIT_WITHADDR_1: For command register of the I2C engine.
2	RWX	PIB_CNTR_REG_BIT_READCONT_1: For command register the I2C engine.
3	RWX	PIB_CNTR_REG_BIT_WITHSTOP_1: For command register the I2C engine.
4:7	RWX	PIB_CNTR_REG_LENGTH_1: MAXIMUM_WRITE = 4 , MAXIMUM_READ = 8.
8:14	RWX	PIB_CNTR_REG_ADDR_1: For command register of I2C engine.
15	RWX	PIB_CNTR_REG_BIT_RNW_1: For command register of I2C engine.
16:17	RWX	PIB_CNTR_REG_SPEED_1: 00 = 100 K 01 = 400 K 10 = 3400 K 11 = 50 K
18:22	RWX	PIB_CNTR_REG_PORT_NUMBER_1: For mode register of I2C engine.
23:25	RWX	REG_ADDR_LEN_1: 00 = No register address in FIFO 01 = 1 byte of FIFOs data is in the register address 10 = 2 bytes of FIFOs data are in the register address 11 = 3 bytes of FIFOs data are in the register address.
26	RWX	ENH_MODE_1: Enable enhanced mode in mode register of I2C engine.
27	RWX	ECC_ENABLE_1: Enables ECC for the current operation.
28	RWX	ECCCHK_DISABLE_1: Disables ECC checking for read operation when ECC is enabled.
29	RWX	UNUSED_1:
30:31	RWX	FAST_MODE_INTERRUPT_STERRING_BITS_1: Decides which master should see the done interrupt of fast_mode.
32:39	RWX	PIB_CNTR_REG_DATA_1_1: Data for I2C FIFO.
40:47	RWX	PIB_CNTR_REG_DATA_2_1: Data for I2C FIFO.
48:55	RWX	PIB_CNTR_REG_DATA_3_1: Data for I2C FIFO.

Bits	SCOM	Field Mnemonic: Description
56:63	RWX	PIB_CNTR_REG_DATA_4_1: Data for I2C FIFO.

Register Name	DATA8to15 Register Read Only Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.DATA8TO15_REGISTER_C
Address	00000000000A1001 (SCOM)
Description	DATA8to15 Register READ_ONLY_FAST_MODE

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	PIB_DATA8TO15_1: Last 8 bytes of data for read. It is not available for write operation.

Register Name	Reset Register Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.RESET_REGISTER_C
Address	00000000000A1001 (SCOM)
Description	Reset Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0	WOX	OVERALL_RESET_1. One bit register resets all registers and the I2C engine.
1	WOX	CHKSW_AR012_1: Debug switch to disable the enhanced PIB error handling.

Register Name	Status Register Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.STATUS_REGISTER_C
Address	00000000000A1002 (SCOM)
Description	Status Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0	ROX	BUS_STATUS_ADDR_NVLD_1: Address invalid.
1	ROX	BUS_STATUS_WRITE_NVLD_1: Write invalid.
2	ROX	BUS_STATUS_READ_NVLD_1: Read invalid.
3	ROX	BUS_STATUS_ADDR_P_ERR_1: Address parity error.
4	ROX	BUS_STATUS_PAR_ERR_1: Data parity error.
5	ROX	BUS_STATUS_LB_PARITY_ERROR_1: Local bus parity error.
6:37	ROX	PIB_DATA0TO7_1: First 8 bytes of data for read and for write the fifth byte to 12th byte.
38:40	RO	constant = 0b000
41	ROX	ECC_CORRECTED_ERROR_1: This warning indicates that 1 bit flip was there in data and been corrected.
42	ROX	ECC_UNCORRECTED_ERROR_1: This error indicates that there are 2 bit flips in read data that cannot be corrected.
43	ROX	ECC_CONFIG_ERROR_1: This error indicates that the control register is ECC_ENABLED for DATA_LENGTH and not equal to 8. OR ECC is enabled for the engine where ECC block is not at all instantiated.
44	ROX	BUS_STATUS_BUSY_1: Local bus busy.

Bits	SCOM	Field Mnemonic: Description
45	ROX	BUS_STATUS_INVALID_COMMAND_1: Invalid command.
46	ROX	BUS_STATUS_PARITY_ERROR_1: Parity error.
47	ROX	BUS_STATUS_BACK_END_OVERRUN_ERROR_1: Back end overrun error.
48	ROX	BUS_STATUS_BACK_END_ACCESS_ERROR_1: Back end access error.
49	ROX	BUS_STATUS_ARBITRATION_LOST_ERROR_1: Arbitration lost error.
50	ROX	BUS_STATUS_NACK_RECEIVED_ERROR_1: NACK received error.
51	ROX	BUS_STATUS_DATA_REQUEST_1: Data request.
52	ROX	BUS_STATUS_COMMAND_COMPLETE_1: Command complete.
53	ROX	BUS_STATUS_STOP_ERROR_1: Stop error.
54	ROX	BUS_STATUS_I2C_PORT_BUSY_1: I2C port busy.
55	ROX	BUS_STATUS_I2C_INTERFACE_BUSY_1: I2C interface busy.
56:63	ROX	BUS_STATUS_FIFO_ENTRY_COUNT_1: FIFO entry count.

Register Name	**DATA0to7 Register Fast Mode**
Mnemonic	TP.TPCHIP.PIB.I2CM.DATA0TO7_REGISTER_C
Address	00000000000A1003 (SCOM)
Description	DATA0to7 Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	PIB_DATA0TO7_1: First eight bytes of data for read and for write, the 5th byte to 12th byte.

Register Name	**FIFO1 Register Read C**
Mnemonic	TP.TPCHIP.PIB.I2CM.FIFO1_REGISTER_READ_C
Address	00000000000A1004 (SCOM)
Description	FIFO1 Register Read C

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_1: Because FIFO is not a normal register, it cannot be completely verified in REGCHK. Thus, this register is a dummy register that is used to maintain the address in HTML FIFO data byte 0. It should be able to read or write 1 byte.
8:31	RO	constant = 0b00000000000000000000000000
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command : Written with a new command when the old command is still in progress. 1 = Parity error: 2 = Back end overrun error: Writing or reading into full or empty FIFO reply. 3 = Back end access error: Writing/reading more data than requested. 4 = Arbitration lost error: I2C bus is held by some other master when trying to access. 5 = NACK received error: The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Command Register C
Mnemonic	TP.TPCHIP.PIB.I2CM.COMMAND_REGISTER_C
Address	00000000000A1005 (SCOM)
Description	COMMAND Register C

Bits	SCOM	Field Mnemonic: Description
0	RWX	WITH_START_1: Decides if the start command is to be issued during the beginning of the operation.
1	RWX	WITH_ADDRESS_1: Decides if the device address is to be sent during the beginning of the operation.
2	RWX	READ_CONTINUE_1: Decides if the next read operation is a continuation of the present operation.
3	RWX	WITH_STOP_1: Decides if the stop command is to be issued during the end of the operation.
4:7	RWX	NOT_USED_1: Not used.
8:14	RWX	DEVICE_ADDRESS_1: Device address of the slave on the I2C bus.
15	RWX	READ_NOT_WRITE_1: I2C read or write.
16:31	RWX	LENGTH_IN_BYTES_1: The length of bytes to be accessed through the I2C bus.
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Mode Register C
Mnemonic	TP.TPCHIP.PIB.I2CM.MODE_REGISTER_C
Address	00000000000A1006 (SCOM)
Description	Mode Register C

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	BIT_RATE_DIVISOR_1: Decides the speed on the I2C bus.
8:9	RWX	BIT_RATE_DIVISOR_1: Decides the speed on the I2C bus.
10:15	RWX	BIT_RATE_DIVISOR_1: Decides the speed on the I2C bus.
16:21	RWX	PORT_NUMBER_1: Port number.
22:25	RO	constant = 0b0000
26	RWX	CHKSW_CMDQUEUEING_1: Debug switch to switch the command queuing option off.
27	RWX	CHKSW_I2C_BUSY_1: A debug switch to switch between the Port Busy Register and I2C busy muxing logic. **Note:** If you do not enable the chicken switch, the older logic behavior occurs.
28	RWX	FGAT_MODE_1: FGAT mode.
29	RWX	DIAG_MODE_1: Diagnostic mode.
30	RWX	PACING_ALLOW_MODE_1: Pacing allow mode.
31	RWX	WRAP_MODE_1: WRAP_MODE.

Bits	SCOM	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Water Mark Register C
Mnemonic	TP.TPCHIP.PIB.I2CM.WATER_MARK_REGISTER_C
Address	00000000000A1007 (SCOM)
Description	WATER_MARK Register C

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	RWX	WATERMARK_REG_1: Water mark register.
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupt Mask Register C
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_MASK_REGISTER_C
Address	00000000000A1008 (SCOM) 00000000000A1009 (SCOM1) 00000000000A100A (SCOM2)
Description	INTERRUPT_MASK Register C

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:15	RO	RO	RO	constant = 0b0000000000000000
16:31	WOX	WOX_OR	WOX_AND	INT_MASK_1: Interrupt mask register.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	Interrupt Mask Register Read_C
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_MASK_REGISTER_READ_C
Address	00000000000A1008 (SCOM)
Description	INTERRUPT_MASK Register read_C

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	ROX	INT_MASK_1: Interrupt mask register.
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupt Condition C
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_COND_C
Address	00000000000A1009 (SCOM)
Description	Interrupt Condition C

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16	ROX	INVALID_CMD_1: Invalid command. A new command was given when the old command was not yet completed.
17	ROX	LBUS_PARITY_ERROR_1: Local bus parity error.
18	ROX	BE_OV_ERROR_1: Back end overrun error. Writing or reading into full or empty FIFO reply.
19	ROX	BE_ACC_ERROR_1: Back end access error. Writing/Reading more data than requested.
20	ROX	ARBITRATION_LOST_ERROR_1: Arbitration lost error. I2C bus is held by some other master when trying to access.
21	ROX	NACK_RECEIVED_ERROR_1: NACK received error. The slave does not respond with the acknowledgment.
22	ROX	DATA_REQUEST_1: Data request. The FIFO must be accessed more to fulfill the expectation.
23	ROX	INT_CONDS_CMD_COMPLETE_1
24	ROX	STOP_ERROR_1: Stop error. Cannot send the stop condition to the bus.
25	ROX	INT_CONDS_I2C_BUSY_1
26	ROX	INT_CONDS_NOT_I2C_BUSY_1
27	RO	constant = 0b0
28	ROX	INT_CONDS_SCL_EQ_1_1. Interrupt conditions.
29	ROX	INT_CONDS_SCL_EQ_0_1

Bits	SCOM	Field Mnemonic: Description
30	ROX	INT_CONDS_SDA_EQ_1_1
31	ROX	INT_CONDS_SDA_EQ_0_1
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupts Register C
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPTS_C
Address	00000000000A100A (SCOM)
Description	Interrupts Register C

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Ints_1. Interrupts.
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Reset I2C C
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_I2C_C
Address	00000000000A100B (SCOM)
Description	IMM_RESET_I2C_C

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_I2C_1. Resets command, mode, watermark, interrupt mask, and status registers.

Register Name	Status Register Engine C
Mnemonic	TP.TPCHIP.PIB.I2CM.STATUS_REGISTER_ENGINE_C
Address	00000000000A100B (SCOM)
Description	STATUS Register ENGINE_C

Bits	SCOM	Field Mnemonic: Description
0	ROX	INVALID_CMD_1: Invalid command. A new command was given when the old command was not yet completed.
1	ROX	LBUS_PARITY_ERROR_1: Local bus parity error.
2	ROX	BE_OV_ERROR_1: Back end overrun error. Writing or reading into full or empty FIFO reply.
3	ROX	BE_ACC_ERROR_1: Back end access error. Writing or reading more data than requested.
4	ROX	ARBITRATION_LOST_ERROR_1: Arbitration lost error. I2C bus is held by some other master when trying to access.
5	ROX	NACK_RECEIVED_ERROR_1: NACK received error. The slave does not respond with the acknowledgment.
6	ROX	DATA_REQUEST_1: Data request. The FIFO must be accessed more to fulfill the expectation.
7	ROX	CMD_COMPLETE_1. Command complete. Indicates the completion of command.
8	ROX	STOP_ERROR_1: Stop error: Cannot send the stop condition to the bus.
9:15	ROX	MAX_NUM_OF_PORTS_1. Maximum number of ports defined for this engine.
16	ROX	ANY_I2C_INT_1
17:18	RO	constant = 0b00
19	ROX	I2C_PORT_HISTORY_BUSY_1
20	ROX	SCL_SYN_1
21	ROX	SDA_SYN_1
22	ROX	I2C_BUSY_1. I2C bus is occupied.
23	ROX	SELF_BUSY_1: Self busy. I2C bus is occupied by itself.
24:27	RO	constant = 0b0000
28:31	ROX	FIFO_ENTRY_COUNT_1. The number of bytes that are present in the FIFO.
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:43	RO	constant = 0b000
44:47	ROX	I2CM_STEERED_INTERRUPTS_1: Steered I2CM_INTERRUPT either for fast mode or legacy mode.
48:63	RO	constant = 0b0000000000000000

Register Name	Extended Status C
Mnemonic	TP.TPCHIP.PIB.I2CM.EXTENDED_STATUS_C
Address	00000000000A100C (SCOM)
Description	Extended Status C

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_SIZE_1. Total FIFO size.
8:10	RO	constant = 0b000
11:15	ROX	MSM_CURR_STATE_1: Current state.
16	ROX	SCL_SYN_ext_1
17	ROX	SDA_SYN_EXT_1
18	ROX	S_SCL_1. Clock input for wrap mode.
19	ROX	S_SDA_1. Data input for wrap mode.
20	ROX	M_SCL_1.Clock output for wrap mode.
21	ROX	M_SDA_1.Data output for wrap mode.
22	ROX	HIGH_WATER_1. FIFO reached highest water level.
23	ROX	LOW_WATER_1. FIFO reached lowest water level.
24	ROX	I2C_BUSY_EXT_1. I2C bus is busy.
25	ROX	SELF_BUSY_1: self busy: I2C bus is held busy by itself.
26:31	RO	constant = 0b010111
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Reset Error C
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_ERR_C
Address	00000000000A100C (SCOM)
Description	IMM Reset Error C

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_ERRORS_1. Resets FIFO. Some status bits and state machine.

Register Name	IMM Sets SCL_C
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_SET_S_SCL_C
Address	00000000000A100D (SCOM)
Description	IMM Sets SCL_C

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SCL_1.Sets output S_SCL.

Register Name	Residual Front End Back End Length C
Mnemonic	TP.TPCHIP.PIB.I2CM.RESIDUAL_FRONT_END_BACK_END_LENGTH_C
Address	00000000000A100D (SCOM)
Description	Residual Front End Back End Length C

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	RESID_FE_LEN_1: Residual front end length register.
16:31	ROX	RESID_BE_LEN_1. Residual back end length register.
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	I2C Busy Register C
Mnemonic	TP.TPCHIP.PIB.I2CM.I2C_BUSY_REGISTER_C
Address	00000000000A100E (SCOM)
Description	I2c Busy Register C

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PORT_BUSY_1. Corresponding port is busy. If it is ‘1’, no one can access. If ‘0’ , it can be accessed.
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Resets SCL_C
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_S_SCL_C
Address	00000000000A100F (SCOM)
Description	IMM_RESET_S_SCL_C

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SCL_1. Resets output S_SCL.

Register Name	IMM Sets SDA_C
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_SET_S_SDA_C
Address	00000000000A1010 (SCOM)
Description	IMM_SET_S_SDA_C

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SDA_1. Sets output S_SDA.

Register Name	IMM Resets SDA_C
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_S_SDA_C
Address	00000000000A1011 (SCOM)
Description	IMM_RESET_S_SDA_C

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SDA_1. Resets output S_SDA.

Register Name	FIFO4 Register READ_C
Mnemonic	TP.TPCHIP.PIB.I2CM.FIFO4_REGISTER_READ_C
Address	00000000000A1012 (SCOM)
Description	FIFO4 Register READ_C

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_1: Because FIFO is not a normal register, it cannot be completely verified in REGCHK. Thus, this register is a dummy register that is used to maintain the address in HTML FIFO data byte 0. It should be able to read or write 1 byte.
8:15	ROX	Reserved field.
16:23	ROX	Reserved field.
24:31	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_1: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_1: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	CC Protect Mode Register
Mnemonic	TP.TPCHIP.PIB.I2CM.PIBI2CM_PROTECT_MODE_REG_C
Address	00000000000A13FE (SCOM)
Description	CC Protect Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE_1: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE_1: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.PIB.I2CM.PIBI2CM_ATOMIC_LOCK_REG_C
Address	00000000000A13FF (SCOM)
Description	Atomic Lock Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE_1: Enable atomic lock.
1:4	ROX	CC_ATOMIC_ID_1: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY_1: Atomic lock counter.

Register Name	Control Register Fast Mode 2
Mnemonic	TP.TPCHIP.PIB.I2CM.CONTROL_REGISTER_D
Address	00000000000A2000 (SCOM)
Description	Control Register Fast Mode 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	PIB_CNTR_REG_BIT_WITHSTART_2: For the command register of the I2C engine.
1	RWX	PIB_CNTR_REG_BIT_WITHADDR_2: For command register of I2C engine.
2	RWX	PIB_CNTR_REG_BIT_READCONT_2: For command register of I2C engine.
3	RWX	PIB_CNTR_REG_BIT_WITHSTOP_2: For command register of I2C engine.

Bits	SCOM	Field Mnemonic: Description
4:7	RWX	PIB_CNTR_REG_LENGTH_2: Maximum_write = 4 , Maximum_read = 8.
8:14	RWX	PIB_CNTR_REG_ADDR_2: For command register of I2C engine.
15	RWX	PIB_CNTR_REG_BIT_RNW_2: For command register of I2C engine.
16:17	RWX	PIB_CNTR_REG_SPEED_2: 00 = 100 K 01 = 400 K 10 = 3400 K 11 = 50 K
18:22	RWX	PIB_CNTR_REG_PORT_NUMBER_2: For mode register of I2C engine.
23:25	RWX	REG_ADDR_LEN_2: 00 = No register address in FIFO 01= 1 byte of the FIFO data is the register address 10 = 2 byte of FIFO data are the register address 11 = 3 byte of FIFO data are are the register address
26	RWX	ENH_MODE_2: Enable enhanced mode in mode register of I2C engine.
27	RWX	ECC_ENABLE_2: Enables ECC for the current operation.
28	RWX	ECCCHK_DISABLE_2: Disables ECC checking for Read operation when ECC is enabled.
29	RWX	UNUSED_2: Reserved. Not used.
30:31	RWX	FAST_MODE_INTERRUPT_STERRING_BITS_2: Decides which master should see the done interrupt of fast_mode.
32:39	RWX	PIB_CNTR_REG_DATA_1_2: Data for I2C FIFO.
40:47	RWX	PIB_CNTR_REG_DATA_2_2: Data for I2C FIFO.
48:55	RWX	PIB_CNTR_REG_DATA_3_2: Data for I2C FIFO.
56:63	RWX	PIB_CNTR_REG_DATA_4_2: Data for I2C FIFO.

Register Name	DATA8to15 Register Read Only Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.DATA8TO15_REGISTER_D
Address	00000000000A2001 (SCOM)
Description	DATA8to15 Register Read Only Fast Mode

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	PIB_DATA8TO15_2: The last 8 bytes of data for read. It is not available for write operation.

Register Name	Reset Register Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.RESET_REGISTER_D
Address	00000000000A2001 (SCOM)
Description	Reset Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0	WOX	OVERALL_RESET_2. One bit register resets all registers and the I2C engine.
1	WOX	CHKSW_AR012_2: Debug switch to disable the enhanced PIB error handling.

Register Name	Status Register Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.STATUS_REGISTER_D
Address	00000000000A2002 (SCOM)
Description	Status Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0	ROX	BUS_STATUS_ADDR_NVLD_2: Address invalid.
1	ROX	BUS_STATUS_WRITE_NVLD_2: Write invalid.
2	ROX	BUS_STATUS_READ_NVLD_2: Read invalid.
3	ROX	BUS_STATUS_ADDR_P_ERR_2: Address parity error.
4	ROX	BUS_STATUS_PAR_ERR_2: Data parity error.
5	ROX	BUS_STATUS_LB_PARITY_ERROR_2: Local bus parity error.
6:37	ROX	PIB_DATA0TO7_2: First eight bytes of data for read and for write, the 5th byte to 12th byte.
38:40	RO	constant = 0b000
41	ROX	ECC_CORRECTED_ERROR_2: This warning indicates that one bit flip was in data and has been corrected.
42	ROX	ECC_UNCORRECTED_ERROR_2: This error indicates that there are two bit flips in read data that cannot be corrected.
43	ROX	ECC_CONFIG_ERROR_2: This the error indicates that the control register is ECC_ENABLED for DATA_LENGTH not equal to eight. OR ECC is enabled for the engine where the ECC block is not at all instantiated.
44	ROX	BUS_STATUS_BUSY_2: Local bus busy.
45	ROX	BUS_STATUS_INVALID_COMMAND_2: Invalid command.
46	ROX	BUS_STATUS_PARITY_ERROR_2: Parity error.
47	ROX	BUS_STATUS_BACK_END_OVERRUN_ERROR_2: Back end overrun error.
48	ROX	BUS_STATUS_BACK_END_ACCESS_ERROR_2: Back end access error.
49	ROX	BUS_STATUS_ARBITRATION_LOST_ERROR_2: Arbitration lost error.
50	ROX	BUS_STATUS_NACK_RECEIVED_ERROR_2: NACK received error.
51	ROX	BUS_STATUS_DATA_REQUEST_2: Data request.
52	ROX	BUS_STATUS_COMMAND_COMPLETE_2: Command complete.
53	ROX	BUS_STATUS_STOP_ERROR_2: Stop error.
54	ROX	BUS_STATUS_I2C_PORT_BUSY_2: I2C port busy.
55	ROX	BUS_STATUS_I2C_INTERFACE_BUSY_2: I2C interface busy.
56:63	ROX	BUS_STATUS_FIFO_ENTRY_COUNT_2: FIFO entry count.

Register Name	DATA0to7 Register Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.DATA0TO7_REGISTER_D
Address	00000000000A2003 (SCOM)
Description	DATA0to7 Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	PIB_DATA0TO7_2: First eight bytes of data for read and for write, the 5th byte to 12th byte.

Register Name	FIFO1 Register Read D
Mnemonic	TP.TPCHIP.PIB.I2CM.FIFO1_REGISTER_READ_D
Address	00000000000A2004 (SCOM)
Description	FIFO1 Register Read D

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_2: Because FIFO is not a normal register, it cannot be completely verified in REGCHK. Thus, this register is a dummy register that is used to maintain the address in HTML FIFO data byte 0. It should be able to read or write 1 byte.
8:31	RO	constant = 0b00000000000000000000000000
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Command Register D
Mnemonic	TP.TPCHIP.PIB.I2CM.COMMAND_REGISTER_D
Address	00000000000A2005 (SCOM)
Description	Command Register D

Bits	SCOM	Field Mnemonic: Description
0	RWX	WITH_START_2: Decides if the start command is to be issued during the beginning of the operation.
1	RWX	WITH_ADDRESS_2: Decides the device address to be sent during the beginning of the operation.
2	RWX	READ_CONTINUE_2: Decides if the next read operation is a continuation of the present operation.
3	RWX	WITH_STOP_2: Decides if the stop command is to be issued during the end of the operation.
4:7	RWX	NOT_USED_2: Not used.
8:14	RWX	DEVICE_ADDRESS_2: Device address of Slave on the I2C bus. Device address of Slave on the I2C Bus.
15	RWX	READ_NOT_WRITE_2: I2C read or write.
16:31	RWX	LENGTH_IN_BYTES_2: The length of bytes to be accessed through the I2C bus.
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.

Bits	SCOM	Field Mnemonic: Description
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Mode Register D
Mnemonic	TP.TPCHIP.PIB.I2CM.MODE_REGISTER_D
Address	00000000000A2006 (SCOM)
Description	Mode Register D

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	BIT_RATE_DIVISOR_2: Decides the speed on the I2C bus. Decides the speed on the I2C bus.
8:9	RWX	BIT_RATE_DIVISOR_2: Decides the speed on the I2C bus.
10:15	RWX	BIT_RATE_DIVISOR_2: Decides the speed on the I2C bus.
16:21	RWX	PORT_NUMBER_2: Port number.
22:25	RO	constant = 0b0000
26	RWX	CHKSW_CMDQUEUEING_2: Debug switch to switch the command queuing option off.
27	RWX	CHKSW_I2C_BUSY_2: Debug switch to switch between the PORT_BUSY register and I2C_BUSY muxing logic. Without this muxed version, this version is older.
28	RWX	FGAT_MODE_2: FGAT mode.
29	RWX	DIAG_MODE_2: Diagnostic mode.
30	RWX	PACING_ALLOW_MODE_2: Pacing allow mode.
31	RWX	WRAP_MODE_2: WRAP_MODE.
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Water Mark Register D
Mnemonic	TP.TPCHIP.PIB.I2CM.WATER_MARK_REGISTER_D
Address	00000000000A2007 (SCOM)
Description	Water Mark Register D

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	RWX	WATERMARK_REG_2: Water mark register.

Bits	SCOM	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupt Mask Register D
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_MASK_REGISTER_D
Address	00000000000A2008 (SCOM) 00000000000A2009 (SCOM1) 00000000000A200A (SCOM2)
Description	Interrupt Mask Register D

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:15	RO	RO	RO	constant = 0b0000000000000000
16:31	WOX	WOX_OR	WOX_AND	INT_MASK_2: Interrupt mask register.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	Interrupt Mask Register Read D
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_MASK_REGISTER_READ_D
Address	00000000000A2008 (SCOM)
Description	Interrupt Mask Register Read D

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	ROX	INT_MASK_2: Interrupt mask register.
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupt Condition D
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_COND_D
Address	00000000000A2009 (SCOM)
Description	Interrupt Condition D

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16	ROX	INVALID_CMD_2: Invalid command. A new command was given when the old command was not yet completed.
17	ROX	LBUS_PARITY_ERROR_2: Local bus parity error.
18	ROX	BE_OV_ERROR_2: Back end overrun error. Writing or reading into full or empty FIFO reply.
19	ROX	BE_ACC_ERROR_2: Back end access error. Writing or reading more data than requested.
20	ROX	ARBITRATION_LOST_ERROR_2: Arbitration lost error: I2C bus is held by some other master when trying to access.
21	ROX	NACK_RECEIVED_ERROR_2: NACK received error: The slave does not respond with the acknowledgment. Interrupt conditions.
22	ROX	DATA_REQUEST_2: Data request: The FIFO must be accessed more to fulfill the expectation.
23	ROX	INT_CONDS_CMD_COMPLETE_2.
24	ROX	STOP_ERROR_2: Stop error: Cannot send the stop condition to the bus.
25	ROX	INT_CONDS_I2C_BUSY_2.
26	ROX	INT_CONDS_NOT_I2C_BUSY_2.
27	RO	constant = 0b0
28	ROX	INT_CONDS_SCL_EQ_1_2.
29	ROX	INT_CONDS_SCL_EQ_0_2.
30	ROX	INT_CONDS_SDA_EQ_1_2.
31	ROX	INT_CONDS_SDA_EQ_0_2.
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupts Register D
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPTS_D
Address	00000000000A200A (SCOM)
Description	Interrupts Register D

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Ints_2: Interrupts.
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	**IMM Reset I2C D**
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_I2C_D
Address	00000000000A200B (SCOM)
Description	IIMM Reset I2C D

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_I2C_2. Resets command, mode, watermark, interrupt mask, and status registers.

Register Name	**Status Register Engine D**
Mnemonic	TP.TPCHIP.PIB.I2CM.STATUS_REGISTER_ENGINE_D
Address	00000000000A200B (SCOM)
Description	Status Register Engine D

Bits	SCOM	Field Mnemonic: Description
0	ROX	INVALID_CMD_2: Invalid command. A new command was given when the old command was not yet completed.
1	ROX	LBUS_PARITY_ERROR_2: Local bus parity error.
2	ROX	BE_OV_ERROR_2: Back end overrun error: Writing or reading into full or empty FIFO reply. back end overrun error.
3	ROX	BE_ACC_ERROR_2: Back end access error. Writing or reading more data than requested. back end access error.
4	ROX	ARBITRATION_LOST_ERROR_2: Arbitration lost error: I2C bus is held by some other master when trying to access.
5	ROX	NACK_RECEIVED_ERROR_2: NACK received error. The slave does not respond with the acknowledgment.
6	ROX	DATA_REQUEST_2: Data request: The FIFO must be accessed more to fulfill the expectation.
7	ROX	CMD_COMPLETE_2. Command complete: Indicates the completion of command.
8	ROX	STOP_ERROR_2: stop error: Cannot send the stop condition to the bus.
9:15	ROX	MAX_NUM_OF_PORTS_2. Maximum number of ports defined for this engine.
16	ROX	ANY_I2C_INT_2.
17:18	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
19	ROX	I2C_PORT_HISTORY_BUSY_2.
20	ROX	SCL_SYN_2.
21	ROX	SDA_SYN_2.
22	ROX	i2c_busy_2. I2C bus is occupied.
23	ROX	SELF_BUSY_2: I2C bus is occupied by itself.
24:27	RO	constant = 0b0000
28:31	ROX	FIFO_ENTRY_COUNT_2: The number of bytes that are present in the FIFO.
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:43	RO	constant = 0b000
44:47	ROX	I2CM_STEERED_INTERRUPTS_2: Steered I2CM_INTERRUPT either for fast mode or legacy mode.
48:63	RO	constant = 0b0000000000000000

Register Name	Extended Status D
Mnemonic	TP.TPCHIP.PIB.I2CM.EXTENDED_STATUS_D
Address	00000000000A200C (SCOM)
Description	Extended Status D

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_SIZE_2. Total FIFO size.
8:10	RO	constant = 0b000
11:15	ROX	MSM_CURR_STATE_2: Current state.
16	ROX	SCL_SYN_ext_2.
17	ROX	SDA_SYN_EXT_2.
18	ROX	S_SCL_2. Clock input for wrap mode.
19	ROX	S_SDA_2. Data input for wrap mode.
20	ROX	M_SCL_2. Clock output for wrap mode.
21	ROX	M_SDA_2. Data output for wrap mode.
22	ROX	HIGH_WATER_2. High water mark. FIFO reached highest water level.
23	ROX	LOW_WATER_2.Low water mark. FIFO reached lowest water level.
24	ROX	I2C_BUSY_EXT_2. I2C bus is busy.
25	ROX	SELF_BUSY_2: Self busy: I2C bus is occupied by itself.
26:31	RO	constant = 0b010111

Bits	SCOM	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Reset Error D
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_ERR_D
Address	00000000000A200C (SCOM)
Description	IMM Reset Error D

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_ERRORS_2. Resets FIFO. Some status bits and state machine.

Register Name	IMM Sets SCL_D
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_SET_S_SCL_D
Address	00000000000A200D (SCOM)
Description	IMM Sets SCL_D

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SCL_2. Sets output S_SCL.

Register Name	Residual Front End Back End Length D
Mnemonic	TP.TPCHIP.PIB.I2CM.RESIDUAL_FRONT_END_BACK_END_LENGTH_D
Address	00000000000A200D (SCOM)
Description	Residual Front End Back End Length D

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	RESID_FE_LEN_2: Residual front end length register.
16:31	ROX	RESID_BE_LEN_2. Residual back end length register.
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.

Bits	SCOM	Field Mnemonic: Description
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	I2C Busy Register D
Mnemonic	TP.TPCHIP.PIB.I2CM.I2C_BUSY_REGISTER_D
Address	00000000000A200E (SCOM)
Description	I2C Busy Register D

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PORT_BUSY_2. The corresponding port is busy. If it is ‘1’ no one can access it. If it is ‘0’, it can be accessed.
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Resets SCL_D
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_S_SCL_D
Address	00000000000A200F (SCOM)
Description	IMM Resets SCL_D

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SCL_2. Resets output S_SCL.

Register Name	IMM Sets SDA_D
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_SET_S_SDA_D
Address	00000000000A2010 (SCOM)
Description	IMM Sets SDA_D

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SDA_2. Sets output S_SDA.

Register Name	IMM Resets SDA_D
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_S_SDA_D
Address	00000000000A2011 (SCOM)
Description	IMM Resets SDA_D

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SDA_2. Resets output S_SDA.

Register Name	FIFO4 Register Read D
Mnemonic	TP.TPCHIP.PIB.I2CM.FIFO4_REGISTER_READ_D
Address	00000000000A2012 (SCOM)
Description	FIFO4 Register Read D

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_2: Because FIFO is not a normal register, it cannot be completely verified in REGCHK. Thus, this register is a dummy register that is used to maintain the address in HTML FIFO data byte 0. It should be able to read or write 1 byte.
8:15	ROX	Reserved field.
16:23	ROX	Reserved field.
24:31	ROX	Reserved field.
32:39	ROX	PEEK_DATA1_2: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_2: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	CC Protect Mode Register
Mnemonic	TP.TPCHIP.PIB.I2CM.PIBI2CM_PROTECT_MODE_REG_D
Address	00000000000A23FE (SCOM)
Description	CC Protect Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE_2: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE_2: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.PIB.I2CM.PIBI2CM_ATOMIC_LOCK_REG_D
Address	00000000000A23FF (SCOM)
Description	Atomic Lock Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE_2: Enable atomic lock.
1:4	ROX	CC_ATOMIC_ID_2: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY_2: Atomic lock counter.

Register Name	CONTROL REGISTER_FAST_MODE_3
Mnemonic	TP.TPCHIP.PIB.I2CM.CONTROL_REGISTER_E
Address	00000000000A3000 (SCOM)
Description	CONTROL REGISTER_FAST_MODE_3

Bits	SCOM	Field Mnemonic: Description
0	RWX	PIB_CNTR_REG_BIT_WITHSTART_3: For command register of I2C engine.
1	RWX	PIB_CNTR_REG_BIT_WITHADDR_3: For command register of I2C engine.
2	RWX	PIB_CNTR_REG_BIT_READCONT_3: For command register of I2C engine.
3	RWX	PIB_CNTR_REG_BIT_WITHSTOP_3: For command register of I2C engine.
4:7	RWX	PIB_CNTR_REG_LENGTH_3: Maximum_write = 4 , Maximum_read = 8.
8:14	RWX	PIB_CNTR_REG_ADDR_3: For command register of I2C engine.
15	RWX	PIB_CNTR_REG_BIT_RNW_3: For command register of I2C engine.
16:17	RWX	PIB_CNTR_REG_SPEED_3: 00 = 100 K 01 = 400 K 10 = 3400 K 11 = 50 K
18:22	RWX	PIB_CNTR_REG_PORT_NUMBER_3: For mode register of I2C engine.
23:25	RWX	REG_ADDR_LEN_3: 00 = No register address in FIFO 01= 1 byte of the FIFO data is the register address 10 = 2 byte of FIFO data are the register address 11 = 3 byte of FIFO data are are the register address
26	RWX	ENH_MODE_3: Enable enhanced mode in mode register of I2C engine.
27	RWX	ECC_ENABLE_3: Enables ECC for the current operation.
28	RWX	ECCCHK_DISABLE_3: Disables ECC checking for Read operation when ECC is enabled.
29	RWX	UNUSED_3: Reserved. Not used.
30:31	RWX	FAST_MODE_INTERRUPT_STERRING_BITS_3: Decides which master should see the done interrupt of FAST_MODE.
32:39	RWX	PIB_CNTR_REG_DATA_1_3: Data for I2C FIFO.
40:47	RWX	PIB_CNTR_REG_DATA_2_3: Data for I2C FIFO.
48:55	RWX	PIB_CNTR_REG_DATA_3_3: Data for I2C FIFO.

Bits	SCOM	Field Mnemonic: Description
56:63	RWX	PIB_CNTR_REG_DATA_4_3: Data for I2C FIFO.

Register Name	DATA8to15 Register Read Only Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.DATA8TO15_REGISTER_E
Address	00000000000A3001 (SCOM)
Description	DATA8to15 Register Register Read Only Fast Mode

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	PIB_DATA8TO15_3: The last 8 bytes of data for read. It is not available for write operation.

Register Name	Reset Register Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.RESET_REGISTER_E
Address	00000000000A3001 (SCOM)
Description	Reset Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0	WOX	OVERALL_RESET_3. One bit register resets all registers and the I2C engine.
1	WOX	CHKSW_AR012_3: Debug switch to disable the enhanced PIB error handling.

Register Name	Status Register Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.STATUS_REGISTER_E
Address	00000000000A3002 (SCOM)
Description	Status Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0	ROX	BUS_STATUS_ADDR_NVLD_3: Address invalid.
1	ROX	BUS_STATUS_WRITE_NVLD_3: Write invalid.
2	ROX	BUS_STATUS_READ_NVLD_3: Read invalid.
3	ROX	BUS_STATUS_ADDR_P_ERR_3: Address parity error.
4	ROX	BUS_STATUS_PAR_ERR_3: Data parity error.
5	ROX	BUS_STATUS_LB_PARITY_ERROR_3: Local bus parity error.
6:37	ROX	PIB_DATA0TO7_3: First eight bytes of data for read and for write, the 5th byte to 12th byte.
38:40	RO	constant = 0b000
41	ROX	ECC_CORRECTED_ERROR_3: This warning indicates that one bit flip was in data and has been corrected.
42	ROX	ECC_UNCORRECTED_ERROR_3: This error indicates that there are two bit flips in read data that cannot be corrected.
43	ROX	ECC_CONFIG_ERROR_3: This the error indicates that the control register is ECC_ENABLED for DATA_LENGTH not equal to eight. OR ECC is enabled for the engine where the ECC block is not at all instantiated.
44	ROX	BUS_STATUS_BUSY_3: Local bus busy.

Bits	SCOM	Field Mnemonic: Description
45	ROX	BUS_STATUS_INVALID_COMMAND_3: Invalid command.
46	ROX	BUS_STATUS_PARITY_ERROR_3: Parity error.
47	ROX	BUS_STATUS_BACK_END_OVERRUN_ERROR_3 = Back end overrun error.
48	ROX	BUS_STATUS_BACK_END_ACCESS_ERROR_3 = Back end access error.
49	ROX	BUS_STATUS_ARBITRATION_LOST_ERROR_3: Arbitration lost error.
50	ROX	BUS_STATUS_NACK_RECEIVED_ERROR_3: NACK received error.
51	ROX	BUS_STATUS_DATA_REQUEST_3: Data request.
52	ROX	BUS_STATUS_COMMAND_COMPLETE_3: command complete.
53	ROX	BUS_STATUS_STOP_ERROR_3: Stop error.
54	ROX	BUS_STATUS_I2C_PORT_BUSY_3: I2C port busy.
55	ROX	BUS_STATUS_I2C_INTERFACE_BUSY_3: I2C interface busy.
56:63	ROX	BUS_STATUS_FIFO_ENTRY_COUNT_3: FIFO entry count.

Register Name	DATA0to7 Register Fast Mode
Mnemonic	TP.TPCHIP.PIB.I2CM.DATA0TO7_REGISTER_E
Address	00000000000A3003 (SCOM)
Description	DATA0to7 Register Fast Mode

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	PIB_DATA0TO7_3: First eight bytes of data for read and for write, the 5th byte to 12th byte.

Register Name	FIFO1 Register Read_E
Mnemonic	TP.TPCHIP.PIB.I2CM.FIFO1_REGISTER_READ_E
Address	00000000000A3004 (SCOM)
Description	FIFO1 Register Read_E

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_3: Because FIFO is not a normal register, it cannot be completely verified in REGCHK. Thus, this register is a dummy register that is used to maintain the address in HTML FIFO data byte 0. It should be able to read or write 1 byte.
8:31	RO	constant = 0b00000000000000000000000000
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3:
41:63	RO	constant = 0b00000000000000000000000

Register Name	Command Register E
Mnemonic	TP.TPCHIP.PIB.I2CM.COMMAND_REGISTER_E
Address	00000000000A3005 (SCOM)
Description	Command Register E

Bits	SCOM	Field Mnemonic: Description
0	RWX	WITH_START_3: Decides if the start command is to be issued during the beginning of the operation.
1	RWX	WITH_ADDRESS_3: Decides the device address to be sent during the beginning of the operation.
2	RWX	READ_CONTINUE_3: Decides if the next read operation is a continuation of the present operation.
3	RWX	WITH_STOP_3: Decides if the stop command is to be issued during the end of the operation.
4:7	RWX	NOT_USED_3: Not used.
8:14	RWX	DEVICE_ADDRESS_3: The device address of slave on the I2C bus.
15	RWX	READ_NOT_WRITE_3: I2C read or write.
16:31	RWX	LENGTH_IN_BYTES_3: The length of bytes to be accessed through the I2C bus.
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Mode Register E
Mnemonic	TP.TPCHIP.PIB.I2CM.MODE_REGISTER_E
Address	00000000000A3006 (SCOM)
Description	Mode Register E

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	BIT_RATE_DIVISOR_3: Decides the speed on the I2C bus.
8:9	RWX	BIT_RATE_DIVISOR_3: Decides the speed on the I2C bus.
10:15	RWX	BIT_RATE_DIVISOR_3: Decides the speed on the I2C bus. port number.
16:21	RWX	PORT_NUMBER_3: Port number.
22:25	RO	constant = 0b0000
26	RWX	CHKSW_CMDQUEUEING_3: Debug switch to switch the command queuing option off.
27	RWX	CHKSW_I2C_BUSY_3: Debug switch to switch between the PORT_BUSY register and I2C_BUSY muxing logic. Without this muxed version, this version is older.
28	RWX	FGAT_MODE_3: FGAT mode.
29	RWX	DIAG_MODE_3: Diagnostic mode.
30	RWX	PACING_ALLOW_MODE_3: Pacing allow mode.

Bits	SCOM	Field Mnemonic: Description
31	RWX	WRAP_MODE_3: WRAP_MODE.
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Water Mark Register E
Mnemonic	TP.TPCHIP.PIB.I2CM.WATER_MARK_REGISTER_E
Address	00000000000A3007 (SCOM)
Description	Water Mark Register E

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	RWX	WATERMARK_REG_3: Water mark register.
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupt Mask Register E
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_MASK_REGISTER_E
Address	00000000000A3008 (SCOM) 00000000000A3009 (SCOM1) 00000000000A300A (SCOM2)
Description	Interrupt Mask Register E

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:15	RO	RO	RO	constant = 0b0000000000000000
16:31	WOX	WOX_OR	WOX_AND	INT_MASK_3: Interrupt mask register
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	Interrupt Mask Register Read E
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_MASK_REGISTER_READ_E
Address	00000000000A3008 (SCOM)
Description	Interrupt Mask Register Read E

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:31	ROX	INT_MASK_3: Interrupt mask register.
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupt Condition E
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPT_COND_E
Address	00000000000A3009 (SCOM)
Description	Interrupt Condition E

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16	ROX	INVALID_CMD_3: Invalid command. A new command was given when the old command was not yet completed.
17	ROX	LBUS_PARITY_ERROR_3: Local bus parity error.
18	ROX	BE_OV_ERROR_3 = Back end overrun error. Writing or reading into full or empty FIFO reply.
19	ROX	BE_ACC_ERROR_3 = Back end access error. Writing/Reading more data than requested.
20	ROX	ARBITRATION_LOST_ERROR_3: Arbitration lost error. I2C bus is held by some other master when trying to access.
21	ROX	NACK_RECEIVED_ERROR_3: NACK received error. The slave does not respond with the acknowledgment.
22	ROX	DATA_REQUEST_3: Data request. The FIFO must be accessed more to fulfill the expectation.
23	ROX	INT_CONDS_CMD_COMPLETE_3
24	ROX	STOP_ERROR_3: Stop error: Cannot send the stop condition to the bus.
25	ROX	INT_CONDS_I2C_BUSY_3
26	ROX	INT_CONDS_NOT_I2C_BUSY_3
27	RO	constant = 0b0
28	ROX	INT_CONDS_SCL_EQ_1_3
29	ROX	INT_CONDS_SCL_EQ_0_3

Bits	SCOM	Field Mnemonic: Description
30	ROX	INT_CONDS_SDA_EQ_1_3
31	ROX	INT_CONDS_SDA_EQ_0_3
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Interrupts Register E
Mnemonic	TP.TPCHIP.PIB.I2CM.INTERRUPTS_E
Address	00000000000A300A (SCOM)
Description	INTERRUPTS_REGISTER_E

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Ints_3. interrupts.
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Reset I2C E
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_I2C_E
Address	00000000000A300B (SCOM)
Description	IMM Reset I2C E

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_I2C_3. Resets command, mode, watermark, interrupt mask, and status registers.

Register Name	Status Register Engine E
Mnemonic	TP.TPCHIP.PIB.I2CM.STATUS_REGISTER_ENGINE_E
Address	00000000000A300B (SCOM)
Description	Status Register Engine E

Bits	SCOM	Field Mnemonic: Description
0	ROX	INVALID_CMD_3: Invalid command. A new command was given when the old command was not yet completed.
1	ROX	LBUS_PARITY_ERROR_3: Local bus parity error.
2	ROX	BE_OV_ERROR_3 = Back end overrun error : Writing or reading into full or empty FIFO reply.
3	ROX	BE_ACC_ERROR_3 = Back end access error : Writing/Reading more data than requested.
4	ROX	ARBITRATION_LOST_ERROR_3: Arbitration lost error: I2C bus is held by some other master when trying to access.
5	ROX	NACK_RECEIVED_ERROR_3: NACK received error. The slave does not respond with the acknowledgment.
6	ROX	DATA_REQUEST_3: The FIFO must be accessed more to fulfill the expectation.
7	ROX	CMD_COMPLETE_3. Indicates the completion of command.
8	ROX	STOP_ERROR_3: stop error: Cannot send the stop condition to the bus.
9:15	ROX	MAX_NUM_OF_PORTS_3. The maximum number of ports defined for this engine.
16	ROX	ANY_I2C_INT_3
17:18	RO	constant = 0b00
19	ROX	I2C_PORT_HISTORY_BUSY_3
20	ROX	SCL_SYN_3.
21	ROX	SDA_SYN_3.
22	ROX	I2C_BUSY_3. I2C bus is occupied.
23	ROX	SELF_BUSY_3: Self busy: I2C bus is occupied by itself.
24:27	RO	constant = 0b0000
28:31	ROX	FIFO_ENTRY_COUNT_3: The number of bytes that are present in the FIFO.
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:43	RO	constant = 0b000
44:47	ROX	I2CM_STEERED_INTERRUPTS_3: Steered I2CM_INTERRUPT either for fast mode or legacy mode.
48:63	RO	constant = 0b0000000000000000

Register Name	Extended Status E
Mnemonic	TP.TPCHIP.PIB.I2CM.EXTENDED_STATUS_E
Address	00000000000A300C (SCOM)
Description	Extended Status E

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_size_3. Total FIFO size.
8:10	RO	constant = 0b000
11:15	ROX	MSM_CURR_STATE_3: Current state.
16	ROX	SCL_SYN_ext_3.
17	ROX	SDA_SYN_EXT_3.
18	ROX	S_SCL_3. Clock input for wrap mode.
19	ROX	S_SDA_3. Data input for wrap mode.
20	ROX	M_SCL_3. Clock output for wrap mode.
21	ROX	M_SDA_3. Data output for wrap mode.
22	ROX	HIGH_WATER_3. FIFO reached highest water level.
23	ROX	LOW_WATER_3. FIFO reached lowest water level.
24	ROX	I2C_BUSY_EXT_3. I2C bus is busy.
25	ROX	SELF_BUSY_3: Self busy. I2C bus is occupied by itself.
26:31	RO	constant = 0b010111
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Reset Error E
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_ERR_E
Address	00000000000A300C (SCOM)
Description	IMM Reset Error E

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_ERRORS_3. Resets FIFO. Some status bits and state machine.

Register Name	IMM Sets SCL_E
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_SET_S_SCL_E
Address	00000000000A300D (SCOM)
Description	IMM Sets SCL_E

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SCL_3. Sets output S_SCL.

Register Name	Residual Front End/Back End Length_E
Mnemonic	TP.TPCHIP.PIB.I2CM.RESIDUAL_FRONT_END_BACK_END_LENGTH_E
Address	00000000000A300D (SCOM)
Description	Residual Front End/Back End Length_E

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	RESID_FE_LEN_3. Residual front end length register.
16:31	ROX	RESID_BE_LEN_3. Residual back end length register.
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	I2C Busy Register E
Mnemonic	TP.TPCHIP.PIB.I2CM.I2C_BUSY_REGISTER_E
Address	00000000000A300E (SCOM)
Description	I2C Busy Register E

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PORT_BUSY_3. The corresponding port is busy. If it is ‘1’, no one can access it. If it is ‘0’, it can be accessed.
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.

Bits	SCOM	Field Mnemonic: Description
41:63	RO	constant = 0b00000000000000000000000

Register Name	IMM Resets SCL_E
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_S_SCL_E
Address	00000000000A300F (SCOM)
Description	IMM_RESET_S_SCL_E

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SCL_3. Resets output S_SCL.

Register Name	IMM Sets SDA_E
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_SET_S_SDA_E
Address	00000000000A3010 (SCOM)
Description	IMM Sets SDA_E

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_SET_S_SDA_3. Sets output S_SDA.

Register Name	IMM Resets SDA_E
Mnemonic	TP.TPCHIP.PIB.I2CM.IMM_RESET_S_SDA_E
Address	00000000000A3011 (SCOM)
Description	IMM Resets SDA_E

Bits	SCOM	Field Mnemonic: Description
0	WOX	IMM_RESET_S_SDA_3. Resets output S_SDA.

Register Name	FIFO4 Register Read E
Mnemonic	TP.TPCHIP.PIB.I2CM.FIFO4_REGISTER_READ_E
Address	00000000000A3012 (SCOM)
Description	FIFO4 Register Read E

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_3: Because FIFO is not a normal register, it cannot be completely verified in REGCHK. Thus, this register is a dummy register that is used to maintain the address in HTML FIFO data byte 0. It should be able to read or write 1 byte.
8:15	ROX	Reserved field.
16:23	ROX	Reserved field.
24:31	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_3: 0 = Invalid command. Written with the new command when the old command is still in progress. 1 = Parity error. 2 = Back end overrun error. Writing or reading into full or empty FIFO reply. 3 = Back end access error. Writing/reading more data than requested. 4 = Arbitration lost error. The I2C bus is held by another master when trying to access. 5 = NACK received error. The slave does not respond with the acknowledgment. 6 = Data request: FIFO must be accessed more to fulfill the expectation. 7 = State M/C idle: I2C state machine is now in idle state.
40	ROX	LBUS_PARITY_ERR1_3: Local bus parity error from the local bus to glue logic.
41:63	RO	constant = 0b00000000000000000000000

Register Name	CC Protect Mode Register
Mnemonic	TP.TPCHIP.PIB.I2CM.PIBI2CM_PROTECT_MODE_REG_E
Address	00000000000A33FE (SCOM)
Description	CC Protect Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE_3: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE_3: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.PIB.I2CM.PIBI2CM_ATOMIC_LOCK_REG_E
Address	00000000000A33FF (SCOM)
Description	Atomic Lock Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE_3: Enable atomic lock.
1:4	ROX	CC_ATOMIC_ID_3: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY_3: Atomic lock counter.

Register Name	Dequeuing Location of Upstream FIFO
Mnemonic	TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_UPFIFO_DATA_OUT
Address	00000000000B0000 (SCOM)
Description	Dequeuing location of upstream FIFO

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved field.

Register Name	Status Register of Upstream FIFO
Mnemonic	TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_UPFIFO_STATUS
Address	00000000000B0001 (SCOM)
Description	Status register of upstream FIFO

Bits	SCOM	Field Mnemonic: Description
0:5	RW	Reserved.
6	ROX	UPFIFO_STATUS_REQ_RESET_FR_SP: External service processor (SP) is requesting a FIFO reset.
7	ROX	UPFIFO_STATUS_REQ_RESET_FR_SBE: SBE is requesting a FIFO reset through downstream path.
8	ROX	UPFIFO_STATUS_DEQUEUED_EOT_FLAG: A FIFO entry has been dequeued with set EOT flag.
9	RW	Reserved.
10	ROX	UPFIFO_STATUS_FIFO_FULL: Upstream FIFO is full.
11	ROX	UPFIFO_STATUS_FIFO_EMPTY: Upstream FIFO is empty.
12:15	ROX	UPFIFO_STATUS_FIFO_ENTRY_COUNT: Number of currently hold entries.
16:23	ROX	UPFIFO_STATUS_FIFO_VALID_FLAGS: Valid flags of all currently hold entries.
24:31	ROX	UPFIFO_STATUS_FIFO_EOT_FLAGS: EOT flags of all currently hold entries.

Register Name	Applying Reset Function to Upstream and Downstream FIFO
Mnemonic	TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_UPFIFO_RESET
Address	00000000000B0004 (SCOM)
Description	Applying reset function to upstream and downstream FIFO.

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.

Register Name	Acknowledging End-of-Transfer (EOT)
Mnemonic	TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_UPFIFO_ACK_EOT
Address	00000000000B0005 (SCOM)
Description	Acknowledging end-of-transfer (EOT).

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.

Register Name	Enqueuing Location of Downstream FIFO
Mnemonic	TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_DOWNFIFO_DATA_IN
Address	00000000000B0010 (SCOM)
Description	Enqueuing location of downstream FIFO

Bits	SCOM	Field Mnemonic: Description
0:31	WOX	Reserved field.

Register Name	Status Register of Downstream FIFO
Mnemonic	TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_DOWNFIFO_STATUS
Address	00000000000B0011 (SCOM)
Description	Status Register of Downstream FIFO

Bits	SCOM	Field Mnemonic: Description
0:5	RW	Reserved.
6	ROX	DNFIFO_STATUS_REQ_RESET_FR_SBE: SBE is requesting a FIFO reset.
7	ROX	DNFIFO_STATUS_REQ_RESET_FR_SP: External Service Processor (SP) is requesting a FIFO reset through upstream path.
8	ROX	DNFIFO_STATUS_DEQUEUED_EOT_FLAG: A FIFO entry has been dequeued with set EOT flag.
9	RW	Reserved.
10	ROX	DNFIFO_STATUS_FIFO_FULL: Downstream FIFO is full.
11	ROX	DNFIFO_STATUS_FIFO_EMPTY: Downstream FIFO is empty.
12:15	ROX	DNFIFO_STATUS_FIFO_ENTRY_COUNT: Number of currently hold entries.
16:23	ROX	DNFIFO_STATUS_FIFO_VALID_FLAGS: Valid flags of ALL currently hold entries.
24:31	ROX	DNFIFO_STATUS_FIFO_EOT_FLAGS: EOT flags of ALL currently hold entries.

Register Name	Signaling Location for End-of-Transfer (EOT)
Mnemonic	TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_DOWNFIFO_SIG_EOT
Address	00000000000B0012 (SCOM)
Description	Signaling location for End-of-transfer (EOT)

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.

Register Name	Signaling Location for Requesting FIFO Reset
Mnemonic	TP.TPVSB.FSI.W.FSI_SBE_FIFO.FSB_DOWNFIFO_REQ_RESET
Address	00000000000B0013 (SCOM)
Description	Signaling location for requesting FIFO reset.

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.

Register Name	PIB History Control and Status Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_PIBHIST_CTRL_STATUS_REG
Address	00000000000D0000 (SCOM)
Description	PIB History Control and Status Register

Bits	SCOM	Field Mnemonic: Description
0	RW	HIST_MANUAL_MODE_EN: 0: history trace always running (default). 1 = Enable manual start/stop of history trace.
1	RW	HIST_START_NOT_STOP: Only valid if HIST_MANUAL_MODE_EN = 1. 0 = Stop history trace (default). 1 = Start history trace.
2	RWX	HIST_FREEZE_HISTORY: 1 = Disables history trace and freezes history registers. This bit is also set when the unit stops on error.
3	RWX	HIST_RESET_HISTORY: 1 = Clear history registers and reset control FSM. This bit is self-resetting.
4	RW	HIST_TRACE_PSU_TRAFFIC: Controls if the PIB traffic from/to the PIB slave address of the PSU is included in history trace. 0 = Do not trace PSU traffic (default). 1 = include PSU traffic.
5:7	RW	HIST_STOP_ON_ERROR_GT: Greater than value for RSP_INFO to stop history sampling. For example: 000 = Default. Stop sampling with RSP_INFO > 0. 001 = Stop sampling with RSP_INFO > 1, and so forth. 111 = Stop on error disabled.
8:15	RW	HIST_CTRL_STATUS_REG_RESERVED: Reserved.

Register Name	PIB History Filter Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_PIBHIST_FILTER_REG
Address	00000000000D0001 (SCOM)
Description	PIB History Filter Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	HIST_FILTER_ADDRESS: Compare address for history trace.
32:63	RW	HIST_FILTER_MASK: Compare mask for history trace.

Register Name	PIB History Last Address Trace Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_PIBHIST_LAST_ADDR_TRACE_REG
Address	00000000000D0002 (SCOM)
Description	PIB History Last Address Trace Register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HIST_LAST_ADDR_TRACE: History trace: last address.

Register Name	PIB History Last Request Data Trace Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_PIBHIST_LAST_REQDATA_TRACE_REG
Address	00000000000D0003 (SCOM)
Description	PIB History Last Request Data Trace Register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HIST_LAST_REQDATA_TRACE: History trace: last request data.

Register Name	PIB History Last Response Data Trace Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_PIBHIST_LAST_RSPDATA_TRACE_REG
Address	00000000000D0004 (SCOM)
Description	PIB History Last Response Data Trace Register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HIST_LAST_RSPDATA_TRACE: History trace: last response data.

Register Name	PIB History Second Last Address Trace Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_PIBHIST_2NDLAST_ADDR_TRACE_REG
Address	00000000000D0005 (SCOM)
Description	PIB History Second Last Address Trace Register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HIST_2NDLAST_ADDR_TRACE: History trace: second last address.

Register Name	PIB History Second Last Request Data Trace Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_PIBHIST_2NDLAST_REQDATA_TRACE_REG
Address	00000000000D0006 (SCOM)
Description	PIB History Second Last Request Data Trace Register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HIST_2NDLAST_REQDATA_TRACE: History trace: second last request data.

Register Name	PIB History Second Last Response Data Trace Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_PIBHIST_2NDLAST_RSPDATA_TRACE_REG
Address	00000000000D0007 (SCOM)
Description	PIB History Second Last Response Data Trace Register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	HIST_2NDLAST_RSPDATA_TRACE: History trace: second last response data.

Register Name	Instrumentation Control and Status Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR_CTRL_STATUS_REG
Address	00000000000D0010 (SCOM)
Description	Instrumentation Control and Status Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INSTR0_MODE: Mode control for instrumentation unit 0: 00 = Disabled. 01 = PIB mode (default). 10 = PCB interrupt mode. 11 = Reserved.
2	RW	INSTR0_STOP_TIMER_EN: 0: Stop measurement manually (default). 1 = Stop measurement based on STOP_TIMER.
3:5	RW	INSTR0_STOP_ON_ERROR_GT: Greater than value for RSP_INFO to stop instrumentation. 000 (default) = Stop sampling with RSP_INFO > 0. 001 = Stop sampling with RSP_INFO > 1, and so forth.
6	RWX	INSTR0_START. 1 = Start measurement (self-resetting with INSTR0_CYCLECNT_RUNNING = 1).
7	RWX	INSTR0_STOP. 1 = Stop measurement (self-resetting with INSTR0_CYCLECNT_RUNNING = 0).
8:9	RW	INSTR1_MODE: Mode control for instrumentation unit 1: 00: Disabled. 01: PIB mode (default). 10: PCB interrupt mode. 11: Reserved.
10	RW	INSTR1_STOP_TIMER_EN: 0 = Stop measurement manually (default). 1 = Stop measurement based on STOP_TIMER.
11:13	RW	INSTR1_STOP_ON_ERROR_GT: Greater than value for RSP_INFO to stop instrumentation. For example: 000 (default) = Stop sampling with RSP_INFO > 0. 001 = Stop sampling with RSP_INFO > 1, and so forth.
14	RWX	INSTR1_START: 1: Start measurement (self-resetting with INSTR1_CYCLECNT_RUNNING = 1).
15	RWX	INSTR1_STOP: 1: Stop measurement (self-resetting with INSTR1_CYCLECNT_RUNNING = 0).
16:17	RW	INSTR2_MODE: Mode control for instrumentation unit 2: 00: Disabled. 01: PIB mode (default). 10: PCB interrupt mode. 11: Reserved.
18	RW	INSTR2_STOP_TIMER_EN: 0: Stop measurement manually (default). 1: Stop measurement based on STOP_TIMER.
19:21	RW	INSTR2_STOP_ON_ERROR_GT: Greater than value for RSP_INFO to stop instrumentation. For example: 000 (default) = Stop sampling with RSP_INFO > 0. 001 = Stop sampling with RSP_INFO > 1, and so forth.
22	RWX	INSTR2_START: 1: Start measurement (self-resetting with INSTR2_CYCLECNT_RUNNING = 1).
23	RWX	INSTR2_STOP: 1: Stop measurement (self-resetting with INSTR2_CYCLECNT_RUNNING = 0).
24	ROX	INSTR0_CYCLECNT_RUNNING: Instrumentation unit 0: flag for cycle counter running.
25	ROX	INSTR0_BUSYCNT_RUNNING: Instrumentation unit 0: flag for busy counter running.
26	ROX	INSTR1_CYCLECNT_RUNNING: Instrumentation unit 1: flag for cycle counter running.
27	ROX	INSTR1_BUSYCNT_RUNNING: Instrumentation unit 1: flag for busy counter running.
28	ROX	INSTR2_CYCLECNT_RUNNING: Instrumentation unit 2: flag for cycle counter running.
29	ROX	INSTR2_BUSYCNT_RUNNING: Instrumentation unit 2: flag for busy counter running.
30	RWX	INSTR0_STOPPED_ON_ERROR: Indicates that instrumentation unit 0 has stopped because of a RSP_INFO > INSTR0_STOP_ON_ERROR_GT. Resetting this bit after the error condition is gone resumes the measurement.

Bits	SCOM	Field Mnemonic: Description
31	RWX	INSTR1_STOPPED_ON_ERROR: Indicates that instrumentation unit 1 has stopped because of a RSP_INFO > INSTR1_STOP_ON_ERROR_GT. Resetting this bit after the error condition is gone resumes the measurement.
32	RWX	INSTR2_STOPPED_ON_ERROR: Indicates that instrumentation unit 1 has stopped because of a RSP_INFO > INSTR1_STOP_ON_ERROR_GT. Resetting this bit after the error condition is gone resumes the measurement.
33	RWX	INSTR0_RESET: 1 = Clear all measurement registers and resets measurement control of instrumentation unit 0. This bit is self-resetting.
34	RWX	INSTR1_RESET: 1 = Clear all measurement registers and resets measurement control of instrumentation unit 1. This bit is self-resetting.
35	RWX	INSTR2_RESET: 1 = Clear all measurement registers and resets measurement control of instrumentation unit 2. This bit is self-resetting.
36	RW	INSTR_INCLUDE_PSU_TRAFFIC: Controls if the PIB traffic from/to the PIB slave address of the PSU is included in measurement. 0 = Do not measure PSU traffic (default). 1 = Include PSU traffic.
37:39	RW	INSTR_CTRL_STATUS_REG_RESERVED: reserved.

Register Name	Instrumentation Stop Timer Register 0
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR0_STOP_TIMER_REG
Address	00000000000D0020 (SCOM)
Description	Instrumentation Stop Timer Register 0

Bits	SCOM	Field Mnemonic: Description
0:39	RW	INSTR0_STOP_TIMER: 40 bit threshold value for instrumentation unit 0 (in # of PIB cycles).

Register Name	Instrumentation Filter Register 0
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR0_FILTER_REG
Address	00000000000D0021 (SCOM)
Description	Instrumentation Filter Register 0

Bits	SCOM	Field Mnemonic: Description
0:31	RW	INSTR0_FILTER_CONTENT: Compare data for instrumentation unit 0.
32:63	RW	INSTR0_FILTER_MASK: Compare mask for instrumentation unit 0.

Register Name	Instrumentation Cycle Count Register 0
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR0_CYCLECNT_REG
Address	00000000000D0022 (SCOM)
Description	Instrumentation Cycle Count Register 0

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR0_CYCLECNT: Measured cycle count of instrumentation unit 0.

Register Name	Instrumentation Active Cycle Count Register 0
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR0_ACTCYCLECNT_REG
Address	00000000000D0023 (SCOM)
Description	Instrumentation Active Cycle Count Register 0

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR0_ACTCYCLECNT: Measured active cycle count of instrumentation unit 0.

Register Name	Instrumentation Event Count Register 0
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR0_EVENTCNT_REG
Address	00000000000D0024 (SCOM)
Description	Instrumentation Event Count Register 0

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	INSTR0_EVENTCNT: Measured event count of instrumentation unit 0. (Number of PIB accesses or number of PCB interrupts).

Register Name	Max Cycle Count Register 0
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR0_MAXCYCLECNT_REG
Address	00000000000D0025 (SCOM)
Description	Max Cycle Count Register 0

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR0_MAXCYCLECNT: Maximum active cycle count of instrumentation unit 0.

Register Name	Min Cycle Count Register 0
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR0_MINCYCLECNT_REG
Address	00000000000D0026 (SCOM)
Description	Min Cycle Count Register 0

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR0_MINCYCLECNT: Minimum active cycle count of instrumentation unit 0. Initial value is xFFFFFFFFFF.

Register Name	Instrumentation Stop Timer Register 1
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR1_STOP_TIMER_REG
Address	00000000000D0030 (SCOM)
Description	Instrumentation Stop Timer Register 1

Bits	SCOM	Field Mnemonic: Description
0:39	RW	INSTR1_STOP_TIMER: 40 bit threshold value for instrumentation unit 0 (in the number of PIB cycles).

Register Name	Instrumentation Filter Register 1
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR1_FILTER_REG
Address	00000000000D0031 (SCOM)
Description	Instrumentation Filter Register 1

Bits	SCOM	Field Mnemonic: Description
0:31	RW	INSTR1_FILTER_CONTENT: Compare data for instrumentation unit 1.
32:63	RW	INSTR1_FILTER_MASK: Compare mask for instrumentation unit 1.

Register Name	Instrumentation Cycle Count Register 1
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR1_CYCLECNT_REG
Address	00000000000D0032 (SCOM)
Description	Instrumentation Cycle Count Register 1

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR1_CYCLECNT: Measured cycle count of instrumentation unit 1.

Register Name	Instrumentation Active Cycle Count Register 1
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR1_ACTCYCLECNT_REG
Address	00000000000D0033 (SCOM)
Description	Instrumentation Active Cycle Count Register 1

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR1_ACTCYCLECNT: Measured active cycle count of instrumentation unit 1.

Register Name	Instrumentation Event Count Register 1
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR1_EVENTCNT_REG
Address	00000000000D0034 (SCOM)
Description	Instrumentation Event Count Register 1

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	INSTR1_EVENTCNT: Measured event count of instrumentation unit 1. (Number of PIB accesses or number of PCB interrupts).

Register Name	Max Cycle Count Register 1
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR1_MAXCYCLECNT_REG
Address	00000000000D0035 (SCOM)
Description	Max Cycle Count Register 1

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR1_MAXCYCLECNT: Maximum active cycle count of instrumentation unit 1.

Register Name	Min Cycle Count Register 1
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR1_MINCYCLECNT_REG
Address	00000000000D0036 (SCOM)
Description	Min Cycle Count Register 1

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR1_MINCYCLECNT: Minimum active cycle count of instrumentation unit 1. Initial value: xFFFFFFFFFF.

Register Name	Instrumentation Stop Timer Register 2
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR2_STOP_TIMER_REG
Address	00000000000D0040 (SCOM)
Description	Instrumentation Stop Timer Register 2

Bits	SCOM	Field Mnemonic: Description
0:39	RW	INSTR2_STOP_TIMER: 40-bit threshold value for instrumentation unit 0 (in number of PIB cycles).

Register Name	Instrumentation Filter Register 2
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR2_FILTER_REG
Address	00000000000D0041 (SCOM)
Description	Instrumentation Filter Register 2

Bits	SCOM	Field Mnemonic: Description
0:31	RW	INSTR2_FILTER_CONTENT: Compare data for instrumentation unit 2.
32:63	RW	INSTR2_FILTER_MASK: Compare mask for instrumentation unit 2.

Register Name	Instrumentation Cycle Count Register 2
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR2_CYCLECNT_REG
Address	00000000000D0042 (SCOM)
Description	Instrumentation Cycle Count Register 2

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR2_CYCLECNT: Measured cycle count of instrumentation unit 2.

Register Name	Instrumentation Active Cycle Count Register 2
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR2_ACTCYCLECNT_REG
Address	00000000000D0043 (SCOM)
Description	Instrumentation Active Cycle Count Register 2

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR2_ACTCYCLECNT: Measured active cycle count of instrumentation unit 2.

Register Name	Instrumentation Event Count Register 2
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR2_EVENTCNT_REG
Address	00000000000D0044 (SCOM)
Description	Instrumentation Event Count Register 2

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	INSTR2_EVENTCNT: Measured event count of instrumentation unit 2. (# of PIB accesses or # of PCB interrupts).

Register Name	Max Cycle Count Register 2
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR2_MAXCYCLECNT_REG
Address	00000000000D0045 (SCOM)
Description	Max Cycle Count Register 2

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR2_MAXCYCLECNT: Maximum active cycle count of instrumentation unit 2.

Register Name	Min Cycle Count Register 2
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_INSTR2_MINCYCLECNT_REG
Address	00000000000D0046 (SCOM)
Description	Min Cycle Count Register 2

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	INSTR2_MINCYCLECNT: Minimum active cycle count of instrumentation unit 2. Initial value: xFFFFFFFFFF.

Register Name	Host/SBE Mailbox 0 Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_HOST_SBE_MBOX0_REG
Address	00000000000D0050 (SCOM)
Description	Host/SBE Mailbox 0 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	HOST_SBE_MBOX0: Mailbox Register for Host-SBE communication.

Register Name	Host/SBE Mailbox 1 Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_HOST_SBE_MBOX1_REG
Address	00000000000D0051 (SCOM)
Description	Host/SBE Mailbox 1 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	HOST_SBE_MBOX1: Mailbox Register for Host-SBE communication.

Register Name	Host/SBE Mailbox 2 Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_HOST_SBE_MBOX2_REG
Address	00000000000D0052 (SCOM)
Description	Host/SBE Mailbox 2 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	HOST_SBE_MBOX2: Mailbox Register for Host-SBE communication.

Register Name	Host/SBE Mailbox 3 Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_HOST_SBE_MBOX3_REG
Address	00000000000D0053 (SCOM)
Description	Host/SBE Mailbox 3 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	HOST_SBE_MBOX3: Mailbox Register for Host-SBE communication.

Register Name	Host/SBE Mailbox 4 Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_HOST_SBE_MBOX4_REG
Address	00000000000D0054 (SCOM)
Description	Host/SBE Mailbox 4 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	HOST_SBE_MBOX4: Mailbox Register for Host-SBE communication.

Register Name	Host/SBE Mailbox 5 Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_HOST_SBE_MBOX5_REG
Address	00000000000D0055 (SCOM)
Description	Host/SBE Mailbox 5 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	HOST_SBE_MBOX5: Mailbox Register for Host-SBE communication.

Register Name	Host/SBE Mailbox 6 Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_HOST_SBE_MBOX6_REG
Address	00000000000D0056 (SCOM)
Description	Host/SBE Mailbox 6 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	HOST_SBE_MBOX6: Mailbox Register for Host-SBE communication.

Register Name	Host/SBE Mailbox 7 Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_HOST_SBE_MBOX7_REG
Address	00000000000D0057 (SCOM)
Description	Host/SBE Mailbox 7 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	HOST_SBE_MBOX7: Mailbox Register for Host-SBE communication.

Register Name	SBE Doorbell Register
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_SBE_DOORBELL_REG
Address	00000000000D0060 (SCOM) 00000000000D0061 (SCOM1) 00000000000D0062 (SCOM2)
Description	SBE Doorbell Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	SBE_DOORBELL_0: Doorbell Register bit to trigger SBE interrupt psu_sbe_interrupt_msg_available. Set by host firmware to inform the SBE about a waiting message in the Host/SBE Mailbox Registers. PSU_SBE_INTERRUPT_MSG_AVAILABLE is set if one of the 16 doorbell bits is set.
1	RW	WO_AND	WO_OR	SBE_DOORBELL_1:
2	RW	WO_AND	WO_OR	SBE_DOORBELL_2:
3	RW	WO_AND	WO_OR	SBE_DOORBELL_3:
4	RW	WO_AND	WO_OR	SBE_DOORBELL_4:
5	RW	WO_AND	WO_OR	SBE_DOORBELL_5:
6	RW	WO_AND	WO_OR	SBE_DOORBELL_6:
7	RW	WO_AND	WO_OR	SBE_DOORBELL_7:
8	RW	WO_AND	WO_OR	SBE_DOORBELL_8:
9	RW	WO_AND	WO_OR	SBE_DOORBELL_9:
10	RW	WO_AND	WO_OR	SBE_DOORBELL_10:

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
11	RW	WO_AND	WO_OR	SBE_DOORBELL_11:
12	RW	WO_AND	WO_OR	SBE_DOORBELL_12:
13	RW	WO_AND	WO_OR	SBE_DOORBELL_13:
14	RW	WO_AND	WO_OR	SBE_DOORBELL_14:
15	RW	WO_AND	WO_OR	SBE_DOORBELL_15:

Register Name	**Host Doorbell Register**
Mnemonic	TP.TPCHIP.PIB.PSU.PSU_HOST_DOORBELL_REG
Address	00000000000D0063 (SCOM) 00000000000D0064 (SCOM1) 00000000000D0065 (SCOM2)
Description	Host Doorbell Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	HOST_DOORBELL_0: Doorbell Register to trigger Host Bridge interrupt TPPSU_TPBR_INTERRUPT_MSG_AVAILABLE. Set by the SBE to inform host firmware about a response message in the Host/SBE Mailbox Registers. TPPSU_TPBR_INTERRUPT_MSG_AVAILABLE is set if one of the 4 doorbell bits is set.
1	RW	WO_AND	WO_OR	HOST_DOORBELL_1:
2	RW	WO_AND	WO_OR	HOST_DOORBELL_2:
3	RW	WO_AND	WO_OR	HOST_DOORBELL_3:
4	RW	WO_AND	WO_OR	HOST_DOORBELL_4:
5	RW	WO_AND	WO_OR	HOST_DOORBELL_5:
6	RW	WO_AND	WO_OR	HOST_DOORBELL_6:
7	RW	WO_AND	WO_OR	HOST_DOORBELL_7:
8	RW	WO_AND	WO_OR	HOST_DOORBELL_8:
9	RW	WO_AND	WO_OR	HOST_DOORBELL_9:
10	RW	WO_AND	WO_OR	HOST_DOORBELL_10:
11	RW	WO_AND	WO_OR	HOST_DOORBELL_11:
12	RW	WO_AND	WO_OR	HOST_DOORBELL_12:
13	RW	WO_AND	WO_OR	HOST_DOORBELL_13:
14	RW	WO_AND	WO_OR	HOST_DOORBELL_14:
15	RW	WO_AND	WO_OR	HOST_DOORBELL_15:

Register Name	**PPE External Interface XCR**
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.SBEPPE.PPE.PPE_XIXCR
Address	00000000000E0000 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt0
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface RAMRA
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.SBEPPE.PPE.PPE_XIRAMRA
Address	00000000000E0001 (SCOM)
Description	PPE External Interface RAMRA

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register CMD Command 000 = Clear Debug Status 001 = Halt 010 = Resume 011 = Single-step 100 = Toggle XSR[TRH] 101 = Soft Reset 110 = Hard Reset 111 = Force Halt0
4:31	RO	constant = 0b00000000000000000000000000000000
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMGA
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.SBEPPE.PPE.PPE_XIRAMGA
Address	00000000000E0002 (SCOM)
Description	PPE External Interface RAMGA

Bits	SCOM	Field Mnemonic: Description
0:31	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMDBG
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.SBEPPE.PPE.PPE_XIRAMDBG
Address	00000000000E0003 (SCOM)
Description	PPE External Interface RAMDBG

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).

Register Name	PPE External Interface RAMEDR
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.SBEPPE.PPE.PPE_XIRAMEDR
Address	00000000000E0004 (SCOM)
Description	PPE External Interface RAMEDR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value is used by the PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can be written only as an XIR when the processor is halted (XSR[HS] = ‘1’).
32:63	ROX	PPE_XIRAMEDR_EDR: Error Data Register. Set on PPE interrupts that are caused by an error. See the PPE Specification for a definition.

Register Name	PPE External Interface DBGPRO
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.SBEPPE.PPE.PPE_XIDBGPRO
Address	00000000000E0005 (SCOM)
Description	PPE External Interface DBGPRO

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:61	RWX	Reserved field.
62:63	RO	constant = 0b00

Register Name	MIB External Interface SIB Information
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.MIB_XISIB
Address	00000000000E0006 (SCOM)
Description	MIB External Interface SIB Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XISIB_PIB_ADDR: PIB transaction buffer current or previous transaction byte address.
32	ROX	MIB_XISIB_PIB_R_NW: PIB transaction buffer current or previous transaction type, read if ‘1’ and write if ‘0’.
33	ROX	MIB_XISIB_PIB_BUSY: Indicates if the transaction buffer is occupied with an ongoing transaction. Busy is cleared when the transaction is completed.

Bits	SCOM	Field Mnemonic: Description
34	ROX	MIB_XISIB_PIB_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. Cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the PIB interface can continue to service I-fetches (only in case of SBE instance).
35:48	RO	constant = 0b00000000000000
49:51	ROX	MIB_XISIB_PIB_RSP_INFO: PIB transaction buffer response information. Current or previous transaction got an error on the PIB interface when nonzero.
52:61	RO	constant = 0b0000000000
62	ROX	MIB_XISIB_PIB_IFETCH_PENDING: When set to '1', indicates that an instruction fetch is pending on the PIB interface.
63	ROX	MIB_XISIB_PIB_DATAOP_PENDING: Indicates a data transaction is pending on the PIB interface when set to '1'.

Register Name	MIB External Interface MEM Information
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.SBEPPE.MIB.MIB_XIMEM
Address	00000000000E0007 (SCOM)
Description	MIB External Interface MEM Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XIMEM_MEM_ADDR: MEM transaction buffer: current or previous transaction byte address.
32	ROX	MIB_XIMEM_MEM_R_NW: MEM transaction buffer: current or previous transaction type. 0 = Write 1 = Read
33	ROX	MIB_XIMEM_MEM_BUSY: Indicates if the transaction buffer is occupied with an ongoing transaction. Busy is cleared when the transaction is completed.
34	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. Cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
35:42	ROX	MIB_XIMEM_MEM_BYTE_ENABLE: MEM transaction buffer: current or previous transaction byte enables.
43	ROX	MIB_XIMEM_MEM_LINE_MODE: MEM transaction buffer: current or previous transaction line mode. Indicates a 32 B read request when set to '1'.
44:48	RO	constant = 0b00000
49:51	ROX	MIB_XIMEM_MEM_ERROR: MEM transaction buffer error code. A current or previous transaction received an error on the memory interface when nonzero.
52:61	RO	constant = 0b0000000000
62	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to '1', indicates that an instruction fetch is pending on the MEM interface.
63	ROX	MIB_XIMEM_MEM_DATAOP_PENDING: When set to '1', indicates that a data transaction is pending on the MEM interface.

Register Name	MIB External Interface Store Gather Buffer Information
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.SBEPPE.MIB.MIB_XISGB
Address	00000000000E0008 (SCOM)
Description	MIB External Interface Store Gather Buffer Information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XISGB_STORE_ADDRESS: Contains either the SGB address 4-byte tag or the address of an imprecise store error that occurred when a previous data transaction was done.
32:34	RO	constant = 0b000
35	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. Cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
36:39	ROX	MIB_XISGB_SGB_BYTE_VALID: Byte valid bits within the 4 B tag. Cleared when the SGB contents are committed, that is, when the SGB contents are either flushed to memory or copied into the transaction buffer. **Note:** These bits can never be set if a MEM IMPRECISE ERROR is pending.
40:62	RO	constant = 0b00000000000000000000000
63	ROX	MIB_XISGB_SGB_FLUSH_PENDING: When set to ‘1’, indicates that a store gather buffer flush to memory is pending on the MEM interface. This can happen only if MEM_BUSY in the MEM transaction buffer is ‘0’.

Register Name	MIB External Interface I-cache Information
Mnemonic	TP.TPCHIP.PIB.SBE.SBEPM.SBEPPE.MIB.MIB_XIICAC
Address	00000000000E0009 (SCOM)
Description	MIB External Interface I-cache Information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:31	RO	constant = 0b00000
32	ROX	Reserved field.
33	RO	constant = 0b0
34	ROX	MIB_XISIB_PIB_IFETCH_PENDING: When set to ‘1’, indicates that an instruction fetch is pending on the PIB interface.
35	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to ‘1’, indicates that an instruction fetch is pending on the MEM interface.
36:39	ROX	Reserved field.
40:43	ROX	Reserved field.
44	RO	constant = 0b0
45	ROX	Reserved field.
46	ROX	Reserved field.
47	ROX	Reserved field.
48:63	RO	constant = 0b0000000000000000

Register Name	Chiplet Control Register 0
Mnemonic	TP.TPCHIP.TPC.CPLT_CTRL0
Address	0000000001000000 (SCOM) 0000000001000010 (SCOM1) 0000000001000020 (SCOM2)
Description	VITL CCFG

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select ABIST clock source for Arrays on Chiplet Boundary. When set to 1, clocks where used from the chiplet with the ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the sync clock for asynchronous asynclatches (initial value 1).
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent plats from going into flush mode (initial value 1).
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force align signal to be sent (initial value 1, drop before dropping FLUSHMODE_INH).
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set array into write-through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: AVP Mode. Switches refresh pulse to phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC:
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC:
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode for example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of N1L latches. Prevent LCK when switching SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC:
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO Select.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: Initial mode for BSC.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: REFCLOCK driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Allows to delay the align by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the align and odd/even toggling latch into flush state. Used for DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock Divider Select 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1.
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM Program Mode.
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE= 1 only. Sensors Calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. LBIST is controlled by pin, not by OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	Chiplet Control Register 1
Mnemonic	TP.TPCHIP.TPC.CPLT_CTRL1
Address	0000000001000001 (SCOM) 0000000001000011 (SCOM1) 0000000001000021 (SCOM2)
Description	VITL CCFG

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL Fence. Protect bleeding into VITL during LBIST or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for perv region.
5	RW	WO_OR	WO_CLEAR	UNUSED_5B: Unused.
6	RW	WO_OR	WO_CLEAR	UNUSED_6B: Unused.
7	RW	WO_OR	WO_CLEAR	TC_REGION3_FENCE: Fence for region OCC.
8	RW	WO_OR	WO_CLEAR	UNUSED_8B: Unused.
9	RW	WO_OR	WO_CLEAR	UNUSED_9B: Unused.
10	RW	WO_OR	WO_CLEAR	UNUSED_10B: Unused.
11	RW	WO_OR	WO_CLEAR	UNUSED_11B: Unused.
12	RW	WO_OR	WO_CLEAR	UNUSED_12B: Unused.
13	RW	WO_OR	WO_CLEAR	UNUSED_13B: Unused.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.
15	RW	WO_OR	WO_CLEAR	RESERVED: reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE:
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	TC_PERV_EXPORT_FREEZE:
21	RW	WO_OR	WO_CLEAR	UNUSED_21B: Unused.
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	Chiplet Configuration Register 0
Mnemonic	TP.TPCHIP.TPC.CPLT_CONF0
Address	0000000001000008 (SCOM) 0000000001000018 (SCOM1) 0000000001000028 (SCOM2)
Description	VITL FUNC

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 select. See the Probe Specification for more details.
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 select. See the Probe Specification for more details.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 select. See the Probe Specification for more details.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3 select. See the Probe Specification for more details.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: ABIST Overflow/Fail Ever Happen Select.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: For Scan Diagnostic to disable scan path.
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from CC or CPLT_CTRL.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in CC, which are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: SYS ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	Chiplet Configuration Register 1
Mnemonic	TP.TPCHIP.TPC.CPLT_CONF1
Address	0000000001000009 (SCOM) 0000000001000019 (SCOM1) 0000000001000029 (SCOM2)
Description	VITL FUNC

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RW	WO_OR	WO_CLEAR	TCPERV_AMUX_VSELECT_CHIP: AMUX CTRL.
4	RW	WO_OR	WO_CLEAR	IOVALID_4D:
5	RW	WO_OR	WO_CLEAR	IOVALID_5D:
6	RW	WO_OR	WO_CLEAR	IOVALID_6D:
7	RW	WO_OR	WO_CLEAR	IOVALID_7D:
8	RW	WO_OR	WO_CLEAR	IOVALID_8D:
9	RW	WO_OR	WO_CLEAR	IOVALID_9D:
10	RW	WO_OR	WO_CLEAR	IOVALID_10D:
11	RW	WO_OR	WO_CLEAR	IOVALID_11D:
12:13	RW	WO_OR	WO_CLEAR	TP_IO_SPI_APSS_MCPRECOMP:
14:15	RW	WO_OR	WO_CLEAR	TP_IO_SPARE2_MCPRECOMP:
16:17	RW	WO_OR	WO_CLEAR	TP_IO_SPARE3_MCPRECOMP:
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	Chiplet Status Register
Mnemonic	TP.TPCHIP.TPC.CPLT_STAT0
Address	0000000001000100 (SCOM)
Description	Interrupt send out on bit change if not masked by the Chiplet Mask Register. Only masks the interrupt, not the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM,EDRAM, ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic out port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic out port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: PLL destout.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done. For LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that the chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	FREE_USAGE_12E: Free usage.
13	ROX	FREE_USAGE_13E: Free usage.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.
16	ROX	FREE_USAGE_16E: Free usage.
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	Chiplet Mask Register
Mnemonic	TP.TPCHIP.TPC.CPLT_MASK0
Address	0000000001000101 (SCOM)
Description	Masking the interrupt on a bitchange of the Chiplet Status Register. Does not mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: Masking bit-wise of the Chiplet Status Register.

Register Name	CTRL Protect Mode Register
Mnemonic	TP.TPCHIP.TPC.CTRL_PROTECT_MODE_REG
Address	00000000010003FE (SCOM)
Description	CTRL Protect Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.TPC.CTRL_ATOMIC_LOCK_REG
Address	00000000010003FF (SCOM)
Description	Atomic Lock Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	PSCOMLE mode register
Mnemonic	TP.TPCHIP.TPC.EPS.PSC.PSCOM_MODE_REG
Address	0000000001010000 (SCOM)
Description	PSCOMLE mode register

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on PCB WDATA parity error.
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: Abort on DL return P0 error.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on DL return WDATA parity error.
4	RW	WATCHDOG_ENABLE: WATCHDOG_ENABLE.
5:6	RW	SCOM_HANG_LIMIT: 0b11 = 256 0b10 = 512 0b01 = 768 0b00 = 1023
7	RW	FORCE_ALL_RINGS: Set to logic 1 if all rings should be enabled independent of ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE:
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE error register
Mnemonic	TP.TPCHIP.TPC.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000001010001 (SCOM)
Description	PSCOMLE Error Register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB WDATA parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return WDATA parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL RDATA parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on the interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on P2S machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel ADDR_INVALID.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB WDATA parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return WDATA parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL RDATA parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on the P2S machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.

Bits	SCOM	Field Mnemonic: Description
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel ADDR invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	**PSCOMLE error mask register**
Mnemonic	TP.TPCHIP.TPC.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	0000000001010002 (SCOM)
Description	PSCOMLE Error Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB WDATA parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return WDATA parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL RDATA parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on P2S machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting for ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel ADDR invalid.
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	**PSCOMLE Address Trap Register**
Mnemonic	TP.TPCHIP.TPC.EPS.PSC.PSC.ADDR_TRAP_REG
Address	0000000001010003 (SCOM)
Description	PSCOMLE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: PCB address of last transaction with error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read-not-write of the last transaction with error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: Reserved 0.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2Parallel state machine at time of error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit: Set to 1 if no parity error detected of satellite number and acknowledge bits.
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: Set if write parity error detected by satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: Set if invalid read or write access detected by satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: Set if invalid register address detected by satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TPCHIP.TPC.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	0000000001010005 (SCOM)
Description	Ring Lock Enable Register

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon write to specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	Write Protect Rings Register
Mnemonic	TP.TPCHIP.TPC.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	0000000001010006 (SCOM)
Description	WRITE PROTECT RINGS Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Write protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TPCHIP.TPC.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	0000000001010007 (SCOM)
Description	Atomic Lock Mask Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: Bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TPCHIP.TPC.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	0000000001010008 (SCOM)
Description	Ring Fence Enable Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: bit mask for ring fencing on a ring-by-ring basis.

Register Name	Trace Array High Data Register
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000001010400 (SCOM)
Description	Trace Array High Data Register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000001010401 (SCOM)
Description	Trace Array Low Data Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace Address.
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator.
53	ROX	TRACE_RUNNING: Trace Run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000001010402 (SCOM)
Description	Trace Control Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when TRACE_RUN.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.

Bits	SCOM	Field Mnemonic: Description
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12:13	RW	LOCAL_CLOCK_GATE_CONTROL: Local clock gate control selection and overwrite.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers: TRA_MUX0_SEL[0:1] and TRA_MUX1_SEL[0:1].
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	TRDATA Configuration Register 0
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000001010403 (SCOM)
Description	TRDATA Configuration Register 0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0:63.

Register Name	TRDATA Configuration Register 1
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000001010404 (SCOM)
Description	TRDATA Configuration Register 1

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64:87.

Register Name	TRDATA Configuration Register 2
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000001010405 (SCOM)
Description	TRDATA Configuration Register 2

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	TRDATA Configuration Register 3
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000001010406 (SCOM)
Description	TRDATA Configuration Register 3

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: pattern_match_patc_0_to_23.

Bits	SCOM	Field Mnemonic: Description
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	TRDATA Configuration Register 4
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000001010407 (SCOM)
Description	TRDATA Configuration Register 4

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	TRDATA Configuration Register 5
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000001010408 (SCOM)
Description	TRDATA Configuration Register 5

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	TRDATA Configuration Register 9
Mnemonic	TP.TPCHIP.TPC.TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000001010409 (SCOM)
Description	TRDATA Configuration Register 9

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable Trace Data Compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account (care about) changes in the Error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeros
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeros
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeros

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: **Note:** The OR of all selected matches is ORed with result of TRIG0_AND. 0B1XXX = Selects MATCHA OR 0bX1XX = Selects MATCHB OR 0bXX1X = Selects MATCHC OR 0bXXX1 = Selects MATCHD OR 0b0000 = Selects to not OR any matches
14:17	RW	TRIG0_AND_MASK: **Note:** The AND of following selected matches is ORed with result of TRIG0_OR. 0b1XXX = Selects MATCHA AND 0bX1XX = Selects MATCHB AND 0bXX1X = Selects MATCHC AND 0bXXX1 = Selects MATCHD AND 0b0000 = Selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: **Note:** The OR of all selected MATCHes is ORed with result of TRIG1_AND. 0b1XXX = Selects MATCHA OR 0bX1XX = Selects MATCHB OR 0bXX1X = Selects MATCHC OR 0bXXX1 = Selects MATCHD OR 0b0000 = Selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: **Note:** The AND of following selected MATCHes is ORed with result of TRIG1_OR. 0b1XXX = Selects MATCHA AND 0bX1XX = Selects MATCHB AND 0bXX1X = Selects MATCHC AND 0bXXX1 = Selects MATCHD AND 0b0000 = Selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0b1000 inverts MATCHA 0b0100 inverts MATCHB 0b0010 inverts MATCHC 0b0001 inverts MATCHD
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_HI_DATA_REG
Address	0000000001010440 (SCOM)
Description	Trace Array High Data Register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_LO_DATA_REG
Address	0000000001010441 (SCOM)
Description	Trace Array Low Data Register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace Address.
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator.
53	ROX	TRACE_RUNNING: Trace Run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRCTRL_CONFIG
Address	0000000001010442 (SCOM)
Description	Trace control configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace_run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12:13	RW	LOCAL_CLOCK_GATE_CONTROL: Local clock gate control selection and overwrite.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers. tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	TRDATA Configuration Register 0
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000001010443 (SCOM)
Description	TRDATA Configuration Register 0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0:63.

Register Name	TRDATA Configuration Register 1
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000001010444 (SCOM)
Description	TRDATA Configuration Register 1

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64:87.

Register Name	TRDATA Configuration Register 2
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000001010445 (SCOM)
Description	TRDATA Configuration Register 2

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	TRDATA Configuration Register 3
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000001010446 (SCOM)
Description	TRDATA Configuration Register 3

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: pattern_match_patc_0_to_23.
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	TRDATA Configuration Register 4
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000001010447 (SCOM)
Description	TRDATA Configuration Register 4

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	TRDATA Configuration Register 5
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000001010448 (SCOM)
Description	TRDATA Configuration Register 5

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	TRDATA Configuration Register 9
Mnemonic	TP.TPCHIP.TPC.TRA0.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000001010449 (SCOM)
Description	TRDATA Configuration Register 9

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable Trace Data Compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account (care about) changes in the Error bit for trace data compression (Default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: **Note:** The OR of all selected MATCHes is ORed with result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: **Note:** The AND of following selected MATCHes is ORed with result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: **Note:** The OR of all selected MATCHes is ORed with result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.

Bits	SCOM	Field Mnemonic: Description
22:25	RW	TRIG1_AND_MASK: **Note:** The AND of following selected MATCHes is ORed with result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Debug Macro Configuration Register 0 for Configuration Component
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_MODE_REG
Address	00000000010107C0 (SCOM)
Description	Debug macro configuration register 0 for configuration component

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: global_broadcast_mode (0:2): 100 = dbg_trace_run and dbg_trace_freeze. 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze. 110 = dbg_triggers_out(0:1). 111 = pc_tcdbg_triggers(0:1) (from core).
3:5	RW	TRACE_SEL_MODE: Select source for trace_run and bank. 001 = Core trace run and bank. 010 = TP broadcast run & 0. 011 = tc_dbg_inter_brcst latched. 100 = tc_dbg_dbg_sync_brcst_rcv. else: dbg_trace_run & dbg_trace_bank.
6:7	RW	TRIG_SEL_MODE: Select source for tcdbg_trigger(0). 10 = global broadcast. 11 = pc_tcdbg_trigger (from core). else: dbg_triggers_out(0:1).
8	RW	STOP_ON_XSTOP_SELECTION: Enable trace stop on checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: Enable trace stop on recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: Enable trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select freeze source: 0 = Local debug freeze. 1 = By broadcast: tp_tcdbg_glb_brcst(1).
12:13	RW	SYNC_BRCST_MODE: Unused, obsolete. See trace_sel_mode.
14	RO	constant = 0b0 sync_brcst_mode.
15	RO	constant = 0b0
16:31	ROX	dbg_status

Bits	SCOM	Field Mnemonic: Description
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Debug Macro Configuration Register 1 for Front End 1 Component
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000010107C1 (SCOM)
Description	Debug macro configuration register 1 for front end 1 component

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = Select constant 0 001 = Select constant 1 -- CONDITION FEEDBACK -- 002 = Select inst1_dbg_cond1. 003 = Select inst1_dbg_cond2. 004 = Select inst1_dbg_cond3. 005 = Select inst1_dbg_cond2timeout. 006 = Select inst2_dbg_cond1. 007 = Select inst2_dbg_cond2. 008 = Select inst2_dbg_cond3. 009 = Select inst2_dbg_cond2timeout. 010 = Select inst3_dbg_cond1 - unused, tied down. 011 = Select inst3_dbg_cond2 - unused, tied down. 012 = Select inst3_dbg_cond3 - unused, tied down. 013 = Select inst3_dbg_cond2timeout - unused, tied down. 014 = Select inst4_dbg_cond1 - unused, tied down. 015 = Select inst4_dbg_cond2 - unused, tied down. 016 = Select inst4_dbg_cond3 - unused, tied down. 017 = Select inst4_dbg_cond2timeout - unused, tied down. 018 = Select inst1_dbg_trig_sp. 019 = Select inst2_dbg_trig_sp. 020 = Select inst3_dbg_trig_sp - unused, tied down. 021 = Select inst4_dbg_trig_sp - unused, tied down. 022 = Select tctrc_tcdbg_trigger_a(0). 023 = Select tctrc_tcdbg_trigger_b(0). 024 = Select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = Select tctrc_tcdbg_trigger_a(1). 026 = Select tctrc_tcdbg_trigger_b(1). 027 = Select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = Select tctrc_tcdbg_trigger_a(2). 029 = Select tctrc_tcdbg_trigger_b(2). 030 = Select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = Select tctrc_tcdbg_trigger_a(3). 032 = Select tctrc_tcdbg_trigger_b(3). 033 = Select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = Select tctrc_tcdbg_trigger_a(4). 035 = Select tctrc_tcdbg_trigger_b(4). 036 = Select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 037 = Select tctrc_tcdbg_trigger_a(5). 038 = Select tctrc_tcdbg_trigger_b(5). 039 = Select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 040 = Select tctrc_tcdbg_trigger_a(6). 041 = Select tctrc_tcdbg_trigger_b(6). 042 = Select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 043 = Select tctrc_tcdbg_trigger_a(7). 044 = Select tctrc_tcdbg_trigger_b(7). 045 = Select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7).

Bits	SCOM	Field Mnemonic: Description
		046 = Select tctrc_tcdbg_trigger_a(8). 047 = Select tctrc_tcdbg_trigger_b(8). 048 = Select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 049 = Select tctrc_tcdbg_trigger_a(9). 050 = Select tctrc_tcdbg_trigger_b(9). 051 = Select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 052 = Select tctrc_tcdbg_trigger_a(10). 053 = Select tctrc_tcdbg_trigger_b(10). 054 = Select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10). 055 = Select tctrc_tcdbg_trigger_a(11). 056 = Select tctrc_tcdbg_trigger_b(11). 057 = Select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11). 058 = Select tctrc_tcdbg_trigger_a(12). 059 = Select tctrc_tcdbg_trigger_b(12). 060 = Select tctrc_tcdbg_trigger_a(12) and tctrc_tcdbg_trigger_b(12). 061 = Select tctrc_tcdbg_trigger_a(13). 062 = Select tctrc_tcdbg_trigger_b(13). 063 = Select tctrc_tcdbg_trigger_a(13) and tctrc_tcdbg_trigger_b(13). 064 = Select tctrc_tcdbg_trigger_a(14). 065 = Select tctrc_tcdbg_trigger_b(14). 066 = Select tctrc_tcdbg_trigger_a(14) and tctrc_tcdbg_trigger_b(14). 067 = Select tctrc_tcdbg_trigger_a(15). 068 = Select tctrc_tcdbg_trigger_b(15). 069 = Select tctrc_tcdbg_trigger_a(15) and tctrc_tcdbg_trigger_b(15). 070 = Select tctrc_tcdbg_trigger_a(16). 071 = Select tctrc_tcdbg_trigger_b(16). 072 = Select tctrc_tcdbg_trigger_a(16) and tctrc_tcdbg_trigger_b(16). 073 = Select tctrc_tcdbg_trigger_a(17). 074 = Select tctrc_tcdbg_trigger_b(17). 075 = Select tctrc_tcdbg_trigger_a(17) and tctrc_tcdbg_trigger_b(17). Logic (Unit) Trigger EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 076 = Select logic_trigger_in(0). 077 = Select logic_trigger_in(1). 078 = Select logic_trigger_in(2). 079 = Select logic_trigger_in(3). 080 = Select logic_trigger_in(4). 081 = Select logic_trigger_in(5). 082 = Select logic_trigger_in(6). 083 = Select logic_trigger_in(7). 084 = Select logic_trigger_in(8). 085 = Select logic_trigger_in(9). 086 = Select logic_trigger_in(10). 087 = Select logic_trigger_in(11). 088 = Select logic_trigger_in(12). 089 = Select logic_trigger_in(13). 090 = Select logic_trigger_in(14). 091 = Select logic_trigger_in(15). 092 = Select pc_tcdbg_trigger(0). 093 = Select pc_tcdbg_trigger(1). 094 = Select tctrc_tcdbg_glb_brcst(0). 095 = Select tctrc_tcdbg_glb_brcst(1). 096 = Select xstop_err. 097 = Select recov_err. 098 = Select spattn. 099 = Select fir_dbg_local_xstop_err. 100 = Select tc_dbg_inter_brcst(0). 101 = Select tc_dbg_inter_brcst(1). -- CORE TRIGGERS (EP chip only) -- **Note:** Set core_slave_mode to honor ec[0:5]_tc_trace_run.

Bits	SCOM	Field Mnemonic: Description
		102 = Select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0). 103 = Select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1). 104 = Select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0). 105 = Select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1). 106 = Select glb_trig_or_trace_in(0). 107 = Select glb_trig_or_trace_in(1). 108 = Select core_local_brcst_trc(0). 109 = Select core_local_brcst_trc(1). 110 = Select glb_freeze_brcst_rec(0). 111 = Select trig_2_extern_in(0). 112 = Select trig_2_extern_in(1). 113 = Select dbg_triggers_out(2). 114 = Select dbg_triggers_out(3). 115 = Select dbg_triggers_out(4). 116 = Select dbg_triggers_out(5). 117 = Select dbg_triggers_out(6). 118 = Select tcdbg_trigger_in(0). 119 = Select tcdbg_trigger_in(1).
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Front end instance 1 c1_inarow_mode.
33	RW	INST1_AND_TRIGGER_MODE1: Front end instance 1 and trigger mode condition1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front end instance 1 inverted trigger mode condition1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front end instance 1 edge trigger mode condition1.
36:38	RWX	INST1_UNUSED_1: Unused.
39	RW	INST1_C2_INAROW_MODE: Front end instance 1 counter 2 in-a-row mode.
40	RW	INST1_AND_TRIGGER_MODE2: Front end instance 1 and trigger mode2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front end instance 1edge trigger.
43:45	RWX	INST1_UNUSED_2: Unused.
46	RW	INST1_COND3_ENABLE_RESET: Front end instance 1 condition3 enable.
47	RW	INST1_EXACT_TO_MODE: Front end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front end instance 1 reset condition2 timer on condition1.
49	RW	INST1_RESET_C3_ON_C0: Front end instance 1 reset condition3 on condition0.
50	RW	INST1_SLOW_TO_MODE: Front end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front end instance 1 exact reset condition3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: inst1 condition1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: inst1 condition2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front end instance 1: reset condition3 for reset_c3_on_c0. 0b100 = dbg_cross_couple_triggers(4). 0b101 = dbg_cross_couple_triggers(12). 0b110 = dbg_cross_couple_triggers(20). 0b111 = dbg_cross_couple_triggers(28).

Register Name	Debug macro configuration register 2 for front end 1 component
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_INST1_COND_REG_2
Address	00000000010107C2 (SCOM)
Description	Debug macro configuration register 2 for front end 1 component

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same of all selectors: 00000 = Selects inst1_cond1_trig_a. 00001 = Selects inst1_cond1_trig_b. 00010 = Selects inst1_cond2_trig_a. 00011 = Selects inst1_cond2_trig_b. 00100 = Selects inst1_condition1. 00101 = Selects inst1_condition2. 00110 = Selects inst1_condition3. 00111 = Selects inst1_cond2_timeout. 01000 = Selects inst2_cond1_trig_a. 01001 = Selects inst2_cond1_trig_b. 01010 = Selects inst2_cond2_trig_a. 01011 = Selects inst2_cond2_trig_b. 01100 = Selects INST2_CONDITION1. 01101 = Selects INST2_CONDITION2. 01110 = Selects INST2_CONDITION3. 01111 = Selects inst2_cond2_timeout. 10000 = Selects inst3_cond1_trig_a. 10001 = Selects inst3_cond1_trig_b. 10010 = Selects inst3_cond2_trig_a. 10011 = Selects inst3_cond2_trig_b. 10100 = Selects inst3_condition1. 10101 = Selects inst3_condition2. 10110 = Selects inst3_condition3. 10111 = Selects inst3_cond2_timeout. 11000 = Selects inst4_cond1_trig_a. 11001 = Selects inst4_cond1_trig_b. 11010 = Selects inst4_cond2_trig_a. 11011 = Selects inst4_cond2_trig_b. 11100 = Selects inst4_condition1. 11101 = Selects inst4_condition2. 11110 = Selects inst4_condition3. 11111 = Selects inst4_cond2_timeout.
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: inst1_cross_couple_select_1_b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: inst1_cross_couple_select_2_a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: inst1_cross_couple_select_2_b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate to compare without actual compare.

Register Name	Debug Macro Configuration Register 2 for Front End 1 Component
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_INST1_COND_REG_3
Address	00000000010107C3 (SCOM)
Description	Debug macro configuration register 2 for front end 1 component

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter TO_CMP compare value for DBG_COND_COMP_1.

Register Name	**Debug Macro Configuration Register 1 for Front End 1 Component**
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000010107C4 (SCOM)
Description	Debug macro configuration register 1 for front end 1 component

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = Select constant 0 001 = Select constant 1 Condition Feedback 002 = Select inst2_dbg_cond1. 003 = Select inst2_dbg_cond2. 004 = Select inst2_dbg_cond3. 005 = Select inst2_dbg_cond2timeout. 006 = Select inst2_dbg_cond1. 007 = Select inst2_dbg_cond2. 008 = Select inst2_dbg_cond3. 009 = Select inst2_dbg_cond2timeout. 010 = Select inst3_dbg_cond1 - unused, tied down. 011 = Select inst3_dbg_cond2 - unused, tied down. 012 = Select inst3_dbg_cond3 - unused, tied down. 013 = Select inst3_dbg_cond2timeout - unused, tied down. 014 = Select inst4_dbg_cond1 - unused, tied down. 015 = Select inst4_dbg_cond2 - unused, tied down. 016 = Select inst4_dbg_cond3 - unused, tied down. 017 = Select inst4_dbg_cond2timeout - unused, tied down. 018 = Select inst2_dbg_trig_sp. 019 = Select inst2_dbg_trig_sp. 020 = Select inst3_dbg_trig_sp - unused, tied down. 021 = Select inst4_dbg_trig_sp - unused, tied down. 022 = Select tctrc_tcdbg_trigger_a(0). 023 = Select tctrc_tcdbg_trigger_b(0). 024 = Select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = Select tctrc_tcdbg_trigger_a(1). 026 = Select tctrc_tcdbg_trigger_b(1). 027 = Select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = Select tctrc_tcdbg_trigger_a(2). 029 = Select tctrc_tcdbg_trigger_b(2). 030 = Select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = Select tctrc_tcdbg_trigger_a(3). 032 = Select tctrc_tcdbg_trigger_b(3). 033 = Select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = Select tctrc_tcdbg_trigger_a(4). 035 = Select tctrc_tcdbg_trigger_b(4). 026 = Select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 027 = Select tctrc_tcdbg_trigger_a(5). 028 = Select tctrc_tcdbg_trigger_b(5). 029 = Select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 030 = Select tctrc_tcdbg_trigger_a(6). 031 = Select tctrc_tcdbg_trigger_b(6). 032 = Select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 033 = Select tctrc_tcdbg_trigger_a(7). 034 = Select tctrc_tcdbg_trigger_b(7). 035 = Select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 036 = Select tctrc_tcdbg_trigger_a(8). 037 = Select tctrc_tcdbg_trigger_b(8). 038 = Select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8).

Bits	SCOM	Field Mnemonic: Description
		039 = Select tctrc_tcdbg_trigger_a(9). 040 = Select tctrc_tcdbg_trigger_b(9). 041 = Select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 042 = Select xstop_err. 043 = Select recov_err. 044 = Select spattn. 045 = Select fir_dbg_local_xstop_err. 046 = Select tc_dbg_inter_brcst(0). 047 = Select tc_dbg_inter_brcst(1). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 102 = Select logic_trigger_in(0). 103 = Select logic_trigger_in(1). 104 = Select logic_trigger_in(2). 105 = Select logic_trigger_in(3). 106 = Select logic_trigger_in(4). 107 = Select logic_trigger_in(5). 108 = Select logic_trigger_in(6). 109 = Select logic_trigger_in(7). 110 = Select logic_trigger_in(8). 111 = Select logic_trigger_in(9). 112 = Select logic_trigger_in(10). 113 = Select logic_trigger_in(11). 114 = Select logic_trigger_in(12). 115 = Select logic_trigger_in(13). 116 = Select logic_trigger_in(14). 117 = Select logic_trigger_in(15). Core Triggers (EP chip only) Note: Set core_slave_mode to honor ec[0:5]_tc_trace_run. 118 = Select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0). 119 = Select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1). 120 = Select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0). 121 = Select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1). Broadcast/Errors 122 = Select glb_trc_bdcst_recv (received global broadcast). 123 = Select edge detected fir_dbg_xstop_err. 124 = Select edge detected fir_dbg_recov_err. 125 = Select edge detected fir_dbg_spatn. 126 … 127 = Select constant 0 (unused)
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Front end instance 1 c1_inarow_mode.
33	RW	INST2_AND_TRIGGER_MODE1: Front end instance 1 and trigger mode condition1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front end instance 1 inverted trigger mode condition1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front end instance 1 edge trigger mode condition1.
36:38	RWX	INST2_UNUSED_1: Unused.
39	RW	INST2_C2_INAROW_MODE: Front end instance 1 Counter 2 in-a-row mode.
40	RW	INST2_AND_TRIGGER_MODE2: Front end instance 1 and trigger mode2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front end instance 1 inverted (not) trigger.

Bits	SCOM	Field Mnemonic: Description
42	RW	INST2_EDGE_TRIGGER_MODE2: Front end instance 1edge trigger.
43:45	RWX	INST2_UNUSED_2: Unused.
46	RW	INST2_COND3_ENABLE_RESET: Front end instance 1 condition3 enable.
47	RW	INST2_EXACT_TO_MODE: Front end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front end instance 1 reset condition2 timer on condition1.
49	RW	INST2_RESET_C3_ON_C0: Front end instance 1 reset condition3 on condition0.
50	RW	INST2_SLOW_TO_MODE: Front end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front end instance 1 exact reset condition3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: inst2 condition1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: inst2 condition2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front end instance 1: reset condition3 for reset_c3_on_c0. 0b100 = DBG_CROSS_COUPLE_TRIGGERS(4). 0B101 = DBG_CROSS_COUPLE_TRIGGERS(12). 0b110 = DBG_CROSS_COUPLE_TRIGGERS(20). 0b111 = DBG_CROSS_COUPLE_TRIGGERS(28).

Register Name	**Debug Macro Configuration Register 2 for Front End 1 Component**
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000010107C5 (SCOM)
Description	Debug macro configuration register 2 for front end 1 component

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same of all selectors: 00000 = Selects INST2_COND1_TRIG_A. 00001 = Selects INST2_COND1_TRIG_B. 00010 = Selects INST2_COND2_TRIG_A. 00011 = Selects INST2_COND2_TRIG_B. 00100 = Selects INST2_CONDITION1. 00101 = Selects INST2_CONDITION2. 00110 = Selects INST2_CONDITION3. 00111 = Selects INST2_COND2_TIMEOUT. 01000 = Selects INST2_COND1_TRIG_A. 01001 = Selects INST2_COND1_TRIG_B. 01010 = Selects INST2_COND2_TRIG_A. 01011 = Selects INST2_COND2_TRIG_B. 01100 = Selects INST2_CONDITION1. 01101 = Selects INST2_CONDITION2. 01110 = Selects INST2_CONDITION3. 01111 = Selects INST2_COND2_TIMEOUT. 10000 = Selects INST3_COND1_TRIG_A. 10001 = Selects INST3_COND1_TRIG_B. 10010 = Selects INST3_COND2_TRIG_A. 10011 = Selects INST3_COND2_TRIG_B. 10100 = Selects INST3_CONDITION1. 10101 = Selects INST3_CONDITION2. 10110 = Selects INST3_CONDITION3. 10111 = Selects INST3_COND2_TIMEOUT. 11000 = Selects INST4_COND1_TRIG_A. 11001 = Selects INST4_COND1_TRIG_B. 11010 = Selects INST4_COND2_TRIG_A. 11011 = Selects INST4_COND2_TRIG_B. 11100 = Selects INST4_CONDITION1. 11101 = Selects INST4_CONDITION2. 11110 = Selects INST4_CONDITION3. 11111 = Selects INST4_COND2_TIMEOUT.
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: INST2_CROSS_COUPLE_SELECT_1_B.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: INST2_CROSS_COUPLE_SELECT_2_A.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: INST2_CROSS_COUPLE_SELECT_2_B.
20:43	RW	INST2_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Force test mode to indicate to compare without actual compare.

Register Name	Debug Macro Configuration Register 2 for Front End 1 Component
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_INST2_COND_REG_3
Address	00000000010107C6 (SCOM)
Description	Debug macro configuration register 2 for front end 1 component

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter TO_CMP compare value for DBG_COND_COMP_1.

Register Name	Debug Macro Configuration Register 10 for Debug Backed Component
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_TRACE_REG_0
Address	00000000010107CD (SCOM)
Description	Debug Macro configuration register 10 for debug back-end component

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: Enable of instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: Enable of instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: Enable slow LFSR mode of front end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: Enable slow LFSR mode of front end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: UNUSED.
7	RW	INST4_SLOW_LFSR_MODE: UNUSED.
8:9	RW	INST1_CONDITION1_TRIG_SEL: Select inst1 condition1 for output (external) triggers. 00 = Do nothing. 01 = TRIGGER_OUT(0). 10 = TRIGGER_OUT(1). 11 = TRIGGER_OUT(2).
10:11	RW	INST1_CONDITION2_TRIG_SEL: Select inst1 condition2 for output (external) triggers. 00 = Do nothing. 01 = TRIGGER_OUT(0). 10 = TRIGGER_OUT(1). 11 = TRIGGER_OUT(2).
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: Select inst1 c2 time-out counter for output (external) triggers. 00 = Do nothing. 01 = TRIGGER_OUT(0). 10 = TRIGGER_OUT(1). 11 = TRIGGER_OUT(2).
14:15	RW	INST2_CONDITION1_TRIG_SEL: Select inst2 condition1 for output (external) triggers. 00 = Do nothing. 01 = TRIGGER_OUT(0). 10 = TRIGGER_OUT(1). 11 = TRIGGER_OUT(2).
16:17	RW	INST2_CONDITION2_TRIG_SEL: Select inst2 condition2 trigger for output (external) triggers. 00 = Do nothing. 01 = TRIGGER_OUT(0). 10 = TRIGGER_OUT(1). 11 = TRIGGER_OUT(2).
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: Select inst2 c2 time-out counter for output (external) triggers. 00 = Do nothing. 01 = TRIGGER_OUT(0). 10 = TRIGGER_OUT(1). 11 = TRIGGER_OUT(2).
20:31	RO	constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: enable trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: enable trigger on freeze.
34:38	RW	CORE_RAS0_TRIG_SEL:
39:43	RW	CORE_RAS1_TRIG_SEL:

Bits	SCOM	Field Mnemonic: Description
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(0). **Note:** Some are N/A (INST3/4 conditions are tied to zero). 0001 = INST1_COND3_STATE_INT(1). 0010 = INST1_COND3_STATE_INT(0). 0011 = INST2_COND3_STATE_INT(1). 0100 = INST2_COND3_STATE_INT(0). 0101 = INST3_COND3_STATE_INT(1). 0110 = INST3_COND3_STATE_INT(0). 0111 = INST4_COND3_STATE_INT(1). 1000 = INST4_COND3_STATE_INT(0). 1001 = INST1_COND3_STATE_INT(1) or INST2_COND3_STATE_INT(1). 1010 = INST1_COND3_STATE_INT(1) and INST2_COND3_STATE_INT(1). 1011 = INST3_COND3_STATE_INT(1) OR INST4_COND3_STATE_INT(1). 1100 = INST3_COND3_STATE_INT(1) and INST4_COND3_STATE_INT(1). 1101 = INST1_COND3_STATE_INT(1) OR INST2_COND3_STATE_INT(1) OR INST3_COND3_STATE_INT(1). 1110 = INST1_COND3_STATE_INT(1) and INST2_COND3_STATE_INT(1) and INST3_COND3_STATE_INT(1). 1111 = INST1_COND3_STATE_INT(1) OR INST2_COND3_STATE_INT(1) OR INST3_COND3_STATE_INT(1) OR INST4_COND3_STATE_INT(1).
54:57	RW	TRIG1_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(1). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = INST1_COND3_STATE_INT(1). 0010 = INST1_COND3_STATE_INT(0). 0011 = INST2_COND3_STATE_INT(1). 0100 = INST2_COND3_STATE_INT(0). 0101 = INST3_COND3_STATE_INT(1). 0110 = INST3_COND3_STATE_INT(0). 0111 = INST4_COND3_STATE_INT(1). 1000 = INST4_COND3_STATE_INT(0). 1001 = INST1_COND3_STATE_INT(1) OR INST2_COND3_STATE_INT(1). 1010 = INST1_COND3_STATE_INT(1) AND INST2_COND3_STATE_INT(1). 1011 = INST3_COND3_STATE_INT(1) OR INST4_COND3_STATE_INT(1). 1100 = INST3_COND3_STATE_INT(1) AND INST4_COND3_STATE_INT(1). 1101 = INST1_COND3_STATE_INT(1) OR INST2_COND3_STATE_INT(1) OR INST3_COND3_STATE_INT(1). 1110 = INST1_COND3_STATE_INT(1) AND INST2_COND3_STATE_INT(1) AND INST3_COND3_STATE_INT(1). 1111 = INST1_COND3_STATE_INT(1) OR INST2_COND3_STATE_INT(1) OR INST3_COND3_STATE_INT(1) OR INST4_COND3_STATE_INT(1).
58:63	RO	constant = 0b000000

Register Name	**Debug Macro Configuration Register 11 for Backend Component**
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_TRACE_REG_1
Address	00000000010107CE (SCOM)
Description	Debug macro configuration register 11 for backend component

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Inst1 action selection , condition1: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: start now, stop after n cycles
2:3	RW	INST1_CONDITION2_ACTION_DO: Inst1 action selection , condition2: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: start now, stop after n cycles.
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Inst1 action selection , c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: start now, stop after n cycles
6:7	RW	INST2_CONDITION1_ACTION_DO: inst2 action selection , condition1: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: start now, stop after n cycles
8:9	RW	INST2_CONDITION2_ACTION_DO: Inst2 action selection , condition2: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: start now, stop after n cycles
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Inst2 action selection , c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: start now, stop after n cycles
12:23	RO	constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For wait-N.
25	RW	INST1_CONDITION2_ACTION_WAITN: For wait-N.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For wait-N.

Bits	SCOM	Field Mnemonic: Description
27	RW	INST2_CONDITION1_ACTION_WAITN: For wait-N.
28	RW	INST2_CONDITION2_ACTION_WAITN: For wait-N.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For wait-N.
30:35	RO	constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (inst1, condition1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (inst1, condition2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (inst2, condition1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (inst2, condition2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst2, c2_timeout).
42:47	RO	constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = INST1_CONDITION1_LT. 001 = INST1_CONDITION2_LT. 010 = INST1_CONDITION3_LT. 011 = INST1_COND2_TIMEOUT_LT. 1XX = disable CHECKSTOP_MODE.
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: enable_fir_trig_xstop: enable checkstop on debug trigger: 0 = Disable checkstop on debug trigger 1 = enable checkstop on debug trigger
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = INST2_CONDITION1_lt. 001 = INST2_CONDITION2_lt. 010 = INST2_CONDITION3_lt. 011 = inst2_cond2_timeout_lt. 1XX = disable checkstop_mode.
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: enable_fir_error_xstop: enable checkstop on fir error: 0 = Disable checkstop on FIR error. 1 = Enable checkstop on FIR error.
56:63	RO	constant = 0b00000000

Register Name	Debug Macro Configuration Register 12 for Backend Component
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000010107CF (SCOM)
Description	Debug Macro configuration register 12 for backend component

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the run-N counter used in trace modes run-N and wait-N.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on XSTOP.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on RUN-N match.
19	RW	FORCE_TEST_MODE: Force run-N condition to be true.

Bits	SCOM	Field Mnemonic: Description
20	RW	ACCUM_HIST_MODE: Accumulate history mode, do not clear history mode when trace_run active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	Trace Start/Stop/Rest Using SCOM Command, Use Write Data(0/1/2) = 1
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.DEBUG_TRACE_CONTROL
Address	00000000010107D0 (SCOM)
Description	Trace start/stop/rest using SCOM command, use write data(0/1/2) = 1

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.
1	WOX	Reserved field.
2	WOX	Reserved field.

Register Name	XTRA/Dedicated Trace Mode Register for Core Triggers
Mnemonic	TP.TPCHIP.TPC.EPS.DBG.XTRA_TRACE_MODE
Address	00000000010107D1 (SCOM)
Description	extra / dedicated trace mode register for core triggers

Bits	SCOM	Field Mnemonic: Description
0:37	RW	XTRA_TRACE_MODE_DATA: extra/dedicated trace mode register for core triggers.

Register Name	OCC_SCOM OCC LFIR
Mnemonic	TP.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIR
Address	0000000001010800 (SCOM) 0000000001010801 (SCOM1) 0000000001010802 (SCOM2)
Description	OCC_SCOM OCC LFIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIR_OCC_FW0: Input tied to 0. Used by OCC Firmware to produce an attention to the FSP.
1	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIR_OCC_FW1: Input tied to 0. Used by OCC Firmware to produce an attention to the FSP.
2	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIR_CME_ERROR_NOTIFY: Input tied to 0. Used by STOP GPE code to indicated to HYP that a CME has indicated a fault.
3	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIR_STOP_RECOVERY_NOTIFY_PRD: Input tied to 0. Written by stop recovery firmware to indicate that the host side actions are complete and that FFDC information is available for analysis toward subsequent guarding and/or deconfiguration. Intended to produce a recoverable attention (by using Action register settings) to the PRD component for such analysis.
4	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCC_HB_ERROR: OCC Heartbeat Error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE0_WATCHDOG_TIMEOUT: GPE0 asserted a watchdog timeout condition.
6	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE1_WATCHDOG_TIMEOUT: GPE1 asserted a watchdog timeout condition.
7	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE2_WATCHDOG_TIMEOUT: GPE2 asserted a watchdog timeout condition.
8	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE3_WATCHDOG_TIMEOUT: GPE3 asserted a watchdog timeout condition.
9	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE0_ERROR: GPE0 asserted an error condition that caused it to halt. Implemented as an OR of the four error outputs from the PPE.
10	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE1_ERROR: GPE1 asserted an error condition that caused it to halt. Implemented as an OR of the four error outputs from the PPE.
11	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE2_ERROR: GPE2 asserted an error condition that caused it to halt. Implemented as an OR of the four error outputs from the PPE.
12	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE3_ERROR: GPE3 asserted an error condition that caused it to halt. Implemented as an OR of the four error outputs from the PPE.
13	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_ERROR: OCB Error (recoverable error).
14	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_UE: SRAM Uncorrectable Error (recoverable error) **Note:** This being on will also have either a srt_read_error or srt_write_error on as well as these each have the UE error included. UE is broken out specifically to allow for array faster characterization.
15	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_CE: SRAM Correctable Error (masked (product); recoverable error (mfg).
16	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_READ_ERROR: SRAM Read Error - asserts if a read operation and any of the following: SRAM Tank Address Parity error; SRAM Uncorrectable error.
17	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_WRITE_ERROR: SRAM Read Error - asserts if a read operation and any of the following: SRAM Tank Address Parity error; if <8 B write (requiring a read, modify, write operation), (SRAM Tank Byte Enable Parity error; SRAM Write Data Parity error; SRAM Uncorrectable error).
18	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_DATAOUT_PERR: SRAM controller detected parity error on tank read data.
19	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_OCI_WRITE_DATA_PARITY: SRAM controller detected OCI write data parity error.
20	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_OCI_BE_PARITY_ERR: SRAM controller detected an OCI byte enable parity error.
21	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_OCI_ADDR_PARITY_ERR: SRAM controller detected an OCI address parity error.
22	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE0_HALTED: GPE0 asserted a halt condition.
23	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE1_HALTED: GPE1 asserted a halt condition.
24	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE2_HALTED: GPE2 asserted a halt condition.
25	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE3_HALTED: GPE3 asserted a halt condition.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
26	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_EXTERNAL_TRAP: External Trigger pin active (recoverable (product).
27	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_CORE_RESET: PowerPC 405 Core Reset Output asserted.
28	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_CHIP_RESET: PowerPC 405 Chip Reset Output asserted.
29	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_SYSTEM_RESET: PowerPC 405 System Reset Output asserted.
30	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_DBGMSRWE: PowerPC 405 Wait State asserted.
31	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_DBGSTOPACK: PowerPC 405 Stop Ack output asserted (recoverable -> logging) Process stopped execution.
32	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_DB_OCI_TIMEOUT: OCB Direct Bridge OCI Timeout. Asserted to flag that no OCI slave acknowledged the direct bridge request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
33	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_DB_OCI_READ_DATA_PARITY: OCB Direct Bridge OCI Read Data Parity Error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
34	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_DB_OCI_SLAVE_ERROR: OCB Direct Bridge OCI SlvError received. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
35	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_PIB_ADDR_PARITY_ERR: OCB PIB Address Parity Error (PIB read or write operation). **Note:** Can be set for either direct bridge or indirect channel operations. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
36	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_DB_PIB_DATA_PARITY_ERR: OCB Direct Bridge PIB Data Error. Indicates the PIB data parity was in error for a PIB write operation to a direct bridge address. **Note:** Write data parity errors to an indirect bridge address are captured in the the OCB Control Status [n] Register for the addressed channel. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
37	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_IDC0_ERROR: Indirect Channel 0 Error. See OCB ControlStatus 0 Register for the reason.
38	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_IDC1_ERROR: Indirect Channel 1 Error. See OCB ControlStatus 1 Register for the reason.
39	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_IDC2_ERROR: Indirect Channel 2 Error. See OCB ControlStatus 2 Register for the reason.
40	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_IDC3_ERROR: Indirect Channel 3 Error. See OCB ControlStatus 3 Register for the reason.
41	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_FSM_ERR: Indicates an FSM error in the read or write machines of the SRAM controller.
42	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_JTAGACC_ERR: JTAG accelerator error. See OJSTAT register for reason.
43	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SPARE_ERR_38: Input tied to 0.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
44	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405_ECC_UE: PowerPC 405 cache UE.
45	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405_ECC_CE: PowerPC 405 cache CE.
46	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405_OCI_MACHINECHECK: PowerPC 405 Machine Check.
47	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRAM_SPARE_DIRECT_ERROR0: SRAM spare direct error.
48	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRAM_SPARE_DIRECT_ERROR1: SRAM spare direct error.
49	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRAM_SPARE_DIRECT_ERROR2: SRAM spare direct error.
50	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRAM_SPARE_DIRECT_ERROR3: SRAM spare direct error.
51	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE0_OCISLV_ERR: OCI slave error for GPE0 (see OCCERRPT for details).
52	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE1_OCISLV_ERR: OCI slave error for GPE1 (see OCCERRPT for details).
53	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE2_OCISLV_ERR: OCI slave error for GPE2 (see OCCERRPT for details).
54	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE3_OCISLV_ERR: OCI slave error for GPE3 (see OCCERRPT for details).
55	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405ICU_M_TIMEOUT: PowerPC 405 ICU timeout on OCI request.
56	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405DCU_M_TIMEOUT: PowerPC 405 DCU timeout on OCI request.
57	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCC_COMPLEX_FAULT: Used by OCC to indicate that a fault occurred (to achieve safe mode). Connected to OCCMISC[firmware_fault].
58	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCC_COMPLEX_NOTIFY: Used by OCC to notify another firmware entity that an event occurred. Connected to OCCMISC[firmware_notify].
59:61	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIR_SPARE_59_61: Implemented but not used. Inputs tied to 0.
62	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_FIR_PARITY_ERR_DUP: Internal FIR parity error duplicate (same as bit 63).
63	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_FIR_PARITY_ERR: Internal FIR parity error.

Register Name	OCC_SCOM OCC LFIR MASK
Mnemonic	TP.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIRMASK
Address	0000000001010803 (SCOM) 0000000001010804 (SCOM1) 0000000001010805 (SCOM2)
Description	OCC_SCOM OCC LFIR MASK

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCC_FW0_MASK:
1	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCC_FW1_MASK:

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SPARE_2_MASK:
3	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SPARE_3_MASK:
4	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCC_HB_MALF_MASK: OCC Heartbeat Error (malfunction alert).
5	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE0_WATCHDOG_TIMEOUT_MASK: GPE0 asserted a watchdog timeout condition.
6	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE1_WATCHDOG_TIMEOUT_MASK: GPE1 asserted a watchdog timeout condition.
7	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE2_WATCHDOG_TIMEOUT_MASK: GPE2 asserted a watchdog timeout condition.
8	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE3_WATCHDOG_TIMEOUT_MASK: GPE3 asserted a watchdog timeout condition.
9	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE0_ERROR_MASK: GPE0 asserted a error condition.
10	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE1_ERROR_MASK: GPE1 asserted a error condition.
11	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE2_ERROR_MASK: GPE2 asserted a error condition.
12	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE3_ERROR_MASK: GPE3 asserted a error condition.
13	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_ERROR_MASK: OCB Error (recoverable error).
14	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_UE_MASK: SRAM Uncorrectable Error (recoverable error).
15	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_CE_MASK: SRAM Correctable Error (masked (product); recoverable error (mfg).
16	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_READ_ERROR_MASK: SRAM Read Error.
17	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_WRITE_ERROR_MASK: SRAM Read Error.
18	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_DATAOUT_PERR_MASK: SRAM controller detected parity error on tank read data.
19	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_OCI_WRITE_DATA_PARITY_MASK: SRAM controller detected OCI write data parity error.
20	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_OCI_BE_PARITY_ERR_MASK: SRAM controller detected an OCI byte enable parity error.
21	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_OCI_ADDR_PARITY_ERR_MASK: SRAM controller detected an OCI address parity error.
22	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE0_HALTED_MASK: GPE0 asserted a halt condition.
23	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE1_HALTED_MASK: GPE1 asserted a halt condition.
24	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE2_HALTED_MASK: GPE2 asserted a halt condition.
25	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE3_HALTED_MASK: GPE3 asserted a halt condition.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
26	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_EXTERNAL_TRAP_MASK: External Trigger pin active (recoverable (product).
27	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_CORE_RESET_MASK: PowerPC 405 Core Reset Output asserted.
28	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_CHIP_RESET_MASK: PowerPC 405 Chip Reset Output asserted.
29	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_SYSTEM_RESET_MASK: PowerPC 405 System Reset Output asserted.
30	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_DBGMSRWE_MASK: PowerPC 405 Wait State asserted.
31	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_DBGSTOPACK_MASK: PowerPC 405 Stop Ack output asserted (recoverable -> logging) Process stopped execution.
32	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_DB_OCI_TIMEOUT_MASK: OCB Direct Bridge OCI Timeout.
33	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_DB_OCI_READ_DATA_PARITY_MASK: OCB Direct Bridge OCI read data parity error.
34	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_DB_OCI_SLAVE_ERROR_MASK: OCB Direct Bridge OCI SlvError error.
35	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_PIB_ADDR_PARITY_ERR_MASK: OCB PIB address parity error.
36	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_DB_PIB_DATA_PARITY_ERR_MASK: OCB PIB data parity error.
37	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_IDC0_ERROR_MASK: Indirect Channel 0 Error.
38	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_IDC1_ERROR_MASK: Indirect Channel 1 Error.
39	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_IDC2_ERROR_MASK: Indirect Channel 2 Error.
40	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_IDC3_ERROR_MASK: Indirect Channel 3 Error.
41	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_FSM_ERR_MASK: SRAM Controller FSM error.
42	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_JTAGACC_ERR_MASK: JTAG accelerator error.
43	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SPARE_ERR_38_MASK:
44	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405_ECC_UE_MASK: PowerPC 405 cache Uncorrectable Error (UE).
45	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405_ECC_CE_MASK: PowerPC 405 cache Correctable Error (CE).
46	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405_OCI_MACHINECHECK_MASK: PowerPC 405 Machine Check.
47	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRAM_SPARE_DIRECT_ERROR0_MASK: SRAM spare direct error.
48	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRAM_SPARE_DIRECT_ERROR1_MASK: SRAM spare direct error.
49	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRAM_SPARE_DIRECT_ERROR2_MASK: SRAM spare direct error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
50	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRAM_SPARE_DIRECT_ERROR3_MASK: SRAM spare direct error.
51	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE0_OCISLV_ERR_MASK: OCI slave error for GPE0 (see OCCERRPT for details).
52	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE1_OCISLV_ERR_MASK: OCI slave error for GPE0 (see OCCERRPT for details).
53	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE2_OCISLV_ERR_MASK: OCI slave error for GPE0 (see OCCERRPT for details).
54	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE3_OCISLV_ERR_MASK: OCI slave error for GPE0 (see OCCERRPT for details).
55	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405ICU_M_TIMEOUT_MASK: PowerPC 405 ICU timeout on OCI request.
56	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405DCU_M_TIMEOUT_MASK: PowerPC 405 DCU timeout on OCI request.
57	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIRMASK_OCC_COMPLEX_FAULT_MASK: Used by OCC to indicate that a fault occurred (to achieve safe mode). Connected to OCCMISC[firmware_fault].
58	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIRMASK_OCC_COMPLEX_NOTIFY_MASK: Used by OCC to notify another firmware entity that an event occurred. Connected to OCCMISC[firmware_notify].
59:61	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SPARE_59_61: Implemented but not used. Inputs tied to 0.
62	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_FIR_PARITY_ERR_DUP_MASK: Internal FIR parity error duplicate (same as bit 63).
63	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_FIR_PARITY_ERR_MASK: Internal FIR parity error.

Register Name	OCC_SCOM OCC LFIR Action0
Mnemonic	TP.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIRACT0
Address	0000000001010806 (SCOM)
Description	OCC_SCOM OCC LFIR Action0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	OCC_SCOM_OCCLFIRACT0_FIR_ACTION0: MSB of action select for corresponding bit in FIR.

Register Name	OCC_SCOM OCC LFIR Action1
Mnemonic	TP.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIRACT1
Address	0000000001010807 (SCOM)
Description	OCC_SCOM OCC LFIR Action1

Bits	SCOM	Field Mnemonic: Description
0:63	RW	OCC_SCOM_OCCLFIRACT1_FIR_ACTION1: LSB of action select for corresponding bit in FIR.

Register Name	OCC_SCOM OCC Error Report Register
Mnemonic	TP.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCERRRPT
Address	000000000101080A (SCOM)
Description	OCC_SCOM OCC Error Report Register

Bits	SCOM	Field Mnemonic: Description
0:9	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_SRAM_CERRRPT: sram_oci_error_bus(0:9) 0 = FSM error write machine0 1 = FSM error write machine1 2 = FSM error read machine0 3 = FSM error read machine1 4 = Write buffer underflow 5 = Write buffer overflow 6:9 are spares.
10:15	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_JTAGACC_CERRPT: JTAG accelerator errors. See OJSTAT register for description.
16	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_C405_DCU_ECC_UE: PowerPC 405 data cache UE detected.
17	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_C405_DCU_ECC_CE: PowerPC 405 data cache CE detected.
18	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_C405_ICU_ECC_UE: PowerPC 405 instruction cache UE detected.
19	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_C405_ICU_ECC_CE: PowerPC 405 instruction cache CE detected.
20:26	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_GPE0_OCISLV_ERR: OCI slave error in GPE 0 0 = Address parity error 1 = Byte enable parity error 2 = Write data parity error 3 = Byte enable error (non-word aligned) 4 = Transfer size error (non-zero transfer size) 5 = Invalid address 6 = Read error (register is not readable).
27	RO	constant = 0b0
28:34	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_GPE1_OCISLV_ERR: OCI slave Error in GPE 1 0 = Address parity error 1 = Byte enable parity error 2 = Write data parity error 3 = Byte enable error (non-word aligned) 4 = Transfer size error (non-zero transfer size) 5 = Invalid address 6 = Read error (register is not readable).
35	RO	constant = 0b0
36:42	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_GPE2_OCISLV_ERR: OCI slave Error in GPE 2 0 = Address parity error 1 = Byte enable parity error 2 = Write data parity error 3 = Byte enable error (non-word aligned) 4 = Transfer size error (non-zero transfer size) 5 = Invalid address 6 = Read error (register is not readable).
43	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
44:50	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_GPE3_OCISLV_ERR: OCI slave error in GPE 3 0 = Address parity error 1 = Byte enable parity error 2 = Write data parity error 3 = Byte enable error (non-word aligned) 4 = Transfer size error (non-zero transfer size) 5 = Invalid address 6 = Read error (register is not readable).
51	RO	constant = 0b0
52:57	RWX_WCLRPART	OCC_SCOM_OCCERRRPT_OCB_OCISLV_ERR: OCI slave error in OCB 0 = Address parity error 1 = Byte enable parity error 2 = Write data parity error 3 = Byte enable error (non-word aligned) 4 = Transfer size error (non-zero transfer size) 5 = Invalid address.
58:63	RO	constant = 0b000000

Register Name	Counter References
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.FMU_MODE_REG
Address	0000000001020000 (SCOM)
Description	Counter References

Bits	SCOM	Field Mnemonic: Description
0:11	RW	TOD_CNTR_REF: To determine time frame the oscillator pulses are counted. This value is compared to a 16-bit wide TOD pulse counter.
12:15	RW	Reserved field.
16	RW	Reserved field.
17:19	RW	POWER_UP_CNTR_REF: To determine time frame the FMU starts counting the oscillator pulses. This value is compared to a 3-bit wide TOD pulse counter. Must be 0b010 in case time to wait must be >= 62.5 ns (16 MHZ).
20:23	RW	Reserved field.

Register Name	Osc Counter1
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.FMU_OSC_CNTR1_REG
Address	0000000001020001 (SCOM)
Description	Stressed Osc Counter for NBTI

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	RESULT_AVAILABLE: FMU result available.
4:27	ROX	OSC_PULSE1_CNTR: Osc Counter1. Stressed OSC Counter for NBTI.

Register Name	Counter References for Internal Pulse
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.FMU_PULSE_GEN_REG
Address	0000000001020001 (SCOM)
Description	Counter References for Internal Pulse

Bits	SCOM	Field Mnemonic: Description
0	WO	FMU_INT_PULSE_ENA: FMU internal TOD pulse generation enable.
1	WO	Reserved field.
2:11	WO	FMU_INT_PULSE_CNTR_REF: Reference value to compare against 10-bit counter for FMU internal TOD pulse generation.

Register Name	OSC Counter 2
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.FMU_OSC_CNTR2_REG
Address	0000000001020002 (SCOM)
Description	Reference OSC Counter for NBTI

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	RESULT_AVAILABLE: FMU result available.
4:27	ROX	OSC_PULSE2_CNTR: OSC Counter2. Stressed OSC Counter for NBTI.

Register Name	Force Operations
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.FMU_FORCE_OP_REG
Address	0000000001020003 (SCOM)
Description	Force Operations

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.
1	WOX	Reserved field.

Register Name	KVREF Data Register
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.FMU_KVREF_DATAREG
Address	0000000001020004 (SCOM)
Description	KVREF data register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	KVREF Tune Data
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.KVREF_TUNE_DATA
Address	0000000001020005 (SCOM)
Description	KVREF Tune Data

Bits	SCOM	Field Mnemonic: Description
0:11	ROX	Reserved field.

Register Name	VMEAS RESULT Register
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.VMEAS_RESULT_REG
Address	0000000001020006 (SCOM)
Description	VMEAS Result Register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved field.

Register Name	KVREF and VMEAS Mode Register
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.KVREF_AND_VMEAS_MODE_STATUS_REG
Address	0000000001020007 (SCOM)
Description	KVREF and VMEAS Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved field.
1	RW	Reserved field.
2	RW	Reserved field.
3:7	RO	constant = 0b00000
8	RWX	Reserved field.
9	RW	Reserved field.
10	RW	Reserved field.
11:15	RO	constant = 0b00000
16	ROX	Reserved field.
17	ROX	Reserved field.
18	ROX	Reserved field.
19	ROX	Reserved field.

Register Name	VMEAS Maximum Result
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.FMU_VMEAS_MAX_RESULT
Address	0000000001020008 (SCOM)
Description	VMEAS Maximum Result

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved field.

Register Name	VMEAS Minimum Result
Mnemonic	TP.TPCHIP.TPC.ITR.FMU.FMU_VMEAS_MIN_RESULT
Address	0000000001020009 (SCOM)
Description	VMEAS Minimum Result

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved field.

Register Name	OSC Error Hold Latch
Mnemonic	TP.TPCHIP.TPC.ITR.OSCERR.OSCERR_HOLD
Address	0000000001020019 (SCOM)
Description	OSC Error hold latch

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	OSCERR_CP: OSC Error hold values for cp.
4:7	RWX	OSCERR_MEM: OSC Error hold values for mem.
8:11	RWX	OSCERR_GX: OSC Error hold values for gx.
12:15	RWX	OSCERR_CPLITE: OSC Error hold values for cplite.

Register Name	OSC Error Mask Latch
Mnemonic	TP.TPCHIP.TPC.ITR.OSCERR.OSCERR_MASK
Address	000000000102001A (SCOM)
Description	OSC Error mask latch

Bits	SCOM	Field Mnemonic: Description
0:3	RW	OSCERR_CP_MASK: OSC error hold values for CP.
4:7	RW	OSCERR_MEM_MASK: OSC error hold values for MEM.
8:11	RW	OSCERR_GX_MASK: OSC error hold values for GX.
12:15	RW	OSCERR_CPLITE_MASK: OSC error hold values for CPLITE.

Register Name	OSC Error MCODE Latch
Mnemonic	TP.TPCHIP.TPC.ITR.OSCERR.OSCERR_MCODE
Address	000000000102001B (SCOM)
Description	OSC Error MCODE Latch

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	OSCERR_MCODE_IN: OSC Error MCODE.

Register Name	Configuration of CC Counters
Mnemonic	TP.TPCHIP.TPC.SYNC_CONFIG
Address	0000000001030000 (SCOM)
Description	Configuration of CC counters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay incoming sync pulse. Default are eight latches including. Async. 0000 = 8 0001 = 2 0010 = 3 0011 = 4 0100 = 5 0101 = 6 0110 = 7 0111 = 8 cycles 1000 = 9 1001 = 10 1010 = 11 1011 = 12 1100 = 13 1101 = 14 1110 = 15 1111 = 16 delay of the reset of the phase counter.
4	RW	LISTEN_TO_SYNC_PULSE_DIS: disable phase counter synchronization by SYNC_PULSE signal (default is enabled) Attention: When LISTEN_TO_SYNC is enabled, the chiplet is corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: Default is 0. When set to 1, the alternative input of the SYNC_PULSE will be used. Attention: When toggling the input select, the chiplet is corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: if set, use OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the CHIPLET_IS_ALIGNED bit. See the CPLT_STAT register.
8	RW	UNIT_REGION_CLKCMD_ENABLE: Enable the unit interface to start/stop one dedicate region. Used for the POWER9 cache/core.
9	RW	DISABLE_PCB_ITR: Disable interrupt generation within CC. The interrupt is sent on each HLD event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enable the VITL align check to compare alignment of incoming sync pulse with 2:1 VITL LCB.
11	RW	SYNC_PULSE_OUT_DIS: Disable SYNC_PULSE output when set to 1, master chiplet will not send sync pulses to slave chiplets anymore.
12:19	RW	UNUSED1219: Unused.

Register Name	OPCG Align
Mnemonic	TP.TPCHIP.TPC.OPCG_ALIGN
Address	0000000001030001 (SCOM)
Description	OPCG Align

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9 = 15:48

Bits	SCOM	Field Mnemonic: Description
4:7	RW	SNOP_ALIGN: SNOP phase alignment 0 = none 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9 = 15:48
8:11	RW	ENOP_ALIGN: ENOP phase alignment 0 = none 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9 = 15:48
12:19	RW	INOP_WAIT: INOP cycle delay (0 - 255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0 - 4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0 - 255).
40	RW	INOP_FORCE_SG: INOP: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: SNOP: Set SG high during SNOP.
42	RW	ENOP_FORCE_SG: ENOP: Set SG high during ENOP (including loop phase).
43	RW	NO_WAIT_ON_CLK_CMD: 0 = A clock change request will first wait the OPCG_WAIT cycles. 1 = A clock change request will not wait, when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0 = Use INOPA setting from OPCG_REG0 1 = Use rising edge of sync pulse 2 = Use UNIT0_SYNC_LVL to align (for AVP - REFRESH0) 3 = Use UNIT1_SYNC_LVL to align (for AVP - REFRESH1)
46	RW	UNUSED46: Unused.
47:51	RW	SCAN_RATIO: SCAN_RATIO (n=0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1) - Default 4:1= 00011.
52:63	RW	OPCG_WAIT_CYCLES: Old PAD value. The delay at the beginning and at the end of the OPCG run. To allow DC signals to be there at the right time (0 4095), there must be a higher than plat depth. Default = 0x020.

Register Name	**OPCG Control Register 0**
Mnemonic	TP.TPCHIP.TPC.OPCG_REG0
Address	0000000001030002 (SCOM)
Description	OPCG Control Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST-mode. Used for LBIST. 1 = RUN-N mode. Used for ABIST/IOBIST.
1	RWX	OPCG_GO: OPCG GO (start OPCG). This bit is cleared when OPCG is done. Poll for OPCG_DONE in CPLT_START the register.
2	RWX	RUN_SCAN0: Run SCAN0. This overrides all BIST mode settings but the SCAN_RATIO), which starts a SCAN0 run. The bit is cleared when OPCG is done. Poll for OPCG_DONE in the CPLT_START register.
3	RW	SCAN0_MODE: Set PRPGs in SCAN0_MODE, but do not run automatic SCAN0 the sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, the OPCG waits for the master chiplet to get started. When KEEP_MS_MODE is 0, SLAVE_MODE is cleared after the incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, the OPCG sends a trigger to all slave chiplets. When KEEP_MS_MODE = 0, MASTER_MODE is cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, OPCG in M/S mode bits are not be cleared after one incoming OPCG trigger. The default is to clear M/S mode bits.

Bits	SCOM	Field Mnemonic: Description
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: Unit pin used for AVP can trigger OPCG (UNIT0_SYNC_LVL).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: Unit pin used for AVP can trigger OPCG (UNIT1_SYNC_LVL).
9	RWX	RUN_CHIPLET_SCAN0: Run SCAN0 on all regions and types. (It clears the chiplet at all.)
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run SCAN0 on all regions and types. It clears the chiplet at all exclude PLL regions. PLL can keep running.
11	RW	RUN_OPCG_ON_UPDATE_DR: Start the OPCG engine when the scan update (update_dr) is received (set pulse). Cronus requires that this bit = 1 for a set-pulse write.
12	RW	RUN_OPCG_ON_CAPTURE_DR: start the OPCG engine when the scan update (capture_dr) is received (set pulse). Cronus requires that this bit = 1 for a set pulse read.
13	RW	STOP_RUNN_ON_XSTOP: RUN-N mode: stop RUN-N on XSTOP.
14	RW	OPCG_STARTS_BIST: RUN-N mode: OPCG engine controls start_bist for ABIST or IOBIST (see the BIST register).
15:20	RW	UNUSED1520: Unused.
10:03:00 PM	RWX	LOOP_COUNT: Loop counter for LBIST and RUN-N. Write = Target value Read = Current counter value. Counts from 0 to target value.

Register Name	OPCG Control Register 1
Mnemonic	TP.TPCHIP.TPC.OPCG_REG1
Address	0000000001030003 (SCOM)
Description	OPCG Control Register 1

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode = Channel scan count (s = 0-4095) Run-n mode: START_BIST match value(0:11).
12:23	RW	MISR_A_VAL: BIST mode = A value for MISR aperture. Run-n mode = START_BIST match value(12:23).
24:35	RW	MISR_B_VAL: BIST mode = b value for MISR aperture Run-n mode = START_BIST match value(24:35).
36:47	RW	MISR_INIT_WAIT: BIST mode = delay MISR aperture. MISRs get active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG creates even and not odd clocks. Used for RUN-N to create only one clock in fast domain. Default is 0.
49	RW	SCAN_CLK_USE_EVEN: Generate scan clock in even cycle instead of odd. Default is 0 = odd for scan.
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: Force RTIM_THOLD low when not in TEST_DC mode (must be 0 at all time).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0: prevent fire of ARY HLD during NSL-fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0: Hold SG high during NSL-fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode: 00 = Enable skitter during LBIST_IP 01 = Enable skitter when MISR_ACTIVE. See MISR_INIT_WAIT 10 = Skitter OPCG_GO mode. Falling edge = start. Rising edge = stop 11 = Unused

Bits	SCOM	Field Mnemonic: Description
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0 = a-1 to b-1, 1 = start to a and b to end).
58	RW	INFINITE_MODE: Infinite mode. Run-n and LBIST run forever and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31).

Register Name	OPCG Control Register 2
Mnemonic	TP.TPCHIP.TPC.OPCG_REG2
Address	0000000001030004 (SCOM)
Description	OPCG Control Register 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: OPCG go for broadcast sequences (start sequence).
01:03:00 AM	RW	PRPG_WEIGHTING: PRPG_ACTIVATE: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16.
4:15	RWX	PRPG_VALUE: Set to 0 for prpg always on, else seed.
16:27	RW	PRPG_A_VAL: A value for PRPG aperture.
28:39	RW	PRPG_B_VAL: B value for PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode (0 = a-1 to b-1, 1 = start to a and b to end).
41:63	RW	UNUSED41_63: Unused.

Register Name	Scan Region and Type
Mnemonic	TP.TPCHIP.TPC.SCAN_REGION_TYPE
Address	0000000001030005 (SCOM)
Description	Scan Region and Type

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: Default is 0, when its set to 1, the MASK bits in the CMSK chain decide, which part will be scanned or scan0. MASK = 1 = scan0, MASK = 0-part or scan chain.
1:2	RO	constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region VITL (Vital = Clock).
4	RWX	SCAN_REGION_PERV: Scan clock region perv (Pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region net.
6	RWX	SCAN_REGION_UNIT2: Scan clock region PIB.
7	RWX	SCAN_REGION_UNIT3: Scan clock region OCC.
8	RWX	SCAN_REGION_UNIT4: Scan clock region ANPERV - E9.
9	RWX	SCAN_REGION_UNIT5: Scan clock region unused.
10	RWX	SCAN_REGION_UNIT6: Scan clock region unused.
11	RWX	SCAN_REGION_UNIT7: Scan clock region unused.
12	RWX	SCAN_REGION_UNIT8: Scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: Scan clock region unused.

Bits	SCOM	Field Mnemonic: Description
14	RWX	SCAN_REGION_UNIT10: Scan clock regions PLLPERV, PLLNEST, PLLNESTFLT, PLLEMFLT, PLLSSCG - TP.
15:47	RO	constant = 0b00000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain func (functional).
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configure and debug configure).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain CCFG/GPTR (Pervasive: CC configure, Others: GPTR).
51	RW	SCAN_TYPE_REGF: Scan chain regf (register files).
52	RW	SCAN_TYPE_LBIST: Scan chain (LBIST).
53	RW	SCAN_TYPE_ABIST: Scan chain (ABIST).
54	RW	SCAN_TYPE_REPR: Scan chain (Array Repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (Array Timing).
56	RW	SCAN_TYPE_BNDY: Scan chain boundry (Boundary I/Os).
57	RW	SCAN_TYPE_FARR: Scan chain FARR (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain CMSK (LBIST channel mask).
59	RW	SCAN_TYPE_INEX: Scan chain idex (c14 ASIC).
60:63	RO	constant = 0b0000

Register Name	Start/Stop of Clocks
Mnemonic	TP.TPCHIP.TPC.CLK_REGION
Address	0000000001030006 (SCOM)
Description	start/stop of Clocks

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: command for clock control: 00 = NOP 01 = START 10 = STOP 11 = PULSE (one pulse).
2	RWX	SLAVE_MODE: when selected, Clock Command will wait for Master chiplet to get started. Bit gets cleared after incoming Slave trigger and KEEP_MS_MODE_AFTER_TRIGGER is set to 0.
3	RWX	MASTER_MODE: when selected, Clock Command will send out trigger to all Slave chiplets. Bit gets cleared after sending out one Master trigger and KEEP_MS_MODE_AFTER_TRIGGER is set to 0.
4	RWX	CLOCK_REGION_PERV: For clock region perv (Pervasive).
5	RWX	CLOCK_REGION_UNIT1: For clock region net.
6	RWX	CLOCK_REGION_UNIT2: For clock region PIB.
7	RWX	CLOCK_REGION_UNIT3: For clock region OCC.
8	RWX	CLOCK_REGION_UNIT4: For clock region ANPERV - E9.
9	RWX	CLOCK_REGION_UNIT5: For clock region unused.
10	RWX	CLOCK_REGION_UNIT6: For clock region unused.
11	RWX	CLOCK_REGION_UNIT7: For clock region unused.
12	RWX	CLOCK_REGION_UNIT8: For clock region unused.
13	RWX	CLOCK_REGION_UNIT9: For clock region unused.

Bits	SCOM	Field Mnemonic: Description
14	RWX	CLOCK_REGION_UNIT10: For clock regions PLLPERV, PLLNEST, PLLNESTFLT, PLLEMFLT, PLLSSCG - TP.
15:47	RO	constant = 0b00000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Select SL THOLDS.
49	RWX	SEL_THOLD_NSL: Select NSL THOLDS.
50	RWX	SEL_THOLD_ARY: Select array THOLD.
51	RO	constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support: default for pulse is ODD phase, when this bit is set, pulse will by applied on EVEN phase.
53:63	RO	constant = 0b00000000000

Register Name	Clocks Running SL
Mnemonic	TP.TPCHIP.TPC.CLOCK_STAT_SL
Address	0000000001030008 (SCOM)
Description	Clocks Running SL

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: Status of perv SL HLD 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT1_SL: Status of net SL HLD 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT2_SL: Status of PIB SL HLD 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT3_SL: Status of OCC SL HLD 0 = Run 1 = Stop
8	ROX	CLOCK_STATUS_UNIT4_SL: status of ANPERV - E9 SL HLD 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT5_SL: status of unused SL HLD 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT6_SL: status of unused SL HLD 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT7_SL: status of unused SL HLD 0 = Run 1 = Stop
12	ROX	CLOCK_STATUS_UNIT8_SL: status of unused SL HLD 0 = Run 1 = Stop

Bits	SCOM	Field Mnemonic: Description
13	ROX	CLOCK_STATUS_UNIT9_SL: status of unused SL HLD 0 = Run 1 = Stop
14	ROX	CLOCK_STATUS_UNIT10_SL: status of PLLPERV, PLLNEST, PLLNESTFLT, PLLEMFLT, PLLSSCG - TP SL HLD 0 = Run 1 = Stop
15:63	RO	constant = 0b11111111111111111111111111111111111111111111111111111

Register Name	Clocks Running NSL
Mnemonic	TP.TPCHIP.TPC.CLOCK_STAT_NSL
Address	0000000001030009 (SCOM)
Description	Clocks running NSL

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: Status of perv NSL HLD 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT1_NSL: Status of net NSL HLD 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT2_NSL: Status of PIB NSL HLD 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT3_NSL: Status of OCC NSL HLD 0 = Run 1 = Stop
8	ROX	CLOCK_STATUS_UNIT4_NSL: Status of ANPERV - E9 NSL HLD 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT5_NSL: Status of unused NSL HLD 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT6_NSL: Status of unused NSL HLD 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT7_NSL: Status of unused NSL HLD 0 = Run 1 = Stop
12	ROX	CLOCK_STATUS_UNIT8_NSL: Status of unused NSL HLD 0 = Run 1 = Stop
13	ROX	CLOCK_STATUS_UNIT9_NSL: Status of unused NSL HLD 0 = Run 1 = Stop

Bits	SCOM	Field Mnemonic: Description
14	ROX	CLOCK_STATUS_UNIT10_NSL: status of PLLPERV, PLLNEST, PLLNESTFLT, PLLEMFLT, PLLSSCG - TP NSL HLD 0 = Run 1 = Stop
15:63	RO	constant = 0b111111111111111111111111111111111111111111111111111111

Register Name	Clocks Running Ary
Mnemonic	TP.TPCHIP.TPC.CLOCK_STAT_ARY
Address	000000000103000A (SCOM)
Description	Clocks Running Ary

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: Status of perv ARY HLD 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT1_ARY: Status of net ARY HLD 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT2_ARY: Status of PIB ARY HLD 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT3_ARY: Status of OCC ARY HLD 0 = Run 1 = Stop
8	ROX	CLOCK_STATUS_UNIT4_ARY: Status of ANPERV - E9 ARY HLD 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT5_ARY: Status of unused ARY HLD 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT6_ARY: Status of unused ARY HLD 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT7_ARY: Status of unused ARY HLD 0 = Run 1 = Stop
12	ROX	CLOCK_STATUS_UNIT8_ARY: Status of unused ARY HLD 0 = Run 1 = Stop
13	ROX	CLOCK_STATUS_UNIT9_ARY: Status of unused ARY HLD 0 = Run 1 = Stop
14	ROX	CLOCK_STATUS_UNIT10_ARY: Status of PLLPERV, PLLNEST, PLLNESTFLT, PLLEMFLT, PLLSSCG - TP ARY HLD 0 = Run 1 = Stop
15:63	RO	constant = 0b111111111111111111111111111111111111111111111111111111

Register Name	ABIST and IOBIST per Region
Mnemonic	TP.TPCHIP.TPC.BIST
Address	0000000001030008 (SCOM)
Description	ABIST and IOBIST per region

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this 0 during ABIST/IOBIST. It can be used to bypass the RUN-N start. When this bit is set, the BIST_START_TEST goes high immediately without waiting for RUN-N. BIST starts with the first HLD clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: Select the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: Select the ABIST engines for EDRAMs.
3	RW	TC_IOBIST_MODE_DC: Select the IOBIST engines.
4	RW	BIST_PERV: Region perv: 1 = BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
5	RW	BIST_UNIT1: Region net: 1 = BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
6	RW	BIST_UNIT2: Region PIB: 1= BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
7	RW	BIST_UNIT3: Region OCC: 1= BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
8	RW	BIST_UNIT4: Region ANPERV: E9: 1= BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
9	RW	BIST_UNIT5: Region unused: 1= BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
10	RW	BIST_UNIT6: Region unused: 1= BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
11	RW	BIST_UNIT7: Region unused: 1= BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
12	RW	BIST_UNIT8: Region unused: 1= BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
13	RW	BIST_UNIT9: Region unused: 1= BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
14	RW	BIST_UNIT10: Regions PLLPERV, PLLNEST, PLLNESTFLT, PLLEMFLT, PLLSSCG - TP: 1= BIST_START_TEST for this region will be triggered. 0 = Region will not take part of the ABIST/IOBIST run.
15:47	RO	constant = 0b00000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: Enable Strobe window only in TE = 1. Mode OPCGGO tester pin is enabling ABIST compare when ABIST has been started. Special setup in ABIST engine is required. Default is 0. System mode can not enable this feature.
49:63	RO	constant = 0b000000000000000

Register Name	XSTOP per Region
Mnemonic	TP.TPCHIP.TPC.XSTOP1
Address	000000000103000C (SCOM)
Description	XSTOP per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: mask for XSTOP to clockstop of select regions (see XSTOP_PERV,XSTOP_UNIT0…n): 0 = Ignore CHKSTOP 1 = Stop on CHKSTOP
1	RW	XSTOP1_UNUSED:
2	RW	TRIGGER_OPCG_ON_XSTOP1: Trigger OPCG on XSTOP instead of performing clockstop.
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, XSTOP will wait independent from flush, default is no wait, when flush in not set.
4	RW	XSTOP1_PERV: Region perv: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
5	RW	XSTOP1_UNIT1: Region net: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
6	RW	XSTOP1_UNIT2: Region PIB: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
7	RW	XSTOP1_UNIT3: Region OCC: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
8	RW	XSTOP1_UNIT4: Region ANPERV - E9: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
9	RW	XSTOP1_UNIT5: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
10	RW	XSTOP1_UNIT6: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
11	RW	XSTOP1_UNIT7: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
12	RW	XSTOP1_UNIT8: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
13	RW	XSTOP1_UNIT9: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
14	RW	XSTOP1_UNIT10: Regions PLLPERV, PLLNEST, PLLNESTFLT, PLLEMFLT, PLLSSCG - TP: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
15:47	RO	constant = 0b00000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:59	RW	XSTOP1_WAIT_CYCLES: Defines, how many cycle XSTOP will wait after dropping flush, before tholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	constant = 0b0000

Register Name	XSTOP per Region
Mnemonic	TP.TPCHIP.TPC.XSTOP2
Address	000000000103000D (SCOM)
Description	XSTOP per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: mask for XSTOP to clockstop of select regions(see XSTOP_PERV,XSTOP_UNIT0…n) 0 = Ignore CHKSTOP 1= Stop on CHKSTOP
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: Trigger OPCG on XSTOP instead of performing clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: when set to 1, XSTOP will wait independent from flush, default is no wait, when flush in not set.
4	RW	XSTOP2_PERV: Region perv: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
5	RW	XSTOP2_UNIT1: Region net: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
6	RW	XSTOP2_UNIT2: Region PIB: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
7	RW	XSTOP2_UNIT3: Region OCC: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
8	RW	XSTOP2_UNIT4: Region ANPERV - E9: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
9	RW	XSTOP2_UNIT5: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
10	RW	XSTOP2_UNIT6: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
11	RW	XSTOP2_UNIT7: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
12	RW	XSTOP2_UNIT8: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
13	RW	XSTOP2_UNIT9: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.

Bits	SCOM	Field Mnemonic: Description
14	RW	XSTOP2_UNIT10: Regions PLLPERV, PLLNEST, PLLNESTFLT, PLLEMFLT, PLLSSCG - TP: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Defines, how many cycle XSTOP will wait after dropping flush, before tholds get dropped. 0-4095 cycles possible.
60:63	RO	constant = 0b0000

Register Name	XSTOP per Region
Mnemonic	TP.TPCHIP.TPC.XSTOP3
Address	000000000103000E (SCOM)
Description	XSTOP per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: mask for XSTOP to clockstop of select regions (see XSTOP_PERV,XSTOP_UNIT0…n): 0 = Ignore CHKSTOP 1= Stop on CHKSTOP
1	RW	XSTOP3_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP3: Trigger OPCG on XSTOP instead of performing clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, XSTOP will wait independent from flush, default is no wait, when flush in not set.
4	RW	XSTOP3_PERV: Region perv: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
5	RW	XSTOP3_UNIT1: Region net: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
6	RW	XSTOP3_UNIT2: Region PIB: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
7	RW	XSTOP3_UNIT3: Region OCC: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
8	RW	XSTOP3_UNIT4: Region ANPERV - E9: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
9	RW	XSTOP3_UNIT5: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
10	RW	XSTOP3_UNIT6: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
11	RW	XSTOP3_UNIT7: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.

Bits	SCOM	Field Mnemonic: Description
12	RW	XSTOP3_UNIT8: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
13	RW	XSTOP3_UNIT9: Region unused: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
14	RW	XSTOP3_UNIT10: Regions PLLPERV, PLLNEST, PLLNESTFLT, PLLEMFLT, PLLSSCG - TP: 1 = Region will be stopped. 0 = Region will keep running on XSTOP.
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Defines how many cycle XSTOP will wait after dropping flush before THOLDS get dropped. 0-4095 cycles possible.
60:63	RO	constant = 0b0000

Register Name	Error Status of CC
Mnemonic	TP.TPCHIP.TPC.ERROR_STATUS
Address	000000000103000F (SCOM)
Description	Error Status of CC

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: Write on read only register.
1	RWX	PCB_READ_NOT_ALLOWED_ERR: Read not allowed. Maybe write only register.
2	RWX	PCB_PARITY_ON_CMD_ERR: Parity error on CMD.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: Invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on address.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: Protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on specification.
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: PCB write while OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: Scan read when OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: Clock CMD in progress.
11	RWX	SCAN_COLLISION_ERR: Scan region selected of running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set scan region which is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG gets triggered while OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: Phase counters inside chiplet out of sync.
15	RWX	CLOCK_CMD_PREVENTED_ERR: Security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on OPCG state machine.
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on scan/clock region/type or clock status register.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG registers.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on sync configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on XSTOP register.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0,4,5,6 registers.

Bits	SCOM	Field Mnemonic: Description
22	RWX	CLKCMD_REQUEST_ERR: Region CLKCMD has one request pending but received a second one.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error. Request/acknowledgment sequence wrong.
24	RWX	VITL_ALIGN_ERR: VITL alignment is out of sync to sync pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 sync LVL pulse are not in sync. AVP broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on self-boot CMD state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	**OPCG Control Register Capture1**
Mnemonic	TP.TPCHIP.TPC.OPCG_CAPT1
Address	0000000001030010 (SCOM)
Description	OPCG Control Register Capture1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000 = 12 cycle 0001 - 1100 = cycle 1-12 1101 - 1111 = 24 normal, no fast.
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (SL, NSL, ARY, SE, FCE).

Register Name	**OPCG Control Register Capture 2**
Mnemonic	TP.TPCHIP.TPC.OPCG_CAPT2
Address	0000000001030011 (SCOM)
Description	OPCG Control Register Capture 2

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2:
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1. Even for fast region or cycle 13 for normal region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1. Odd for fast region or cycle 14 for normal region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_15_02EVEN: Sequence cycle 2. Even for fast region or cycle 15 for normal region (SL, NSL, ARY, SE, FCE).

Bits	SCOM	Field Mnemonic: Description
19:23	RW	SEQ_16_02ODD: Sequence cycle 2. Odd for fast region or cycle 16 for normal region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3. Even for fast region or cycle 17 for normal region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3. Odd for fast region or cycle 18 for normal region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4. Even for fast region or cycle 19 for normal region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4. Odd for fast region or cycle 20 for normal region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5. Even for fast region or cycle 21 for normal region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5. Odd for fast region or cycle 22 for normal region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6. Even for fast region or cycle 23 for normal region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6. Odd for fast region or cycle 24 for normal region (SL, NSL, ARY, SE, FCE).

Register Name	OPCG Control Register Capture 3
Mnemonic	TP.TPCHIP.TPC.OPCG_CAPT3
Address	0000000001030012 (SCOM)
Description	OPCG Control Register Capture 3

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7. Even for fast region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_07ODD: Sequence cycle 7. Odd for fast region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_08EVEN: Sequence cycle 8. Even for fast region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_08ODD: Sequence cycle 8. Odd for fast region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_09EVEN: Sequence cycle 9. Even for fast region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_09ODD: Sequence cycle 9. Odd for fast region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_10EVEN: Sequence cycle 10. Even for fast region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_10ODD: Sequence cycle 10. Odd for fast region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_11EVEN: Sequence cycle 11. Even for fast region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_11ODD: Sequence cycle 11. Odd for fast region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_12EVEN: Sequence cycle 12. Even for fast region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12ODD: Sequence cycle 12. Odd for fast region (SL, NSL, ARY, SE, FCE).

Register Name	Debug CBS CC Register
Mnemonic	TP.TPCHIP.TPC.DBG_CBS_CC
Address	0000000001030013 (SCOM)
Description	Debug CBS CC Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset Endpoint - Is the CC and CTRL in reset state.
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped, when enabled, need plat-depth cycles to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test Enable.
4	ROX	DBG_CBS_REQ: CBS Interface. Request (Latched).
5:7	ROX	DBG_CBS_CMD: CBS Interface. Command (Latched).
8:12	ROX	DBG_CBS_STATE: CBS Command State Machine 00000 = Idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS Protocol Error. REQ raised, although state machine is not in IDLE. RESET_EP is required to clear this bit. No impact on IPL.
15	ROX	DBG_PCB_IDLE: PCB Interface in IDLE state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: Current/latest OPCG MODE 0 = NOP 1 = LBIST 2 = ABIST 3 = RUN-N 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN with CaptureDR 9 = CLK Change Request 10 - 15 = Unused
20:23	ROX	DBG_LAST_OPCG_MODE: Previous OPCG MODE.
24	ROX	DBG_PCB_ERROR: PCB Interface Error, Read CC Error Register or set CBS_CMD = 001 to switch FSI CBS Debug Information to CC Error Register.
25	ROX	DBG_PARITY_ERROR: Any Parity Error, non PCB Parity. Read CC Error Register or set CBS_CMD = 001 to switch FSI CBS debug information to CC Error Register.
26	ROX	DBG_CC_ERROR: Any other CC Error. Read CC Error Register or set CBS_CMD = 001 to switch FSI CBS Debug Information to CC Error Register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: Is 1 when the a valid align pulse WS is sent out.
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: RESET will clear that bit. The first PCB request will set it.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: Rising or falling edge on test enable. After reset, RESET_EP must be cleared. There is no impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on VITL_CLKOFF. After reset, RESET_EP must be cleared. There is no impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: Only representation of CC acknowledge signal going to FSI.

Register Name	CC Protect Mode Register
Mnemonic	TP.TPCHIP.TPC.CC_PROTECT_MODE_REG
Address	00000000010303FE (SCOM)
Description	CC Protect Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.TPC.CC_ATOMIC_LOCK_REG
Address	00000000010303FF (SCOM)
Description	Atomic Lock Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	CC_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	Global Checkstop FIR
Mnemonic	TP.TPCHIP.TPC.XFIR
Address	0000000001040000 (SCOM)
Description	Global checkstop FIR

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any XSTOP).
1	RWX	XFIR_IN1: XSTOP broadcast by using OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: XSTOP from pervasive unit.
4	RWX	XFIR_IN4: Checkstop from OCC complex.
5	RWX	XFIR_IN5: Unused.
6	RWX	XFIR_IN6: Unused.
7	RWX	XFIR_IN7: Unused.
8	RWX	XFIR_IN8: Unused.
9	RWX	XFIR_IN9: Unused.
10	RWX	XFIR_IN10: Unused.
11	RWX	XFIR_IN11: Unused.
12	RWX	XFIR_IN12: Unused.
13	RWX	XFIR_IN13: Unused.

Bits	SCOM	Field Mnemonic: Description
14	RWX	XFIR_IN14: Unused.
15	RWX	XFIR_IN15: Unused.
16	RWX	XFIR_IN16: Unused.
17	RWX	XFIR_IN17: Unused.
18	RWX	XFIR_IN18: Unused.
19	RWX	XFIR_IN19: Unused.
20	RWX	XFIR_IN20: Unused.
21:25	RWX	XFIR_IN21: unused.
26	RWX	XFIR_IN26: XSTOP on debug trigger and LOCAL_XSTOP to recoverable.

Register Name	Global Recoverable FIR
Mnemonic	TP.TPCHIP.TPC.RFIR
Address	0000000001040001 (SCOM)
Description	Global recoverable FIR

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop unused.
1	ROX	LFIR_RECOV_ERR: Recoverable error from pervasive unit.
2	ROX	RFIR_IN4: recov from OCC(405 core).
3	ROX	RFIR_IN5: Unused.
4	ROX	RFIR_IN6: Unused.
5	ROX	RFIR_IN7: Unused.
6	ROX	RFIR_IN8: Unused.
7	ROX	RFIR_IN9: Unused.
8	ROX	RFIR_IN10: Unused.
9	ROX	RFIR_IN11: Unused.
10	ROX	RFIR_IN12: Unused.
11	ROX	RFIR_IN13: Unused.
12	ROX	RFIR_IN14: Unused.
13	ROX	RFIR_IN15: Unused.
14	ROX	RFIR_IN16: Unused.
15	ROX	RFIR_IN17: Unused.
16	ROX	RFIR_IN18: Unused.
17	ROX	RFIR_IN19: Unused.
18	ROX	RFIR_IN20: unused.
19:23	ROX	RFIR_IN21: Unused.

Register Name	FIR Mask
Mnemonic	TP.TPCHIP.TPC.FIR_MASK
Address	0000000001040002 (SCOM)
Description	FIR Mask

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR summary bit(any xstop).
1	RW	FIR_MASK_IN1: Mask for XFIR from other chiplets.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: Mask for XFIR from pervasive unit error.
4	RW	FIR_MASK_IN4: Mask for OCC(405 core) RFIR/XFIR.
5	RW	FIR_MASK_IN5: Unused.
6	RW	FIR_MASK_IN6: Unused.
7	RW	FIR_MASK_IN7: Unused.
8	RW	FIR_MASK_IN8: Unused.
9	RW	FIR_MASK_IN9: Unused.
10	RW	FIR_MASK_IN10: Unused.
11	RW	FIR_MASK_IN11: Unused.
12	RW	FIR_MASK_IN12: Unused.
13	RW	FIR_MASK_IN13: Unused.
14	RW	FIR_MASK_IN14: Unused.
15	RW	FIR_MASK_IN15: Unused.
16	RW	FIR_MASK_IN16: Unused.
17	RW	FIR_MASK_IN17: Unused.
18	RW	FIR_MASK_IN18: Unused.
19	RW	FIR_MASK_IN19: Unused.
20	RW	FIR_MASK_IN20: Unused.
21:25	RW	FIR_MASK_IN21: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local XSTOP to recoverable error.

Register Name	Special Attention
Mnemonic	TP.TPCHIP.TPC.SPATTN
Address	0000000001040004 (SCOM) 0000000001040005 (SCOM1) 0000000001040006 (SCOM2)
Description	Special Attention

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Special attention from OCC complex.
1	ROX	NCX	NCX	SPATTN_IN1: Unused special attentions.
2	ROX	NCX	NCX	SPATTN_IN2: Unused special attentions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	ROX	NCX	NCX	SPATTN_IN3: Unused special attentions.
4	ROX	NCX	NCX	SPATTN_IN4: Unused special attentions.
5	ROX	NCX	NCX	SPATTN_IN5: Unused special attentions.
6	ROX	NCX	NCX	SPATTN_IN6: Unused special attentions.
7	ROX	NCX	NCX	SPATTN_IN7: Unused special attentions.
8	ROX	NCX	NCX	SPATTN_IN8: Unused special attentions.
9	ROX	NCX	NCX	SPATTN_IN9: Unused special attentions.

Register Name	Special Attention Mask
Mnemonic	TP.TPCHIP.TPC.SPA_MASK
Address	0000000001040007 (SCOM)
Description	Special Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	Mode Register
Mnemonic	TP.TPCHIP.TPC.EPS.FIR.MODE_REG
Address	0000000001040008 (SCOM)
Description	Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop chip TOD on checkstop (unused in POWER9).
5	RW	MODE_IN5: Stop chip TOD on recoverable (unused in POWER9).
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enable XSTOP on special attention.
9	RW	MODE_IN9: MASK_DIRECT/LOCAL_ERROR.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention
Mnemonic	TP.TPCHIP.TPC.HOSTATTN
Address	0000000001040009 (SCOM)
Description	Host Attention

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host Attention Summary Bit.
1	ROX	HOSTATTN_IN1: Unused.
2	ROX	HOSTATTN_IN2: Unused.
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	Local FIR
Mnemonic	TP.TPCHIP.TPC.LOCAL_FIR
Address	000000000104000A (SCOM) 000000000104000B (SCOM1) 000000000104000C (SCOM2)
Description	Local FIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Local errors from GPIO (PCB error).
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, …).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from thermal (trip error) critical error.
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from thermal (trip error) fatal error.
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Therm VOLTTRIP error.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from debug (error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from trace array (error).
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Local errors from trace array (SCOM error).
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Local errors from ITR (PCBIF ERR(13), FMU ERR(14)).
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Local errors from ITR (PCBIF ERR(13), FMU ERR(14)).
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Local errors from PCB (error).
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Local errors from I2CM (error).
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Local errors from TOD (error).
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Local errors from TOD (error).
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Local errors from TOD (error).
21	RWX	WOX_AND	WOX_OR	FIR_IN21: local errors from PORT2 (error).
22	RWX	WOX_AND	WOX_OR	FIR_IN22: FIR error from SBE.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: FIR error from SBE.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: FIR error from SBE.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: FIR error from SBE.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: FIR error from SBE.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: FIR error from SBE.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: FIR error from SBE.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: FIR error from SBE.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: FIR error from SBE.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: local error from OTP.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: local error from EXT trigger.
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Fast XSTOP FIR error.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: PCB MCAST GRP error.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: PCB Parity error.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: OSC SW FIR error.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: OSC SW FIR error.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Local errors from PIBMEM (ECC error(37). Bad array address error(38)).
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Local errors from PIBMEM (ECC error(37). Bad array address error(38)).
40	RWX	WOX_AND	WOX_OR	FIR_IN40: OTP correctable error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction alert (local XSTOP in another chiplet).

Register Name	Local FIR Mask
Mnemonic	TP.TPCHIP.TPC.EPS.FIR.LOCAL_FIR_MASK
Address	000000000104000D (SCOM) 000000000104000E (SCOM1) 000000000104000F (SCOM2)
Description	Local FIR Mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for LEM error collection vector.

Register Name	Local FIR Action0
Mnemonic	TP.TPCHIP.TPC.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000001040010 (SCOM)
Description	Local FIR Action0

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: ACTION0 mask.

Register Name	Local FIR Action1
Mnemonic	TP.TPCHIP.TPC.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000001040011 (SCOM)
Description	Local FIR Action1

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: Action1 mask.

Register Name	Group XSTOP Mask Register
Mnemonic	TP.TPCHIP.TPC.EPS.FIR.GXSTOP_TRIG_REG
Address	0000000001040013 (SCOM)
Description	Group XSTOP Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for OOB system checkstop Input (0).

Bits	SCOM	Field Mnemonic: Description
6	RW	GXSTP_TRIG_IN6: Mask bit for OOB system checkstop Input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group0 XSTOP Mask Register
Mnemonic	TP.TPCHIP.TPC.EPS.FIR.GXSTOP0_MASK_REG
Address	0000000001040014 (SCOM)
Description	Group0 XSTOP Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP0_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for OOB system checkup input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for OOB system checkup input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group1 XSTOP Mask Register
Mnemonic	TP.TPCHIP.TPC.EPS.FIR.GXSTOP1_MASK_REG
Address	0000000001040015 (SCOM)
Description	Group1 XSTOP Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for OOB system checkstop input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for OOB system checkstop input (1).

Bits	SCOM	Field Mnemonic: Description
7	RW	GXSTP1_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP1_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group2 XSTOP Mask Register
Mnemonic	TP.TPCHIP.TPC.EPS.FIR.GXSTOP2_MASK_REG
Address	0000000001040016 (SCOM)
Description	Group2 XSTOP Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for OOB system checkstop input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for OOB system checkstop input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	Summary Mask Register
Mnemonic	TP.TPCHIP.TPC.EPS.FIR.SUM_MASK_REG
Address	0000000001040017 (SCOM)
Description	Summary Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type4 (host attention summary bit.

Register Name	Local Checkstop
Mnemonic	TP.TPCHIP.TPC.LOCAL_XSTOP_ERR
Address	0000000001040018 (SCOM)
Description	Local Checkstop

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit.
1	ROX	LOCAL_XSTOP_IN1: Unused.
2	ROX	LOCAL_XSTOP_IN2: Unused.
3	ROX	LOCAL_XSTOP_IN3: Unused.
4	ROX	LOCAL_XSTOP_IN4: Unused.
5	ROX	LOCAL_XSTOP_IN5: Unused.
6	ROX	LOCAL_XSTOP_IN6: Unused.
7	ROX	LOCAL_XSTOP_IN7: Unused.
8	ROX	LOCAL_XSTOP_IN8: Unused.
9	ROX	LOCAL_XSTOP_IN9: Unused.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask
Mnemonic	TP.TPCHIP.TPC.LOCAL_XSTOP_MASK
Address	0000000001040019 (SCOM)
Description	Local Checkstop Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask
Mnemonic	TP.TPCHIP.TPC.HOSTATTN_MASK
Address	000000000104001A (SCOM)
Description	Host Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Thermal Sensor Loop1 Results
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.DTS_RESULT0
Address	0000000001050000 (SCOM)
Description	DTS Thermal Sensor Loop1 Results

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.DTS_TRC_RESULT
Address	0000000001050003 (SCOM)
Description	DTS Trace Results

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.

Register Name	CPM and DTS Enables and Controls
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.THERM_MODE_REG
Address	000000000105000F (SCOM)
Description	CPM and DTS Enables and Controls

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: Force TPC_THERM_THRES_MAC clock gating off and activates clocks.
2:4	RW	THERM_THRES_TRIP_ENA: THERM_THRES_TRIP compare enables. 1xx = trip0 - Warning x1x = trip1 - Critical xx1 = trip2 - Fatal

Bits	SCOM	Field Mnemonic: Description
5	RW	THERM_DTS_SAMPLE_ENA: 0 = No DTS sampling 1 = DTS sampling is enabled and below counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is feed into an 18-bit counter, with the THERM_SAMPLE_PULSE_CNT it is possible to select a high-order bit of the counter. To enable a resolutions of sampling DTSS between 2.5 us and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a DTS sample. 0000 = 16 ms. 0001: 8 ms. 0010 = 4 ms. 0011: 2 ms. 0100 = 1 ms. 0101: 0.5 ms. 0110 = 250 us. 0111: 125 us. 1000 = 62.5us. 1001: 31.3 us. 1010 = 15.6 us. 1011: 7.8 us. 1100 = 3.9 us. 1101: 2 us. 1110 = 1 us. 1111: 0.5 us.
10:11	RW	THERM_THRES_MODE_ENA: Forces max or min mode in threshold unit: 00 = Is off. 11 = Is illegal. 10 = Max mode. 01 = Min mode.
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: 0 = THERM_OVERFLOW_ERR will be enabled. 1 = THERM_OVERFLOW_ERR will be disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result will be provided with PCB read ADDR_V(4): 0000 = DTS 0. 0001 = DTS 1. 0010 = DTS 2. 0100 = DTS 4. 1111 = Worst Case Sensor.
20:21	RW	THERM_DTS_ENABLE_L1: loop1 DTS enables: 1x: DTS 0 available. x1: DTS 1 available.
22:34	RO	constant = 0b0000000000000
35:36	RW	Reserved field.

Register Name	Skitter Control Register
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.SKITTER_MODE_REG
Address	0000000001050010 (SCOM)
Description	Skitter Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold current sample.
1	RW	DISABLE_SKITTER_STICKINESS: I 0 = Accumulation mode 1 = Samples new value each cycle and resets sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0 = hold_on_trigger0. bit1: _on_trigger1.
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0 = reset_sticky_on_trigger0. bit1: reset_sticky_on_trigger1.
8:9	RW	SKITTER_SAMPLE_GUTS: Selects guts to measure: 00 = GUTS1. 01 = GUTS2. 10 = GUTS3. 11 = GUTS4.
10:43	RO	constant = 0b00000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold current sample on the DBG trigger. This has highest priority.
45	ROX	SKITTER_DATA_V_LT: If '1', the data that is requested by a skitter force read register has finished, and data is present in skitter data register in the collector macro. The data can be read by any combination of V25/V26/V27 PCB reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.INJECT_REG
Address	0000000001050011 (SCOM)
Description	Error Injection Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00 = no injection. 01: warning trip level injection. 10 = critical trip level injection. 11: fatal trip level injection.
2:3	RW	THERM_INJECT_MODE: 00 = No injection. 01 = Injection on the next DTS sample. 10 = Solid injection for the next DTS samples until bit setting changes. 11 = Not used.

Register Name	Control/Force Reset Register
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.CONTROL_REG
Address	0000000001050012 (SCOM)
Description	Control/Force Reset Register

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved field.
1	WO_1P	Reserved field.
2	WO_1P	Reserved field.

Bits	SCOM	Field Mnemonic: Description
3	WO_1P	Reserved field.
4	WO_1P	Reserved field.
5	WO_1P	Reserved field.
6	WO_1P	Reserved field.
7	WO_1P	Reserved field.
8	WO_1P	Reserved field.
9	WO_1P	Reserved field.
10	WO_1P	Reserved field.
11	WO_1P	Reserved field.
12	WO_1P	Reserved field.

Register Name	Thermal Error Status Register
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.ERR_STATUS_REG
Address	0000000001050013 (SCOM)
Description	Thermal Error Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Therm mode register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter mode register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter force register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan initialized version register parity error mask.
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt mode register parity error mask.

Bits	SCOM	Field Mnemonic: Description
22	RO	constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: Thres state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Force skitter read one hot error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	constant = 0b00000000
40:43	ROX	Reserved field.
44:46	ROX	Reserved field.
47	ROX	Reserved field.
48	ROX	Reserved field.
49:50	ROX	Reserved field.
51:54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Skitter Force Read Register**
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.SKITTER_FORCE_REG
Address	0000000001050014 (SCOM)
Description	Skitter Force Read Register

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter.

Register Name	**Skitter Clock SRC Control Register**
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000001050016 (SCOM)
Description	Skitter Clock SRC Control Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects clock to measure: 000 = Local mesh clock. 001 = External pin SKITTER_C1_1_IN. 010 = Local D1CLK only if D_MODE = 1. 011 = External pin SKITTER_C1_2_IN. 100 = Local LCLK only if D_MODE = 1. 101 = External pin SKITTER_C1_3_IN. 110 = Unused. 111 = External pin SKITTER_C1_4_IN.
3:35	RO	constant = 0b00000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: To select delay to be added between clock source mux and inverter chain (base line delay is 12.2 psec) of SKITTER0. 00 = No delay. 01 = 0.6 psec. 10 = 1.8 psec. 11 = 5 psec.

Register Name	Skitter Data Register Read Bit [0:63]
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.SKITTER_DATA0
Address	0000000001050019 (SCOM)
Description	Skitter Data Register Read Bit 0:63

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bit [32:95]
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.SKITTER_DATA1
Address	000000000105001A (SCOM)
Description	Skitter Data Register Read Bit [32:95]

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bits [6:127]
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.SKITTER_DATA2
Address	000000000105001B (SCOM)
Description	Skitter Data Register Read Bits [6:127]

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Time stamp Counter Read
Mnemonic	TP.TPCHIP.TPC.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000105001C (SCOM)
Description	Timestamp Counter Read

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.

3. TB Chiplet PCB Slave

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TP.TPCHIP.NET.PCBSLPERV.ASSIST_INTERRUPT_REG	0x00000000010F0011	553
TP.TPCHIP.NET.PCBSLPERV.ATOMIC_LOCK_REG	0x00000000010F03FF	561
TP.TPCHIP.NET.PCBSLPERV.ATTN_INTERRUPT_REG	0x00000000010F001A	554
TP.TPCHIP.NET.PCBSLPERV.EDRAM_STATUS	0x00000000010F0029	558
TP.TPCHIP.NET.PCBSLPERV.ERROR_REG	0x00000000010F001F	555
TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_0_REG	0x00000000010F0020	556
TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_1_REG	0x00000000010F0021	557
TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_2_REG	0x00000000010F0022	557
TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_3_REG	0x00000000010F0023	557
TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_4_REG	0x00000000010F0024	557
TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_5_REG	0x00000000010F0025	558
TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_6_REG	0x00000000010F0026	558
TP.TPCHIP.NET.PCBSLPERV.HEARTBEAT_REG	0x00000000010F0018	554
TP.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_1	0x00000000010F0001	552
TP.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_2	0x00000000010F0002	553
TP.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_3	0x00000000010F0003	553
TP.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_4	0x00000000010F0004	553
TP.TPCHIP.NET.PCBSLPERV.NET_CTRL0	0x00000000010F0040	559
TP.TPCHIP.NET.PCBSLPERV.NET_CTRL1	0x00000000010F0044	560
TP.TPCHIP.NET.PCBSLPERV.PLL_LOCK_REG	0x00000000010F0019	554
TP.TPCHIP.NET.PCBSLPERV.PRE_COUNTER_REG	0x00000000010F0028	558
TP.TPCHIP.NET.PCBSLPERV.PRIMARY_ADDRESS_REG	0x00000000010F0000	552
TP.TPCHIP.NET.PCBSLPERV.PROTECT_MODE_REG	0x00000000010F03FE	560
TP.TPCHIP.NET.PCBSLPERV.RECOV_INTERRUPT_REG	0x00000000010F001B	555
TP.TPCHIP.NET.PCBSLPERV.SLAVE_CONFIG_REG	0x00000000010F001E	555
TP.TPCHIP.NET.PCBSLPERV.TIMEOUT_REG	0x00000000010F0010	553
TP.TPCHIP.NET.PCBSLPERV.VITAL_SCAN_OUT	0x00000000010F0017	554
TP.TPCHIP.NET.PCBSLPERV.XSTOP_INTERRUPT_REG	0x00000000010F001C	555
TP.TPCHIP.PIB.PCBMS.BIT_SEL_REG_2	0x00000000000F0008	536
TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.ERROR_STATUS_REG	0x00000000000F0034	552
TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.HOST_MASK_REG	0x00000000000F0033	551
TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT1_REG	0x00000000000F0020	549
TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT2_REG	0x00000000000F0023	549
TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT3_REG	0x00000000000F0026	550
TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT4_REG	0x00000000000F0029	550
TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT_CONF_REG	0x00000000000F002F	551
TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT_HOLD_REG	0x00000000000F0032	551
TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT_TYPE_MASK_REG	0x00000000000F002C	550
TP.TPCHIP.PIB.PCBMS.DEVICE_ID_REG	0x00000000000F000F	536
TP.TPCHIP.PIB.PCBMS.ERROR_REG	0x00000000000F001F	549
TP.TPCHIP.PIB.PCBMS.FIRST_ERR_REG	0x00000000000F001E	548
TP.TPCHIP.PIB.PCBMS.FIRST_REPLY_REG	0x00000000000F0018	547

Mnemonic	Address	Page
TP.TPCHIP.PIB.PCBMS.IGNORE_PAR_REG	0x00000000000F001C	548
TP.TPCHIP.PIB.PCBMS.INTERRUPT_TYPE_REG	0x00000000000F001A	547
TP.TPCHIP.PIB.PCBMS.MCAST_COMP_MASK_REG	0x00000000000F0017	547
TP.TPCHIP.PIB.PCBMS.MCAST_COMP_REG	0x00000000000F0015	546
TP.TPCHIP.PIB.PCBMS.MCAST_COMP_VAL_REG	0x00000000000F0016	547
TP.TPCHIP.PIB.PCBMS.MCAST_GRP_0_SLAVES_REG	0x00000000000F0000	534
TP.TPCHIP.PIB.PCBMS.MCAST_GRP_1_SLAVES_REG	0x00000000000F0001	534
TP.TPCHIP.PIB.PCBMS.MCAST_GRP_2_SLAVES_REG	0x00000000000F0002	535
TP.TPCHIP.PIB.PCBMS.MCAST_GRP_3_SLAVES_REG	0x00000000000F0003	535
TP.TPCHIP.PIB.PCBMS.MCAST_GRP_4_SLAVES_REG	0x00000000000F0004	535
TP.TPCHIP.PIB.PCBMS.MCAST_GRP_5_SLAVES_REG	0x00000000000F0005	535
TP.TPCHIP.PIB.PCBMS.MCAST_GRP_6_SLAVES_REG	0x00000000000F0006	535
TP.TPCHIP.PIB.PCBMS.REC_ACK_REG	0x00000000000F0010	536
TP.TPCHIP.PIB.PCBMS.REC_ERR_REG0	0x00000000000F0011	537
TP.TPCHIP.PIB.PCBMS.REC_ERR_REG1	0x00000000000F0012	539
TP.TPCHIP.PIB.PCBMS.REC_ERR_REG2	0x00000000000F0013	541
TP.TPCHIP.PIB.PCBMS.REC_ERR_REG3	0x00000000000F0014	544
TP.TPCHIP.PIB.PCBMS.RESET_REG	0x00000000000F001D	548
TP.TPCHIP.PIB.PCBMS.TIMEOUT_REG	0x00000000000F0019	547

The POWER9 processor registers are listed in the following tables.

Register Name	**Number of Slaves in Multicast Group 0**
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_GRP_0_SLAVES_REG
Address	00000000000F0000 (SCOM)
Description	This register specifies the number of slaves in multicast group 0.

Bits	**SCOM**	**Field Mnemonic: Description**
0:5	RWX	SLAVES_MCAST_GROUP_0: This field specifies the number of slaves in multicast group 0.

Register Name	**Number of Slaves in Multicast Group 1**
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_GRP_1_SLAVES_REG
Address	00000000000F0001 (SCOM)
Description	This register specifies the number of slaves in multicast group 1.

Bits	**SCOM**	**Field Mnemonic: Description**
0:5	RWX	SLAVES_MCAST_GROUP_1: This field specifies the number of slaves in multicast group 1.

Register Name	Number of Slaves in Multicast Group 2
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_GRP_2_SLAVES_REG
Address	00000000000F0002 (SCOM)
Description	This register specifies the number of slaves in multicast group 2.

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_2: This field specifies the number of slaves in multicast group 2.

Register Name	Number of Slaves in Multicast Group 3
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_GRP_3_SLAVES_REG
Address	00000000000F0003 (SCOM)
Description	This register specifies the number of slaves in multicast group 3.

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_3: This field specifies the number of slaves in multicast group 3.

Register Name	Number of Slaves in Multicast Group 4
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_GRP_4_SLAVES_REG
Address	00000000000F0004 (SCOM)
Description	This register specifies the number of slaves in multicast group 4.

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_4: This field specifies the number of slaves in multicast group 4.

Register Name	Number of Slaves in Multicast Group 5
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_GRP_5_SLAVES_REG
Address	00000000000F0005 (SCOM)
Description	This register specifies the number of slaves in multicast group 5.

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_5: This field specifies the number of slaves in multicast group 5.

Register Name	Number of Slaves in Multicast Group 6
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_GRP_6_SLAVES_REG
Address	00000000000F0006 (SCOM)
Description	This register specifies the number of slaves in multicast group 6.

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_6: This field specifies the number of slaves in multicast group 6.

Register Name	Selects Bit to be Returned by Multicast Read
Mnemonic	TP.TPCHIP.PIB.PCBMS.BIT_SEL_REG_2
Address	00000000000F0008 (SCOM)
Description	This register selects the bit to be returned by a multicast read operation.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	BIT_SELECT_REGISTER_FSP2PIB: This field selects the bit to be returned by the Multicast Read Register. This bit is determined by the PIB master even though the PIB master and multicast Read Register have the same address.

Register Name	Chip
Mnemonic	TP.TPCHIP.PIB.PCBMS.DEVICE_ID_REG
Address	00000000000F000F (SCOM)
Description	ID readout.

Bits	SCOM	Field Mnemonic: Description
0:19	RO	CFAM_CHIPID: This field is also known as cfam_chipid.
20	RO	constant = 0b0
21:31	RO	VENDOR_ID: The IBM ID is 0x49
32:35	RO	constant = 0b0000
36:38	RW	SOCKET_ID: Socket position Socket 0x0 is connected to the primary service element. Socket 0x1 is connected to the secondary service element (high end only).
39	RW	CHIPPOS_ID: DCM position 0 = SCMs or the first chip on the DCM 1 = The second chip on the DCM (always a slave)
40	RO	IO_TP_VSB_CHIP_POS
41:47	RO	constant = 0b0000000
48	ROX	FUSE_NX_ALLOW_CRYPTO: 1 = NX crypto-functionality is enabled (export regulation).
49	ROX	FUSE_VMX_CRYPTO_DIS: 1 = VMX crypto-functionality is disabled (export regulation).
50	ROX	FUSE_FP_THROTTLE_EN: 1 = Floating point is throttled (export regulation).
51	RO	TP_NP_NVLINK_DISABLE: Indicates that NVLink is disabled.
52	RO	FUSE_TOPOLOGY_2CHIP
53:54	RO	FUSE_TOPOLOGY_GROUP
55:63	RO	constant = 0b000000000

Register Name	Slave Response during Multicast Access Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.REC_ACK_REG
Address	00000000000F0010 (SCOM)
Description	This register contains information about the slaves that responded during a multicast access operation.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	RECEIVE_ACKNOWLEDGE_REGISTER: This field contains information about which slave responded during a multicast access operation.

Register Name	Slave Error Response during Multicast Access Register 0
Mnemonic	TP.TPCHIP.PIB.PCBMS.REC_ERR_REG0
Address	00000000000F0011 (SCOM)
Description	This register contains information about which slave responded with an error during a multicast access operation.

Bits	SCOM	Field Mnemonic: Description
0	ROX	MASTER_RESPONSE_BIT: This bit indicates that the PCBMS has responded.
1:3	RWX_WAND	MASTER_ERROR_CODE: This bit specifies the master error code.
4	ROX	SLAVE1_RESPONSE_BIT: This bit indicates that that Slave1 has responded.
5:7	RWX_WAND	SLAVE1_ERROR_CODE: This field indicates the Slave1 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
8	ROX	SLAVE2_RESPONSE_BIT: This bit indicates that Slave2 has responded.
9:11	RWX_WAND	SLAVE2_ERROR_CODE: This field indicates the Slave2 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
12	ROX	SLAVE3_RESPONSE_BIT: This bit indicates that Slave3 has responded.
13:15	RWX_WAND	SLAVE3_ERROR_CODE: This field indicates the Slave3 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
16	ROX	SLAVE4_RESPONSE_BIT: This bit indicates that Slave4 has responded.
17:19	RWX_WAND	SLAVE4_ERROR_CODE: This field indicates the Slave4 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
20	ROX	SLAVE5_RESPONSE_BIT: This bit indicates that Slave5 has responded.
21:23	RWX_WAND	SLAVE5_ERROR_CODE: This field indicates the Slave5 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
24	ROX	SLAVE6_RESPONSE_BIT: This bit indicates that Slave6 has responded.

Bits	SCOM	Field Mnemonic: Description
25:27	RWX_WAND	SLAVE6_ERROR_CODE: This field indicates the Slave6 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
28	ROX	SLAVE7_RESPONSE_BIT: This bit indicates that Slave7 has responded.
29:31	RWX_WAND	SLAVE7_ERROR_CODE: This field indicates the Slave7 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
32	ROX	SLAVE8_RESPONSE_BIT: This bit indicates that Slave8 has responded.
33:35	RWX_WAND	SLAVE8_ERROR_CODE: This field indicates the Slave8 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
36	ROX	SLAVE9_RESPONSE_BIT: This bit indicates that Slave9 has responded.
37:39	RWX_WAND	SLAVE9_ERROR_CODE: This field indicates the Slave9 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
40	ROX	SLAVE10_RESPONSE_BIT: This bit indicates that Slave10 has responded.
41:43	RWX_WAND	SLAVE10_ERROR_CODE: This field indicates the Slave10 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
44	ROX	SLAVE11_RESPONSE_BIT: This bit indicates that Slave11 has responded.
45:47	RWX_WAND	SLAVE11_ERROR_CODE: This field indicates the Slave11 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
48	ROX	SLAVE12_RESPONSE_BIT: This bit indicates that Slave12 has responded.
49:51	RWX_WAND	SLAVE12_ERROR_CODE: This field indicates the Slave12 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
52	ROX	SLAVE13_RESPONSE_BIT: This bit indicates that Slave13 has responded.

Bits	SCOM	Field Mnemonic: Description
53:55	RWX_WAND	SLAVE13_ERROR_CODE: This field indicates the Slave13 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
56	ROX	SLAVE14_RESPONSE_BIT: This bit indicates that Slave14 has responded.
57:59	RWX_WAND	SLAVE14_ERROR_CODE: This field indicates the Slave14 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
60	ROX	SLAVE15_RESPONSE_BIT: This bit indicates that Slave15 has responded.
61:63	RWX_WAND	SLAVE15_ERROR_CODE: This field indicates the Slave15 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout

Register Name	Slave Error Response during Multicast Access Register 1
Mnemonic	TP.TPCHIP.PIB.PCBMS.REC_ERR_REG1
Address	00000000000F0012 (SCOM)
Description	This register contains information about which slave responded with an error during a multicast access operation.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SLAVE16_RESPONSE_BIT: This bit indicates that Slave16 has responded.
1:3	RWX_WAND	SLAVE16_ERROR_CODE: This field indicates the Slave16 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
4	ROX	SLAVE17_RESPONSE_BIT: This bit indicates that Slave17 has responded.
5:7	RWX_WAND	SLAVE17_ERROR_CODE: This field indicates the Slave17 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
8	ROX	SLAVE18_RESPONSE_BIT: This bit indicates that Slave18 has responded.
9:11	RWX_WAND	SLAVE18_ERROR_CODE: This field indicates the Slave18 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
12	ROX	SLAVE19_RESPONSE_BIT: This bit indicates that Slave19 has responded.

Bits	SCOM	Field Mnemonic: Description
13:15	RWX_WAND	SLAVE19_ERROR_CODE: This field indicates the Slave19 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
16	ROX	SLAVE20_RESPONSE_BIT: This bit indicates that Slave20 has responded.
17:19	RWX_WAND	SLAVE20_ERROR_CODE: This field indicates the Slave20 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
20	ROX	SLAVE21_RESPONSE_BIT: This bit indicates that Slave21 has responded.
21:23	RWX_WAND	SLAVE21_ERROR_CODE: This field indicates the Slave21 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
24	ROX	SLAVE22_RESPONSE_BIT: This bit indicates that Slave22 has responded.
25:27	RWX_WAND	SLAVE22_ERROR_CODE: This field indicates the Slave22 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
28	ROX	SLAVE23_RESPONSE_BIT: This bit indicates that Slave23 has responded.
29:31	RWX_WAND	SLAVE23_ERROR_CODE: This field indicates the Slave23 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
32	ROX	SLAVE24_RESPONSE_BIT: This bit indicates that Slave24 has responded.
33:35	RWX_WAND	SLAVE24_ERROR_CODE: This field indicates the Slave24 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
36	ROX	SLAVE25_RESPONSE_BIT: This bit indicates that Slave25 has responded.
37:39	RWX_WAND	SLAVE25_ERROR_CODE: This field indicates the Slave25 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
40	ROX	SLAVE26_RESPONSE_BIT: This bit indicates that Slave26 has responded.

Bits	SCOM	Field Mnemonic: Description
41:43	RWX_WAND	SLAVE26_ERROR_CODE: This field indicates the Slave26 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
44	ROX	SLAVE27_RESPONSE_BIT: This bit indicates that Slave27 has responded.
45:47	RWX_WAND	SLAVE27_ERROR_CODE: This field indicates the Slave27 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
48	ROX	SLAVE28_RESPONSE_BIT: This bit indicates that Slave28 has responded.
49:51	RWX_WAND	SLAVE28_ERROR_CODE: This field indicates the Slave28 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
52	ROX	SLAVE29_RESPONSE_BIT: This bit indicates that Slave29 has responded.
53:55	RWX_WAND	SLAVE29_ERROR_CODE: This field indicates the Slave29 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
56	ROX	SLAVE30_RESPONSE_BIT: This bit indicates that Slave30 has responded.
57:59	RWX_WAND	SLAVE30_ERROR_CODE: This field indicates the Slave30 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
60	ROX	SLAVE31_RESPONSE_BIT: This bit indicates that Slave31 has responded.
61:63	RWX_WAND	SLAVE31_ERROR_CODE: This field indicates the Slave31 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout

Register Name	Slave Error Response during Multicast Access Register 2
Mnemonic	TP.TPCHIP.PIB.PCBMS.REC_ERR_REG2
Address	00000000000F0013 (SCOM)
Description	This register contains information about which slave responded with an error during a multicast access.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SLAVE32_RESPONSE_BIT: This bit indicates that Slave32 has responded.

Bits	SCOM	Field Mnemonic: Description
1:3	RWX_WAND	SLAVE32_ERROR_CODE: This field indicates the Slave32 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
4	ROX	SLAVE33_RESPONSE_BIT: This bit indicates that Slave33 has responded.
5:7	RWX_WAND	SLAVE33_ERROR_CODE: This field indicates the Slave33 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
8	ROX	SLAVE34_RESPONSE_BIT: This bit indicates that Slave34 has responded.
9:11	RWX_WAND	SLAVE34_ERROR_CODE: This field indicates the Slave34 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
12	ROX	SLAVE35_RESPONSE_BIT: This bit indicates that Slave35 has responded.
13:15	RWX_WAND	SLAVE35_ERROR_CODE: This field indicates the Slave35 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
16	ROX	SLAVE36_RESPONSE_BIT: This bit indicates that Slave36 has responded.
17:19	RWX_WAND	SLAVE36_ERROR_CODE: This field indicates the Slave36 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
20	ROX	SLAVE37_RESPONSE_BIT: This bit indicates that Slave37 has responded.
21:23	RWX_WAND	SLAVE37_ERROR_CODE: This field indicates the Slave37 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
24	ROX	SLAVE38_RESPONSE_BIT: This bit indicates that Slave38 has responded.
25:27	RWX_WAND	SLAVE38_ERROR_CODE: This field indicates the Slave38 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
28	ROX	SLAVE39_RESPONSE_BIT: This bit indicates that Slave39 has responded.

Bits	SCOM	Field Mnemonic: Description
29:31	RWX_WAND	SLAVE39_ERROR_CODE: This field indicates the Slave39 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
32	ROX	SLAVE40_RESPONSE_BIT: This bit indicates that Slave40 has responded.
33:35	RWX_WAND	SLAVE40_ERROR_CODE: This field indicates the Slave40 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
36	ROX	SLAVE41_RESPONSE_BIT: This bit indicates that Slave41 has responded.
37:39	RWX_WAND	SLAVE41_ERROR_CODE: This field indicates the Slave41 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
40	ROX	SLAVE42_RESPONSE_BIT: This bit indicates that Slave42 has responded.
41:43	RWX_WAND	SLAVE42_ERROR_CODE: This field indicates the Slave42 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
44	ROX	SLAVE43_RESPONSE_BIT: This bit indicates that Slave43 has responded.
45:47	RWX_WAND	SLAVE43_ERROR_CODE: This field indicates the Slave43 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
48	ROX	SLAVE44_RESPONSE_BIT: This bit indicates that Slave44 has responded.
49:51	RWX_WAND	SLAVE44_ERROR_CODE: This field indicates the Slave44 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
52	ROX	SLAVE45_RESPONSE_BIT: This bit indicates that Slave45 has responded.
53:55	RWX_WAND	SLAVE45_ERROR_CODE: This field indicates the Slave46 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
56	ROX	SLAVE46_RESPONSE_BIT: This bit indicates that Slave46 has responded.

Bits	SCOM	Field Mnemonic: Description
57:59	RWX_WAND	SLAVE46_ERROR_CODE: This field indicates the Slave46 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
60	ROX	SLAVE47_RESPONSE_BIT: This bit indicates that Slave47 has responded.
61:63	RWX_WAND	SLAVE47_ERROR_CODE: This field indicates the Slave47 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout

Register Name	Slave Error Response during Multicast Access Register 3
Mnemonic	TP.TPCHIP.PIB.PCBMS.REC_ERR_REG3
Address	00000000000F0014 (SCOM)
Description	This register contains information about which slave responded with an error during a multicast access operation.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SLAVE48_RESPONSE_BIT: This bit indicates that Slave48 has responded.
1:3	RWX_WAND	SLAVE48_ERROR_CODE: This field indicates the Slave48 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
4	ROX	SLAVE49_RESPONSE_BIT: This bit indicates that Slave49 has responded.
5:7	RWX_WAND	SLAVE49_ERROR_CODE: This field indicates the Slave49 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
8	ROX	SLAVE50_RESPONSE_BIT: This bit indicates that Slave50 has responded.
9:11	RWX_WAND	SLAVE50_ERROR_CODE: This field indicates the Slave50 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
12	ROX	SLAVE51_RESPONSE_BIT: This bit indicates that Slave51 has responded.
13:15	RWX_WAND	SLAVE51_ERROR_CODE: This field indicates the Slave51 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
16	ROX	SLAVE52_RESPONSE_BIT: This bit indicates that Slave52 has responded.

Bits	SCOM	Field Mnemonic: Description
17:19	RWX_WAND	SLAVE52_ERROR_CODE: This field indicates the Slave52 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
20	ROX	SLAVE53_RESPONSE_BIT: This bit indicates that Slave53 has responded.
21:23	RWX_WAND	SLAVE53_ERROR_CODE: This field indicates the Slave53 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
24	ROX	SLAVE54_RESPONSE_BIT: This bit indicates that Slave54 has responded.
25:27	RWX_WAND	SLAVE54_ERROR_CODE: This field indicates the Slave54 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
28	ROX	SLAVE55_RESPONSE_BIT: This bit indicates that Slave55 has responded.
29:31	RWX_WAND	SLAVE55_ERROR_CODE: This field indicates the Slave55 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
32	ROX	SLAVE56_RESPONSE_BIT: This bit indicates that Slave56 has responded.
33:35	RWX_WAND	SLAVE56_ERROR_CODE: This field indicates the Slave56 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
36	ROX	SLAVE57_RESPONSE_BIT: This bit indicates that Slave57 has responded.
37:39	RWX_WAND	SLAVE57_ERROR_CODE: This field indicates the Slave57 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
40	ROX	SLAVE58_RESPONSE_BIT: This bit indicates that Slave58 has responded.
41:43	RWX_WAND	SLAVE58_ERROR_CODE: This field indicates the Slave58 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
44	ROX	SLAVE59_RESPONSE_BIT: This bit indicates that Slave59 has responded.

Bits	SCOM	Field Mnemonic: Description
45:47	RWX_WAND	SLAVE59_ERROR_CODE: This field indicates the Slave59 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
48	ROX	SLAVE60_RESPONSE_BIT: This bit indicates that Slave60 has responded.
49:51	RWX_WAND	SLAVE60_ERROR_CODE: This field indicates the Slave60 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
52	ROX	SLAVE61_RESPONSE_BIT: This bit indicates that Slave61 has responded.
53:55	RWX_WAND	SLAVE61_ERROR_CODE: This field indicates the Slave61 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
56	ROX	SLAVE62_RESPONSE_BIT: This bit indicates that Slave62 has responded.
57:59	RWX_WAND	SLAVE62_ERROR_CODE: This field indicates the Slave62 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout
60	ROX	SLAVE63_RESPONSE_BIT: This bit indicates that Slave63 has responded.
61:63	RWX_WAND	SLAVE63_ERROR_CODE: This field indicates the Slave63 error code. 000 = OK 010 = Chiplet offline 100 = Invalid address 110 = Parity error/unexpected/wrong packet 111 = Timeout

Register Name	Mode Select for Multicast Compare
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_COMP_REG
Address	00000000000F0015 (SCOM)
Description	This register specifies the mode of the multicast compare operation.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MULTICAST_COMPARE_REGISTER: Mode select for multicast compare. 00 = Equal (=) 01 = Less than (<) 10 = Not equal (!=) 11= Greater than or equal to (>=)

Register Name	Multicast Compare Operation Comparison Value
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_COMP_VAL_REG
Address	00000000000F0016 (SCOM)
Description	This register specifies the value to compare against during a multicast compare operation.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MULTICAST_COMPARE_VALUE_REGISTER: This field specifies value to compare against during a multicast compare operation. This value is not replicated per master. There is only a single copy.

Register Name	Multicast Compare Operation Mask Value
Mnemonic	TP.TPCHIP.PIB.PCBMS.MCAST_COMP_MASK_REG
Address	00000000000F0017 (SCOM)
Description	This register specifies the mask value to be used during a multicast compare operation.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MULTICAST_COMPARE_MASK_REGISTER: This field specifies the mask value to be used during a multicast compare operation.

Register Name	First Reply Packet Slave Address
Mnemonic	TP.TPCHIP.PIB.PCBMS.FIRST_REPLY_REG
Address	00000000000F0018 (SCOM)
Description	This register contains the slave address of the first reply packet.

Bits	SCOM	Field Mnemonic: Description
0:5	ROX	FIRST_REPLY_REGISTER: This field contains slave address of the first reply packet.

Register Name	PCB Master Timeout Value
Mnemonic	TP.TPCHIP.PIB.PCBMS.TIMEOUT_REG
Address	00000000000F0019 (SCOM)
Description	This register contains the timeout value for the PCB master.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	TIMEOUT_REGISTER: Contains the timeout value for the PCB master.

Register Name	Interrupt Register for Special Attention, Checkstop, Recoverable Error
Mnemonic	TP.TPCHIP.PIB.PCBMS.INTERRUPT_TYPE_REG
Address	00000000000F001A (SCOM)
Description	This interrupt register specifies if the error is a special attention, checkstop, or recoverable error.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WAND	ATTENTION: Attention.

Bits	SCOM	Field Mnemonic: Description
1	RWX_WAND	RECOVERABLE_ERROR: Recoverable error.
2	RWX_WAND	CHECKSTOP: Checkstop.

Register Name	Ignore Parity Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.IGNORE_PAR_REG
Address	00000000000F001C (SCOM)
Description	If set to 1, accesses to the PCB master are forwarded to the PCB. Also, all interrupts are forwarded to the interrupt controller. If set to 0, accesses with parity errors to the PCB master are not forwarded to the PCB. Interrupt packets with parity errors are not forwarded to the interrupt controller.

Bits	SCOM	Field Mnemonic: Description
0	RW	IGNORE_PARITY_REG: Set to 0 to block accesses with parity errors from the PCB and to ignore interrupt packets with parity error.
1	RW	DISABLE_ECC_CORRECTION: If set, the ECC error correction feature is off.
2	RWX_WCLRPART	ECC_S_BIT_ERROR: Set by hardware on a single-bit ECC error. Cleared on writing.
3	RW	CHKSW_AR012: If set, the AR012 architecture is used.

Register Name	Reset Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.RESET_REG
Address	00000000000F001D (SCOM)
Description	Bit 0 resets all PCB elements outside of the standby domain. Bit 1 resets all endpoints.

Bits	SCOM	Field Mnemonic: Description
0	RW	RESET_PCB: Resets all PCB elements outside of the standby domain.
1	RW	RESET_ENDPOINTS: Unused: Resets all endpoints that are attached to the PCB. The bit is now in the FSI Domain.
2	RW	TIMEOUT_RESET_EN: Enable for autoreset PCB on a PCB timeout.

Register Name	PCB Master Error Register, Contains First Error
Mnemonic	TP.TPCHIP.PIB.PCBMS.FIRST_ERR_REG
Address	00000000000F001E (SCOM)
Description	PCB master error register, contains first error.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	FIRST_TIMEOUT_ACTIVE: Active when the master ran into a timeout.
1	RWX_WCLRREG	FIRST_PARITY_ERR: A parity error on internal FSMs occurred.
2	RWX_WCLRREG	FIRST_BEAT_NUM_ERR: A beat with wrong beat number was received.
3	RWX_WCLRREG	FIRST_BEAT_REC_ERR: An unexpected beat was received.
4	RWX_WCLRREG	FIRST_RECEIVED_ERROR: An error packet was received.
5	RWX_WCLRREG	FIRST_RX_PCB_DATA_P_ERR: A data parity on incoming packet occurred.

Bits	SCOM	Field Mnemonic: Description
6	RWX_WCLRREG	FIRST_PIB_ADDR_P_ERR: A parity error on PIB address occurred.
7	RWX_WCLRREG	FIRST_PIB_DATA_P_ERR: A parity error on PIB data occurred.

Register Name	Internal PCB Master Error Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.ERROR_REG
Address	00000000000F001F (SCOM)
Description	Internal PCB master error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	TIMEOUT_ACTIVE: Active when the master ran into a timeout.
1	RWX_WCLRREG	PARITY_ERR: A parity error on internal FSMs occurred.
2	RWX_WCLRREG	BEAT_NUM_ERR: A beat with a wrong beat number was received.
3	RWX_WCLRREG	BEAT_REC_ERR: An unexpected beat was received.
4	RWX_WCLRREG	RECEIVED_ERROR: An error packet received.
5	RWX_WCLRREG	RX_PCB_DATA_P_ERR: A data parity on and incoming packet occurred.
6	RWX_WCLRREG	PIB_ADDR_P_ERR: A parity error on PIB address occurred.
7	RWX_WCLRREG	PIB_DATA_P_ERR: A parity error on PIB data occurred.

Register Name	Interrupt Presentation Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT1_REG
Address	00000000000F0020 (SCOM) 00000000000F0021 (SCOM1) 00000000000F0022 (SCOM2)
Description	Interrupt presentation register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:55	RWX	WOX_OR	WOX_AND	INTERRUPT1: Interrupt type 1 (gp) for up to 56 chiplets.

Register Name	Interrupt Presentation Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT2_REG
Address	00000000000F0023 (SCOM) 00000000000F0024 (SCOM1) 00000000000F0025 (SCOM2)
Description	Interrupt presentation register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:55	RWX	WOX_OR	WOX_AND	INTERRUPT2: Interrupt type 2 (cc) for up to 56 chiplets.

Register Name	Interrupt Presentation Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT3_REG
Address	00000000000F0026 (SCOM) 00000000000F0027 (SCOM1) 00000000000F0028 (SCOM2)
Description	Interrupt presentation register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:55	RWX	WOX_OR	WOX_AND	INTERRUPT3: Interrupt type 3 (--) for up to 56 chiplets.

Register Name	Interrupt Presentation Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT4_REG
Address	00000000000F0029 (SCOM) 00000000000F002A (SCOM1) 00000000000F002B (SCOM2)
Description	Interrupt presentation register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:55	RWX	WOX_OR	WOX_AND	INTERRUPT4: Interrupt type 4 (--) for up to 56 chiplets.

Register Name	Interrupt Type Mask Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT_TYPE_MASK_REG
Address	00000000000F002C (SCOM) 00000000000F002D (SCOM1) 00000000000F002E (SCOM2)
Description	Interrupt type mask register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_GP: Mask all BIST Done interrupts. 0 = Active 1 = Masked
1	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_CC: Mask all clock state change interrupts. 0 = Active 1 = Masked
2	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_UNUSED2: Mask all clock state change interrupts. 0 = Active 1 = Masked
3	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_UNUSED3: Mask all clock state change interrupts. 0 = Active 1 = Masked

Register Name	Interrupt Configuration Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT_CONF_REG
Address	00000000000F002F (SCOM) 00000000000F0030 (SCOM1) 00000000000F0031 (SCOM2)
Description	This register is used to configure interrupts.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_UNUSED0: Reserved
1:3	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_SEL0: Select for OOB return #0
4	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_UNUSED4: Reserved
5:7	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_SEL1: Select for OOB return #1
8	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_GP: Configuration for BIST Done interrupts 0 = Or 1 = And
9	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_CC: Configuration for clock state change interrupts 0 = Or 1 = And
10	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_UNUSED2: Configuration for clock state change interrupts 0 = Or 1 = And
11	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_UNUSED3: Configuration for clock state change interrupts 0 = Or 1 = And

Register Name	Last interrupt packet received from PCB Master
Mnemonic	TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.INTERRUPT_HOLD_REG
Address	00000000000F0032 (SCOM)
Description	The last interrupt packet was received from the PCB master.

Bits	SCOM	Field Mnemonic: Description
0:25	ROX	INTERRUPT_HOLD: The last interrupt packet received from the PCB master

Register Name	IPOLL Mask Register
Mnemonic	TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.HOST_MASK_REG
Address	00000000000F0033 (SCOM)
Description	This register indicates the mask error type.

Bits	SCOM	Field Mnemonic: Description
0	RW	IPOLL_MASK_0: Mask error type0 for Host/Core/Millicode
1	RW	IPOLL_MASK_1: Mask error type1 for Host/Core/Millicode
2	RW	IPOLL_MASK_2: Mask error type2 for Host/Core/MillicodE
3	RW	IPOLL_MASK_3: Mask error type3 for Host/Core/Millicode

Bits	SCOM	Field Mnemonic: Description
4	RW	IPOLL_MASK_4: Mask error type4 for Host/Core/Millicode
5	RW	IPOLL_MASK_5: Mask interrupt for Host/Core/Millicode
6	RW	ERROR_MASK_0: Mask error type0 for FSP/BMC
7	RW	ERROR_MASK_1: Mask error type1 for FSP/BMC
8	RW	ERROR_MASK_2: Mask error type2 for FSP/BMC
9	RW	ERROR_MASK_3: Mask error type3 for FSP/BMC
10	RW	ERROR_MASK_4: Mask error type4 for FSP/BMC
11	RW	ERROR_MASK_5: Mask interrupt for FSP/BMC

Register Name	**Status of the Errors**
Mnemonic	TP.TPCHIP.PIB.PCBMS.COMP.INTR_COMP.ERROR_STATUS_REG
Address	00000000000F0034 (SCOM)
Description	This register contains the status of the errors.

Bits	SCOM	Field Mnemonic: Description
0:5	ROX	ipoll_err_masked: Status of IPOLL errors
6:11	ROX	fsi_err_masked: Status of FSI errors

Register Name	**Slave Primary Address**
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.PRIMARY_ADDRESS_REG
Address	00000000010F0000 (SCOM)
Description	This register contains the slave primary address.

Bits	SCOM	Field Mnemonic: Description
0:5	RO	Reserved field. (Access type is primary_address).

Register Name	**Multicast Group 1**
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_1
Address	00000000010F0001 (SCOM)
Description	Multicast group 1

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting.

Register Name	Multicast Group 2
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_2
Address	00000000010F0002 (SCOM)
Description	Multicast group 2

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting.

Register Name	Multicast Group 3
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_3
Address	00000000010F0003 (SCOM)
Description	Multicast group 3

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting.

Register Name	Multicast Group 4
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_4
Address	00000000010F0004 (SCOM)
Description	Multicast group 4

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting.

Register Name	Timeout Select Register
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.TIMEOUT_REG
Address	00000000010F0010 (SCOM)
Description	Timeout select register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	Reserved field. (Access type is int_timeout).

Register Name	Assist Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.ASSIST_INTERRUPT_REG
Address	00000000010F0011 (SCOM)
Description	Assist Interrupt Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. Access type is attn.
1	ROX	Reserved field. Access type is recov.
2	ROX	Reserved field. Access type is xstop.

Register Name	Vital Scan Out
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.VITAL_SCAN_OUT
Address	00000000010F0017 (SCOM)
Description	Vital scan out

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.

Register Name	Chiplet Heartbeat Register
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.HEARTBEAT_REG
Address	00000000010F0018 (SCOM)
Description	Chiplet heartbeat register

Bits	SCOM	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: The chiplet heartbeat is not detected.

Register Name	Lock Indications from PLLs
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.PLL_LOCK_REG
Address	00000000010F0019 (SCOM)
Description	Lock indications from PLLs

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field. (Access type is lock).

Register Name	Attn Interrupt
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.ATTN_INTERRUPT_REG
Address	00000000010F001A (SCOM)
Description	Attention interrupt

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is attention).

Register Name	Recov Interrupt
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.RECOV_INTERRUPT_REG
Address	00000000010F001B (SCOM)
Description	Recov interrupt

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is recov).

Register Name	Xstop Interrupt
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.XSTOP_INTERRUPT_REG
Address	00000000010F001C (SCOM)
Description	Xstop interrupt

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is xstop).

Register Name	Slave Configuration Register
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.SLAVE_CONFIG_REG
Address	00000000010F001E (SCOM)
Description	Slave configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check.
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malfunction alert. Switch back to level.
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop.
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses.
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet.
5	RW	CFG_DISABLE_FORCE_TO_ZERO: Disable force to zero for error cases.
6	RW	CFG_PM_DISABLE: Disable power management set/reset interface for net_ctrl registers.
7	RW	CFG_PM_MUX_DISABLE: Disable pm MUX request signal.
8:13	RW	ERROR_MASK: Mask bits for slave error reporting.
14:15	RW	Reserved.

Register Name	Error Capture Register
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.ERROR_REG
Address	00000000010F001F (SCOM)
Description	Error capture register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on PCB bus.

Bits	SCOM	Field Mnemonic: Description
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by chiplet. 000 = No error 001 = XSCOM command blocked from pending errors 010 = Chiplet offline 011 = Partial good 100 = Invalid address/address error/bad access type 101 = Clock error 110 = Parity error/received unexpected packet/wrong packet number 111 = Timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in data buffer.
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in chiplet FSM
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on chiplet interface occurred.
13	RWX_WCLEAR	INFO_ERROR: Parity error on chiplet information lines occurred.
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error occurred
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error in the PCB interface component for the internal endpoint occurred
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that the chiplet is offline.
18	RWX_WCLEAR	EDRAM_SEQUENCE_ERR: An error in the EDRAM power up sequence occurred.
19	RWX_WCLEAR	CTRL_REG_PARITY_ERROR: Control register parity is bad.
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: Address register parity is bad.
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: Timeout select register parity is bad.
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: Slave configuration register parity is bad.
23	RWX_WCLEAR	UNUSED_1:
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: Div register parity is bad.
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: Unlock from chiplet PLL

Register Name	Hang Pulse Generation Register 0
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_0_REG
Address	00000000010F0020 (SCOM)
Description	Hang pulse generation register 0

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0 Time period = 2value * (precounter_reg + 1) / pcb_freq, 34 >= value > 0
6	RW	SUPPRESS_HANG_0: If set to 1, hang pulses are suppressed in the case of an xstop.

Register Name	Hang Pulse Generation Register 1
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_1_REG
Address	00000000010F0021 (SCOM)
Description	Hang pulse generation register 1

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1 Time period = 2value * (precounter_reg + 1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_1: If set to 1, hang pulses are suppressed in the case of an xstop.

Register Name	Hang Pulse Generation Register 2
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_2_REG
Address	00000000010F0022 (SCOM)
Description	Hang pulse generation register 2

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2 Time period = 2value * (precounter_reg + 1) / pcb_freq, 34 > = value > 0
6	RW	SUPPRESS_HANG_2: If set to 1, hang pulses are suppressed in the case of an xstop.

Register Name	Hang Pulse Generation Register 3
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_3_REG
Address	00000000010F0023 (SCOM)
Description	Hang pulse generation register 3

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3 Time period = 2value * (precounter_reg + 1) / pcb_freq, 34 >= value > 0
6	RW	SUPPRESS_HANG_3: If set to 1, hang pulses are suppressed in the case of an xstop.

Register Name	Hang Pulse Generation Register 4
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_4_REG
Address	00000000010F0024 (SCOM)
Description	Hang pulse generation register 4

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4 Time period = 2value * (precounter_reg + 1) / pcb_freq, 34 >= value > 0
6	RW	SUPPRESS_HANG_4: If set to 1, hang pulses are suppressed in the case of an xstop.

Register Name	Hang Pulse Generation Register 5
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_5_REG
Address	00000000010F0025 (SCOM)
Description	This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5 Time period = 2 value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_5: If set to 1, hang pulses are suppressed in the case of an xstop.

Register Name	Hang Pulse Generation Register 6
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.HANG_PULSE_6_REG
Address	00000000010F0026 (SCOM)
Description	Hang pulse generation register 6. This hang counter is used exclusively for the heartbeat generation.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6 Time period = 2 value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_6: If set to 1, hang pulses are suppressed in the case of an xstop.

Register Name	Divider for Hang Counter Clock
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.PRE_COUNTER_REG
Address	00000000010F0028 (SCOM)
Description	Divider for hang counter clock

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0).

Register Name	EDRAM Control Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.EDRAM_STATUS
Address	00000000010F0029 (SCOM)
Description	EDRAM control status register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	EDRAM_STAT: EDRAM control status

Register Name	**NET CTRL0 Register**
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.NET_CTRL0
Address	00000000010F0040 (SCOM) 00000000010F0041 (SCOM1) 00000000010F0042 (SCOM2)
Description	NET CTRL0 Register (N/A in Pervasive Chiplet)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if the chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	CLK_ASYNC_RESET: POWER9 cache chiplet: EQ Skew adjust reset POWER9 core chiplet: Core duty cycle adjust reset POWER9 memory chiplet: Memory glitchless multiplexer async reset
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Test enable for chiplet PLL
4	RWX	RWX_WAND	RWX_WOR	PLL_RESET: Reset for chiplet PLL
5	RWX	RWX_WAND	RWX_WOR	PLL_BYPASS: Enable bypass for chiplet PLL
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain
8	RWX	RWX_WAND	RWX_WOR	VITAL_PHASE: Phase for vital domain
9	RWX	RWX_WAND	RWX_WOR	FLUSH_ALIGN_OVR: Override flush, flush_nto1, align in chiplet to 1
10	RWX	RWX_WAND	RWX_WOR	VITAL_AL: Align for vital domain
11	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic
12	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic
14	RWX	RWX_WAND	RWX_WOR	MPW3: LCB control signal for vital logic
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain
17	RWX	RWX_WAND	RWX_WOR	FLUSH_SCAN_N: Flush scan control
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet
19	RWX	RWX_WAND	RWX_WOR	CPLT_RCTRL: Chiplet receiver enable
20	RWX	RWX_WAND	RWX_WOR	CPLT_DCTRL: Chiplet driver enable
21	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access).
22	RWX	RWX_WAND	RWX_WOR	ADJ_FUNC_CLKSEL: POWER9 cache chiplet: clock select for skew adjust/duty cycle adjust logic POWER9 core chiplet: skew sense to skew adjust fencing
23:24	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access).
25	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, the PCB slave reports ‘Chiplet Offline.’
26	RWX	RWX_WAND	RWX_WOR	LVLTRANS_FENCE: Fence control for level translators
27	RWX	RWX_WAND	RWX_WOR	ARRAY_WRITE_ASSIST_EN: Array write assist
28	RWX	RWX_WAND	RWX_WOR	HTB_INTEST: HTB in-test mode
29	RWX	RWX_WAND	RWX_WOR	HTB_EXTEST: HTB in-test mode

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
30	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access).
31	RWX	RWX_WAND	RWX_WOR	PLLFORCE_OUT_EN: PLL force out enable

Register Name	NET CTRL1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.NET_CTRL1
Address	00000000010F0044 (SCOM) 00000000010F0045 (SCOM1) 00000000010F0046 (SCOM2)
Description	NET CTRL1 Register (N/A in Pervasive Chiplet).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	PLL_CLKIN_SEL: PLL CLKIN select.
1	RWX	RWX_WAND	RWX_WOR	CLK_DCC_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 duty cycle control bypass POWER9 core chiplet: Core duty cycle control bypass POWER9 mem chiplet: Memory duty cycle control bypass
2	RWX	RWX_WAND	RWX_WOR	CLK_PDLY_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 progdly bypass POWER9 core chiplet: Core progdly bypass POWER9 mem chiplet: Memory progdly bypass.
3	RWX	RWX_WAND	RWX_WOR	CLK_DIV_BYPASS_EN: Enable clock div bypass.
4	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX0_SEL: Select for REFCLK mux0
5	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX1_SEL: Select for REFCLK mux1
6	RWX	RWX_WAND	RWX_WOR	PLL_BNDY_BYPASS_EN: Bypass for IOP PLL
7	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access).
8:15	RWX	RWX_WAND	RWX_WOR	DPLL_TEST_SEL: DPLL testout MUXing
16:19	RWX	RWX_WAND	RWX_WOR	SB_STRENGTH: Sector buffer driver strength
20	RWX	RWX_WAND	RWX_WOR	ASYNC_TYPE:
21	RWX	RWX_WAND	RWX_WOR	ASYNC_OBS:
22	RWX	RWX_WAND	RWX_WOR	CPM_CAL_SET: CPM calibrate
23	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET0: POWER9 cache chiplet: L2-0 duty cycle adjust reset
24	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET1: POWER9 cache chiplet: L2-1 duty cycle adjust reset
25	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_EN: Clock pulse mode enable
26:27	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_MODE: Clock pulse mode setting
28:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access).

Register Name	Protect Mode Register
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.PROTECT_MODE_REG
Address	00000000010F03FE (SCOM)
Description	Protect mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.NET.PCBSLPERV.ATOMIC_LOCK_REG
Address	00000000010F03FF (SCOM)
Description	Atomic lock register

Bits	SCOM	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID
5:7	RO	constant = 0b000
8:15	ROX	ATOMIC_ACTIVITY: Atomic lock counter

4. PB Chiplet (Nest Chiplet 0)

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
CAPP0.CXA_TOP.CXA_XPT.XPT_PMULET.PMU_CNTRB_REG	0x0000000002010825	624
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.DEBUG_CONTROL	0x0000000002010811	614
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_ACTION0_REG	0x0000000002010806	607
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_ACTION1_REG	0x0000000002010807	607
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_MASK_REG	0x0000000002010803	605
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_REG	0x0000000002010800	602
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA0	0x0000000002010850	633
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA1	0x0000000002010851	633
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA10	0x000000000201085A	635
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA11	0x000000000201085B	635
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA12	0x000000000201085C	635
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA13	0x000000000201085D	636
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA14	0x000000000201085E	636
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA15	0x000000000201085F	636
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA2	0x0000000002010852	633
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA3	0x0000000002010853	634
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA4	0x0000000002010854	634
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA5	0x0000000002010855	634
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA6	0x0000000002010856	634
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA7	0x0000000002010857	634
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA8	0x0000000002010858	635
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA9	0x0000000002010859	635
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_TIMER	0x0000000002010845	630
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.PMU_CNTRA_CFG	0x0000000002010814	615
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.PMU_CNTRB_CFG	0x0000000002010824	623
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.TLBI_ERROR_REPORT	0x000000000201080D	611
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.XPT_CONTROL	0x000000000201081C	620
CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.XPT_PMU_EVENTS_SEL	0x0000000002010822	622
CAPP0.CXA_TOP.CXA_XPT.XPT_TOD.TFMR	0x0000000002010827	625
CAPP0.CXA_TOP.CXA_XPT.XPT_TOD.TOD_SYNC000	0x0000000002010826	624
CAPP0.CXA_TOP.ERR_RPT_CLR	0x0000000002010813	615
CAPP0.CXA_TOP.XPT_ERROR_REPORT	0x000000000201080C	609
NX.CH4.ADDR_0_HASH_FUNCTION_REG	0x0000000002011141	669
NX.CH4.ADDR_10_HASH_FUNCTION_REG	0x000000000201114B	671
NX.CH4.ADDR_1_HASH_FUNCTION_REG	0x0000000002011142	669
NX.CH4.ADDR_2_HASH_FUNCTION_REG	0x0000000002011143	669
NX.CH4.ADDR_3_HASH_FUNCTION_REG	0x0000000002011144	670
NX.CH4.ADDR_4_HASH_FUNCTION_REG	0x0000000002011145	670
NX.CH4.ADDR_5_HASH_FUNCTION_REG	0x0000000002011146	670
NX.CH4.ADDR_6_HASH_FUNCTION_REG	0x0000000002011147	670
NX.CH4.ADDR_7_HASH_FUNCTION_REG	0x0000000002011148	670
NX.CH4.ADDR_8_HASH_FUNCTION_REG	0x0000000002011149	671
NX.CH4.ADDR_9_HASH_FUNCTION_REG	0x000000000201114A	671
NX.CH4.DATATAG_0_HASH_FUNCTION_REG	0x000000000201114C	671
NX.CH4.DATATAG_1_HASH_FUNCTION_REG	0x000000000201114D	671
NX.CH4.DATATAG_2_HASH_FUNCTION_REG	0x000000000201114E	672
NX.CH4.DATATAG_3_HASH_FUNCTION_REG	0x000000000201114F	672
NX.CH4.DATATAG_4_HASH_FUNCTION_REG	0x0000000002011150	672

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NX.CH4.DATATAG_5_HASH_FUNCTION_REG	0x0000000002011151	672
NX.CH4.GZIP_CONTROL_REG	0x0000000002011140	669
NX.CH4.GZIP_ERRRPT_HOLD_REG	0x0000000002011152	672
NX.DBG.NX_DEBUGMUX_CTRL	0x000000000201110A	667
NX.DBG.NX_DMA_ENG_FIR	0x0000000002011100	664
NX.DBG.NX_DMA_ENG_FIR_ACTION0	0x0000000002011106	666
NX.DBG.NX_DMA_ENG_FIR_ACTION1	0x0000000002011107	667
NX.DBG.NX_DMA_ENG_FIR_MASK	0x0000000002011103	666
NX.DBG.NX_DMA_ENG_FIR_WOF	0x0000000002011108	667
NX.DBG.NX_ERRORINJ_CTRL	0x000000000201110C	668
NX.DBG.NX_TRIGGER_CTRL	0x000000000201110B	667
NX.DMA.DMA_VAS_MMIO_BAR	0x000000000201105E	643
NX.DMA.EFT_MAX_BYTE_CNT	0x0000000002011059	641
NX.DMA.GZIP_MAX_BYTE_CNT	0x000000000201105B	642
NX.DMA.SU_CH0_ABORT_CSB	0x0000000002011043	638
NX.DMA.SU_CH1_ABORT_CSB	0x0000000002011045	638
NX.DMA.SU_CH2_ABORT_CSB	0x0000000002011047	638
NX.DMA.SU_CH3_ABORT_CSB	0x0000000002011049	638
NX.DMA.SU_CH4_ABORT_CSB	0x000000000201104B	639
NX.DMA.SU_CRB_KILL_REQ	0x0000000002011053	639
NX.DMA.SU_DMA_ERROR_REPORT_0	0x0000000002011057	641
NX.DMA.SU_DMA_ERROR_REPORT_1	0x0000000002011058	641
NX.DMA.SU_ENGINE_ENABLE	0x0000000002011041	637
NX.DMA.SU_INBOUND_WRITE_CONTROL	0x0000000002011042	637
NX.DMA.SU_PERFMON_CONTROL_0	0x0000000002011054	639
NX.DMA.SU_PERFMON_CONTROL_1	0x0000000002011055	640
NX.DMA.SU_STATUS	0x0000000002011040	636
NX.DMA.SYM_MAX_BYTE_CNT	0x000000000201105A	641
NX.DMA.WATCHDOG_HANG_TIMERS_CNTL	0x000000000201105C	642
NX.PBI.CQ_WRAP.NXCQ_SCOM.NXCQ_PB_MODE_REG	0x0000000002011095	647
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_ACTION0_REG	0x0000000002011086	645
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_ACTION1_REG	0x0000000002011087	645
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_MASK_REG	0x0000000002011083	644
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_REG	0x0000000002011080	643
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_WOF_REG	0x0000000002011088	645
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_MISC_CONTROL_REG	0x00000000020110A8	651
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_MMIO_BAR	0x000000000201108D	645
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_DEBUG_REG	0x0000000002011090	646
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_ECC_REG	0x0000000002011091	646
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_ERR_RPT_0	0x00000000020110A2	650
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_ERR_RPT_1	0x00000000020110A1	649
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PMU0_CONTROL_REG	0x00000000020110A6	650
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PMU0_COUNTER_REG	0x00000000020110A7	651
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PMU1_CONTROL_REG	0x00000000020110A9	652
NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PMU1_COUNTER_REG	0x00000000020110AA	652
NX.PBI.CQ_WRAP.NX_DEBUG_SNAPSHOT_0	0x00000000020110A4	650
NX.PBI.CQ_WRAP.NX_DEBUG_SNAPSHOT_1	0x00000000020110A5	650
NX.PBI.PBI_RNG.NX_RNG_BYPASS	0x00000000020110E4	663

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NX.PBI.PBI_RNG.NX_RNG_CFG	0x00000000020110E0	661
NX.PBI.PBI_RNG.NX_RNG_RDELAY	0x00000000020110E5	663
NX.PBI.PBI_RNG.NX_RNG_RESET	0x00000000020110E6	663
NX.PBI.PBI_RNG.NX_RNG_ST0	0x00000000020110E1	662
NX.PBI.PBI_RNG.NX_RNG_ST1	0x00000000020110E2	662
NX.PBI.PBI_RNG.NX_RNG_ST2	0x00000000020110E3	662
NX.PBI.PBI_RNG.NX_RNG_ST3	0x00000000020110E8	664
NX.PBI.PBI_SHIM.ERAT_STATUS_CONTROL	0x00000000020110D6	660
NX.PBI.PBI_UMAC.EFT_HI_PRIOR_RCV_FIFO_ASB	0x00000000020110C6	655
NX.PBI.PBI_UMAC.EFT_HI_PRIOR_RCV_FIFO_BAR	0x00000000020110C0	653
NX.PBI.PBI_UMAC.EFT_HI_PRIOR_RCV_FIFO_CNTL	0x00000000020110C3	653
NX.PBI.PBI_UMAC.EFT_LO_PRIOR_RCV_FIFO_ASB	0x00000000020110CF	658
NX.PBI.PBI_UMAC.EFT_LO_PRIOR_RCV_FIFO_BAR	0x00000000020110C9	656
NX.PBI.PBI_UMAC.EFT_LO_PRIOR_RCV_FIFO_CNTL	0x00000000020110CC	657
NX.PBI.PBI_UMAC.GZIP_HI_PRIOR_RCV_FIFO_ASB	0x00000000020110C8	655
NX.PBI.PBI_UMAC.GZIP_HI_PRIOR_RCV_FIFO_BAR	0x00000000020110C2	653
NX.PBI.PBI_UMAC.GZIP_HI_PRIOR_RCV_FIFO_CNTL	0x00000000020110C5	654
NX.PBI.PBI_UMAC.GZIP_LO_PRIOR_RCV_FIFO_ASB	0x00000000020110D1	658
NX.PBI.PBI_UMAC.GZIP_LO_PRIOR_RCV_FIFO_BAR	0x00000000020110CB	656
NX.PBI.PBI_UMAC.GZIP_LO_PRIOR_RCV_FIFO_CNTL	0x00000000020110CE	657
NX.PBI.PBI_UMAC.RNG_FAILED_INT	0x00000000020110E7	664
NX.PBI.PBI_UMAC.SEND_WC_BASE_ADDR	0x00000000020110D2	659
NX.PBI.PBI_UMAC.SU_ERAT_ERROR_RPT	0x00000000020110D7	660
NX.PBI.PBI_UMAC.SU_UMAC_ERROR_RPT	0x00000000020110D3	659
NX.PBI.PBI_UMAC.SU_UMAC_ERROR_RPT1	0x00000000020110D8	661
NX.PBI.PBI_UMAC.SYM_HI_PRIOR_RCV_FIFO_ASB	0x00000000020110C7	655
NX.PBI.PBI_UMAC.SYM_HI_PRIOR_RCV_FIFO_BAR	0x00000000020110C1	653
NX.PBI.PBI_UMAC.SYM_HI_PRIOR_RCV_FIFO_CNTL	0x00000000020110C4	654
NX.PBI.PBI_UMAC.SYM_LO_PRIOR_RCV_FIFO_ASB	0x00000000020110D0	658
NX.PBI.PBI_UMAC.SYM_LO_PRIOR_RCV_FIFO_BAR	0x00000000020110CA	656
NX.PBI.PBI_UMAC.SYM_LO_PRIOR_RCV_FIFO_CNTL	0x00000000020110CD	657
NX.PBI.PBI_UMAC.UMAC_STATUS_CONTROL	0x00000000020110D5	660
NX.PBI.PBI_UMAC.VAS_MMIO_BASE_ADDR	0x00000000020110D4	659
TP.TCN0.N0.BIST	0x0000000002030008	682
TP.TCN0.N0.CC_ATOMIC_LOCK_REG	0x00000000020303FF	690
TP.TCN0.N0.CC_PROTECT_MODE_REG	0x00000000020303FE	690
TP.TCN0.N0.CLK_REGION	0x0000000002030006	678
TP.TCN0.N0.CLOCK_STAT_ARY	0x0000000002030000	681
TP.TCN0.N0.CLOCK_STAT_NSL	0x0000000002030009	679
TP.TCN0.N0.CLOCK_STAT_SL	0x0000000002030008	679
TP.TCN0.N0.CPLT_CONF0	0x0000000002000008	571
TP.TCN0.N0.CPLT_CONF1	0x0000000002000009	572
TP.TCN0.N0.CPLT_CTRL0	0x0000000002000000	568
TP.TCN0.N0.CPLT_CTRL1	0x0000000002000001	570
TP.TCN0.N0.CPLT_MASK0	0x0000000002000101	574
TP.TCN0.N0.CPLT_STAT0	0x0000000002000100	573
TP.TCN0.N0.CTRL_ATOMIC_LOCK_REG	0x00000000020003FF	574
TP.TCN0.N0.CTRL_PROTECT_MODE_REG	0x00000000020003FE	574

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TP.TCN0.N0.DBG_CBS_CC	0x0000000002030013	689
TP.TCN0.N0.EPS.DBG.DBG_INST1_COND_REG_1	0x00000000020107C1	590
TP.TCN0.N0.EPS.DBG.DBG_INST1_COND_REG_2	0x00000000020107C2	593
TP.TCN0.N0.EPS.DBG.DBG_INST1_COND_REG_3	0x00000000020107C3	594
TP.TCN0.N0.EPS.DBG.DBG_INST2_COND_REG_1	0x00000000020107C4	594
TP.TCN0.N0.EPS.DBG.DBG_INST2_COND_REG_2	0x00000000020107C5	596
TP.TCN0.N0.EPS.DBG.DBG_INST2_COND_REG_3	0x00000000020107C6	597
TP.TCN0.N0.EPS.DBG.DBG_MODE_REG	0x00000000020107C0	589
TP.TCN0.N0.EPS.DBG.DBG_TRACE_MODE_REG_2	0x00000000020107CF	601
TP.TCN0.N0.EPS.DBG.DBG_TRACE_REG_0	0x00000000020107CD	598
TP.TCN0.N0.EPS.DBG.DBG_TRACE_REG_1	0x00000000020107CE	599
TP.TCN0.N0.EPS.DBG.DEBUG_TRACE_CONTROL	0x00000000020107D0	602
TP.TCN0.N0.EPS.DBG.XTRA_TRACE_MODE	0x00000000020107D1	602
TP.TCN0.N0.EPS.FIR.GXSTOP0_MASK_REG	0x0000000002040014	698
TP.TCN0.N0.EPS.FIR.GXSTOP1_MASK_REG	0x0000000002040015	699
TP.TCN0.N0.EPS.FIR.GXSTOP2_MASK_REG	0x0000000002040016	699
TP.TCN0.N0.EPS.FIR.GXSTOP_TRIG_REG	0x0000000002040013	698
TP.TCN0.N0.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000002040010	697
TP.TCN0.N0.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000002040011	697
TP.TCN0.N0.EPS.FIR.LOCAL_FIR_MASK	0x000000000204000D	697
TP.TCN0.N0.EPS.FIR.MODE_REG	0x0000000002040008	694
TP.TCN0.N0.EPS.FIR.SUM_MASK_REG	0x0000000002040017	700
TP.TCN0.N0.EPS.PSC.PSC.ADDR_TRAP_REG	0x0000000002010003	577
TP.TCN0.N0.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG	0x0000000002010007	578
TP.TCN0.N0.EPS.PSC.PSC.PSCOM_ERROR_MASK	0x0000000002010002	576
TP.TCN0.N0.EPS.PSC.PSC.PSCOM_MODE_REG	0x0000000002010000	574
TP.TCN0.N0.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG	0x0000000002010001	575
TP.TCN0.N0.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG	0x0000000002010008	578
TP.TCN0.N0.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG	0x0000000002010005	577
TP.TCN0.N0.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG	0x0000000002010006	578
TP.TCN0.N0.EPS.THERM.CONTROL_REG	0x0000000002050012	704
TP.TCN0.N0.EPS.THERM.DTS_RESULT0	0x0000000002050000	701
TP.TCN0.N0.EPS.THERM.DTS_TRC_RESULT	0x0000000002050003	701
TP.TCN0.N0.EPS.THERM.ERR_STATUS_REG	0x0000000002050013	704
TP.TCN0.N0.EPS.THERM.INJECT_REG	0x0000000002050011	703
TP.TCN0.N0.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000002050016	706
TP.TCN0.N0.EPS.THERM.SKITTER_DATA0	0x0000000002050019	706
TP.TCN0.N0.EPS.THERM.SKITTER_DATA1	0x000000000205001A	706
TP.TCN0.N0.EPS.THERM.SKITTER_DATA2	0x000000000205001B	706
TP.TCN0.N0.EPS.THERM.SKITTER_FORCE_REG	0x0000000002050014	705
TP.TCN0.N0.EPS.THERM.SKITTER_MODE_REG	0x0000000002050010	703
TP.TCN0.N0.EPS.THERM.THERM_MODE_REG	0x000000000205000F	702
TP.TCN0.N0.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000205001C	707
TP.TCN0.N0.ERROR_STATUS	0x000000000203000F	686
TP.TCN0.N0.FIR_MASK	0x0000000002040002	692
TP.TCN0.N0.HOSTATTN	0x0000000002040009	695
TP.TCN0.N0.HOSTATTN_MASK	0x000000000204001A	701
TP.TCN0.N0.LOCAL_FIR	0x000000000204000A	696

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TP.TCN0.N0.LOCAL_XSTOP_ERR	0x0000000002040018	700
TP.TCN0.N0.LOCAL_XSTOP_MASK	0x0000000002040019	701
TP.TCN0.N0.OPCG_ALIGN	0x0000000002030001	673
TP.TCN0.N0.OPCG_CAPT1	0x0000000002030010	687
TP.TCN0.N0.OPCG_CAPT2	0x0000000002030011	688
TP.TCN0.N0.OPCG_CAPT3	0x0000000002030012	688
TP.TCN0.N0.OPCG_REG0	0x0000000002030002	675
TP.TCN0.N0.OPCG_REG1	0x0000000002030003	676
TP.TCN0.N0.OPCG_REG2	0x0000000002030004	676
TP.TCN0.N0.RFIR	0x0000000002040001	692
TP.TCN0.N0.SCAN_REGION_TYPE	0x0000000002030005	677
TP.TCN0.N0.SPATTN	0x0000000002040004	694
TP.TCN0.N0.SPA_MASK	0x0000000002040007	694
TP.TCN0.N0.SYNC_CONFIG	0x0000000002030000	673
TP.TCN0.N0.TRA0.TR0.TRACE_HI_DATA_REG	0x0000000002010400	578
TP.TCN0.N0.TRA0.TR0.TRACE_LO_DATA_REG	0x0000000002010401	578
TP.TCN0.N0.TRA0.TR0.TRACE_TRCTRL_CONFIG	0x0000000002010402	579
TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x0000000002010403	579
TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x0000000002010404	579
TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_2	0x0000000002010405	580
TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x0000000002010406	580
TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x0000000002010407	580
TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x0000000002010408	580
TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x0000000002010409	581
TP.TCN0.N0.TRA0.TR1.TRACE_HI_DATA_REG	0x0000000002010440	582
TP.TCN0.N0.TRA0.TR1.TRACE_LO_DATA_REG	0x0000000002010441	582
TP.TCN0.N0.TRA0.TR1.TRACE_TRCTRL_CONFIG	0x0000000002010442	582
TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_0	0x0000000002010443	583
TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_1	0x0000000002010444	583
TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_2	0x0000000002010445	583
TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_3	0x0000000002010446	583
TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_4	0x0000000002010447	584
TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_5	0x0000000002010448	584
TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_9	0x0000000002010449	584
TP.TCN0.N0.TRA1.TR0.TRACE_HI_DATA_REG	0x0000000002010480	585
TP.TCN0.N0.TRA1.TR0.TRACE_LO_DATA_REG	0x0000000002010481	586
TP.TCN0.N0.TRA1.TR0.TRACE_TRCTRL_CONFIG	0x0000000002010482	586
TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_0	0x0000000002010483	586
TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_1	0x0000000002010484	587
TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_2	0x0000000002010485	587
TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_3	0x0000000002010486	587
TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_4	0x0000000002010487	587
TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_5	0x0000000002010488	588
TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_9	0x0000000002010489	588
TP.TCN0.N0.XFIR	0x0000000002040000	690
TP.TCN0.N0.XSTOP1	0x000000000203000C	683
TP.TCN0.N0.XSTOP2	0x000000000203000D	684
TP.TCN0.N0.XSTOP3	0x000000000203000E	685

The POWER9 processor registers are listed in the following tables.

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Register Name	Chiplet Control Register 0
Mnemonic	TP.TCN0.N0.CPLT_CTRL0
Address	0000000002000000 (SCOM) 0000000002000010 (SCOM1) 0000000002000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select the ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks are used from a chiplet with ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the synchronous clock for asynchronous latches. (The initial value is 1.)
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode. (The initial value is 1.)
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force an alignment signal to be sent. (The initial value is 1. Drop before dropping flushmode_inh.)
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set the array into write through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: AVP mode. Switches from refresh pulse to phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC:
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC:
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode. For example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of N1L latches. Prevent lock when switching SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC:
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO select.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INT mode for BSC.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Enables delaying the alignment by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into flush state. For DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select. 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM program mode.
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only. Sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. LBIST is controlled by Pin, not by OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	Chiplet Control Register 1
Mnemonic	TP.TCN0.N0.CPLT_CTRL1
Address	0000000002000001 (SCOM) 0000000002000011 (SCOM1) 0000000002000021 (SCOM2)
Description	This register contains the second set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL fence. Protect the VITL region logic from pollution by other regions during LBIST, or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for the pervasive region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for region NX.
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for regions CXA0 - CAPP.
7	RW	WO_OR	WO_CLEAR	TC_REGION3_FENCE: Fence for regions PBIOE0 - PB.
8	RW	WO_OR	WO_CLEAR	TC_REGION4_FENCE: Fence for regions PBIOE1 - PB .
9	RW	WO_OR	WO_CLEAR	TC_REGION5_FENCE: Fence for regions PBIOE2 - PB.
10	RW	WO_OR	WO_CLEAR	UNUSED_10B: Unused.
11	RW	WO_OR	WO_CLEAR	UNUSED_11B: Unused.
12	RW	WO_OR	WO_CLEAR	UNUSED_12B: Unused.
13	RW	WO_OR	WO_CLEAR	UNUSED_13B: Unused.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.
15	RW	WO_OR	WO_CLEAR	RESERVED: Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE:
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	UNUSED_20B: Unused.
21	RW	WO_OR	WO_CLEAR	UNUSED_21B: Unused.
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	Chiplet Configuration Register 0
Mnemonic	TP.TCN0.N0.CPLT_CONF0
Address	0000000002000008 (SCOM) 0000000002000018 (SCOM1) 0000000002000028 (SCOM2)
Description	This register contains the first set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 select.
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 select.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 select.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: ABIST overflow/failure indication select.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection. Enables the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from CC or CPLT_CTRL.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in CC, which are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: System ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	**Chiplet Configuration Register 1**
Mnemonic	TP.TCN0.N0.CPLT_CONF1
Address	0000000002000009 (SCOM) 0000000002000019 (SCOM1) 0000000002000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0D: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1D: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2D: Unused.
3	RW	WO_OR	WO_CLEAR	UNUSED_3D: Unused.
4	RW	WO_OR	WO_CLEAR	IOVALID_4D:
5	RW	WO_OR	WO_CLEAR	IOVALID_5D:
6	RW	WO_OR	WO_CLEAR	IOVALID_6D:
7	RW	WO_OR	WO_CLEAR	IOVALID_7D:
8	RW	WO_OR	WO_CLEAR	IOVALID_8D:
9	RW	WO_OR	WO_CLEAR	IOVALID_9D:
10	RW	WO_OR	WO_CLEAR	IOVALID_10D:
11	RW	WO_OR	WO_CLEAR	IOVALID_11D:
12	RW	WO_OR	WO_CLEAR	FREE_USAGE_12D: Free usage.
13	RW	WO_OR	WO_CLEAR	FREE_USAGE_13D: Free usage.
14	RW	WO_OR	WO_CLEAR	FREE_USAGE_14D: Free usage.
15	RW	WO_OR	WO_CLEAR	FREE_USAGE_15D: Free usage.
16	RW	WO_OR	WO_CLEAR	FREE_USAGE_16D: Free usage.
17	RW	WO_OR	WO_CLEAR	FREE_USAGE_17D: Free usage.
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	**Chiplet Status Register**
Mnemonic	TP.TCN0.N0.CPLT_STAT0
Address	0000000002000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask Register. A mask only masks the interrupt, *not* the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM and EDRAM ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic output port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic output port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done for LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that the chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	FREE_USAGE_12E: Free usage.
13	ROX	FREE_USAGE_13E: Free usage.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.
16	ROX	FREE_USAGE_16E: Free usage.
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.

Bits	SCOM	Field Mnemonic: Description
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	Chiplet Mask Register
Mnemonic	TP.TCN0.N0.CPLT_MASK0
Address	0000000002000101 (SCOM)
Description	This register masks the interrupt on a bit change of the Chiplet Status Register. It does *not* mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: This field provides bitwise masking of the Chiplet Status Register.

Register Name	Control Protect Mode Register
Mnemonic	TP.TCN0.N0.CTRL_PROTECT_MODE_REG
Address	00000000020003FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: This bit enables read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: This bit enables write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCN0.N0.CTRL_ATOMIC_LOCK_REG
Address	00000000020003FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: This bit enables an atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: This field contains the atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: This field is an atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCN0.N0.EPS.PSC.PSC.PSCOM_MODE_REG
Address	0000000002010000 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on a PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on a PCB write data parity error.
2	RW	UNUSED_2B. Unused.

Bits	SCOM	Field Mnemonic: Description
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on a DL return write data parity error.
4	RW	WATCHDOG_ENABLE: Watchdog enable.
5:6	RW	SCOM_HANG_LIMIT: 0b11 = 256 0b10 = 512 0b01 = 768 0b00 = 1023
7	RW	FORCE_ALL_RINGS: This bit is set to a logical 1 if all rings must be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on statevec parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCN0.N0.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000002010001 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on p2s machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.

Bits	SCOM	Field Mnemonic: Description
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on p2s machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	PSCOMLE Error Mask Register
Mnemonic	TP.TCN0.N0.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	0000000002010002 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on the interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on the p2s machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting or ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.

Bits	SCOM	Field Mnemonic: Description
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCN0.N0.EPS.PSC.PSC.ADDR_TRAP_REG
Address	0000000002010003 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: This field contains the PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write, of the last transaction with an error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: Reserved 0.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2 parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit. This bit is set to 1 if no parity error is detected in the satellite number or acknowledgment bits.
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: This bit is set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: This bit is set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: This bit is set if an invalid register address is detected by the satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TCN0.N0.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	0000000002010005 (SCOM)
Description	This register enables the ring lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon write to specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	Write Protect Rings Register
Mnemonic	TP.TCN0.N0.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	0000000002010006 (SCOM)
Description	This register writes ring protect bit maps.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Writes a protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TCN0.N0.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	0000000002010007 (SCOM)
Description	This register provides a bit mask for atomic locking.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: This field provides a bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TCN0.N0.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	0000000002010008 (SCOM)
Description	This register provides a bit mask for ring fencing.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: This field provides a bit mask for ring fencing on a ring-by-ring basis.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000002010400 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000002010401 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.

Bits	SCOM	Field Mnemonic: Description
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address pointing to the last entry.

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000002010402 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when trace run.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: Enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000002010403 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0:63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000002010404 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64:87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000002010405 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000002010406 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000002010407 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000002010408 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN0.N0.TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000002010409 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression. Stores data every cycle.
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.

Bits	SCOM	Field Mnemonic: Description
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: DD1 workaround. Stretches the trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_HI_DATA_REG
Address	0000000002010440 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_LO_DATA_REG
Address	0000000002010441 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address pointing to last entry.

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_TRCTRL_CONFIG
Address	0000000002010442 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables ab unconditional forced write when trace is run.

Bits	SCOM	Field Mnemonic: Description
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: Enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000002010443 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000002010444 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000002010445 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0-23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000002010446 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000002010447 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000002010448 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN0.N0.TRA0.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000002010449 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression (stores data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.

Bits	SCOM	Field Mnemonic: Description
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field

Register Name	**Trace Array High Data Register**
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_HI_DATA_REG
Address	0000000002010480 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_LO_DATA_REG
Address	0000000002010481 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_TRCTRL_CONFIG
Address	0000000002010482 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000002010483 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000002010484 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000002010485 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000002010486 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000002010487 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000002010488 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN0.N0.TRA1.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000002010489 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression (stores data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.

Bits	SCOM	Field Mnemonic: Description
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field

Register Name	Debug Mode Register
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_MODE_REG
Address	00000000020107C0 (SCOM)
Description	This register is the debug macro configuration register 0 for the configuration component.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: Global broadcast mode (0 - 2): 100 = dbg_trace_run and dbg_trace_freeze 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze 110 = dbg_triggers_out(0 to 1) 111 = pc_tcdbg_triggers(0 to 1) (from core)
3:5	RW	TRACE_SEL_MODE: Select source for trace_run and bank: 001 = core trace run and bank 010 = tp broadcast run and 0 011 = tc_dbg_inter_brcst latched 100 = tc_dbg_dbg_sync_brcst_rcv else: dbg_trace_run and dbg_trace_bank
6:7	RW	TRIG_SEL_MODE: Select source for tcdbg_trigger(0): 10 = global broadcast 11 = pc_tcdbg_trigger (from core) else: dbg_triggers_out(0:1)
8	RW	STOP_ON_XSTOP_SELECTION: This bit enables a trace stop on a checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: This bit enables a trace stop on a recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: This bit enables a trace stop on special attention.

Bits	SCOM	Field Mnemonic: Description
11	RW	FREEZE_SEL_MODE: Select freeze source: 0 = local debug freeze 1 = via broadcast: tp_tcdbg_glb_brcst(1)
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode; currently unused because obsolete. See trace_sel_mode.
14	RO	constant = 0b0 sync_brcst_mode
15	RO	constant = 0b0
16:31	ROX	DBG_STATUS: Debug status.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000020107C1 (SCOM)
Description	This register is the debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0): 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst1_dbg_cond1 003 select inst1_dbg_cond2 004 select inst1_dbg_cond3 005 select inst1_dbg_cond2timeout 006 select inst2_dbg_cond1 007 select inst2_dbg_cond2 008 select inst2_dbg_cond3 009 select inst2_dbg_cond2timeout 010 select inst3_dbg_cond1 - unused, tied down 011 select inst3_dbg_cond2 - unused, tied down 012 select inst3_dbg_cond3 - unused, tied down 013 select inst3_dbg_cond2timeout - unused, tied down 014 select inst4_dbg_cond1 - unused, tied down 015 select inst4_dbg_cond2 - unused, tied down 016 select inst4_dbg_cond3 - unused, tied down 017 select inst4_dbg_cond2timeout - unused, tied down 018 select inst1_dbg_trig_sp 019 select inst2_dbg_trig_sp 020 select inst3_dbg_trig_sp - unused, tied down 021 select inst4_dbg_trig_sp - unused, tied down 022 select tctrc_tcdbg_trigger_a(0) 023 select tctrc_tcdbg_trigger_b(0) 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0) 025 select tctrc_tcdbg_trigger_a(1) 026 select tctrc_tcdbg_trigger_b(1) 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1) 028 select tctrc_tcdbg_trigger_a(2) 029 select tctrc_tcdbg_trigger_b(2) 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2) 031 select tctrc_tcdbg_trigger_a(3) 032 select tctrc_tcdbg_trigger_b(3) 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3)

Bits	SCOM	Field Mnemonic: Description
		034 select tctrc_tcdbg_trigger_a(4) 035 select tctrc_tcdbg_trigger_b(4) 036 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4) 037 select tctrc_tcdbg_trigger_a(5) 038 select tctrc_tcdbg_trigger_b(5) 039 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5) 040 select tctrc_tcdbg_trigger_a(6) 041 select tctrc_tcdbg_trigger_b(6) 042 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6) 043 select tctrc_tcdbg_trigger_a(7) 044 select tctrc_tcdbg_trigger_b(7) 045 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7) 046 select tctrc_tcdbg_trigger_a(8) 047 select tctrc_tcdbg_trigger_b(8) 048 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8) 049 select tctrc_tcdbg_trigger_a(9) 050 select tctrc_tcdbg_trigger_b(9) 051 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9) 052 select tctrc_tcdbg_trigger_a(10) 053 select tctrc_tcdbg_trigger_b(10) 054 select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10) 055 select tctrc_tcdbg_trigger_a(11) 056 select tctrc_tcdbg_trigger_b(11) 057 select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11) 058 select tctrc_tcdbg_trigger_a(12) 059 select tctrc_tcdbg_trigger_b(12) 060 select tctrc_tcdbg_trigger_a(12) and tctrc_tcdbg_trigger_b(12) 061 select tctrc_tcdbg_trigger_a(13) 062 select tctrc_tcdbg_trigger_b(13) 063 select tctrc_tcdbg_trigger_a(13) and tctrc_tcdbg_trigger_b(13) 064 select tctrc_tcdbg_trigger_a(14) 065 select tctrc_tcdbg_trigger_b(14) 066 select tctrc_tcdbg_trigger_a(14) and tctrc_tcdbg_trigger_b(14) 067 select tctrc_tcdbg_trigger_a(15) 068 select tctrc_tcdbg_trigger_b(15) 069 select tctrc_tcdbg_trigger_a(15) and tctrc_tcdbg_trigger_b(15) 070 select tctrc_tcdbg_trigger_a(16) 071 select tctrc_tcdbg_trigger_b(16) 072 select tctrc_tcdbg_trigger_a(16) and tctrc_tcdbg_trigger_b(16) 073 select tctrc_tcdbg_trigger_a(17) 074 select tctrc_tcdbg_trigger_b(17) 075 select tctrc_tcdbg_trigger_a(17) and tctrc_tcdbg_trigger_b(17) -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 local core checkstop, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare 076 select logic_trigger_in(0) 077 select logic_trigger_in(1) 078 select logic_trigger_in(2) 079 select logic_trigger_in(3) 080 select logic_trigger_in(4) 081 select logic_trigger_in(5) 082 select logic_trigger_in(6) 083 select logic_trigger_in(7) 084 select logic_trigger_in(8) 085 select logic_trigger_in(9) 086 select logic_trigger_in(10) 087 select logic_trigger_in(11) 088 select logic_trigger_in(12) 089 select logic_trigger_in(13) 090 select logic_trigger_in(14) 091 select logic_trigger_in(15)

Bits	SCOM	Field Mnemonic: Description
		092 select pc_tcdbg_trigger(0) 093 select pc_tcdbg_trigger(1) 094 select tctrc_tcdbg_glb_brcst(0) 095 select tctrc_tcdbg_glb_brcst(1) 096 select xstop_err 097 select recov_err 098 select spattn 099 select fir_dbg_local_xstop_err 100 select tc_dbg_inter_brcst(0) 101 select tc_dbg_inter_brcst(1) -- CORE TRIGGERS (EP chip only) -- **Note**: set core_slave_mode to honor ec[0:5]_tc_trace_run 102 select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0) 103 select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1) 104 select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0) 105 select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1) 106 select glb_trig_or_trace_in(0) 107 select glb_trig_or_trace_in(1) 108 select core_local_brcst_trc(0) 109 select core_local_brcst_trc(1) 110 select glb_freeze_brcst_rec(0) 111 select trig_2_extern_in(0) 112 select trig_2_extern_in(1) 113 select dbg_triggers_out(2) 114 select dbg_triggers_out(3) 115 select dbg_triggers_out(4) 116 select dbg_triggers_out(5) 117 select dbg_triggers_out(6) 118 select tcdbg_trigger_in(0) 119 select tcdbg_trigger_in(1)
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Front-end instance 1, counter 1 in-a-row mode.
33	RW	INST1_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST1_UNUSED_1: Unused.
39	RW	INST1_C2_INAROW_MODE: Front-end instance 1, counter 2 in-a-row mode.
40	RW	INST1_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST1_UNUSED_2: Unused
46	RW	INST1_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST1_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST1_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST1_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.

Bits	SCOM	Field Mnemonic: Description
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: Instance 1 condition 1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: Instance 1 condition 2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front-end instance 1: reset condition 3 for reset_c3_on_c0: 0b100 = dbg_cross_couple_triggers(4) 0b101 = dbg_cross_couple_triggers(12) 0b110 = dbg_cross_couple_triggers(20) 0b111 = dbg_cross_couple_triggers(28)

Register Name	Debug Instance 1 Condition 2 Register
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_INST1_COND_REG_2
Address	00000000020107C2 (SCOM)
Description	This is debug macro configuration register 2 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same of all selectors: 00000 - Selects inst1_cond1_trig_a. 00001 - Selects inst1_cond1_trig_b. 00010 - Selects inst1_cond2_trig_a. 00011 - Selects inst1_cond2_trig_b. 00100 - Selects inst1_condition1. 00101 - Selects inst1_condition2. 00110 - Selects inst1_condition3. 00111 - Selects inst1_cond2_timeout. 01000 - Selects inst2_cond1_trig_a. 01001 - Selects inst2_cond1_trig_b. 01010 - Selects inst2_cond2_trig_a. 01011 - Selects inst2_cond2_trig_b. 01100 - Selects inst2_condition1. 01101 - Selects inst2_condition2. 01110 - Selects inst2_condition3. 01111 - Selects inst2_cond2_timeout. 10000 - Selects inst3_cond1_trig_a. 10001 - Selects inst3_cond1_trig_b. 10010 - Selects inst3_cond2_trig_a. 10011 - Selects inst3_cond2_trig_b. 10100 - Selects inst3_condition1. 10101 - Selects inst3_condition2. 10110 - Selects inst3_condition3. 10111 - Selects inst3_cond2_timeout. 11000 - Selects inst4_cond1_trig_a. 11001 - Selects inst4_cond1_trig_b. 11010 - Selects inst4_cond2_trig_a. 11011 - Selects inst4_cond2_trig_b. 11100 - Selects inst4_condition1. 11101 - Selects inst4_condition2. 11110 - Selects inst4_condition3. 11111 - Selects inst4_cond2_timeout.
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: Instance 1 cross couple select 1 b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: Instance 1 cross couple select 2 a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: Instance 1 cross couple select 2 b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.

Bits	SCOM	Field Mnemonic: Description
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate to compare without an actual compare.

Register Name	Debug Instance 1 Condition 3 Register
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_INST1_COND_REG_3
Address	00000000020107C3 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to compare the value for dbg_cond_comp_1.

Register Name	Debug Instance 2 Condition 1 Register
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000020107C4 (SCOM)
Description	This is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst2_dbg_cond1. 003 select inst2_dbg_cond2. 004 select inst2_dbg_cond3. 005 select inst2_dbg_cond2timeout. 006 select inst2_dbg_cond1. 007 select inst2_dbg_cond2. 008 select inst2_dbg_cond3. 009 select inst2_dbg_cond2timeout. 010 select inst3_dbg_cond1 - Unused, tied down. 011 select inst3_dbg_cond2 - Unused, tied down. 012 select inst3_dbg_cond3 - Unused, tied down. 013 select inst3_dbg_cond2timeout - Unused, tied down. 014 select inst4_dbg_cond1 - Unused, tied down. 015 select inst4_dbg_cond2 - Unused, tied down. 016 select inst4_dbg_cond3 - Unused, tied down. 017 select inst4_dbg_cond2timeout - Unused, tied down. 018 select inst2_dbg_trig_sp. 019 select inst2_dbg_trig_sp. 020 select inst3_dbg_trig_sp - Unused, tied down. 021 select inst4_dbg_trig_sp - Unused, tied down. 022 select tctrc_tcdbg_trigger_a(0). 023 select tctrc_tcdbg_trigger_b(0). 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 select tctrc_tcdbg_trigger_a(1). 026 select tctrc_tcdbg_trigger_b(1). 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 select tctrc_tcdbg_trigger_a(2). 029 select tctrc_tcdbg_trigger_b(2). 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 select tctrc_tcdbg_trigger_a(3). 032 select tctrc_tcdbg_trigger_b(3). 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3).

Bits	SCOM	Field Mnemonic: Description
		034 select tctrc_tcdbg_trigger_a(4). 035 select tctrc_tcdbg_trigger_b(4). 026 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 027 select tctrc_tcdbg_trigger_a(5). 028 select tctrc_tcdbg_trigger_b(5). 029 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 030 select tctrc_tcdbg_trigger_a(6). 031 select tctrc_tcdbg_trigger_b(6). 032 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 033 select tctrc_tcdbg_trigger_a(7). 034 select tctrc_tcdbg_trigger_b(7). 035 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 036 select tctrc_tcdbg_trigger_a(8). 037 select tctrc_tcdbg_trigger_b(8). 038 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 039 select tctrc_tcdbg_trigger_a(9). 040 select tctrc_tcdbg_trigger_b(9). 041 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 042 select xstop_err. 043 select recov_err. 044 select spattn. 045 select fir_dbg_local_xstop_err. 046 select tc_dbg_inter_brcst(0). 047 select tc_dbg_inter_brcst(1). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 102 select logic_trigger_in(0). 103 select logic_trigger_in(1). 104 select logic_trigger_in(2). 105 select logic_trigger_in(3). 106 select logic_trigger_in(4). 107 select logic_trigger_in(5). 108 select logic_trigger_in(6). 109 select logic_trigger_in(7). 110 select logic_trigger_in(8). 111 select logic_trigger_in(9). 112 select logic_trigger_in(10). 113 select logic_trigger_in(11). 114 select logic_trigger_in(12). 115 select logic_trigger_in(13). 116 select logic_trigger_in(14). 117 select logic_trigger_in(15). -- CORE TRIGGERS (EP chip only) -- Note: set core_slave_mode to honor ec[0:5]_tc_trace_run. 118 select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0). 119 select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1). 120 select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0). 121 select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1). -- BROADCAST / ERRORS. 122 select glb_trc_bdcst_recv (received global broadcast). 123 select edge detected fir_dbg_xstop_err. 124 select edge detected fir_dbg_recov_err. 125 select edge detected fir_dbg_spatn. 126 ... 127 select constant 0 (unused)
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).

Bits	SCOM	Field Mnemonic: Description
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Front-end instance 1 counter 1 in-a-row mode.
33	RW	INST2_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition1.
36:38	RWX	INST2_UNUSED_1: Unused.
39	RW	INST2_C2_INAROW_MODE: Front-end instance 1 counter 2 in-a-row mode.
40	RW	INST2_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST2_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST2_UNUSED_2: Unused.
46	RW	INST2_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST2_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST2_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST2_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: Instance 2 condition 1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: Instance 2 condition 2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front-end instance 1, reset condition 3 for reset_c3_on_c0: 0b100 = dbg_cross_couple_triggers(4). 0b101 = dbg_cross_couple_triggers(12). 0b110 = dbg_cross_couple_triggers(20). 0b111 = dbg_cross_couple_triggers(28).

Register Name	**Debug Instance 2 Condition 2 Register**
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000020107C5 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same of all selectors: 00000 - Selects inst2_cond1_trig_a. 00001 - Selects inst2_cond1_trig_b. 00010 - Selects inst2_cond2_trig_a. 00011 - Selects inst2_cond2_trig_b. 00100 - Selects inst2_condition1. 00101 - Selects inst2_condition2. 00110 - Selects inst2_condition3. 00111 - Selects inst2_cond2_timeout. 01000 - Selects inst2_cond1_trig_a. 01001 - Selects inst2_cond1_trig_b. 01010 - Selects inst2_cond2_trig_a. 01011 - Selects inst2_cond2_trig_b. 01100 - Selects inst2_condition1. 01101 - Selects inst2_condition2. 01110 - Selects inst2_condition3. 01111 - Selects inst2_cond2_timeout. 10000 - Selects inst3_cond1_trig_a. 10001 - Selects inst3_cond1_trig_b. 10010 - Selects inst3_cond2_trig_a. 10011 - Selects inst3_cond2_trig_b. 10100 - Selects inst3_condition1. 10101 - Selects inst3_condition2. 10110 - Selects inst3_condition3. 10111 - Selects inst3_cond2_timeout. 11000 - Selects inst4_cond1_trig_a. 11001 - Selects inst4_cond1_trig_b. 11010 - Selects inst4_cond2_trig_a. 11011 - Selects inst4_cond2_trig_b. 11100 - Selects inst4_condition1. 11101 - Selects inst4_condition2. 11110 - Selects inst4_condition3. 11111 - Selects inst4_cond2_timeout.
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: Instance 2 cross couple select 1 b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: Instance 2 cross couple select 2 a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: Instance 2 cross couple select 2 b.
20:43	RW	INST2_TO_CMP_LT: Compares the value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Forces test mode to indicate compare without actual compare.

Register Name	Debug Instance 2 Condition 3 Register
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_INST2_COND_REG_3
Address	00000000020107C6 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_TRACE_REG_0
Address	00000000020107CD (SCOM)
Description	This is debug macro configuration register 0 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: This bit enables instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: This bit enables instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: This bit enables slow LFSR mode of front-end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: This bit enables slow LFSR mode of front-end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: This field selects instance 1 condition 1 for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
10:11	RW	INST1_CONDITION2_TRIG_SEL: This field selects instance 1 condition 2 for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: This field selects instance 1 condition 2 time-out counter for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
14:15	RW	INST2_CONDITION1_TRIG_SEL: This field selects instance 2 condition 1 for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
16:17	RW	INST2_CONDITION2_TRIG_SEL: This field selects instance 2 condition 2 trigger for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: This field selects instance 2 condition 2 time-out counter for output (external) triggers. 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
20:31	RO	constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: This bit enables trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: This bit enables trigger on freeze.

Bits	SCOM	Field Mnemonic: Description
34:38	RW	CORE_RAS0_TRIG_SEL:
39:43	RW	CORE_RAS1_TRIG_SEL:
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(0). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)
54:57	RW	TRIG1_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(1). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)
58:63	RO	constant = 0b000000

Register Name	**Debug Trace 1 Register**
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_TRACE_REG_1
Address	00000000020107CE (SCOM)
Description	This is debug macro configuration register 1 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Instance 1 action selection, condition 1: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
2:3	RW	INST1_CONDITION2_ACTION_DO: Instance 1 action selection, condition 2: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Instance 1 action selection, c2_timeout: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
6:7	RW	INST2_CONDITION1_ACTION_DO: Instance 2 action selection, condition 1: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
8:9	RW	INST2_CONDITION2_ACTION_DO: Instance 2 action selection, condition 2: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Instance 2 action selection, c2_timeout: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
12:23	RO	constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For wait-N.
25	RW	INST1_CONDITION2_ACTION_WAITN: For wait-N.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For wait-N.

Bits	SCOM	Field Mnemonic: Description
27	RW	INST2_CONDITION1_ACTION_WAITN: For wait-N.
28	RW	INST2_CONDITION2_ACTION_WAITN: For wait-N.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For wait-N.
30:35	RO	constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (inst1, condition1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (inst1, condition2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (instance 2, condition1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (instance 2, condition2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 2, c2_timeout).
42:47	RO	constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select an additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt 001 = inst1_condition2_lt 010 = inst1_condition3_lt 011 = inst1_cond2_timeout_lt 1XX = Disable checkstop_mode
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: Enable_fir_trig_xstop: Enable checkstop on debug trigger: 0 = Disable a checkstop on the debug trigger 1 = Enable a checkstop on the debug trigger
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt 001 = inst2_condition2_lt 010 = inst2_condition3_lt 011 = inst2_cond2_timeout_lt 1XX = Disable checkstop_mode
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: enable_fir_error_xstop: Enable checkstop on FIR error: 0 = Disable checkstop on a FIR error. 1 = Enable checkstop on a FIR error.
56:63	RO	constant = 0b00000000

Register Name	Debug Trace Mode 2 Register
Mnemonic	TP.TCN0.N0.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000020107CF (SCOM)
Description	This is debug macro configuration register 2 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the run-N counter used in trace modes run-N and wait-N.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on run-N match.
19	RW	FORCE_TEST_MODE: FORCE run-N condition to be true.

Bits	SCOM	Field Mnemonic: Description
20	RW	ACCUM_HIST_MODE: Accumulate history mode; do not clear history mode when trace_run is active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	Debug Trace Control Register
Mnemonic	TP.TCN0.N0.EPS.DBG.DEBUG_TRACE_CONTROL
Address	00000000020107D0 (SCOM)
Description	This is the trace start/stop/rest using SCOM command register. Use write data(0/1/2) = 1. This is a reserved register

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field
1	WOX	Reserved field
2	WOX	Reserved field

Register Name	Extra Trace Mode Register
Mnemonic	TP.TCN0.N0.EPS.DBG.XTRA_TRACE_MODE
Address	00000000020107D1 (SCOM)
Description	Extra or dedicated trace mode register for core triggers

Bits	SCOM	Field Mnemonic: Description
0:37	RW	This register provides an extra or dedicated trace mode register for core triggers.

Register Name	CXA FIR Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_REG
Address	0000000002010800 (SCOM) 0000000002010801 (SCOM1) 0000000002010802 (SCOM2)
Description	This register is the local FIR register for the CAPP.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	BAR_PE: Informational PE. Generic bucket for errors that are informational.
1	RWX	WOX_AND	WOX_OR	REGISTER_PE: System checkstop PE. Generic bucket for errors that are system checkstop.
2	RWX	WOX_AND	WOX_OR	MASTER_ARRAY_CE: Correctable error on master array. Included uOP and CRESP arrays.
3	RWX	WOX_AND	WOX_OR	MASTER_ARRAY_UE: Uncorrectable error on Master array. Includes uOP and CRESP arrays.
4	RWX	WOX_AND	WOX_OR	TIMER_EXPIRED_RECOV_ERROR: Precise directory epoch timeout. Coarse directory epoch timeout. rtagPool epoxh data hang timeout. Recovery sequencer hang detection.
5	RWX	WOX_AND	WOX_OR	TIMER_EXPIRED_XSTOP_ERROR: Recovery sequencer hang detection.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6	RWX	WOX_AND	WOX_OR	PSL_CMD_UE: XPT detected uncorrectable error on processor bus data determined to be a PSL command. The PSL command does not propagate past XPT.
7	RWX	WOX_AND	WOX_OR	PSL_CMD_SUE: XPT detected special uncorrectable error on processor bus data determined to be a PSL command. The PSL command does not propagate past XPT.
8	RWX	WOX_AND	WOX_OR	SNOOP_ARRAY_CE: Correctable error on snooper array. Includes precise dir, coarse dir, and uOP.
9	RWX	WOX_AND	WOX_OR	SNOOP_ARRAY_UE: Uncorrectable error on snooper array. Includes precise DIR, coarse DIR, and uOP.
10	RWX	WOX_AND	WOX_OR	RECOVERY_FAILED: CAPP recovery failed.
11	RWX	WOX_AND	WOX_OR	ILLEGAL_LPC_BAR_ACCESS: Illegal LPC BAR Access. Error detected when a snooper or master write operation is attempted to the fine directories in LPC-only mode, or when the operation hits the LPC BAR region in LPC DISJOINT mode. Also, fires if a directory hit is found on a read operation within the LPC BAR range.
12	RWX	WOX_AND	WOX_OR	XPT_RECOVERABLE_ERROR: Recoverable errors detected in transport.
13	RWX	WOX_AND	WOX_OR	MASTER_RECOVERABLE_ERROR: Recoverable errors detected in Master.
14	RWX	WOX_AND	WOX_OR	SNOOPER_RECOVERABLE_ERROR: Spare FIR bits allocated for future use.
15	RWX	WOX_AND	WOX_OR	SECURE_SCOM_ERROR: Error detected in secure SCOM satellite.
16	RWX	WOX_AND	WOX_OR	MASTER_SYS_XSTOP_ERROR: System checkstop errors detected in the master (invalid state, control checker).
17	RWX	WOX_AND	WOX_OR	SNOOPER_SYS_XSTOP_ERROR: System checkstop errors detected in the snooper (invalid state, control checker).
18	RWX	WOX_AND	WOX_OR	XPT_SYS_XSTOP_ERROR: System checkstop errors detected in transport (invalid state, control checker).
19	RWX	WOX_AND	WOX_OR	MUOP_ERROR_1: Master uOP FIR 1.
20	RWX	WOX_AND	WOX_OR	MUOP_ERROR_2: Master uOP FIR 2.
21	RWX	WOX_AND	WOX_OR	MUOP_ERROR_3: Master uOP FIR 3.
22	RWX	WOX_AND	WOX_OR	SUOP_ERROR_1: Snooper uOP FIR 1.
23	RWX	WOX_AND	WOX_OR	SUOP_ERROR_2: Snooper uOP FIR 2.
24	RWX	WOX_AND	WOX_OR	SUOP_ERROR_3: Snooper uOP FIR 3.
25	RWX	WOX_AND	WOX_OR	POWERBUS_MISC_ERROR: Miscellaneous informational processor bus errors including unsolicited processor bus data. Unsolicited cResp.
26	RWX	WOX_AND	WOX_OR	POWERBUS_INTERFACE_PE: Parity error on processor bus interface (address/aTag/tTaag/rTag APC, SNP TLBI).
27	RWX	WOX_AND	WOX_OR	POWERBUS_DATA_HANG_ERROR: Any processor bus data hang poll error.
28	RWX	WOX_AND	WOX_OR	POWERBUS_HANG_ERROR: Any processor bus command hang error (domestic address range).
29	RWX	WOX_AND	WOX_OR	LD_CLASS_CMD_ADDR_ERR: Processor bus address error detected by APC on a load-class command.
30	RWX	WOX_AND	WOX_OR	ST_CLASS_CMD_ADDR_ERR: Processor bus address error detected by APC on a store-class command.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
31	RWX	WOX_AND	WOX_OR	PHB_LINK_DOWN: PPHB0 or PHB1 interface has asserted link down.
32	RWX	WOX_AND	WOX_OR	LD_CLASS_CMD_FOREIGN_LINK_FAIL: APC received ack_dead or ack_ed_dead from the foreign interface on a load-class command.
33	RWX	WOX_AND	WOX_OR	FOREIGN_LINK_HANG_ERROR: Any processor bus command hang error (foreign address range).
34	RWX	WOX_AND	WOX_OR	XPT_POWERBUS_CE: CE on data received from processor bus and destined for either XPT data array (and back to processor bus) or PSL command or link delay response packet.
35	RWX	WOX_AND	WOX_OR	XPT_POWERBUS_UE: UE on data received from processor bus and destined for XPT data array (and back to processor bus) or link delay response packet.
36	RWX	WOX_AND	WOX_OR	XPT_POWERBUS_SUE: SUE on data received from processor bus and destined for XPT data array (and back to processor bus) or link delay response packet.
37	RWX	WOX_AND	WOX_OR	TLBI_TIMEOUT: TLBI Timeout error. TLBI requires re-IPL to recover.
38	RWX	WOX_AND	WOX_OR	TLBI_SOT_ERR: Illegal SOT operation detected in P8BC mode.
39	RWX	WOX_AND	WOX_OR	TLBI_BAD_OP_ERR: TLBI bad operation error. TLBI requires re-IPL to recover.
40	RWX	WOX_AND	WOX_OR	TLBI_SEQ_NUM_PARITY_ERR: Parity error detected on TLBI sequence number.
41	RWX	WOX_AND	WOX_OR	ST_CLASS_CMD_FOREIGN_LINK_FAIL: APC received ack_dead or ack_ed_dead from the foreign interface on a store-class command.
42	RWX	WOX_AND	WOX_OR	TIME_BASE_ERR: An error has occurred with timebase. This is an indication that the timebase value can no longer be assumed to be correct.
43	RWX	WOX_AND	WOX_OR	TRANSPORT_INFORMATIONAL_ERR: Transport informational error.
44	RWX	WOX_AND	WOX_OR	APC_ARRAY_CMD_CE_ERPT: CE on PSL command queue array in APC.
45	RWX	WOX_AND	WOX_OR	APC_ARRAY_CMD_UE_ERPT: UE on PSL command queue array in APC.
46	RWX	WOX_AND	WOX_OR	PSL_CREDIT_TIMEOUT_ERR: PSL credit timeout error.
47	RWX	WOX_AND	WOX_OR	SPARE_2: Spare FIR bits allocated for future use.
48	RWX	WOX_AND	WOX_OR	HYPERVISOR: Hypervisor.
49	RWX	WOX_AND	WOX_OR	SPARE_3: Spare FIR bits allocated for future use.
50	RWX	WOX_AND	WOX_OR	SCOM_ERR2: Local FIR parity error RAS duplicate.
51	RWX	WOX_AND	WOX_OR	SCOM_ERR: Local FIR parity error of ACTION/MASK registers.
52:63	RO	RO	RO	constant = 0b000000000000

Register Name	CXA FIR Mask Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_MASK_REG
Address	0000000002010803 (SCOM) 0000000002010804 (SCOM1) 0000000002010805 (SCOM2)
Description	Error mask register. (Action0, mask) = Action select (0, 0) = Recoverable error (0, 1) = Masked (1, x) = Checkstop error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	BAR_PE_MASK: Informational PE Mask. Generic bucket for errors that are informational.
1	RW	WO_AND	WO_OR	REGISTER_PE_MASK: System checkstop PE mask. Generic bucket for errors that are system checkstop.
2	RW	WO_AND	WO_OR	MASTER_ARRAY_CE_MASK: Correctable error on master array. Includes uOP and CRESP arrays Mask.
3	RW	WO_AND	WO_OR	MASTER_ARRAY_UE_MASK: Uncorrectable error on master array. Includes uOP and CRESP arrays Mask.
4	RW	WO_AND	WO_OR	TIMER_EXPIRED_RECOV_ERROR_MASK: Precise directory epoch timeout Mask. Coarse directory epoch timeout mask. rtagPool epoxh data hang timeout mask. Recovery sequencer hang detection mask.
5	RW	WO_AND	WO_OR	TIMER_EXPIRED_XSTOP_ERROR_MASK: Recovery sequencer hang detection mask.
6	RW	WO_AND	WO_OR	PSL_CMD_UE_MASK: XPT detected uncorrectable error on processor bus data determined to be a PSL command Mask. The PSL command does not propagate past XPT.
7	RW	WO_AND	WO_OR	PSL_CMD_SUE_MASK: XPT detected Special uncorrectable error on processor bus data determined to be a PSL command mask. The PSL command does not propagate past XPT.
8	RW	WO_AND	WO_OR	SNOOP_ARRAY_CE_MASK: Correctable error on Snooper array. Includes precise directory, coarse directory, and uOP mask.
9	RW	WO_AND	WO_OR	SNOOP_ARRAY_UE_MASK: Uncorrectable error on Snooper array. Includes precise directory, coarse directory, and uOP Mask.
10	RW	WO_AND	WO_OR	RECOVERY_FAILED_MASK: CAPP recovery failed mask.
11	RW	WO_AND	WO_OR	ILLEGAL_LPC_BAR_ACCESS_MASK: Error detected when a snooper or master write operation is attempted to the fine directories in LPC-only mode, or when the operation hits the LPC BAR region in LPC disjoint mode. Also, activates if a directory hit is found on a read operation within the LPC BAR range.
12	RW	WO_AND	WO_OR	XPT_RECOVERABLE_ERROR_MASK: Recoverable errors detected in xpt mask.
13	RW	WO_AND	WO_OR	MASTER_RECOVERABLE_ERROR_MASK: Recoverable errors detected in Master mask.
14	RW	WO_AND	WO_OR	SNOOPER_RECOVERABLE_ERROR_MASK: Spare FIR bits allocated for future use mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
15	RW	WO_AND	WO_OR	SECURE_SCOM_ERROR_MASK: Error detected in secure SCOM satellite Mask.
16	RW	WO_AND	WO_OR	MASTER_SYS_XSTOP_ERROR_MASK: System checkstop errors detected in Master (invalid state, control checker) mask.
17	RW	WO_AND	WO_OR	SNOOPER_SYS_XSTOP_ERROR_MASK: System checkstop errors detected in Snooper (invalid state, control checker) mask.
18	RW	WO_AND	WO_OR	XPT_SYS_XSTOP_ERROR_MASK: System checkstop errors detected in Transport (invalid state, control checker) Mask.
19	RW	WO_AND	WO_OR	MUOP_ERROR_1_MASK: Master uOP FIR 1 mask.
20	RW	WO_AND	WO_OR	MUOP_ERROR_2_MASK: Master uOP FIR 2 mask.
21	RW	WO_AND	WO_OR	MUOP_ERROR_3_MASK: Master uOP FIR 3 mask.
22	RW	WO_AND	WO_OR	SUOP_ERROR_1_MASK: Snooper uOP FIR 1 mask.
23	RW	WO_AND	WO_OR	SUOP_ERROR_2_MASK: Snooper uOP FIR 2 mask.
24	RW	WO_AND	WO_OR	SUOP_ERROR_3_MASK: Snooper uOP FIR 3 mask.
25	RW	WO_AND	WO_OR	POWERBUS_MISC_ERROR_MASK: Miscellaneous informational processor bus errors mask including unsolicited processor bus data and unsolicited cResp.
26	RW	WO_AND	WO_OR	POWERBUS_INTERFACE_PE_MASK: Parity error on processor bus interface (address/aTag/tTag/rTag APC, SNP TLBI) mask.
27	RW	WO_AND	WO_OR	POWERBUS_DATA_HANG_ERROR_MASK: Any processor bus data hang poll error mask.
28	RW	WO_AND	WO_OR	POWERBUS_HANG_ERROR_MASK: Any processor bus command hang error (domestic address range) mask.
29	RW	WO_AND	WO_OR	LD_CLASS_CMD_ADDR_ERR_MASK: processor bus address error detected by APC on a load-class command mask.
30	RW	WO_AND	WO_OR	ST_CLASS_CMD_ADDR_ERR_MASK: Processor bus address error detected by APC on a store-class command mask.
31	RW	WO_AND	WO_OR	PHB_LINK_DOWN_MASK: PPHB0 or PHB1 interface has asserted linkdown Mask.
32	RW	WO_AND	WO_OR	LD_CLASS_CMD_FOREIGN_LINK_FAIL_MASK: APC received ack_dead or ack_ed_dead from the foreign interface on a load-class command mask.
33	RW	WO_AND	WO_OR	FOREIGN_LINK_HANG_ERROR_MASK: Any processor bus command hang error (foreign address range) mask.
34	RW	WO_AND	WO_OR	XPT_POWERBUS_CE_MASK: CE on data received from processor bus and destined for either XPT data array (and back to processor bus) or PSL command or link delay response packet mask.
35	RW	WO_AND	WO_OR	XPT_POWERBUS_UE_MASK: UE on data received from processor bus and destined for XPT data array (and back to processor bus) or link delay response packet mask.
36	RW	WO_AND	WO_OR	XPT_POWERBUS_SUE_MASK: SUE on data received from processor bus and destined for XPT data array (and back to processor bus) or link delay response packet mask.
37	RW	WO_AND	WO_OR	TLBI_TIMEOUT_MASK: TLBI Timeout error. TLBI requires re-IPL to recover mask.
38	RW	WO_AND	WO_OR	TLBI_SOT_ERR_MASK: Illegal SOT op detected in POWER8 BC mode. TLBI requires re-IPL to recover mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
39	RW	WO_AND	WO_OR	TLBI_BAD_OP_ERR_MASK: TLBI bad op error. TLBI requires re-IPL to recover mask.
40	RW	WO_AND	WO_OR	TLBI_SEQ_NUM_PARITY_ERR_MASK: Parity error detected on TLBI sequence number mask.
41	RW	WO_AND	WO_OR	ST_CLASS_CMD_FOREIGN_LINK_FAIL_MASK: APC received ack_dead or ack_ed_dead from the foreign interface on a store-class command mask.
42	RW	WO_AND	WO_OR	TIME_BASE_ERR_MASK: An error has occurred with timebase. This is an indication that the time-base value can no longer be assumed to be correct.
43	RW	WO_AND	WO_OR	TRANSPORT_INFORMATIONAL_ERR_MASK: Transport informational error mask.
44	RW	WO_AND	WO_OR	APC_ARRAY_CMD_CE_ERPT_MASK: CE on PSL command queue array in APC mask.
45	RW	WO_AND	WO_OR	APC_ARRAY_CMD_UE_ERPT_MASK: UE on PSL command queue array in APC mask.
46	RW	WO_AND	WO_OR	PSL_CREDIT_TIMEOUT_ERR_MASK: PSL credit timeout error mask.
47	RW	WO_AND	WO_OR	SPARE_2_MASK: Spare FIR bits allocated for future use mask.
48	RW	WO_AND	WO_OR	SPARE_3_MASK: Spare FIR bits allocated for future use mask.
49	RW	WO_AND	WO_OR	HYPERVISOR_MASK: Hypervisor mask.
50	RW	WO_AND	WO_OR	SCOM_ERR2_MASK: Local FIR parity error RAS duplicate mask.
51	RW	WO_AND	WO_OR	SCOM_ERR_MASK: Local FIR parity error of ACTION/MASK registers mask.
52:63	RO	RO	RO	constant = 0b000000000000

Register Name	Pervasive FIR Action 0 Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_ACTION0_REG
Address	0000000002010806 (SCOM)
Description	This register is the action select for the FIR bits.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	FIR_ACTION0: MSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0, 0) = Checkstop. (0, 1) = Recoverable. (1, 0) = Recoverable interrupt. (1, 1) = Machine check.

Register Name	Pervasive FIR Action 1 Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_ACTION1_REG
Address	0000000002010807 (SCOM)
Description	This register is the second bit of action select, if necessary.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	FIR_ACTION1: LSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action select. (x, x, 1) = Masked. (0, 0, 0) = Checkstop. (0, 1, 0) = Recoverable Error. (1, 0, 0) = Recoverable Interrupt. (1, 1, 0) = Machine Check.

Register Name	Snoop Error Report Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ERROR_REPORT_REG
Address	000000000201080A (SCOM)
Description	This register is the SCOM access of snp c_err_rpt latches.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	CXA_SNP_C_ERR_RPT_HOLD_DATA: SNP c_err report hold value.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	APC Master Error Report Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC1.ERRRPT
Address	000000000201080B (SCOM)
Description	This register is the output of the APC cerr_rpt hold latches.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	Reserved field.
17	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
18	ROX	Reserved field.
19	ROX	Reserved field.
20	ROX	Reserved field.
21	ROX	Reserved field.
22	ROX	Reserved field.
23	ROX	Reserved field.
24	ROX	Reserved field.
25	ROX	Reserved field.
26	ROX	Reserved field.
27	ROX	Reserved field.
28	ROX	Reserved field.
29	ROX	Reserved field.
30	ROX	Reserved field.
31	ROX	Reserved field.
32	ROX	Reserved field.
33	ROX	Reserved field.
34	ROX	Reserved field.
35	ROX	Reserved field.
36	ROX	Reserved field.
37	ROX	Reserved field.
38	ROX	Reserved field.
39	ROX	Reserved field.
40	ROX	Reserved field.
41	ROX	Reserved field.
42	ROX	Reserved field.
43	ROX	Reserved field.
44	ROX	Reserved field.
45	ROX	Reserved field.
46:63	RO	constant = 0b0000000000000000

Register Name	Transport Error Hold Register
Mnemonic	CAPP0.CXA_TOP.XPT_ERROR_REPORT
Address	0000000002010800 (SCOM)
Description	This register contains hold latches for the conditions that result in FIR errors.

Bits	SCOM	Field Mnemonic: Description
0	ROX	XPT_PSL_CMD_UE_ERRHOLD: PSL command uncorrectable error.
1	ROX	XPT_PSL_CMD_SUE_ERRHOLD: PSL command special uncorrectable error.
2	ROX	XPT_SC_RDATA_PARITY_ERRHOLD: EPT register read data parity error.

Bits	SCOM	Field Mnemonic: Description
3	ROX	APC_SC_RDATA_PARITY_ERRHOLD: APC register read data parity error.
4	ROX	SN_SC_RDATA_PARITY_ERRHOLD: Snoop register read data parity error .
5	ROX	NX_DATA_RTAG_PARITY_ERRHOLD: Processor bus RTAG parity error.
6	ROX	NXPBXPT_PBRCV_ECC_CE_ERRHOLD: Processor bus data or PSL command correctable error.
7	ROX	NXPBXPT_PBRCV_ECC_UE_ERRHOLD: Processor bus data uncorrectable error.
8	ROX	NXPBXPT_PBRCV_ECC_SUE_ERRHOLD: Processor bus data Special uncorrectable error.
9	ROX	XPT_DBG_CTL_REG_PARITY_ERRHOLD: Debug Bus Mux Control Register write data parity error.
10	ROX	XPT_CFG_REG_PARITY_ERRHOLD: Transport Control Register write data parity error.
11	ROX	CAPP_ERR_STAT_CTL_REG_PARITY_ERRHOLD: CAPP Error Status and Control Register write data parity error.
12	ROX	PMU_CNTRA_CFG_REG_PARITY_ERRHOLD: PMU Counter Configuration Register0 write data parity error.
13	ROX	PMU_CNTRB_CFG_REG_PARITY_ERRHOLD: PMU Counter Configuration Register1 write data parity error.
14	ROX	XPT_PMU_EVENT_SEL_REG_PARITY_ERRHOLD: XPT PMU Event Select Register write data parity error.
15	ROX	PE0_CXA_LINKDOWN_ERRHOLD: PE0 link down.
16	ROX	PE1_CXA_LINKDOWN_ERRHOLD: PE1 link down.
17	ROX	SB_SCOM_ERRHOLD: Secure SCOM internal error.
18	ROX	PBXMIT_MSGQ_SEQ_ERRHOLD: Transport message queue sequencer not one hot error.
19	ROX	PBXMIT_DXMIT_SEQ_ERRHOLD: Transport transmit queue sequencer not one hot error.
20	ROX	EPH_REC_TMR_CNTL_REG_PARITY_ERRHOLD: Epoch and Recovery Timers Control Register write data parity error
21	ROX	RCS_RECOVERY_FAILED_ERRHOLD: CAPP recovery failed.
22	ROX	RCS_STATE_MACHINE_ERRHOLD: Recovery sequencer FSM invalid state.
23	ROX	NXPBXPT_PBRCV_LNK_RSP_ECC_UE_ERRHOLD: Secure link response packet UE.
24	ROX	NXPBXPT_PBRCV_LNK_RSP_ECC_SUE_ERRHOLD: Secure link response packet SUE.
25	ROX	LNK_RSP_PKT_DISCARDED_ERRHOLD: Secure link response packet discarded.
26	ROX	SECURE_LNK_RSP_PKT_NOT_VALID_ERRHOLD: Secure link response packet not valid.
27	ROX	SECURE_LNK_SCOM_CONFLICT_ERRHOLD: Secure link response packet conflict with SCOM access.
28	ROX	UNSOLICITED_DATA_RCV_ERROR_ERRHOLD: Unsolicited data received.
29	ROX	AS_RCMD0_PARITY_ERR_ERRHOLD: AS as endpoint rcmd0 parity error.
30	ROX	AS_REGS_PARITY_ERR_ERRHOLD: AS as Endpoint Register parity error.
31	ROX	AS_SM_ERROR_ERRHOLD: AS as endpoint state machine error.
32	ROX	AS_REG_RDATA_PERR_ERRHOLD: AS as Endpoint Register Read data parity error.
33	ROX	DFS_SM_ERROR_ERRHOLD: DFS state machine error.
34	ROX	TB_XPT_ERROR_FIR_ERR_ERRHOLD: Time base error.
35	ROX	TB_CMD_DISCARDED_ERRHOLD: Time base command discarded.
36	ROX	TB_REG_RDATA_PERR_ERRHOLD: Time base command discarded.
37	ROX	RNG_WR_ENBL_REG_PERR_ERRHOLD: RNG Write Enable Configuration Register parity error.
38	ROX	SSA_ECC_HI_UE_ERRHOLD: Message queue high UE.

Bits	SCOM	Field Mnemonic: Description
39	ROX	SSA_ECC_HI_CE_ERRHOLD: Message queue high CE.
40	ROX	SSA_ECC_HI_SUE_ERRHOLD: Message queue high SUE.
41	ROX	SSA_ECC_LO_SUE_ERRHOLD: Message queue low SUE.
42	ROX	SSA_ECC_LO_CE_ERRHOLD: Message queue low CE.
43	ROX	SSA_ECC_LO_UE_ERRHOLD: Message queue low UE.
44	ROX	CXACQPB_MUX_ECC_CE_ERRHOLD: CQ multiplexer CE.
45	ROX	CXACQPB_MUX_ECC_UE_ERRHOLD: CQ multiplexer UE.
46	ROX	APC0_SC_RDATA_PARITY_ERRHOLD: APC0 Register parity error.
47	ROX	CREDIT_TIMEOUT_ERRHOLD: CAPP Credit timeout.
48	ROX	TLBI_SC_RDATA_PARITY_ERRHOLD: TLBI SCOM parity error.
49	ROX	TLBI_REGS_PARITY_ERRHOLD: TLBI Register parity error.
50	ROX	RCS_RECOVERY_TIMEOUT_ERRHOLD: CAPP recovery timeout.
51	ROX	TBST0_BADIN_ERRHOLD: Timebase state machine in State 0 and SCOM TFMR write of bit (18) move_chip_tod_to_tb.
52	ROX	TBST6_BADIN_ERRHOLD: Timebase state machine in State 6 and SCOM TFMR write of 1 bit (18) move_chip_tod_to_tb.
53	ROX	TBST7_BADIN_ERRHOLD: Timebase state machine in State 7 and SCOM TFMR write of 1 bit (16) load_tod_mod or (18) move_chip_tod_to_tb.
54	ROX	TWO_TFMRCMDS_ERR_ERRHOLD: SCOM TFMR write of 1 to both bits (16) load_tod_mod and bit (18) move_chip_tod_to_tb.
55	ROX	TB_MISSING_SYNC_ERRHOLD: Indicates a SYNC pulse was not received in the time specified by the sync_bit_sel control bits.
56	ROX	TB_MISSING_STEP_ERRHOLD: Indicates that a step pulse was not received in the time specified by the max_cyc_bet_steps control bits.
57	ROX	TB_RESIDUE_ERR_ERRHOLD: Indicates a parity or residue error has compromised the integrity of the timebase.
58	ROX	TX_TFMR_CORRUPT_ERRHOLD: Indicates a parity error has been detected on the TFMR Register.
59	ROX	TBST_CORRUPT_ERRHOLD: Indicates a TFMR invalid TB state machine state.
60	ROX	TBST9_BADIN_ERRHOLD: Timebase state machine in state 9 and SCOM TFMR write of 1 bit (16) load_tod_mod or (18) move_chip_tod_to_tb.
61:63	RO	constant = 0b000

Register Name	TLBI Error Hold Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.TLBI_ERROR_REPORT
Address	000000000201080D (SCOM)
Description	This register contains hold latches for the conditions that result in FIR errors.

Bits	SCOM	Field Mnemonic: Description
0	ROX	TLBI_IN_TIMEOUT: Data hang timeout.
1	ROX	TLBI_IN_SEQ_ERR: Error in TLBI internal sequencers.
2	ROX	TLBI_IN_SEQ_PERR: TLBI sequence number parity error.
3	ROX	TLBI_IN_BAD_OP_ERR: TLBI bad op error.

Bits	SCOM	Field Mnemonic: Description
4	ROX	TLBI_IN_SNP_ADDR_PERR: TLBI snoop address parity error.
5	ROX	TLBI_IN_SNP_TTAG_PERR: TLBI snoop TTAG parity error.
6:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	CAPP Error Status and Control Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_EPT.CAPP_ERR_STATUS_CONTROL
Address	000000000201080E (SCOM)
Description	This register contains status and controls for the error recovery process.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	ERROR_RECOVERY_INITIATED: If this bit is set (= 1) a recoverable error has been detected and the CAPP recovery process has been initiated. Once set, this bit remains set until cleared by firmware or POR.
1	RWX_WCLRPART	ERROR_RECOVERY_COMPLETE: If Error Recovery Initiated is 1 and this bit is 0, the CAPP recovery process is in progress. If Error Recovery Initiated is 1 and this bit is 1, the CAPP recovery process has completed. If Error Recovery Initiated is 0, Error Recovery Complete = 1 is not meaningful. Once set, this bit remains set until cleared by firmware or POR.
2	RO	constant = 0b0
3	RWX	TLBI_PSL_DEAD: This bit is set by hardware when Error Recovery Initiated is set, asserting the core_is_dead signal to the TLBI macro informing it that PSL must be considered non-operational, possibly with outstanding TLBI requests. When core_is_dead = 1, the snoop machine in TLBI stops waiting for not_my_lpar_id or tlbi_response command from PSL. TLBI acts as if PSL has returned something and goes back to idle. When error recovery is complete and firmware wants to reinitialize the TLBI, it writes this bit and TLBI Fence to 0 in the same SCOM write operation.
4	RWX	TLBI_FENCE: This bit is set by hardware when Error Recovery Initiated is set. This bit drives the tlbie_fence_lvl signal to the TLBI macro, which normally informs the macro that the core is going to sleep but here is used as part of error initiation and recovery. The tlbie_fence_lvl tells the macro to start ignoring the new TLBIES, but still finishes up the TLBIES received before tlbie_fence_lvl went high. When recovery is complete and firmware wants to reinitialize the TLBI, it writes this bit and the TLBI PSL is dead to 0 in the same SCOM write operation.
5	RWX_WCLRPART	RECOVERY_FAILED: Recovery did not complete successfully. Bits 6 - 9 specify the reason for the failure.
6	RWX_WCLRPART	RTAGFLUSH_FAILED: During recovery an error was detected while trying to flush the rTagPool.
7	RWX_WCLRPART	PRECISE_DIR_FLUSH_FAILED: During recovery an error was detected while trying to flush the precise directory.
8	RWX_WCLRPART	COURSE_DIR_FLUSH_FAILED: During recovery an error was detected while trying to flush the course directory.
9	RWX_WCLRPART	RECOVERY_HANG_DETECTED: The recovery actions timed out and a hang was declared.
10:11	RWX_WCLRPART	EPOCH_VALUE: Epoch value captured when error recovery is initiated.
12:13	RO	constant = 0b00
14	WO_1P	FORCE_QUIESCE: Force CAPP to quiesce.
15	ROX	QUIESCE_DONE: When set to 1, the force quiesce is in progress. When set to 0, the quiesce has completed.
16:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Flush SUE State Map Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.FLUSHSHUE
Address	000000000201080F (SCOM)
Description	This register is 1 bit per state decode. When set to 1, it requires a flush with SUE during directory flush.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	FLUSH_SUE_STATE_MAP: DIR Flush SUE state map. 1 bit per state decode.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Error Inject Register
Mnemonic	CAPP0.CXA_TOP.APC_ERRINJ
Address	0000000002010810 (SCOM)
Description	This register controls error injection.

Bits	SCOM	Field Mnemonic: Description
0	RW	APC_ERRINJ_ENABLE: APC master error inject enable.
1	RW	APC_ERRINJ_DBLERR: APC master 0 = inject 1-bit ECC error. When set to 1, inject 2-bit ECC error.
2	RW	APC_ERRINJ_CONTINUOUS: APC master 0 = inject error once. When set to 1, inject error continuously.
3:6	RO	constant = 0b0000
7:11	RW	APC_ERRINJ_TARGET: APC master error inject target selection.
12	RW	SNP_ERROR_INJECT_ENABLE: SNP master error inject enable.
13	RW	SNP_INJECT_DBL_ECC_ERROR: SNP Master 0 = inject 1-bit ECC error. When set to 1, inject 2-bit ECC error.
14	RW	SNP_INJECT_CONTINOUS_ERROR: SNP master 0 = inject error once. When set to 1, inject error continuously.
15:16	RO	constant = 0b00
17:23	RW	SNP_ERROR_INJECT_TARGET: SNP Master error inject target selection.
24:31	RO	constant = 0b00000000
32	RW	XPT_ERROR_INJECT_ENABLE: XPT master error inject enable.
33:34	RW	XPT_ERROR_TYPE: XPT error type: 00 = Inject CE 01 = Inject UE 10 = Inject SUE 11 = Reserved.
35	RW	XPT_INJECT_CONTINUOUS_ERROR: XPT continuous mode. When set to 1, continuously inject the error. When set to 0, inject on the next operation.
36:39	RW	XPT_ERROR_INJECT_TARGET: XPT Error inject target: 0000 = Write buffer array 0 0001 = Write buffer array 1 0010-1111 = Reserved
40:63	RO	Constant = 0b000000000000000000000000

Register Name	Debug Bus Multiplexer Control Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.DEBUG_CONTROL
Address	0000000002010811 (SCOM)
Description	This register selects which unit drives the bus, and which port of its 16 - 1 multiplexer drives the bus.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	BLOCK_MUX_PORT_SEL: Selects 1 of up to 16 block internal debug buses to source the block debug bus output.
4:11	RW	BLOCK_SEL: One-hot bit vector that selects the block to drive the debug bus. Bit blocks: 4 apc0 5 apc1 6 snpfe 7 snpfe_dir 8 snpbe 9 snpbe_uop 10 tlbi 11 xpt If all block select bits are 0, the debug bus is degated and no switching on the main trunk of the debug bus occurs.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Trigger Bus Multiplexer Control Register
Mnemonic	CAPP0.CXA_TOP.CXA_TRIGCTL
Address	0000000002010812 (SCOM)
Description	This register selects and enables trigger events.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CXA_TRIGCTL_PORTSEL: APC master trigger selection.
4	RW	CXA_TRIGCTL_APC0_ENABLE: APC master trigger enable for apc0.
5	RW	CXA_TRIGCTL_APC1_ENABLE: APC master trigger enable for apc1.
6	RW	SNPFE_TRIGGER_ENABLE: SNP FE trigger enable.
7	RW	SNPFE_DIR_TRIGGER_ENABLE: SNP FE DIR trigger enable.
8	RW	SNPBE_TRIGGER_ENABLE: SNP BE trigger enable.
9	RW	SNPBE_UOP_TRIGGER_ENABLE: SNP BE UOP trigger enable.
10	RW	Reserved field.
11	RW	Reserved field.
12:15	RW	SNP_MUX_PORT_SEL: Selects 1 of up to 16 block internal trigger conditions to source the SNP trigger bus bit 1.
16:19	RW	Reserved field.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Error Report Clear Register
Mnemonic	CAPP0.CXA_TOP.ERR_RPT_CLR
Address	0000000002010813 (SCOM)
Description	This register clears all the CAPP c_err_rpt error hold latches when written to.

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved.
1:63	RO	Not implemented.

Register Name	PMU Counter A Configuration Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.PMU_CNTRA_CFG
Address	0000000002010814 (SCOM)
Description	The PMU Counter A Configuration Register controls the configuration of the PMU Counters.

Bits	SCOM	Field Mnemonic: Description
0	RW	PMUA_COUNTER0_ENABLE: When set to 1, this bit enables PMU Counter0.
1	RW	PMUA_COUNTER1_ENABLE: When set to 1, this bit enables PMU Counter1.
2	RW	PMUA_COUNTER2_ENABLE: When set to 1, this bit enables PMU Counter2.
3	RW	PMUA_COUNTER3_ENABLE: When set to 1, this bit enables PMU Counter3.
4:6	RW	PMUA_PRESCALER_SELECT: Determines which, if any, prescaler counter to apply to all 16-bit PMU counters.
7	RW	PMUA_COUNTER_FREEZE_MODE: Indicates a counter should freeze on overflow. When set to 0, free running. When set to 1, freeze on overflow.
8	RW	PMUA_COUNTER_RESET_MODE: Indicates how a counter should reset. When set to 0, free running. When set to 1, reset on SCOM read.
9:12	RW	PMUA_COUNTER0_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter0.
13	RW	PMUA_COUNTER0_POSEDGE_SELECT: When set to 1, the PMU only counts the event rising edge. When set to 0, the PMU counts every cycle the event is asserted (high).
14:15	RW	PMUA_COUNTER0_BIT_PAIR_SELECT: Indicates how the event pairs must be combined to increment this PMU counter.
16:19	RW	PMUA_COUNTER1_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter1.
20	RW	PMUA_COUNTER1_POSEDGE_SELECT: When set to 1, the PMU only counts the event rising edge. When set to 0, the PMU counts every cycle the event is asserted (high).
21:22	RW	PMUA_COUNTER1_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
23:26	RW	PMUA_COUNTER2_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter2.
27	RW	PMUA_COUNTER2_POSEDGE_SELECT: When set to 1, the PMU only counts the event rising edge. When set to 0, the PMU counts every cycle the event is asserted (high).
28:29	RW	PMUA_COUNTER2_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
30:33	RW	PMUA_COUNTER3_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter3.

Bits	SCOM	Field Mnemonic: Description
34	RW	PMUA_COUNTER3_POSEDGE_SELECT: When set to 1, the PMU only counts the event rising edge. When set to 0, the PMU counts every cycle the event is asserted (high).
35:36	RW	PMUA_COUNTER3_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
37:38	RW	PMUA_PMU_PORT_SELECT: Chooses the final PMU events to feed to the counters.
39:63	RO	constant = 0b00000000000000000000000000

Register Name	PMU Counters A Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_PMULET.PMU_CNTRA_REG
Address	0000000002010815 (SCOM)
Description	The PMU Counters A Register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PMU_COUNTERA_0: PMU Counter0.
16:31	ROX	PMU_COUNTERA_1: PMU Counter1.
32:47	ROX	PMU_COUNTERA_2: PMU Counter2.
48:63	ROX	PMU_COUNTERA_3: PMU Counter3.

Register Name	APC Master PMU Events Select Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC1.APC_PMUSEL
Address	0000000002010816 (SCOM)
Description	This register controls APC performance monitor event selections.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	APC_PMUSEL_GRPSEL: APC master PMU events group selection. Valid values of 0 - 4.
4:5	RO	constant = 0b00
6:11	RW	APC_PMUSEL_FSMJ_EVENT_SEL: APC master PMU events FSMJ event selection. Valid values of 0 - 9.
12	RO	constant = 0b0
13:19	RW	APC_PMUSEL_FSMJ_FSM_SEL: APC master PMU FSMJ FSM selection. Valid values of 0, 1, 8, 9, 16, 17, 24, 25 for read FSMs. Valid values of 64, 65, 72, 73, 80, 81, 88, 89 for write FSMs.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	Snoop PMU Events Select Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_PMU_EVENTS_SELECT_REG
Address	0000000002010817 (SCOM)
Description	This register controls which group of events go on the CXA SNP PMON bus. This bus is sent to the PMU input bus multiplexer in XPT where further bit selection is performed on input to the PMU counters.

Bits	SCOM	Field Mnemonic: Description
0:3	WO	CXA_SNP_PMU_GROUP_SELECT: Selects which one of four snoop PMU event groups is sent. Use only values 0 to 3.
4:5	RO	constant = 0b00
6:11	WO	CXA_SNP_PMU_FSMJ_EVENT_SELECT: Selects which one of eight FSMJ events get routed to the FAMJ event. Use only values 0 to 7.
12:13	RO	constant = 0b00
14:19	WO	CXA_SNP_PMU_FSMJ_FSM_SELECT: Selects which one of four snoop state machines is used for FSMJ event counting. Use only values of 0, 1 , 2, and 3.
20:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	APC Master Processor Bus Control Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.APCTL
Address	0000000002010818 (SCOM)
Description	This register controls Processor Bus operations.

Bits	SCOM	Field Mnemonic: Description
0	RW	APCCTL_ENB_CRESP_EXAM: Enables APC master examining cResps. When disabled, prevents false assertion of unexpected CRESP FIR when cResps for PHB are seen. (APC RD FSM spoofs PHB unit ID).
1	RW	APCCTL_ADR_BAR_MODE: addr_bar_mode. Set to 1 when chip equals group. Small system address map. Reduces the number of group ID bits to two and eliminates the chip ID bits. All chips have an ID of 0. Nn scope is not available in this mode.
2	RW	APCCTL_DISABLE_NN_RN: Disables nn_rn scope.
3	RW	APCCTL_DISABLE_VG_NOT_SYS: disable_vg_not_sys scope.
4	RW	APCCTL_DISABLE_G: disable_group scope.
5	RW	APCCTL_DISABLE_LN: disable_ln scope.
6	RW	APCCTL_SKIP_G: Skip increment to group scope. Only used by read machines.
7	RW	APCCTL_HANG_ARE: Hangs on address error.
8	RW	APCCTL_HANG_DEAD: Hangs on Ack_*dead.
9	RW	APCCTL_CFG_BKILL_INC: cfg bkill inc.
10	RW	Reserved field.
11	RW	Reserved field.
12	RW	APCCTL_DISABLE_PSL_CMDQUEUE: disable_psl_cmdqueue. When set to 0, the PSL command queue is enabled. Order of commands is restored in queue using queue ID as a write pointer. When set to 1, the PSL command queue is disabled or bypassed. PSL can only have one command outstanding per APC machine.
13	RW	APCCTL_ENABLE_MASTER_RETRY_BACKOFF: enable_master_retry_backoff. When set to 0, master_retry_backoff due to excessive rty_lpc_only is disabled. When set to 1, master_retry_backoff due to excessive rty_lpc_only is enabled.

Bits	SCOM	Field Mnemonic: Description
14:16	RW	SCPTGT_LFSR_MODE: Mode for LFSRs used in scope_target counter logic selects count of average number of clocks before LFSR rolls over: 0 = On average every 64 K clocks 1 = On average every 32 K clocks 2 = On average every 16 K clocks 3 = On average every 8 K clocks 4 = On average every 4 K clocks 5 = On average every 2 K clocks 6 = On average every 1 K clocks 7 = On average every 512 clocks
17	RW	APCCTL_ENABLE_RD_VG_SCOPE_PREDICT: enable_rd_vg_scope_predict. 0 = rd_vg_scope_predictor is disabled. 1 = rd_vg_scope_predictor is enabled.
18	RW	Reserved field.
19:38	RO	constant = 0b00000000000000000000
39:45	RW	WR_EPSILON_VALUE: Write epsilon value.
46:55	RO	constant = 0b0000000000
56:63	RW	APCCTL_MAX_RETRY: Maximum retry count. When set to 0, retry forever.

Register Name	**APC Master Configuration Register**
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.APCFG
Address	0000000002010819 (SCOM)
Description	This register controls the PHB selection, hang_poll_scale, speculative HPC state, POWER8/POWER9 mode, and addr(8:13).

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1	RW	Reserved field.
2:3	RW	APCCTL_PHB_SEL: PHB select: 01 selects PHB 10 selects Alink
4:7	RW	HANG_POLL_SCALE: Determines the number of hang polls that must be detected to indicate a hang poll to the logic.
8:12	RW	SPEC_HPC_DIR_STATE: Speculative HPC DIR state value.
13	RW	Reserved field.
14	RW	APCCTL_POWER9_MODE: When set to 0, in POWER8 backwards compatibility mode. When set to 1, in POWER9 mode.
15:20	RW	APCCTL_SYSADDR: Used for address bits 8:13 in PB commands and SNP DIR compares.
21	RW	APCCTL_MEM_SEL_MODE: Memory select mode as defined in PB Arch V4. 0 = Memory select mode 0 1 = Memory select mode 1
22	RW	APCCTL_ENB_FRC_ADDR13: Enables forcing of addr(13) = 1 when P8BC mode AND mem_sel_mode = 0 AND pslcmd.rfs_class ! = 0. 0 = Disabled 1 = enabled
23:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	Snoop CAPI Configuration Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_CAPI_CFG_REG
Address	000000000201081A (SCOM)
Description	This register controls the configuration of the precise and coarse directories and controls other snooper functions whose setup is dependent on the discovered CAPI device.

Bits	SCOM	Field Mnemonic: Description
0	RW	CXA_SNP_ENABLE_TTYPE_DECODE: When set to 1, this bit enables tType decode in the snoop pipeline. When set to 0, tTypes are not decoded and the snoop pipelines are disabled.
1	RO	constant = 0b0
2:3	RW	CXA_SNP_PRECISE_DIR_SIZE: These bits control the size of the ways of the precise directory. Directory size can be further reduced by not allocating entries to a particular way.
4	RW	CXA_SNP_COARSE_DIR_ENABLE: The coarse directory must be enabled to participate in the memory coherence protocol. If the coarse directory is disabled, the effect is as if the coarse directory always misses on a search access and the results of reads and writes to coarse directory entries are unpredictable.
5	RW	CXA_SNP_COARSE_DIR_SECTORS: Coarse directory sector configuration varies under control of this bit allowing the capacity of memory covered by the directory to be either 8 MB or 256 MB.
6	RW	CXA_SNP_MCD_CHICKEN_SWITCH: This switch is to be used only if the MCD cannot be configured to cover the address space specified by the BHR address range (Remote Address Base Address/Mask Register).
7:11	RW	CXA_SNP_BHR_DIR_STATE: This is the directory state value used to indicate that the remote address BAR has been hit (BHR BAR hit remote).
12:13	RW	CXA_SNP_LPC_MODE:
14:31	RO	constant = 0b0000000000000000000
32:37	RW	CXA_SNP_CT_COMPARE_VECTOR: Used to compare the CT field of COP request commands, bits 30:35 of address for match.
38:39	RW	CXA_SNP_PHB_FILTER_CNTL:
40:63	RW	CXA_SNP_EPOCH_TEST_VECTOR: Used to determine epoch timeouts when there are multiple hits on the directory.

Register Name	Snoop Control Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_CNTL_REG
Address	000000000201081B (SCOM)
Description	This register contains CAPI-device-independent snooper controls and parameters.

Bits	SCOM	Field Mnemonic: Description
0	RW	CXA_SNP_READ_EPSILON_MODE: Controls which read epsilon tier* is loaded into the read epsilon counter for read commands of various scopes.
1:2	RO	constant = 0b00
3:11	RW	CXA_SNP_READ_EPSILON_TIER0: Read epsilon mode controls whether this value loads the read epsilon counter tier 0.
12:14	RO	constant = 0b000
15:23	RW	CXA_SNP_READ_EPSILON_TIER1: Read epsilon mode controls whether this value loads the read epsilon counter tier 1.
24	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
25:35	RW	CXA_SNP_READ_EPSILON_TIER2: Read epsilon mode controls whether this value loads the read epsilon counter tier 2.
36:44	RO	constant = 0b000000000
45:47	RW	CXA_SNP_ADDRESS_PIPELINE_MASTERWAIT_COUNT: Maximum number of cycles an APC master can wait before swapping the arbitration priority between APC and the snooper.
48:51	RW	CXA_SNP_DATA_HANG_POLL_SCALE: Number of dhang_polls it takes to increment the DHANG counter in snoop. Actual count is scale + 1. Value of 0000 = decimal 1 counts.
52:63	RO	constant = 0b000000000000

Register Name	Transport Control Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.XPT_CONTROL
Address	000000000201081C (SCOM)
Description	This register contains configuration and threshold values.

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SEND_PACKET_TIMER_VALUE: The send packet timer, which is used to determine when the XPT has waited long enough for a next message to pack, is loaded from this field. The timer is used in conjunction with the CI Store Buffer Threshold field and expires when the number of cycles specified by that field has passed. When the CI Store Buffer Threshold is set to '11'x, the timer starts when a message is loaded into an empty buffer. When the CI Store Buffer Threshold timer is not set to '11'x, the timer is started when a new message is loaded into a buffer and the number of CI store buffers in use is greater than the value specified by the CI Store Buffer Threshold. When a message packet is sent, the timer is reset and is not running and the buffer is marked empty. A send packet timer value of x'000' specifies 1024 cycles.
10:13	RW	CI_STORE_BUFFER_THRESHOLD: The number of PHB0 CI Store buffers in use must exceed the CI Store Buffer Threshold before the Send Message Timer affects when XPT sends message packets (see Send Packet Timer Value). The values of this field apply as follows: 000 – 101 - Message packet is delayed until either the packet is full or the timer has expired when the number of CI store buffers in use exceeds this value. When the number of buffers in use does not exceed this value, the message packet is not delayed and can be sent when there is a break in the message send requests from the APC, snooper, or TLBI units. 11x - Message packet is delayed until either the packet is full or the timer has expired. To disable this function, set the threshold to a value of `101'. With this setting, the timer is active only when the number of in-use buffers is 6, which is all of them, stopping additional packets to be sent until the CI store buffers clear out.
14:17	RW	MAX_LPC_DATA_PBH0_CI_STORE_BUFFERS: This field is the maximum number of PHB port 0 CI Store Buffers that can be used for LPC data packets. Six CI Store Buffers are available and a minimum of two are reserved for message data packets. 00: Four buffers can be used. 01: One buffer can be used. 10: Two buffers can be used. 11: Three buffers can be used.
18:21	RW	TLBI_DATA_POLL_PULSE_DIV: Number of data polls received before signaling TLBI hang-detection timer has expired.
22:25	RW	SN_WRT_DBUF_MAX_CREDIT: Defines the maximum number of snooper write-data cache lines that can be sent to PSL without return of credit (LPC mode). This configuration is for the number of credits available per snooper data queue in the PSL. There is one snooper data queue per snooper in CAPP. For each snooper data queue, there is a counter tracking the number of credits available. For each full or partial cache line sent, a counter is incremented for the data queue specified by the snooper sending the data. When the counter reaches the value in this field, no more cache lines can be sent and are allowed to backup into the snoopers and eventually backup onto the processor bus (no snoopers to dispatch). A value of 0 in this field means 16 credits per snooper data queue.

Bits	SCOM	Field Mnemonic: Description
26:27	RW	RESERVED: Reserved.
28:36	RW	SN_MSG_MAX_CREDIT: Defines the maximum number of messages (SN_snoop, SN_write, tlbi_set, ASE, APC credit consumer) that can be sent to PSL without return of credit. For each message sent requiring a credit, a counter is incremented. When the counter reaches the value in this field, no more messages can be sent that require credits. A value of 0 in this field means 512 credits. Initialized to 32.
37	RW	BENIGN_PTR_DATA: Used to indicate the format of the line sent during rTagPool flush sequence when the rfs_class = '10' 0 = Sends a line of all zeros 1 = Sends a line of all ones
38	RW	TLBIE_STALL_EN: Enables CAPP stalling the PSL if CAPP is overflowing with TLBIES.
39:41	RW	TLBIE_STALL_THRESHOLD: The number of TLBIES pending required before the CAPP starts the stall count. Minimum is 1; maximum is 7.
42:45	RW	TLBIE_STALL_CMPLT_CNT: The number of TLBIES to be completed before CAPP stops stalling the PSL. Minimum that should be set is 1; maximum is 8.
46:53	RW	TLBIE_STALL_DELAY_CNT: The number of cycles CAPP waits while over the threshold before stalling the PSL. This count is in increments of 128 cycles, up to 32 K. A value of zero is invalid.
54:57	RO	constant = 0b0000
58:61	RW	XPT_CI_BUFF_MIN: Determines the lowest value CI store buffer used in the PHB.
62	RW	CI_BUFF_AVAIL: The number of CI store buffers available in the PHB, 0 = 6 buffers 1 = 14 buffers
63	WO	LOAD_CI_BUFF: Initial setup of the lowest CI Store Buffer Used counter and PHB RTAG generation.

Register Name	Canned pResp Map Register 0
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_CAN_PRESP_REG0
Address	000000000201081D (SCOM)
Description	This register controls the canned pResp issued to the processor bus by the snooper in the event an rCmd hits the directory but the snoop uOP table access fails for any reason.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	CXA_SNP_0_CANNED_PRESP_0: For composite directory states 0 – 31. If the corresponding bit = 1 and the snoop uOP table lookup for this rCmd failed regardless of cause, a pResp of lpc_ack is issued.
32:63	RW	CXA_SNP_0_CANNED_PRESP_1: For composite directory states 0 - 31 plus 32. If the corresponding bit = 1 and the snoop uOP table lookup for this rCmd failed regardless of cause, a pResp of rty_lpc is issued.

Register Name	Canned pResp Map Register 1
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_CAN_PRESP_REG1
Address	000000000201081E (SCOM)
Description	This register controls the canned pResp issued to the processor bus by the snooper in the event an rCmd hits the directory, but the snoop uOP table access fails for any reason.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	CXA_SNP_1_CANNED_PRESP_0: For composite directory states 0 - 31. If the corresponding bit = 1 and the snoop uOP table lookup for this rCmd fails regardless of cause, a pResp of lpc_ack is issued.

Bits	SCOM	Field Mnemonic: Description
32:63	RW	CXA_SNP_1_CANNED_PRESP_1: For composite directory states 0 - 31 plus 32. If the corresponding bit = 1 and the snoop uOP table lookup for this rCmd fails regardless of cause, a pResp of rty_lpc is issued.

Register Name	Canned pResp Map Register 2
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_CAN_PRESP_REG2
Address	000000000201081F (SCOM)
Description	This register controls the canned pResp issued to the processor bus by the snooper in the event an rCmd hits the directory, but the snoop uOP table access fails for any reason.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	CXA_SNP_2_CANNED_PRESP_0: For composite directory states 0 – 31. If the corresponding bit = 1 and the snoop uOP table look-up for this rCmd fails regardless of cause, a pResp of lpc_ack is issued.
32:63	RW	CXA_SNP_2_CANNED_PRESP_1: For composite directory states 0 - 31 plus 32. If the corresponding bit = 1 and the snoop uOP table look-up for this rCmd fails regardless of cause, a pResp of rty_lpc is issued.

Register Name	Flush cp_ig State Map Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.FLUSHCPIG
Address	0000000002010820 (SCOM)
Description	This register has one bit per state decode. A 1 requires a flush with cp_ig during directory flush.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	FLUSH_CP_IG_STATE_MAP: DIR Flush cp_ig state map. One bit per state decode.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	APC Master LCO Target Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.APCLCO
Address	0000000002010821 (SCOM)
Description	This register controls LCO target selection.

Bits	SCOM	Field Mnemonic: Description
0:11	RW	APCLCO_TARGET_VALID: List of valid LCO targets.
12	RW	APCLCO_TARGET_ID0: Used for bit 0 of LCO target_id.
13:15	RW	APCLCO_TARGET_MIN: Minimum number of eligible LCO targets. Must be > = the sum of valid targets.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	XPT PMU Events Select Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.XPT_PMU_EVENTS_SEL
Address	0000000002010822 (SCOM)
Description	This register selects which of the 64 events are on each bit of the PMU output bus.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	XPT_PMON_GROUP_SELECT: Selects which one of 64 XPT PMU events sources bit 0 of the 8-bit XPT PMU output bus.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	APC FSM Read Machine Mask Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.APCRDFSMMASK
Address	0000000002010823 (SCOM)
Description	This register controls RD FSM. It can then be used in CAPP. Must match values used in the PHB configuration register (TBD), CAPP Snoop PHB tTag Filter Mask Register, and PSL machine allocation register (TBD).

Bits	SCOM	Field Mnemonic: Description
0:47	RW	APC_RDFSM_MASK: List of RD FSMs used by APC.
48:63	RO	constant = 0b0000000000000000

Register Name	PMU Counter B Configuration Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.PMU_CNTRB_CFG
Address	0000000002010824 (SCOM)
Description	This register controls the configuration of the PMU counters.

Bits	SCOM	Field Mnemonic: Description
0	RW	PMUB_COUNTER0_ENABLE: When set to 1, this bit enables PMU Counter0.
1	RW	PMUB_COUNTER1_ENABLE: When set to 1, this bit enables PMU Counter1.
2	RW	PMUB_COUNTER2_ENABLE: When set to 1, this bit enables PMU Counter2.
3	RW	PMUB_COUNTER3_ENABLE: When set to 1, this bit enables PMU Counter3.
4:6	RW	PMUB_PRESCALER_SELECT: Determines which, if any, prescaler counter to apply to all 16-bit PMU counters.
7	RW	PMUB_COUNTER_FREEZE_MODE: Indicates a counter should freeze on overflow. 0 = Free running 1 = Freeze on overflow
8	RW	PMUB_COUNTER_RESET_MODE: Indicates how a counter should reset. 0 = Free running 1 = Reset on SCOM read
9:12	RW	PMUB_COUNTER0_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter0.
13	RW	PMUB_COUNTER0_POSEDGE_SELECT: When set to 1, the PMU only counts the event rising edge. When set to 0, the PMU counts every cycle the event is asserted (high).
14:15	RW	PMUB_COUNTER0_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
16:19	RW	PMUB_COUNTER1_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter1.
20	RW	PMUB_COUNTER1_POSEDGE_SELECT: When set to 1, the PMU only counts the event rising edge. When set to 0, the PMU counts every cycle the event is asserted (high).

Bits	SCOM	Field Mnemonic: Description
21:22	RW	PMUB_COUNTER1_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
23:26	RW	PMUB_COUNTER2_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter2.
27	RW	PMUB_COUNTER2_POSEDGE_SELECT: When set to 1, the PMU only counts the event rising edge. When set to 0, the PMU will count every cycle the event is asserted (high).
28:29	RW	PMUB_COUNTER2_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
30:33	RW	PMUB_COUNTER3_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter3.
34	RW	PMUB_COUNTER3_POSEDGE_SELECT: When set to 1, the PMU only counts the event rising edge. When set to 0, the PMU counts every cycle the event is asserted (high).
35:36	RW	PMUB_COUNTER3_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
37:38	RW	PMUB_PMU_PORT_SELECT: Chooses final PMU events to feed to the counters.
39:63	RO	constant = 0b00000000000000000000000000

Register Name	**PMU Counters B Register**
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_PMULET.PMU_CNTRB_REG
Address	0000000002010825 (SCOM)
Description	The PMU Counters B Register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PMU_COUNTERB_0: PMU counter0.
16:31	ROX	PMU_COUNTERB_1: PMU counter1.
32:47	ROX	PMU_COUNTERB_2: PMU counter2.
48:63	ROX	PMU_COUNTERB_3: PMU counter3.

Register Name	**TOD SYNC000 Register**
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_TOD.TOD_SYNC000
Address	0000000002010826 (SCOM)
Description	tod sync000

Bits	SCOM	Field Mnemonic: Description
0:54	RWX	TIMEBASE: Timebase register.
55:59	ROX	TIMEBASE: Timebase register.
60:63	WO	CHIP_TOD_STATUS: Chip time of day status.

Register Name	CAPP Timebase Control Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_TOD.TFMR
Address	0000000002010827 (SCOM)
Description	This register is the time facility management register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	Reserved field.
8:9	RW	Reserved field.
10	RW	Reserved field.
11:13	RW	Reserved field.
14	RW	Reserved field.
15	RW	Reserved field.
16	RWX	Reserved field.
17	RWX	Reserved field.
18	RWX	Reserved field.
19	RWX	Reserved field.
20	RWX	Reserved field.
21	RWX	Reserved field.
22	RWX	Reserved field.
23	RWX	Reserved field.
24	WOX	Reserved field.
25:26	RO	constant = 0b00
27	WOX_CLEAR	Reserved field.
28:31	ROX	Reserved field.
32:35	ROX	Reserved field.
36:39	RO	constant = 0b0000
40	ROX	Reserved field.
41	ROX	Reserved field.
42	ROX	Reserved field.
43	WOX_CLEAR	Reserved field.
44	WOX_CLEAR	Reserved field.
45	WOX_CLEAR	Reserved field.
46	WOX_CLEAR	Reserved field.
47:50	ROX	CHIP_TOD_STATUS: Chip time of day status.
51	ROX	Reserved field.
52:59	RO	constant = 0b00000000
60	WOX_CLEAR	Reserved field.

Register Name	Snoop Array Address Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ARRAY_ADDR_REG
Address	0000000002010828 (SCOM)
Description	This register is used to SCOM read and write of the SNP Arrays.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RWX	CXA_SNP_ARRAY_ADDRESS: SNP SCOM array address.
16:63	RO	constant = 0b0000000000000000000000000000000000000000000000000

Register Name	Snoop Array Read Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ARRAY_READ_REG
Address	0000000002010829 (SCOM)
Description	This register holds data read via SCOM of the SNP arrays.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	CXA_SNP_ARRAY_READ_DATA: SNP SCOM array read data.

Register Name	APC Master Array Address Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC1.APC_ARRY_ADDR
Address	000000000201082A (SCOM)
Description	This register holds the address for Array Access 2 instances of CRESP arrays to get four read ports. Writes to either instance writes to both. Read-only reads from one instance. encd_array_select: CRESP read copy0/write copies 0 - 1 for decodes = 0x0 through 0x5. uop read/write for decode = 0x6. CRESP read copy1/write copies 0 - 1 for decodes = 0x8 through 0xC. array_address: address for selected array. This register increments on each access initiated by R/W to the APC Array Data Register.

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant = 0b00
2	RWX	Reserved field.
3:11	RWX	APCARY_ADDRESS: Address for APC Master Array access.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	APC Master Array Read Data Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC1.APC_ARRY_RDDATA
Address	000000000201082B (SCOM)
Description	This register holds read data for array access read from array reads data. The address used is in the APC Array Data Register and is auto-incremented when the W/R operation completes.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	APCARY_RDDATA: Read data for APC master array access.

Register Name	CAPP Epoch and Recovery Timers Control Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_EPT.CAPP_EPOCH_AND_RECOVERY_TMR_CONTROL
Address	000000000201082C (SCOM)
Description	This register contains the enables and period controls for the epoch and recovery timers.

Bits	SCOM	Field Mnemonic: Description
0	RW	EPOCH_TIMER_ENABLE: When set to 1, the epoch timer is enabled. When set to 0, it is disabled.
1	RW	RECOVERY_TIMER_ENABLE: When set to 1, the recovery Timer is enabled. When set to 0, it is disabled.
2:31	RO	constant = 0b00000000000000000000000000000000
32:47	RW	EPOCH_TIMER_PERIOD_MASK: The mask determines the timer period. The mask and timer incrementers are bitwise ORed and AND reduced. When the output of the AND is 1, the timer has expired. By filling in the mask with ones from the most-significant bit to the least-significant bit, the timer pulse is divided by powers of 2. If zeros are placed between ones in the mask, the timer divider is be non-uniform.
48:63	RW	RECOVERY_TIMER_PERIOD_MASK: The mask determines the timer period. The mask and timer incrementers are bitwise ORed and AND reduced. When the output of the AND is 1, the timer has expired. By filling in the mask with ones from the most-significant bit to the least-significant bit, the timer pulse is divided by powers of 2. If zeros are placed between ones in the mask, the timer divider will be non-uniform.

Register Name	APC Master PSL TTYPE Remap Register 0
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.PSLTTMAP0
Address	000000000201082D (SCOM)
Description	This register is used for POWER8 backward compatibility mode to map a PSL TTYPE/TSIZE to a new PSL ttype. When enabled, a match on ttype(0:4) and non-masked tsize(0:6) in a POWER8 PSL command causes the PSL ttype to be replaced with psl_ttype_replace(0:5). Only 1 of the 4 PSLTTMAP registers causes a replacement.

Bits	SCOM	Field Mnemonic: Description
0	RW	PSLTTMAP0_VALID: Enable.
1:5	RW	PSLTTMAP0_TTYPE_MATCH: psl_ttype(0:4) value to compare for in the PSL command.
6:12	RW	PSLTTMAP0_TSIZE_MATCH: psl_tsize(0:6) value to compare for in the PSL command.
13:19	RW	PSLTTMAP0_TSIZE_MASK: psl_tsize(0:6) mask for compare. When set to 1, forces a match for that bit.
20:25	RW	PSLTTMAP0_TTYPE_REPLACE: psl_ttype(0:5) to use for replacement on match.
26:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	APC Master PSL TTYPE Remap Register 1
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.PSLTTMAP1
Address	000000000201082E (SCOM)
Description	This register is used for POWER8 backward compatibility mode to map a PSL TTYPE/TSIZE to a new PSL TTYPE. When enabled, a match on ttype(0:4) and non-masked tsize(0:6) in a POWER8 PSL command causes the PSL TTYPE to be replaced with psl_ttype_replace(0:5). Only one of the four PSLTTMAP registers causes a replacement.

Bits	SCOM	Field Mnemonic: Description
0	RW	PSLTTMAP1_VALID: Enable.

Bits	SCOM	Field Mnemonic: Description
1:5	RW	PSLTTMAP1_TTYPE_MATCH: psl_ttype(0:4) value to compare for in PSL command.
6:12	RW	PSLTTMAP1_TSIZE_MATCH: psl_tsize(0:6) value to compare for in PSL command.
13:19	RW	PSLTTMAP1_TSIZE_MASK: psl_tsize(0:6) mask for compare. When set to 1, forces a match for that bit.
20:25	RW	PSLTTMAP1_TTYPE_REPLACE: psl_ttype(0:5) to use for replacement on match.
26:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	**APC Master PSL TTYPE Remap Register 2**
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.PSLTTMAP2
Address	0000000002010 82F (SCOM)
Description	This register is used for POWER8 backward compatibility mode to map a PSL TTYPE/TSIZE to a new PSL TTYPE. When enabled, a match on ttype(0:4) and non-masked tsize(0:6) in a POWER8 PSL command causes the PSL TTYPE to be replaced with psl_ttype_replace(0:5). Only one of the four PSLTTMAP registers causes a replacement.

Bits	SCOM	Field Mnemonic: Description
0	RW	PSLTTMAP2_VALID: Enable.
1:5	RW	PSLTTMAP2_TTYPE_MATCH: psl_ttype(0:4) value to compare for in PSL command.
6:12	RW	PSLTTMAP2_TSIZE_MATCH: psl_tsize(0:6) value to compare for in PSL command.
13:19	RW	PSLTTMAP2_TSIZE_MASK: psl_tsize(0:6) mask for compare. When set to 1, forces a match for that bit.
20:25	RW	PSLTTMAP2_TTYPE_REPLACE: psl_ttype(0:5) to use for replacement on match.
26:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	**APC Master PSL TTYPE Remap Register 3**
Mnemonic	CAPP0.CXA_TOP.CXA_APC0.PSLTTMAP3
Address	0000000002010830 (SCOM)
Description	This register is used for POWER8 backward compatibility mode to map a PSL TTYPE/TSIZE to a new PSL TTYPE. When enabled, a match on ttype(0:4) and non-masked tsize(0:6) in a POWER8 PSL command causes the PSL TTYPE to be replaced with psl_ttype_replace(0:5). Only one of the four PSLTTMAP registers causes a replacement.

Bits	SCOM	Field Mnemonic: Description
0	RW	PSLTTMAP3_VALID: Enable.
1:5	RW	PSLTTMAP3_TTYPE_MATCH: psl_ttype(0:4) value to compare for in PSL command.
6:12	RW	PSLTTMAP3_TSIZE_MATCH: psl_tsize(0:6) value to compare for in PSL command.
13:19	RW	PSLTTMAP3_TSIZE_MASK: psl_tsize(0:6) mask for compare. When set to 1, forces a match for that bit.
20:25	RW	PSLTTMAP3_TTYPE_REPLACE: psl_ttype(0:5) to use for replacement on match.
26:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	PHB TTAG Filter Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_PHB_TTAG_FILTER_REG
Address	0000000002010831 (SCOM)
Description	This register is used to define which of the 48 APC FSMs Read Machines are available for use and, thus, which tTags to care about.

Bits	SCOM	Field Mnemonic: Description
0:47	RW	CXA_SNP_PHB_TTAG_FILTER: For APC FSMs 0 - 47, set each bit to 1 for each queue that is available to CAPP for use.
48:63	RO	constant = 0b0000000000000000

Register Name	Remote Address Base Address/Mask Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_REMOTE_ADDR_BAR_BARM_REG
Address	0000000002010840 (SCOM)
Description	This register contains the base address/mask to determine whether a processor bus address hits the remote address space in the off-chip FPGA. When hit, it causes the assertion of the BHR DIR value in the address pipeline. The remote BAR represents the addresses owned by the PSL, which is a memory controller LPC.

Bits	SCOM	Field Mnemonic: Description
0	RW	CXA_SNP_BAR_EN: BAR enable.
1:18	RW	CXA_SNP_BAR_SIZE: BAR size.
19:45	RW	CXA_SNP_BAR_STARTING_ADDRESS: BAR starting address.
46:49	RO	constant = 0b0000
50:54	RW	CXA_SNP_BAR_SYSTEM: 5-bit system address.
55:63	RO	constant = 0b000000000

Register Name	Snoop Array Write Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ARRAY_WRITE_REG
Address	0000000002010841 (SCOM)
Description	This register is the SCOM write data for SNP arrays.

Bits	SCOM	Field Mnemonic: Description
0:63	WO	CXA_SNP_ARRAY_WRITE_DATA: SNP SCOM array write data.

Register Name	APC Master Array Write Data Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC1.APC_ARRY_WRDATA
Address	0000000002010842 (SCOM)
Description	This register holds write data for array access write-to-array writes to this register. The address used is in the APC Array Address Register. The address is auto-incremented when W/R operation completes.

Bits	SCOM	Field Mnemonic: Description
0:63	WOX	APCARY_WRDATA: W/R data for APC master array access.

Register Name	Flush uOP Configuration Register
Mnemonic	CAPP0.CXA_TOP.CXA_APC1.DFSUOP1
Address	0000000002010843 (SCOM)
Description	This register is the uOP1 word used during directory flush.

Bits	SCOM	Field Mnemonic: Description
0:55	RW	DFSUOP1_WORD:
56:63	RO	constant = 0b00000000

Register Name	Remote Address Base Address/Mask Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_REMOTE_ADDR_BAR_BARM_REG1
Address	0000000002010844 (SCOM)
Description	This register contains the base address/mask to determine whether a processor bus address hits the remote address space in the off-chip FPGA. When hit, it causes the assertion of the BHR DIR value in the address pipeline. The remote BAR represents the addresses owned by the PSL, which is a memory controller LPC.

Bits	SCOM	Field Mnemonic: Description
0	RW	CXA_SNP_BAR1_EN: BAR enable.
1:18	RW	CXA_SNP_BAR1_SIZE: BAR Size.
19:45	RW	CXA_SNP_BAR1_STARTING_ADDRESS: BAR starting address.
46:49	RO	constant = 0b0000
50:54	RW	CXA_SNP_BAR1_SYSTEM: 5-bit system address.
55:63	RO	constant = 0b000000000

Register Name	Link Delay Timer Register
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_TIMER
Address	0000000002010845 (SCOM)
Description	This register contains the 29-bit counter and status bits.

Bits	SCOM	Field Mnemonic: Description
0:28	ROX	LINK_DELAY_TIMER_VALUE: 29-bit LFSR counter value.
29:31	RO	constant = 0b000
32	ROX	LINK_TIMER_VALID: When set to 0, timer value is not valid. When set to 1, timer value is valid.
33	ROX	LINK_RESP_PKT_RCV: When set to 0, response packet has not been received. When set to 1, response packet received.
34	ROX	LINK_SECURE_LINK_ERR: When set to 0, no error detected, When set to 1, error detected.
35:63	RO	constant = 0b00000000000000000000000000000

Register Name	AS Endpoint Tuple Register 0
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE0
Address	0000000002010846 (SCOM)
Description	AS endpoint tuple register 0 .

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RWX	ASE_TUPLE0_LPID: LPID (0:11).
06:19:00 AM	RO	constant = 0b0000
20:39	RWX	ASE_TUPLE0_PID: PID (0:15).
40:43	RO	constant = 0b0000
44:59	RWX	ASE_TUPLE0_TID: TID (0:15).
60:62	RO	constant = 0b000
63	RWX	ASE_TUPLE0_VALID: Valid.

Register Name	AS Endpoint Tuple Register 1
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE1
Address	0000000002010847 (SCOM)
Description	AS Endpoint tuple register 1 .

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RWX	ASE_TUPLE1_LPID: LPID (0:11).
16:19	RO	constant = 0b0000
20:39	RWX	ASE_TUPLE1_PID: PID (0:15).
40:43	RO	constant = 0b0000
44:59	RWX	ASE_TUPLE1_TID: TID (0:15).
60:62	RO	constant = 0b000
63	RWX	ASE_TUPLE1_VALID: Valid.

Register Name	AS Endpoint Tuple Register 2
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE2
Address	0000000002010848 (SCOM)
Description	AS endpoint tuple register 2.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RWX	ASE_TUPLE2_LPID: LPID (0:11).
16:19	RO	constant = 0b0000
20:39	RWX	ASE_TUPLE2_PID: PID (0:15).

Bits	SCOM	Field Mnemonic: Description
40:43	RO	constant = 0b0000
44:59	RWX	ASE_TUPLE2_TID: TID (0:15).
60:62	RO	constant = 0b000
63	RWX	ASE_TUPLE2_VALID: Valid.

Register Name	AS Endpoint Tuple Reg 3
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE3
Address	0000000002010849 (SCOM)
Description	AS endpoint tuple register 3.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RWX	ASE_TUPLE3_LPID: LPID (0:11).
16:19	RO	constant = 0b0000
20:39	RWX	ASE_TUPLE3_PID: PID (0:15).
40:43	RO	constant = 0b0000
44:59	RWX	ASE_TUPLE3_TID: TID (0:15).
60:62	RO	constant = 0b000
63	RWX	ASE_TUPLE3_VALID: Valid.

Register Name	Remote MMIO Base Address/Mask Register
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_REMOTE_MMIO_BAR_BARM_REG
Address	000000000201084A (SCOM)
Description	This register contains the base address/mask to determine whether a processor bus address hits the remote MMIO space in the off-chip FPGA. When hit, it causes the assertion of the BHR DIR value in the address pipeline. The remote BAR represents the addresses owned by the PSL, which is a memory controller LPC.

Bits	SCOM	Field Mnemonic: Description
0	RW	CXA_SNP_MMIO_BAR_EN: BAR enable.
1:12	RO	constant = 0b000000000000
13:21	RW	CXA_SNP_MMIO_BAR_MS_GROUP_CHIP: Must match reflected address bits 13:21 for memory select, group, and chip ID.
22:52	RW	CXA_SNP_MMIO_BAR_STARTING_ADDRESS: BAR starting address.
53:63	RO	constant = 0b00000000000

Register Name	Remote MMIO Base Address/Mask Register 1
Mnemonic	CAPP0.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_REMOTE_MMIO_BAR_BARM_REG1
Address	000000000201084B (SCOM)
Description	This register contains the base address/mask to determine whether a processor bus address hits the remote MMIO space in the off-chip FPGA. When hit, it causes the assertion of the BHR DIR value in the address pipeline. The remote BAR represents the addresses owned by the PSL, which is a memory controller LPC.

Bits	SCOM	Field Mnemonic: Description
0	RW	CXA_SNP_MMIO_BAR1_EN: BAR enable.
1:12	RO	constant = 0b000000000000
13:21	RW	CXA_SNP_MMIO_BAR1_MS_GROUP_CHIP: Must match reflected address bits 13:21 for memory select, group and chip ID.
22:52	RW	CXA_SNP_MMIO_BAR1_STARTING_ADDRESS: BAR starting address.
53:63	RO	constant = 0b00000000000

Register Name	Link Delay Response Data Buffer Register 0
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA0
Address	0000000002010850 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 1
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA1
Address	0000000002010851 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 2
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA2
Address	0000000002010852 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 3
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA3
Address	0000000002010853 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 4
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA4
Address	0000000002010854 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 5
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA5
Address	0000000002010855 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 6
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA6
Address	0000000002010856 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 7
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA7
Address	0000000002010857 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 8
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA8
Address	0000000002010858 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 9
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA9
Address	0000000002010859 (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 10
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA10
Address	000000000201085A (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 11
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA11
Address	000000000201085B (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 12
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA12
Address	000000000201085C (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 13
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA13
Address	000000000201085D (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 14
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA14
Address	000000000201085E (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	Link Delay Response Data Buffer Register 15
Mnemonic	CAPP0.CXA_TOP.CXA_XPT.XPT_SCOMFIR.LINK_DELAY_RESP_DATA15
Address	000000000201085F (SCOM)
Description	This register contains 8 bytes of a 128-byte line buffer used to hold the link-delay response packet.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved field.

Register Name	CDM Status Register
Mnemonic	NX.DMA.SU_STATUS
Address	0000000002011040 (SCOM)
Description	CDM Status Register

Bits	SCOM	Field Mnemonic: Description
0:53	RO	constant = 0b00000000000000000000000000000000000000000000000000000
54	RWX	HMI_ACTIVE: NX has driven an HMI Interrupt (local checkstop) to the system.
55	ROX	PBI_IDLE: No requests being processed or queued from PBI.
56	ROX	DMA_CH0_IDLE: No current or pending requests are being processed by channel 0.
57	ROX	DMA_CH1_IDLE: No current or pending requests are being processed by channel 1.
58	ROX	DMA_CH2_IDLE: No current or pending requests are being processed by channel 2.
59	ROX	DMA_CH3_IDLE: No current or pending requests are being processed by channel 3.
60	ROX	DMA_CH4_IDLE: No current or pending requests are being processed by channel 4.
61:63	RO	constant = 0b000

Register Name	DMA Engine Enable Register
Mnemonic	NX.DMA.SU_ENGINE_ENABLE
Address	0000000002011041 (SCOM)
Description	DMA Engine Enable Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	ALLOW_CRYPTO: Enables CRYPTO eFUSE value.
1:56	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
57	RWX	CH3_SYM_ENABLE: Enables channel 3 SYM engine. Cannot be set when allow_crypto = 0.
58	RWX	CH2_SYM_ENABLE: Enables channel 2 SYM engine. Cannot be set when allow_crypto = 0.
59:60	RO	constant = 0b00
61	RW	CH4_GZIP_ENABLE: Enables channel 4 GZIP engine.
62	RW	CH1_EFT_ENABLE: Enables channel 1 842 engine.
63	RW	CH0_EFT_ENABLE: Enables channel 0 842 engine.

Register Name	DMA Configuration Register
Mnemonic	NX.DMA.SU_INBOUND_WRITE_CONTROL
Address	0000000002011042 (SCOM)
Description	DMA Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:11	RW	GZIPCOMP_MAX_INRD: Maximum number of outstanding inbound PBI read requests per channel for GZIP compression.
12:15	RW	GZIPDECOMP_MAX_INRD: Maximum number of outstanding inbound PBI read requests per channel for GZIP decompression.
16	RW	GZIP_COMP_PREFETCH_ENABLE: Enable for compression read prefetch hint for GZIP.
17	RW	GZIP_DECOMP_PREFETCH_ENABLE: Enable for decompression read prefetch hint for GZIP.
18:22	RO	constant = 0b00000
23	RW	EFT_COMP_PREFETCH_ENABLE: Enable for compression read prefetch hint for 842.
24	RW	EFT_DECOMP_PREFETCH_ENABLE: Enable for decompression read prefetch hint for 842.
25:28	RW	SYM_MAX_INRD: Maximum number of outstanding inbound PBI read requests per symmetric channel.
29:32	RO	constant = 0b0000
33:36	RW	EFTCOMP_MAX_INRD: Maximum number of outstanding inbound PBI read requests per channel for 842 compression/bypass.
37:40	RW	EFTDECOMP_MAX_INRD: Maximum number of outstanding inbound PBI read requests per channel for 842 decompression.
41:47	RO	constant = 0b0000000
48	RW	SYM_CPB_CHECK_DISABLE: Hardware checking of AES/SHA CPB parameters.
49:55	RO	constant = 0b0000000
56	RW	EFT_SPBC_WRITE_ENABLE: Enable SPBC write for 842.
57:63	RO	constant = 0b0000000

Register Name	Channel 0 Current CSB Address Register
Mnemonic	NX.DMA.SU_CH0_ABORT_CSB
Address	0000000002011043 (SCOM)
Description	Channel 0 Current CSB Address Register

Bits	SCOM	Field Mnemonic: Description
0:59	ROX	Reserved.
60:62	RO	constant = 0b000
63	ROX	Reserved.

Register Name	Channel 1 Current CSB Address Register
Mnemonic	NX.DMA.SU_CH1_ABORT_CSB
Address	0000000002011045 (SCOM)
Description	Channel 1 Current CSB Address Register

Bits	SCOM	Field Mnemonic: Description
0:59	ROX	Reserved.
60:62	RO	constant = 0b000
63	ROX	Reserved.

Register Name	Channel 2 Current CSB Address Register
Mnemonic	NX.DMA.SU_CH2_ABORT_CSB
Address	0000000002011047 (SCOM)
Description	Channel 2 Current CSB Address Register

Bits	SCOM	Field Mnemonic: Description
0:59	ROX	Reserved.
60:62	RO	constant = 0b000
63	ROX	Reserved.

Register Name	Channel 3 Current CSB Address Register
Mnemonic	NX.DMA.SU_CH3_ABORT_CSB
Address	0000000002011049 (SCOM)
Description	Channel 3 Current CSB Address Register

Bits	SCOM	Field Mnemonic: Description
0:59	ROX	Reserved.
60:62	RO	constant = 0b000
63	ROX	Reserved.

Register Name	Channel 4 Current CSB Address Register
Mnemonic	NX.DMA.SU_CH4_ABORT_CSB
Address	000000000201104B (SCOM)
Description	Channel 4 Current CSB Address Register

Bits	SCOM	Field Mnemonic: Description
0:59	ROX	Reserved.
60:62	RO	constant = 0b000
63	ROX	Reserved.

Register Name	CRB Kill Request Register
Mnemonic	NX.DMA.SU_CRB_KILL_REQ
Address	0000000002011053 (SCOM)
Description	CRB Kill Request Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	CRB_KILL_ENABLE: Enable CRB kill action in NX.
1	RWX	CRB_KILL_DONE: CRB kill finished.
2	RWX	CRB_KILL_SUMMARY: Set by hardware if at least one CRB has been killed in the unit. Logically the or_reduce of bits 4:15 of this register.
3	RO	constant = 0b0
4:7	RWX	CRB_KILL_DISPATCH_SLOT_KILLED_CNT: Count of the CRBs matching the send window context ID match value that have been removed from the dispatch slots in UMAC.
8:11	RWX	CRB_KILL_PREFETCH_CHANNEL_CNT: Count of the CRBs matching the send window context ID match value that have been removed from the DMA Controller prefetch channel.
12:15	RWX	CRB_KILL_ACTIVE_CHANNEL_CNT: Count of the CRBs matching the send window context ID match value that have been removed from the DMA Controller current channel and algorithm engine.
16:31	RWX	CRB_KILL_SWC_VALUE: Send window context ID match value for CRB Kill.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Performance Monitor Control 0 Register
Mnemonic	NX.DMA.SU_PERFMON_CONTROL_0
Address	0000000002011054 (SCOM)
Description	Performance Monitor Control 0 Register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	PERFMON_LPID: LPID for PERFMON configuration matching.
12:23	RW	PERFMON_LPID_MASK: LPID match-enable mask for PERFMON configuration matching.
24:43	RW	PERFMON_PID: PID for PERFMON configuration matching.
44:63	RW	PERFMON_PID_MASK: PID match enable mask for PERFMON configuration matching.

Register Name	Performance Monitor Control 1 Register
Mnemonic	NX.DMA.SU_PERFMON_CONTROL_1
Address	0000000002011055 (SCOM)
Description	Performance Monitor Control 1 Register

Bits	SCOM	Field Mnemonic: Description
0:26	RO	constant = 0b00000000000000000000000000
27:28	RW	PERFMON_GZIP_FC_SELECT: FC select for GZIP performance monitoring events. 0x = All 10 = Compress 11 = Decompress
29:30	RW	PERFMON_842_FC_SELECT: FC select for 842 performance monitoring events. 0x = All 10 = Compress 11 = Decompress
31:34	RW	PERFMON_DMA_MUX_SELECT: Performance monitor DMA multiplexer selects.
35:37	RW	PERFMON_EFT_MUX_SELECT: Performance monitor EFT multiplexer selects.
38:40	RW	PERFMON_GZIP_MUX_SELECT: Performance monitor GZIP multiplexer selects.
41:44	RW	PERFMON_ERAT_MUX_SELECT: Performance monitor ERAT multiplexer selects.
45:47	RW	PERFMON_UMAC_MUX_SELECT: Performance monitor UMAC multiplexer selects.
48:51	RW	PERFMON_PBI_MUX_SELECT: Performance monitor PBI multiplexer selects.
52	RW	PERFMON_SHA_LATENCY_CFG: Marking configuration for sha. 0 : HW 1 : HW with match
53	RO	constant = 0b0
54	RW	PERFMON_MD5_LATENCY_CFG: Marking configuration for MD5. 0 : HW 1 : HW with match
55	RO	constant = 0b0
56	RW	PERFMON_AES_LATENCY_CFG: Marking configuration for AES. 0 : HW 1 : HW with match
57	RO	constant = 0b0
58	RW	PERFMON_AESSHA_LATENCY_CFG: Marking configuration for AESSHA. 0 : HW 1 : HW with match
59	RO	constant = 0b0
60	RW	PERFMON_GZIP_LATENCY_CFG: Marking configuration for GZIP. 0 : HW 1 : HW with match
61	RO	constant = 0b0
62	RW	PERFMON_842_LATENCY_CFG: Marking configuration for 842. 0 : HW 1 : HW with match
63	RO	constant = 0b0

Register Name	DMA CERR Report Register 0
Mnemonic	NX.DMA.SU_DMA_ERROR_REPORT_0
Address	0000000002011057 (SCOM)
Description	DMA CERR Report Register 0

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	DMA_ERROR_REPORT_0:

Register Name	DMA CERR Report Register 1
Mnemonic	NX.DMA.SU_DMA_ERROR_REPORT_1
Address	0000000002011058 (SCOM)
Description	DMA CERR Report Register 1

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	DMA_ERROR_REPORT_1:
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	EFT Maximum Byte Count Register
Mnemonic	NX.DMA.EFT_MAX_BYTE_CNT
Address	0000000002011059 (SCOM)
Description	EFT Maximum Byte Count Register

Bits	SCOM	Field Mnemonic: Description
0:4	RW	EFT_MAX_BYTE_CNT_LIMIT: Maximum byte count for 842 engine operations.
5:12	RW	EFT_MAX_SRC_DDE_CNT: EFT maximum source DDE count.
13:20	RW	EFT_MAX_TARGET_DDE_CNT: EFT maximum target DDE count.
21:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	SYM Maximum Byte Count Register
Mnemonic	NX.DMA.SYM_MAX_BYTE_CNT
Address	000000002201105A (SCOM)
Description	SYM Maximum Byte Count Register

Bits	SCOM	Field Mnemonic: Description
0:4	RW	SYM_MAX_BYTE_CNT_LIMIT: Maximum byte count for SYM engine operations.
5:12	RW	SYM_MAX_SRC_DDE_CNT: SYM maximum source DDE count.
13:20	RW	SYM_MAX_TARGET_DDE_CNT: SYM maximum target DDE count.
21:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	GZIP Maximum Byte Count Register
Mnemonic	NX.DMA.GZIP_MAX_BYTE_CNT
Address	000000000201105B (SCOM)
Description	GZIP Maximum Byte Count Register

Bits	SCOM	Field Mnemonic: Description
0:4	RW	GZIP_MAX_BYTE_CNT_LOW: Maximum byte count low threshold for GZIP engine operations.
5:9	RW	GZIP_MAX_BYTE_CNT_HIGH: Maximum byte count high threshold for GZIP engine operations.
10	RW	GZIP_MAX_BYTE_CNT_THRESHOLD: Maximum byte count high is applied when this bit is set. Otherwise, Maximum byte count low is applied.
11:18	RW	GZIP_MAX_SRC_DDE_CNT: GZIP maximum source DDE count.
19:26	RW	GZIP_MAX_TARGET_DDE_CNT: GZIP maximum target DDE count.
27:63	RO	constant = 0b00000000000000000000000000000000000000000

Register Name	Watchdog and Hang Timers Control Register
Mnemonic	NX.DMA.WATCHDOG_HANG_TIMERS_CNTL
Address	000000000201105C (SCOM)
Description	Watchdog and Hang Timers Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CH0_WATCHDOG_TIMER_ENBL: Channel 0 watchdog timer is enabled.
1:4	RW	CH0_WATCHDOG_REF_DIV: This field allows the watchdog timer reference oscillator to be divided by powers of two.
5	RW	CH1_WATCHDOG_TIMER_ENBL: Channel 1 watchdog timer is enabled.
6:9	RW	CH1_WATCHDOG_REF_DIV: This field allows the watchdog timer reference oscillator to be divided by powers of two.
10	RW	CH2_WATCHDOG_TIMER_ENBL: Channel 2 watchdog timer is enabled.
11:14	RW	CH2_WATCHDOG_REF_DIV: This field allows the watchdog timer reference oscillator to be divided by powers of two.
15	RW	CH3_WATCHDOG_TIMER_ENBL: Channel 3 Watchdog Timer is enabled.
16:19	RW	CH3_WATCHDOG_REF_DIV: This field allows the watchdog timer reference oscillator to be divided by powers of two.
20	RW	CH4_WATCHDOG_TIMER_ENBL: Channel 4 watchdog timer is enabled.
21:24	RW	CH4_WATCHDOG_REF_DIV: This field allows the watchdog timer reference oscillator to be divided by powers of two.
25	RW	DMA_HANG_TIMER_ENBL: DMA hang timer is enabled.
26:29	RW	DMA_HANG_TIMER_REF_DIV: This field allows the DMA hang timer reference oscillator to be divided by powers of two.
30:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	DMA VAS MMIO BAR Register
Mnemonic	NX.DMA.DMA_VAS_MMIO_BAR
Address	000000000201105E (SCOM)
Description	DMA VAS MMIO BAR Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:38	RW	VAS_MMIO_BAR: Base address of VAS MMIO region.
39:63	RO	constant = 0b00000000000000000000000000

Register Name	PBI CQ FIR Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_REG
Address	0000000002011080 (SCOM) 0000000002011081 (SCOM1) 0000000002011082 (SCOM2)
Description	PBI CQ FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PBI_PE_FIR: PBI internal parity error.
1	RWX	WOX_AND	WOX_OR	PBUS_ECC_CE_FIR: Processor bus CE error.
2	RWX	WOX_AND	WOX_OR	PBUS_ECC_UE_FIR: Processor bus UE error.
3	RWX	WOX_AND	WOX_OR	PBUS_ECC_SUE_FIR: Processor bus SUE error.
4	RWX	WOX_AND	WOX_OR	INBD_ARRAY_ECC_CE_FIR: Inbound array CE error.
5	RWX	WOX_AND	WOX_OR	INBD_ARRAY_ECC_UE_FIR: Inbound array UE error.
6	RWX	WOX_AND	WOX_OR	PASTE_REJECT_FIR: Paste request rejected.
7	RWX	WOX_AND	WOX_OR	PBUS_CMD_HANG_FIR: Processor bus command hang error.
8	RWX	WOX_AND	WOX_OR	PBUS_READ_ARE_FIR: Processor bus read address error.
9	RWX	WOX_AND	WOX_OR	PBUS_WRITE_ARE_FIR: Processor bus write address error.
10	RWX	WOX_AND	WOX_OR	PBUS_MISC_HW_FIR: Processor bus miscellaneous error.
11	RWX	WOX_AND	WOX_OR	MMIO_BAR_PE_FIR: MMIO BAR parity error.
12	RWX	WOX_AND	WOX_OR	UMAC_WC_INT_ADDR_UE_FIR: UMAC detected SUE on WC Interrupt.
13	RWX	WOX_AND	WOX_OR	PBUS_LOAD_LINK_ERR_FIR: ACK_DEAD CRESP received by read command.
14	RWX	WOX_AND	WOX_OR	PBUS_STORE_LINK_ERR_FIR: ACK_DEAD CRESP received by write command.
15	RWX	WOX_AND	WOX_OR	PBUS_LINK_ABORT_FIR: Link check aborted while waiting on data.
16	RWX	WOX_AND	WOX_OR	PBI_INTERNAL_HANG_FIR: Hang poll time expired on internal transfer.
17	RWX	WOX_AND	WOX_OR	ERAT_ARRAY_PE_FIR: Parity error on ERAT arrays.
18	RWX	WOX_AND	WOX_OR	ERAT_ARRAY_CE_FIR: Correctable error on ERAT arrays.
19	RWX	WOX_AND	WOX_OR	ERAT_ARRAY_UE_FIR: Uncorrectable error on ERAT arrays.
20	RWX	WOX_AND	WOX_OR	ERAT_ARRAY_SUE_FIR: Special uncorrectable error on ERAT arrays.
21	RWX	WOX_AND	WOX_OR	ERAT_CICO_HANG_FIR: Hang on checkin/checkout request to NMMU.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22	RWX	WOX_AND	WOX_OR	ERAT_CNTRL_ERR_FIR: ERAT control logic error.
23	RWX	WOX_AND	WOX_OR	PB_XLAT_DATA_UE_FIR: Uncorrectable error on the processor bus data for xlate.
24	RWX	WOX_AND	WOX_OR	PB_XLAT_DATA_SUE_FIR: Special uncorrectable error on the processor bus data for XLATE.
25	RWX	WOX_AND	WOX_OR	UMAC_LD_LINK_ERR_FIR: ACK_DEAD CRESP received by UMAC read command.
26	RWX	WOX_AND	WOX_OR	UMAC_LINK_ABORT_FIR: Link check aborted while waiting on UMAC data.
27	RWX	WOX_AND	WOX_OR	UMAC_CRB_UE_FIR: Uncorrectable error on CRB QW0/4.
28	RWX	WOX_AND	WOX_OR	UMAC_CRB_SUE_FIR: Special uncorrectable error on CRB QW0/4.
29	RWX	WOX_AND	WOX_OR	ERAT_LOCAL_CSTOP_FIR: UMAC has detected a control logic error.
30	RWX	WOX_AND	WOX_OR	Reserved field.
31	RWX	WOX_AND	WOX_OR	Reserved field.
32	RWX	WOX_AND	WOX_OR	RNG_FIRST_FAIL_FIR: A first noise source in the RNG has failed.
33	RWX	WOX_AND	WOX_OR	RNG_SECOND_FAIL_FIR: A second noise source in the RNG has failed.
34	RWX	WOX_AND	WOX_OR	RNG_CNTRL_LOGIC_ERR_FIR: RNG has detected a control logic error.
35	RWX	WOX_AND	WOX_OR	NMMU_LOCAL_XSTOP_FIR: NMMU has signaled local checkstop.
36	RWX	WOX_AND	WOX_OR	VAS_LOCAL_XSTOP_FIR: VAS has signaled local checkstop.
37	RWX	WOX_AND	WOX_OR	PBCQ_CNTRL_LOGIC_ERR_FIR: PBCQ has detected a control logic error.
38	RWX	WOX_AND	WOX_OR	FAILED_LINK_ON_INTERRUPT_FIR: PBCQ has detected a failed link on an interrupt.
39:41	RWX	WOX_AND	WOX_OR	Reserved field.
42	RWX	WOX_AND	WOX_OR	FIR_SCOM_PE_FIR: FIR/SCOM satellite parity error.
43	RWX	WOX_AND	WOX_OR	FIR_SCOM_PE_DUP_FIR: FIR/SCOM satellite parity error duplicate.
44:63	RO	RO	RO	constant = 0b0000000000000000000

Register Name	PBI CQ FIR Mask Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_MASK_REG
Address	0000000002011083 (SCOM) 0000000002011084 (SCOM1) 0000000002011085 (SCOM2)
Description	PBI CQ FIR Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:43	RW	WO_AND	WO_OR	NX_CQ_FIR_MASK:
44:63	RO	RO	RO	constant = 0b0000000000000000000

Register Name	PBI CQ FIR Action0 Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_ACTION0_REG
Address	0000000002011086 (SCOM)
Description	This register is an action select for the corresponding bit in FIR. (Action0, Action1) = Action select (0, 0) = Checkstop (0, 1) = Recoverable (1, 0) = Unused (1, 1) = Local checkstop

Bits	SCOM	Field Mnemonic: Description
0:43	RW	NX_CQ_FIR_ACTION0:
44:63	RO	constant = 0b00000000000000000000

Register Name	PBI CQ FIR Action1 Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_ACTION1_REG
Address	0000000002011087 (SCOM)
Description	This register is an action select for the corresponding bit in FIR. (Action0, Action1) = Action select (0, 0) = Checkstop (0, 1) = Recoverable (1, 0) = Unused (1, 1) = Local checkstop

Bits	SCOM	Field Mnemonic: Description
0:43	RW	NX_CQ_FIR_ACTION1:
44:63	RO	constant = 0b00000000000000000000

Register Name	PBI CQ FIR WOF Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_WOF_REG
Address	0000000002011088 (SCOM)
Description	PBI CQ FIR WOF Register

Bits	SCOM	Field Mnemonic: Description
0:43	RWX_WCLRREG	Reserved.
44:63	RO	constant = 0b00000000000000000000

Register Name	Processor Bus MMIO BAR Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_MMIO_BAR
Address	000000002201108D (SCOM)
Description	processor bus MMIO BAR Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:51	RW	MMIO_BAR: MMIO bar for NX.
52	RW	MMIO_BAR_ENABLE: Enable MMIO for NX.
53:63	RO	constant = 0b00000000000

Register Name	Processor Bus Debug Control Register 1
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_DEBUG_REG
Address	0000000002011090 (SCOM)
Description	processor bus Debug Control Register 1

Bits	SCOM	Field Mnemonic: Description
0:7	RW	NXCQ_TRACE_CNTL: 0:2 Trace select 000-011 : CQ machines 100 : SHM-CQ interface 101-111 : Unused 3 0 - Sequentially rotate through the set of queues 0 ... 15 1 - Trace the Select Queues set of queuesTrace a fixed queue number when tracing queues 4:7 Queue number when tracing a fixed queue.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	NX Processor Bus Error Injection Configuration Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_ECC_REG
Address	0000000002011091 (SCOM)
Description	NX processor bus Error Injection Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	NXCQ_ECC_INJECT_MODE: Determines the number of times to inject the ECC error.
2:3	RW	NXCQ_ECC_INJECT_TYPE: Determines the type of ECC error injected.
4	RW	NXCQ_PBCQ_INJECT_ENABLE: Enables ECC inject on PBCQ arrays.
5:8	RW	NXCQ_PBCQ_ARRAY: 000 = DMA read, high half of the data (0:63, itag(0)) 001 = DMA read, low half of the data (64:127, itag(1)) 100 = Checkout Response 110 = CRB UMAC Data, high half of the data (0:63) 111 = CRB UMAC Data, low half of the data (64:127)
9:15	RW	Reserved.
16	RW	NXCQ_RNG_INJECT_ENABLE: 0 = Error inject disabled. 1 = Error inject enabled
17	RW	NXCQ_RNG_INJECT_ACTION: 0 = Inject error once at next array access (single) 1 = Inject error for every array access (continuous)
18:23	RW	Reserved.
24	RW	NXCQ_ERAT_ARRAY_ENABLE: 0 = Error inject disabled 1 = Error inject enabled.

Bits	SCOM	Field Mnemonic: Description
25	RW	NXCQ_ERAT_ARRAY_TYPE: 0 = Single-bit error 1 = double-bit error
26	RW	NXCQ_ERAT_ARRAY_ACTION: 0 = Inject error once at next array access (single) 1 = Inject error for every array access (continuous)
27:30	RW	NXCQ_ERAT_ARRAY_SELECT: 0000 = WC ID CAM 0001 = WC QW0 0010 = WC QW1 0011 = WC PSWID 0100 = FSW 0101 = MissQueue 0110 = Checkout/in request 0111 = ERAT CAM 1000 = ERAT RA
31:63	RO	constant = 0b0000000000000000000000000000000000000

Register Name	Processor Bus MODE Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NXCQ_PB_MODE_REG
Address	0000000002011095 (SCOM)
Description	processor bus MODE Register

Bits	SCOM	Field Mnemonic: Description
0	RW	DMA_WR_DISABLE_LN: For DMA write machine requests: 0 = Master can request Ln scope 1 = Master shall not request Ln scope
1	RW	DMA_WR_DISABLE_GROUP: For DMA write machine requests: 0 = Master can request G scope 1 = Master shall not request G scope
2	RW	DMA_WR_DISABLE_VG_NOT_SYS: For DMA write machine requests: 0 = Master can request Vg scope 1 = Master shall not request Vg scope, but can use Vg (SYS).
3	RW	DMA_WR_DISABLE_NN_RN: For DMA write machine requests: 0 = Master can request Nn or Rn scope 1 = Master shall not request Nn or Rn scope
4	RW	DMA_RD_DISABLE_LN: For DMA read machine requests: 0 Master can request Ln scope 1 = Master shall not request Ln scope.
5	RW	DMA_RD_DISABLE_GROUP: For DMA read machine requests: 0 = Master can request G scope 1 = Master shall not request G scope
6	RW	DMA_RD_DISABLE_VG_NOT_SYS: For DMA read machine requests: 0 = Master can request Vg scope 1 = Master shall not request Vg scope, but can use Vg (SYS)
7	RW	DMA_RD_DISABLE_NN_RN: For DMA read machine requests: 0 Master can request Nn or Rn scope 1 Master shall not request Nn or Rn scope

Bits	SCOM	Field Mnemonic: Description
8	RW	UMAC_WR_DISABLE_LN: For UMAC write machine requests: 0 Master can request Ln scope 1 Master shall not request Ln scope
9	RW	UMAC_WR_DISABLE_GROUP: For UMAC write machine requests: 0 = Master can request G scope 1 = Master shall not request G scope
10	RW	UMAC_WR_DISABLE_VG_NOT_SYS: For UMAC write machine requests: 0 = Master can request Vg scope 1 = Master shall not request Vg scope, but can use Vg (SYS)
11	RW	UMAC_WR_DISABLE_NN_RN: For UMAC write machine requests: 0 = Master can request Nn or Rn scope 1 = Master shall not request Nn or Rn scope
12	RW	UMAC_RD_DISABLE_LN: For UMAC read machine requests: 0 = Master can request Ln scope 1 = Master shall not request Ln scope
13	RW	UMAC_RD_DISABLE_GROUP: For UMAC read machine requests: 0 = Master can request G scope 1 = Master shall not request G scope
14	RW	UMAC_RD_DISABLE_VG_NOT_SYS: For UMAC read machine requests: 0 = Master can request Vg scope 1 = Master shall not request Vg scope, but can use Vg (SYS)
15	RW	UMAC_RD_DISABLE_NN_RN: For UMAC read machine requests: 0 = Master can request Nn or Rn scope 1 = Master shall not request Nn or Rn scope
16:17	RW	NX_FREEZE_MODES: Data arbitration priority percentage: 00 = Behavior unchanged 01 = Pass data/ECC as is 10 = Freeze data pattern with good ECC 11 = Illegal
18:19	RW	RESERVED: Reserved.
20	RW	DMA_WR_NOT_INJECT: For DMA writes. When set to 1, a write machine shall not issue cl_dma_inj, but rather cl_dma_w. When set to 0, a write machine can issue cl_dma_inj.
21	RW	DMA_PARTIAL_WRT_NOT_INJECT: For DMA partial writes. When set to 1, a write machine shall not issue dma_pr_inj, but rather dma_pr_w. When set to 0, a write machine can issue dma_pr_inj.
22	RW	RD_GO_M_QOS: Controls the setting of the quality of service (q) bit in the secondary encode of the rd_go_m command. This command is only issued as the read (R) of the WRP protocol. If this bit = 1, the q bit = 1. This means high quality of service, that is, the memory controller must treat this as a high-priority request.
23	RW	ADDR_BAR_MODE: Specifies the address mapping mode in use for the system. 0 = Small system address map. Reduces the number of group ID bits to 2 and eliminates the chip ID bits. All chips have an ID of 0. Nn scope is not available in this mode. 1 = Large system address map. Uses 4 bits for the group ID and 3 bits for the chip ID.
24	RW	SKIP_G: Scope mode control set by firmware when the topology is chip = group. **Note**: This CS does not disable the use of group scope. It modifies the progression of scope when the command starts at nodal scope. 0 = The progression from nodal to group scope is followed when the combined response indicates rty_inc or sfStat (as applicable to the command) is set. 1 = When the scope of the command is nodal and the command is in the Read, RWITM, or is an atomic RMW and fetch command (found in the Ack_BK group), and the combined response is rty_inc or the sfStat is set in the data, the command scope progression skips group and goes to Vg scope.

Bits	SCOM	Field Mnemonic: Description
25:26	RW	DATA_ARB_LFSR_CONFIG: Data arbitration priority percentage: 00 = Choose XLATE 50% of the time 01 = Choose XLATE 75% of the time 10 = Choose XLATE 88% of the time 11 = Choose XLATE 100% of the time
27	RW	NXCQ_HANG_SM_ON_ARE: The control to enable or disable hanging the master FSM on a combined response of addr_error. When set to 1, a master getting an addr_error combined response hangs. This is used as a debug aid and must be disabled (set to 0).
28	RW	NXCQ_HANG_SM_ON_LINK_FAIL: The control to enable or disable hanging the master FSM on a combined response of ack_*dead. When set to 1, a master getting an ack_*dead combined response hangs. This is used as a debug aid and must be disabled (set to 0).
29	RW	CFG_PUMP_MODE: NX uses this control only for unit random backoff 0 = chip_is_node. Ln scope is constrained to the master's chip group. Scope is constrained to all chips specified by the topology as part of the group (coherent logical X link connections). 1 = chip_is_group. Both Ln and G scope are constrained to the master's chip. In this mode, it is recommended that skip_g be set for best performance.
30	RW	DISABLE_FLOW_SCOPE: Set to 1 to disable the use of flow based scope in the write queues.
31	RW	DISABLE_PMU_SNOOPING: Set to 1 to disable snooping of Global PMU command.
32	RW	ENDABLE_PMU_CNT_RESET: Set to 1 to enable resetting PMU counters by snooped PMISC global PMU command.
33	RW	DISABLE_WRP: Set to 1 to disable the WRP protocol.
34:39	RW	Unused: Unused.
40:47	RW	DMA_RD_VG_RESET_TIMER_MASK: Mask for timer to reset read Vg scope predictor: FF = 64 K cycles FE = 32 K cycles FC = 16 K cycles F8 = 8 K cycles 80 = 512 cycles.
48:55	RW	DMA_WR_VG_RESET_TIMER_MASK: Mask for timer to reset write Vg scope predictor: FF = 64 K cycles FE = 32 K cycles FC = 16 K cycles F8 = 8 K cycles 80 = 512 cycles
56:63	RO	constant = 0b00000000

Register Name	Processor Bus Error Report Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_ERR_RPT_1
Address	00000000020110A1 (SCOM)
Description	processor bus Error Report Register

Bits	SCOM	Field Mnemonic: Description
0:10	RO	Reserved field.
11:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	Processor Bus Parity Error Report Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_ERR_RPT_0
Address	00000000020110A2 (SCOM)
Description	processor bus parity Error Report Register

Bits	SCOM	Field Mnemonic: Description
0:62	RO	Reserved field.
63	ROX	NX_PBI_WRITE_IDLE: All PBI write engines are idle.

Register Name	NX Snapshot of Debug Bus Bits 0 to 63
Mnemonic	NX.PBI.CQ_WRAP.NX_DEBUG_SNAPSHOT_0
Address	00000000020110A4 (SCOM)
Description	NX Snapshot of Debug Bus bits 0 to 63

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	NX_DEBUG_SNAPSHOT_B0_63: NX snapshot of debug bus bits 0 - 63.

Register Name	NX Snapshot of Debug Bus bits 64 to 87
Mnemonic	NX.PBI.CQ_WRAP.NX_DEBUG_SNAPSHOT_1
Address	00000000020110A5 (SCOM)
Description	NX Snapshot of Debug Bus bits 64 to 87

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	NX_DEBUG_SNAPSHOT_B64_87: NX snapshot of debug bus bits 64 – 87.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	NX PMU0 Control Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PMU0_CONTROL_REG
Address	00000000020110A6 (SCOM)
Description	NX PMU0 Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PMU0_ENABLE: When set to 1, this bit enables PMUlet0.
1	RW	NX_PMU0_FREEZE: When set to 1, this bit freezes the counters.
2	RW	NX_PMU0_RESET: When set to 1, this bit generates a reset pulse.
3	RW	NX_PMU0_DIS_GLOB_SCOM: When set to 1, this bit disables the effect of the Global PMISC command on the PMULet.
4:5	RW	NX_PMU0_PRESCALAR_SEL0: Determines the prescalar counter to apply to counter 0.
6:7	RW	NX_PMU0_PRESCALAR_SEL1: Determines the prescalar counter to apply to counter 1.
8:9	RW	NX_PMU0_PRESCALAR_SEL2: Determines the prescalar counter to apply to counter 2.
10:11	RW	NX_PMU0_PRESCALAR_SEL3: Determines the prescalar counter to apply to counter 3.

Bits	SCOM	Field Mnemonic: Description
12:13	RW	NX_PMU0_CNT0_PAIR_OP: Indicates how the event pairs should be combined to increment counter 0.
14:15	RW	NX_PMU0_CNT1_PAIR_OP: Indicates how the event pairs should be combined to increment counter 1.
16:17	RW	NX_PMU0_CNT2_PAIR_OP: Indicates how the event pairs should be combined to increment counter 2.
18:19	RW	NX_PMU0_CNT3_PAIR_OP: Indicates how the event pairs should be combined to increment counter 3.
20:22	RW	NX_PMU0_CNT0_MUX_SEL: Select 8-bit bus to route to the PMUlet counter 0.
23:25	RW	NX_PMU0_CNT1_MUX_SEL: Select 8-bit bus to route to the PMUlet counter 1.
26:28	RW	NX_PMU0_CNT2_MUX_SEL: Select 8-bit bus to route to the PMUlet counter 2.
29:31	RW	NX_PMU0_CNT3_MUX_SEL: Select 8-bit bus to route to the PMUlet counter 3.
32	RW	NX_PMU0_FREEZE_ON_OVERFLOW: When set to 1, this bit freezes the counters when any of the counters overflows.
33:35	RW	NX_PMU0_CASCADE: PMU counter cascade SEL.
36:63	RO	constant = 0b00000000000000000000000000000

Register Name	**NX PMU0 Counter Register**
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PMU0_COUNTER_REG
Address	00000000020110A7 (SCOM)
Description	NX PMU0 Counter Register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	NX_PMU0_COUNTER_0: NX PMU0 counter 0.
16:31	ROX	NX_PMU0_COUNTER_1: NX PMU0 counter 1.
32:47	ROX	NX_PMU0_COUNTER_2: NX PMU0 counter 2.
48:63	ROX	NX_PMU0_COUNTER_3: NX PMU0 counter 3.

Register Name	**NX Miscellaneous Control Register**
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_MISC_CONTROL_REG
Address	00000000020110A8 (SCOM)
Description	NX Miscellaneous Control Register

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:7	RW	HANG_POLL_SCALE: Determines how many hang polls must be detected to indicate a hang poll to the logic.
8:11	RW	HANG_DATA_SCALE: Determines how many data polls must be detected to indicate a data poll to the logic.
12:15	RW	HANG_SHM_SCALE: Determines how many data polls must be detected to indicate a shim poll to the logic. A shim poll is created by the CQ logic to detect hangs of SMs while waiting on exchanges with the shim logic.
16:19	RW	ERAT_DATA_POLL_SCALE: Determines how many data polls must be detected to indicate a data poll to the ERAT logic.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	NX PMU1 Control Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PMU1_CONTROL_REG
Address	00000000020110A9 (SCOM)
Description	NX PMU1 Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PMU1_ENABLE: When set to 1, this bit enables PMUlet1.
1	RW	NX_PMU1_FREEZE: When set to 1, this bit freezes the counters.
2	RW	NX_PMU1_RESET: When set to 1, this bit generates a reset pulse.
3	RW	NX_PMU1_DIS_GLOB_SCOM: When set to 1, this bit disables the effect of the Global PMISC command on the PMULet.
4:5	RW	NX_PMU1_PRESCALAR_SEL0: Determines the prescalar counter to apply to counter 0.
6:7	RW	NX_PMU1_PRESCALAR_SEL1: Determines the prescalar counter to apply to counter 1.
8:9	RW	NX_PMU1_PRESCALAR_SEL2: Determines the prescalar counter to apply to counter 2.
10:11	RW	NX_PMU1_PRESCALAR_SEL3: Determines the prescalar counter to apply to counter 3.
12:13	RW	NX_PMU1_CNT0_PAIR_OP: Indicates how the event pairs must be combined to increment counter 0.
14:15	RW	NX_PMU1_CNT1_PAIR_OP: Indicates how the event pairs must be combined to increment counter 1.
16:17	RW	NX_PMU1_CNT2_PAIR_OP: Indicates how the event pairs must be combined to increment counter 2.
18:19	RW	NX_PMU1_CNT3_PAIR_OP: Indicates how the event pairs must be combined to increment counter 3.
20:22	RW	NX_PMU1_CNT0_MUX_SEL: Select 8-bit bus to route to the PMUlet counter 0.
23:25	RW	NX_PMU1_CNT1_MUX_SEL: Select 8-bit bus to route to the PMUlet counter 1.
26:28	RW	NX_PMU1_CNT2_MUX_SEL: Select 8-bit bus to route to the PMUlet counter 2.
29:31	RW	NX_PMU1_CNT3_MUX_SEL: Select 8-bit bus to route to the PMUlet counter 3.
32	RW	NX_PMU1_FREEZE_ON_OVERFLOW: When set to 1, this bit freezes the counters when any of the counters overflow.
33:35	RW	NX_PMU1_CASCADE: PMU counter cascade SEL.
36:63	RO	constant = 0b00000000000000000000000000000

Register Name	NX PMU1 Counter Register
Mnemonic	NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PMU1_COUNTER_REG
Address	00000000020110AA (SCOM)
Description	NX PMU1 Counter Register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	NX_PMU1_COUNTER_0: NX PMU1 Counter 0.
16:31	ROX	NX_PMU1_COUNTER_1: NX PMU1 Counter 1.
32:47	ROX	NX_PMU1_COUNTER_2: NX PMU1 Counter 2.
48:63	ROX	NX_PMU1_COUNTER_3: NX PMU1 Counter 3.

Register Name	UMAC EFT High-Priority Receive FIFO BAR Register
Mnemonic	NX.PBI.PBI_UMAC.EFT_HI_PRIOR_RCV_FIFO_BAR
Address	00000000020110C0 (SCOM)
Description	This register specifies the base address and size of the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:53	RW	EFT_HI_PRIORITY_RCV_FIFO_BAR: EFT high-priority receive FIFO BAR.
54:56	RW	EFT_HI_PRIORITY_RCV_FIFO_BAR_SIZE: EFT high-priority receive FIFO size.
57:63	RO	constant = 0b0000000

Register Name	UMAC SYM High-Priority Receive FIFO BAR Register
Mnemonic	NX.PBI.PBI_UMAC.SYM_HI_PRIOR_RCV_FIFO_BAR
Address	00000000020110C1 (SCOM)
Description	This register specifies the base address and size of the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:53	RW	SYM_HI_PRIORITY_RCV_FIFO_BAR: SYM high-priority receive FIFO BAR.
54:56	RW	SYM_HI_PRIORITY_RCV_FIFO_BAR_SIZE: SYM high-priority receive FIFO size.
57:63	RO	constant = 0b0000000

Register Name	UMAC GZIP High-Priority Receive FIFO BAR Register
Mnemonic	NX.PBI.PBI_UMAC.GZIP_HI_PRIOR_RCV_FIFO_BAR
Address	00000000020110C2 (SCOM)
Description	This register specifies the base address and size of the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:53	RW	GZIP_HI_PRIORITY_RCV_FIFO_BAR: GZIP high-priority receive FIFO BAR.
54:56	RW	GZIP_HI_PRIORITY_RCV_FIFO_BAR_SIZE: GZIP high-priority receive FIFO size.
57:63	RO	constant = 0b0000000

Register Name	UMAC EFT High-Priority Receive FIFO Control Register
Mnemonic	NX.PBI.PBI_UMAC.EFT_HI_PRIOR_RCV_FIFO_CNTL
Address	00000000020110C3 (SCOM)
Description	This register defines various access and arbitration controls with the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000

Bits	SCOM	Field Mnemonic: Description
4:11	RWX	EFT_HI_PRIORITY_RCV_FIFO_READ_OFFSET: EFT high-priority receive FIFO read Offset.
12:14	RO	constant = 0b000
15:23	RWX	EFT_HI_PRIORITY_RCV_FIFO_QUEUED: EFT high-priority receive FIFO queued Count.
24:26	RO	constant = 0b000
27:35	RW	EFT_HI_PRIORITY_RCV_FIFO_HI_PRIMAX: EFT high-priority receive FIFO maximum CRBs.
36:63	RO	constant = 0b00000000000000000000000000000

Register Name	**UMAC SYM High-Priority Receive FIFO Control Register**
Mnemonic	NX.PBI.PBI_UMAC.SYM_HI_PRIOR_RCV_FIFO_CNTL
Address	00000000020110C4 (SCOM)
Description	This register defines various access and arbitration controls with the associated Receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:11	RWX	SYM_HI_PRIORITY_RCV_FIFO_READ_OFFSET: SYM high-priority receive FIFO read offset.
12:14	RO	constant = 0b000
15:23	RWX	SYM_HI_PRIORITY_RCV_FIFO_QUEUED: SYM high-priority receive FIFO queued count.
24:26	RO	constant = 0b000
27:35	RW	SYM_HI_PRIORITY_RCV_FIFO_HI_PRIMAX: SYM high-priority receive FIFO maximum CRBs.
36:63	RO	constant = 0b00000000000000000000000000000

Register Name	**UMAC GZIP High-Priority Receive FIFO Control Register**
Mnemonic	NX.PBI.PBI_UMAC.GZIP_HI_PRIOR_RCV_FIFO_CNTL
Address	00000000020110C5 (SCOM)
Description	This register defines various access and arbitration controls with the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:11	RWX	GZIP_HI_PRIORITY_RCV_FIFO_READ_OFFSET: GZIP high-priority receive FIFO read offset.
12:14	RO	constant = 0b000
15:23	RWX	GZIP_HI_PRIORITY_RCV_FIFO_QUEUED: GZIP high-priority receive FIFO queued count.
24:26	RO	constant = 0b000
27:35	RW	GZIP_HI_PRIORITY_RCV_FIFO_HI_PRIMAX: GZIP high-priority receive FIFO maximum CRBs.
36:63	RO	constant = 0b00000000000000000000000000000

Register Name	UMAC EFT High-Priority Receive FIFO ASB Match Register
Mnemonic	NX.PBI.PBI_UMAC.EFT_HI_PRIOR_RCV_FIFO_ASB
Address	00000000020110C6 (SCOM)
Description	This register contains the LPID, PID, and TID values that must match the LPID, PID, and TID values presented by a snooped asb_notify if the asb_notify is to be acknowledged.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RW	EFT_HI_PRIORITY_RCV_FIFO_ASB_LPID: LPID.
16:19	RO	constant = 0b0000
20:39	RW	EFT_HI_PRIORITY_RCV_FIFO_ASB_PID: PID.
40:43	RO	constant = 0b0000
44:59	RW	EFT_HI_PRIORITY_RCV_FIFO_ASB_TID: TID.
60:62	RO	constant = 0b000
63	RW	EFT_HI_PRIORITY_RCV_FIFO_ASB_ENABLE: Enable.

Register Name	UMAC SYM High-Priority Receive FIFO ASB Match Register
Mnemonic	NX.PBI.PBI_UMAC.SYM_HI_PRIOR_RCV_FIFO_ASB
Address	00000000020110C7 (SCOM)
Description	This register contains the LPID, PID, and TID values that must match the LPID, PID, and TID values presented by a snooped asb_notify if the asb_notify is to be acknowledged.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RW	SYM_HI_PRIORITY_RCV_FIFO_ASB_LPID: LPID.
16:19	RO	constant = 0b0000
20:39	RW	SYM_HI_PRIORITY_RCV_FIFO_ASB_PID: PID.
40:43	RO	constant = 0b0000
44:59	RW	SYM_HI_PRIORITY_RCV_FIFO_ASB_TID: TID.
60:62	RO	constant = 0b000
63	RW	SYM_HI_PRIORITY_RCV_FIFO_ASB_ENABLE: Enable.

Register Name	UMAC GZIP High-Priority Receive FIFO ASB Match Register
Mnemonic	NX.PBI.PBI_UMAC.GZIP_HI_PRIOR_RCV_FIFO_ASB
Address	00000000020110C8 (SCOM)
Description	This register contains the LPID, PID, and TID values that must match the LPID, PID, and TID values presented by a snooped asb_notify if the asb_notify is to be acknowledged.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RW	GZIP_HI_PRIORITY_RCV_FIFO_ASB_LPID: LPID.
16:19	RO	constant = 0b0000

Bits	SCOM	Field Mnemonic: Description
20:39	RW	GZIP_HI_PRIORITY_RCV_FIFO_ASB_PID: PID.
40:43	RO	constant = 0b0000
44:59	RW	GZIP_HI_PRIORITY_RCV_FIFO_ASB_TID: TID.
60:62	RO	constant = 0b000
63	RW	GZIP_HI_PRIORITY_RCV_FIFO_ASB_ENABLE: Enable.

Register Name	UMAC EFT Normal-Priority Receive FIFO BAR Register
Mnemonic	NX.PBI.PBI_UMAC.EFT_LO_PRIOR_RCV_FIFO_BAR
Address	00000000020110C9 (SCOM)
Description	This register specifies the base address and size of the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:53	RW	EFT_LO_PRIORITY_RCV_FIFO_BAR: EFT normal-priority receive FIFO BAR.
54:56	RW	EFT_LO_PRIORITY_RCV_FIFO_BAR_SIZE: EFT normal-priority receive FIFO size.
57:63	RO	constant = 0b0000000

Register Name	UMAC SYM Normal-Priority Receive FIFO BAR Register
Mnemonic	NX.PBI.PBI_UMAC.SYM_LO_PRIOR_RCV_FIFO_BAR
Address	00000000020110CA (SCOM)
Description	This register specifies the base address and size of the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:53	RW	SYM_LO_PRIORITY_RCV_FIFO_BAR: SYM normal-priority receive FIFO BAR.
54:56	RW	SYM_LO_PRIORITY_RCV_FIFO_BAR_SIZE: SYM normal-priority receive FIFO size.
57:63	RO	constant = 0b0000000

Register Name	UMAC GZIP Normal-Priority Receive FIFO BAR Register
Mnemonic	NX.PBI.PBI_UMAC.GZIP_LO_PRIOR_RCV_FIFO_BAR
Address	00000000020110CB (SCOM)
Description	This register specifies the base address and size of the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:53	RW	GZIP_LO_PRIORITY_RCV_FIFO_BAR: GZIP normal-priority receive FIFO BAR.
54:56	RW	GZIP_LO_PRIORITY_RCV_FIFO_BAR_SIZE: GZIP normal-priority receive FIFO size.
57:63	RO	constant = 0b0000000

Register Name	UMAC EFT Low-Priority Receive FIFO Control Register
Mnemonic	NX.PBI.PBI_UMAC.EFT_LO_PRIOR_RCV_FIFO_CNTL
Address	00000000020110CC (SCOM)
Description	This register defines various access and arbitration controls with the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:11	RWX	EFT_LO_PRIORITY_RCV_FIFO_READ_OFFSET: EFT low-priority receive FIFO read offset.
12:14	RO	constant = 0b000
15:23	RWX	EFT_LO_PRIORITY_RCV_FIFO_QUEUED: EFT low-priority receive FIFO queued count.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	UMAC SYM Low-Priority Receive FIFO Control Register
Mnemonic	NX.PBI.PBI_UMAC.SYM_LO_PRIOR_RCV_FIFO_CNTL
Address	00000000020110CD (SCOM)
Description	This register defines various access and arbitration controls with the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:11	RWX	SYM_LO_PRIORITY_RCV_FIFO_READ_OFFSET: SYM low-priority receive FIFO read offset.
12:14	RO	constant = 0b000
15:23	RWX	SYM_LO_PRIORITY_RCV_FIFO_QUEUED: SYM low-priority receive FIFO queued count.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	UMAC GZIP Low-Priority Receive FIFO Control Register
Mnemonic	NX.PBI.PBI_UMAC.GZIP_LO_PRIOR_RCV_FIFO_CNTL
Address	00000000020110CE (SCOM)
Description	This register defines various access and arbitration controls with the associated receive FIFO.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:11	RWX	GZIP_LO_PRIORITY_RCV_FIFO_READ_OFFSET: GZIP low-priority receive FIFO read offset.
12:14	RO	constant = 0b000
15:23	RWX	GZIP_LO_PRIORITY_RCV_FIFO_QUEUED: GZIP low-priority receive FIFO queued count.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	UMAC EFT Normal-Priority Receive FIFO ASB Match Register
Mnemonic	NX.PBI.PBI_UMAC.EFT_LO_PRIOR_RCV_FIFO_ASB
Address	00000000020110CF (SCOM)
Description	This register contains the LPID, PID, and TID values that must match the LPID, PID, and TID values presented by a snooped asb_notify if the asb_notify is to be acknowledged.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RW	EFT_LO_PRIORITY_RCV_FIFO_ASB_LPID: LPID.
16:19	RO	constant = 0b0000
20:39	RW	EFT_LO_PRIORITY_RCV_FIFO_ASB_PID: PID.
40:43	RO	constant = 0b0000
44:59	RW	EFT_LO_PRIORITY_RCV_FIFO_ASB_TID: TID.
60:62	RO	constant = 0b000
63	RW	EFT_LO_PRIORITY_RCV_FIFO_ASB_ENABLE: Enable.

Register Name	UMAC SYM Normal-Priority Receive FIFO ASB Match Register
Mnemonic	NX.PBI.PBI_UMAC.SYM_LO_PRIOR_RCV_FIFO_ASB
Address	00000000020110D0 (SCOM)
Description	This register contains the LPID, PID, and TID values that must match the LPID, PID, and TID values presented by a snooped asb_notify if the asb_notify is to be acknowledged.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RW	SYM_LO_PRIORITY_RCV_FIFO_ASB_LPID: LPID.
16:19	RO	constant = 0b0000
20:39	RW	SYM_LO_PRIORITY_RCV_FIFO_ASB_PID: PID.
40:43	RO	constant = 0b0000
44:59	RW	SYM_LO_PRIORITY_RCV_FIFO_ASB_TID: TID.
60:62	RO	constant = 0b000
63	RW	SYM_LO_PRIORITY_RCV_FIFO_ASB_ENABLE: Enable.

Register Name	UMAC GZIP Normal-Priority Receive FIFO ASB Match Register
Mnemonic	NX.PBI.PBI_UMAC.GZIP_LO_PRIOR_RCV_FIFO_ASB
Address	00000000020110D1 (SCOM)
Description	This register contains the LPID, PID, and TID values that must match the LPID, PID, and TID values presented by a snooped asb_notify if the asb_notify is to be acknowledged.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RW	GZIP_LO_PRIORITY_RCV_FIFO_ASB_LPID: LPID.
16:19	RO	constant = 0b0000

Bits	SCOM	Field Mnemonic: Description
20:39	RW	GZIP_LO_PRIORITY_RCV_FIFO_ASB_PID: PID.
40:43	RO	constant = 0b0000
44:59	RW	GZIP_LO_PRIORITY_RCV_FIFO_ASB_TID: TID.
60:62	RO	constant = 0b000
63	RW	GZIP_LO_PRIORITY_RCV_FIFO_ASB_ENABLE: Enable.

Register Name	UMAC Send Window Context BAR Register
Mnemonic	NX.PBI.PBI_UMAC.SEND_WC_BASE_ADDR
Address	00000000020110D2 (SCOM)
Description	This register specifies the base address of the send window context (send WC) region of memory from where send WC information is fetched for a given CRB.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:40	RW	SEND_WC_BAR: Send WC BAR.
41:63	RO	constant = 0b00000000000000000000000

Register Name	UMAC Error Report 0 Register
Mnemonic	NX.PBI.PBI_UMAC.SU_UMAC_ERROR_RPT
Address	00000000020110D3 (SCOM)
Description	UMAC Error Report 0 Register

Bits	SCOM	Field Mnemonic: Description
0:55	ROX	UMAC_ERROR_RPT:
56:63	RO	constant = 0b00000000

Register Name	UMAC VAS MMIO BAR Register
Mnemonic	NX.PBI.PBI_UMAC.VAS_MMIO_BASE_ADDR
Address	00000000020110D4 (SCOM)
Description	This register specifies the base address of the MMIO region of the on-chip VAS. NX uses this BAR to return send and receive window credits.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:38	RW	VAS_MMIO_BAR: VAS MMIO BAR.
39:63	RO	constant = 0b00000000000000000000000000

Register Name	UMAC Status And Control Register
Mnemonic	NX.PBI.PBI_UMAC.UMAC_STATUS_CONTROL
Address	00000000020110D5 (SCOM)
Description	This register contains status and configuration values.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1	RWX	CRB_READS_ENBL: Enables CRB reads.
2	RWX	CRB_READS_HALTED: CRB reads halted.
3	ROX	UMAC_IDLE: UMAC is in idle state.
4	RW	QUIESCE_REQUEST: Request to check for quiesce status.
5	RWX	QUIESCE_ACHEIVED: NX in quiesce state during quiesce request.
6	RWX	QUIESCE_FAILED: NX not in quiesce state during quiesce request.
7	ROX	UMAC_QUIESCED: UMAC is quiesced.
8	RW	PASTE_ADDR_ALIGN: When generating the address for a paste to the fault send window, this. bit controls the alignment of the sendWCID(0:15) in the generated address. 0 = Align sendWCID(0:15) with address(36:51) for 4 KB page. 1 = Align sendWCID(0:15) with address(32:47) for 64 KB page.
9:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	ERAT Status and Control Register
Mnemonic	NX.PBI.PBI_SHIM.ERAT_STATUS_CONTROL
Address	00000000020110D6 (SCOM)
Description	This register contains status and configuration values.

Bits	SCOM	Field Mnemonic: Description
0	RW	FORCE_ERAT_BYPASS: ERAT configuration: Forces bypass of ERAT, RA = EA (8:63).
1	RW	ERAT_IDLE:
2	RW	ERAT_VALID_ENTRY:
3	RW	DISABLE_ERAT_HIT_UNDER_BARRIER: Disables ERAT hits when an invalidate barrier is active.
4:5	RO	constant = 0b00
6	RW	DISABLE_PROMOTE: Chicken switch: Disables promote, force checkin.
7	RW	DISABLE_CHECKIN_HANG_TIMER: Disables checkin hang timer.
8	RW	DISABLE_CHECKOUT_HANG_TIMER: Disables checkout hang timer.
9:11	RW	SPECULATIVE_CHECKIN_COUNT: Speculative checkin count.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	ERAT Error Report Register
Mnemonic	NX.PBI.PBI_UMAC.SU_ERAT_ERROR_RPT
Address	00000000020110D7 (SCOM)
Description	ERAT Error Report Register

Bits	SCOM	Field Mnemonic: Description
0:47	ROX	ERAT_ERROR_RPT:
48:63	RO	constant = 0b0000000000000000

Register Name	UMAC Error Report 1 Register
Mnemonic	NX.PBI.PBI_UMAC.SU_UMAC_ERROR_RPT1
Address	00000000020110D8 (SCOM)
Description	UMAC Error Report 1 Register

Bits	SCOM	Field Mnemonic: Description
0:5	ROX	UMAC_ERROR_RPT1:
6:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	RNG Status and Control Register
Mnemonic	NX.PBI.PBI_RNG.NX_RNG_CFG
Address	00000000020110E0 (SCOM)
Description	RNG Status and Control Register

Bits	SCOM	Field Mnemonic: Description
0:9	ROX	FAIL_REG: Self test hard fail status.
10	ROX	RNG0_FAIL: RNG0 fail status.
11	ROX	RNG1_FAIL: RNG1 fail status.
12	RW	INTERRUPT_SENT: Interrupt sent to processor bus.
13:15	RO	constant = 0b000
16	RW	BIST_ENABLE: RNG BIST enable.
17	ROX	BIST_COMPLETE: RNG BIST complete.
18	ROX	RNG0_BIST_FAIL: RNG0 BIST fail status.
19	ROX	RNG1_BIST_FAIL: RNG1 BIST fail status.
20:22	RW	BIST_BIT_FAIL_TH: RNG BIST bit fail threshold.
23	RW	RNG0_INJ_CONTINOUS_ERROR: RNG0 inject continuous error.
24	RW	RNG1_INJ_CONTINOUS_ERROR: RNG1 inject continuous error.
25:29	RO	constant = 0b00000
30:37	RW	ST2_RESET_PERIOD: RNG Self Test Register 2 reset period.
38	RW	RRN_BYPASS_ENABLE: RRN bypass enable.
39	RW	MASK_TOGGLE_ENABLE: Conditioner mask toggle enable.
40	RW	SAMPTEST_ENABLE: Samptest enable.
41	RW	REPTEST_ENABLE: Reptest enable.
42	RW	ADAPTEST_1BIT_ENABLE: Adaptest 1-bit enable.
43	RW	ADAPTEST_ENABLE: Adaptest enable.
44	ROX	COND_STARTUP_TEST_FAIL: Conditioner startup test fail.

Bits	SCOM	Field Mnemonic: Description
45	RO	constant = 0b0
46:61	RW	PACE_RATE: Pace rate.
62	RO	constant = 0b0
63	RW	RNG_ENABLE: RNG enable.

Register Name	RNG Self Test Register 0
Mnemonic	NX.PBI.PBI_RNG.NX_RNG_ST0
Address	00000000020110E1 (SCOM)
Description	RNG Self Test Register 0

Bits	SCOM	Field Mnemonic: Description
0:1	RW	REPTEST_MATCH_TH: Repetition count match count threshold.
2:6	RW	REPTEST_SOFT_FAIL_TH: Repetition count soft fail threshold.
7:8	RW	ADAPTEST_SAMPLE_SIZE: Adaptive proportion sample size.
9:11	RW	ADAPTEST_WINDOW_SIZE: Adaptive proportion window size.
12:23	RW	ADAPTEST_RRN_RNG0_MATCH_TH: Adaptive proportion RRN RNG0 match threshold.
24:35	RW	ADAPTEST_RRN_RNG1_MATCH_TH: Adaptive proportion RRN RNG1 match threshold.
36:47	RW	ADAPTEST_CRN_RNG0_MATCH_TH: Adaptive proportion CRN RNG0 match threshold.
48:59	RW	ADAPTEST_CRN_RNG1_MATCH_TH: Adaptive proportion CRN RNG1 match threshold.
60:63	RO	constant = 0b0000

Register Name	RNG Self Test Register 1
Mnemonic	NX.PBI.PBI_RNG.NX_RNG_ST1
Address	00000000020110E2 (SCOM)
Description	RNG Self Test Register 1

Bits	SCOM	Field Mnemonic: Description
0:6	RW	ADAPTEST_SOFT_FAIL_TH: Adaptive proportion soft fail threshold.
7:22	RW	ADAPTEST_1BIT_MATCH_TH_MIN: Adaptive proportion 1-bit match threshold minimum.
23:38	RW	ADAPTEST_1BIT_MATCH_TH_MAX: Adaptive proportion 1-bit match threshold maximum.
39:63	RO	constant = 0b00000000000000000000000000

Register Name	RNG Self Test Register 2
Mnemonic	NX.PBI.PBI_RNG.NX_RNG_ST2
Address	00000000020110E3 (SCOM)
Description	RNG Self Test Register 2

Bits	SCOM	Field Mnemonic: Description
0:7	RWX_WCLRREG	ADAPTEST_SOFT_FAIL_COUNT_RRN_RNG0: Adaptive proportion RRN RNG0 soft fail count.
8:15	RWX_WCLRREG	ADAPTEST_SOFT_FAIL_COUNT_RRN_RNG1: Adaptive proportion RRN RNG1 soft fail count.
16:23	RWX_WCLRREG	ADAPTEST_SOFT_FAIL_COUNT_CRN_RNG0: Adaptive proportion CRN RNG0 soft fail count.
24:31	RWX_WCLRREG	ADAPTEST_SOFT_FAIL_COUNT_CRN_RNG1: Adaptive proportion CRN RNG1 soft fail count.
32:37	RWX_WCLRREG	REPTEST_SOFT_FAIL_COUNT_RNG0: Repetition Test RNG0 soft fail count.
38:43	RWX_WCLRREG	REPTEST_SOFT_FAIL_COUNT_RNG1: Repetition Test RNG1 soft fail count.
44:63	RO	constant = 0b00000000000000000000

Register Name	RNG RRN Bypass Register
Mnemonic	NX.PBI.PBI_RNG.NX_RNG_BYPASS
Address	00000000020110E4 (SCOM)
Description	RNG RRN Bypass Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	RRN_BYPASS_DATA: RRN Bypass Data.

Register Name	RNG Read Delay Parameters Register
Mnemonic	NX.PBI.PBI_RNG.NX_RNG_RDELAY
Address	00000000020110E5 (SCOM)
Description	RNG Read Delay Parameters Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	RNG_CQ_RDELAY_FILL_THRESHOLD: Read delay fill threshold.
2:3	RW	RNG_CQ_RDELAY_DRAIN_THRESHOLD: Read delay drain threshold.
4:5	RO	constant = 0b00
6	RW	RNG_CQ_RDELAY_LFSR_RESEED_EN: Read delay LFSR reseed enable.
7:11	RW	RNG_CQ_RDELAY_READ_RTY_RATIO: Read delay Read retry ratio.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	RNG Reset Register
Mnemonic	NX.PBI.PBI_RNG.NX_RNG_RESET
Address	00000000020110E6 (SCOM)
Description	This register resets the RNG.

Bits	SCOM	Field Mnemonic: Description
0	WO_SETPART_3P	RNG_RESET: RNG reset.

Register Name	RNG Failed Interrupt Address Register
Mnemonic	NX.PBI.PBI_UMAC.RNG_FAILED_INT
Address	00000000020110E7 (SCOM)
Description	This register specifies the address used to optionally post an interrupt when both RNG noise sources have failed.

Bits	SCOM	Field Mnemonic: Description
0	RW	RNG_FAILED_INT_ENABLE: RNG failed interrupt enable.
1:7	RO	constant = 0b0000000
8:51	RW	RNG_FAILED_INT_ADDRESS: RNG failed interrupt address.
52:63	RO	constant = 0b000000000000

Register Name	RNG Self Test Register 3
Mnemonic	NX.PBI.PBI_RNG.NX_RNG_ST3
Address	00000000020110E8 (SCOM)
Description	RNG Self Test Register 3

Bits	SCOM	Field Mnemonic: Description
0	RW	SAMPTEST_RRN_ENABLE: Sample rate RRN enable.
1:3	RW	SAMPTEST_WINDOW_SIZE: Sample rate window size.
4:19	RW	SAMPTEST_MATCH_TH_MIN: Sample rate match threshold minimum.
20:35	RW	SAMPTEST_MATCH_TH_MAX: Sample rate rate maximum.
36:63	RO	constant = 0b00000000000000000000000000000000

Register Name	DMA and Engine Fault Isolation Register
Mnemonic	NX.DBG.NX_DMA_ENG_FIR
Address	0000000002011100 (SCOM) 0000000002011101 (SCOM1) 0000000002011102 (SCOM2)
Description	DMA and Engine Fault Isolation Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	RESERVED_00_FIR: Reserved FIR bit 0.
1	RWX	WOX_AND	WOX_OR	ICS_INVALID_STATE_FIR: ICS invalid state error FIR bit.
2	RWX	WOX_AND	WOX_OR	RESERVED_02_FIR: Reserved FIR bit 2.
3	RWX	WOX_AND	WOX_OR	RESERVED_03_FIR: Reserved FIR bit 3.
4	RWX	WOX_AND	WOX_OR	CH0_842_ECC_CE_FIR: Channel 0 842 array corrected ECC error FIR bit.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	CH0_842_ECC_UE_FIR: Channel 0 842 array uncorrectable ECC error FIR bit.
6	RWX	WOX_AND	WOX_OR	CH1_842_ECC_CE_FIR: Channel 1 842 array corrected ECC error FIR bit.
7	RWX	WOX_AND	WOX_OR	CH1_842_ECC_UE_FIR: Channel 1 842 array uncorrectable ECC error FIR bit.
8	RWX	WOX_AND	WOX_OR	NONZERO_CSB_CC_FIR: DMA non-zero CSB CC detected FIR bit. Programming error.
9	RWX	WOX_AND	WOX_OR	DMA_ECC_CE_FIR: DMA array correctable ECC error FIR bit.
10	RWX	WOX_AND	WOX_OR	DMA_OUTWR_INRD_ECC_CE_FIR: DMA outbound write/inbound read correctable ECC error FIR bit.
11	RWX	WOX_AND	WOX_OR	CH5_AMF_ECC_CE_FIR: Channel 5 AMF array corrected ECC error FIR bit.
12	RWX	WOX_AND	WOX_OR	CH6_AMF_ECC_CE_FIR: Channel 6 AMF array corrected ECC error FIR bit.
13	RWX	WOX_AND	WOX_OR	CH7_AMF_ECC_CE_FIR: Channel 7 AMF array corrected ECC error FIR bit.
14	RWX	WOX_AND	WOX_OR	OTHER_SCOM_SAT_FIR: Error from other SCOM satellites FIR bit.
15	RWX	WOX_AND	WOX_OR	DMA_INVALID_STATE_RECOV_FIR: DMA invalid state error FIR bit. Unrecoverable despite name.
16	RWX	WOX_AND	WOX_OR	DMA_INVALID_STATE_UNRECOV_FIR: DMA invalid state error FIR bit.
17	RWX	WOX_AND	WOX_OR	DMA_ECC_UE_FIR: DMA array uncorrectable ECC error FIR bit.
18	RWX	WOX_AND	WOX_OR	DMA_OUTWR_INRD_ECC_UE_FIR: DMA outbound write/inbound read uncorrectable ECC error FIR bit.
19	RWX	WOX_AND	WOX_OR	DMA_INRD_DONE_ERR_FIR: DMA inbound read error FIR bit.
20	RWX	WOX_AND	WOX_OR	CH0_INVALID_STATE_FIR: Channel 0 invalid state error FIR bit.
21	RWX	WOX_AND	WOX_OR	CH1_INVALID_STATE_FIR: Channel 1 invalid state error FIR bit.
22	RWX	WOX_AND	WOX_OR	CH2_INVALID_STATE_FIR: Channel 2 invalid state error FIR bit.
23	RWX	WOX_AND	WOX_OR	CH3_INVALID_STATE_FIR: Channel 3 invalid state error FIR bit.
24	RWX	WOX_AND	WOX_OR	CH4_INVALID_STATE_FIR: Channel 4 invalid state error FIR bit.
25	RWX	WOX_AND	WOX_OR	CH5_INVALID_STATE_FIR: Channel 5 invalid state error FIR bit.
26	RWX	WOX_AND	WOX_OR	CH6_INVALID_STATE_FIR: Channel 6 invalid state error FIR bit.
27	RWX	WOX_AND	WOX_OR	CH7_INVALID_STATE_FIR: Channel 7 invalid state error FIR bit.
28	RWX	WOX_AND	WOX_OR	CH5_AMF_ECC_UE_FIR: Channel 5 AMF array uncorrectable ECC error FIR bit.
29	RWX	WOX_AND	WOX_OR	CH6_AMF_ECC_UE_FIR: Channel 6 AMF array uncorrectable ECC error FIR bit.
30	RWX	WOX_AND	WOX_OR	CH7_AMF_ECC_UE_FIR: Channel 7 AMF array uncorrectable ECC error FIR bit.
31	RWX	WOX_AND	WOX_OR	CRB_ECC_UE_FIR: UE error on CRB(CSB address, CCB) FIR bit.
32	RWX	WOX_AND	WOX_OR	CRB_ECC_SUE_FIR: SUE error on CRB(CSB address, CCB) FIR bit.
33	RWX	WOX_AND	WOX_OR	DMA_OUTWR_INRD_ECC_SUE_FIR: SUE error on something other than CRB (CSB address, CCB) FIR bit.
34	RWX	WOX_AND	WOX_OR	RESERVED_34_FIR: Reserved FIR bit 34.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
35	RWX	WOX_AND	WOX_OR	RESERVED_35_FIR: Reserved FIR bit 35.
36	RWX	WOX_AND	WOX_OR	CH4_AMF_ECC_CE_FIR: Channel 4 AMF array corrected ECC error FIR bit.
37	RWX	WOX_AND	WOX_OR	CH4_AMF_ECC_UE_FIR: Channel 4 AMF array uncorrectable ECC error FIR bit.
38	RWX	WOX_AND	WOX_OR	RESERVED_38_FIR: Reserved FIR bit 38.
39	RWX	WOX_AND	WOX_OR	RESERVED_39_FIR: Reserved FIR bit 39.
40	RWX	WOX_AND	WOX_OR	RESERVED_40_FIR: Reserved FIR bit 40.
41	RWX	WOX_AND	WOX_OR	RESERVED_41_FIR: Reserved FIR bit 41.
42	RWX	WOX_AND	WOX_OR	RESERVED_42_FIR: Reserved FIR bit 42.
43	RWX	WOX_AND	WOX_OR	RESERVED_43_FIR: Reserved FIR bit 43.
44	RWX	WOX_AND	WOX_OR	RESERVED_44_FIR: Reserved FIR bit 44.
45	RWX	WOX_AND	WOX_OR	RESERVED_45_FIR: Reserved FIR bit 45.
46	RWX	WOX_AND	WOX_OR	RESERVED_46_FIR: Reserved FIR bit 46.
47	RWX	WOX_AND	WOX_OR	RESERVED_47_FIR: Reserved FIR bit 47.
48	RWX	WOX_AND	WOX_OR	FIR_SCOM_PE_FIR: FIR/SCOM satellite parity error FIR bit.
49	RWX	WOX_AND	WOX_OR	FIR_SCOM_PE_DUP_FIR: FIR/SCOM satellite parity error FIR bit duplicate.
50:63	RO	RO	RO	constant = 0b00000000000000

Register Name	DMA and Engine FIR Mask Register
Mnemonic	NX.DBG.NX_DMA_ENG_FIR_MASK
Address	0000000002011103 (SCOM) 0000000002011104 (SCOM1) 0000000002011105 (SCOM2)
Description	DMA and Engine FIR Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:49	RW	WO_AND	WO_OR	NX_DMA_ENG_FIR_MASK_BITS: DMA and Engine FIR Mask Register.
50:63	RO	RO	RO	constant = 0b00000000000000

Register Name	DMA and Engine FIR Action 0 Register
Mnemonic	NX.DBG.NX_DMA_ENG_FIR_ACTION0
Address	0000000002011106 (SCOM)
Description	DMA and Engine FIR Action 0 Register

Bits	SCOM	Field Mnemonic: Description
0:49	RW	NX_DMA_ENG_FIR_ACTION0_BITS: DMA and Engine FIR Action 0 Register.
50:63	RO	constant = 0b00000000000000

Register Name	DMA and Engine FIR Action 1 Register
Mnemonic	NX.DBG.NX_DMA_ENG_FIR_ACTION1
Address	0000000002011107 (SCOM)
Description	DMA and Engine FIR Action 1 Register

Bits	SCOM	Field Mnemonic: Description
0:49	RW	NX_DMA_ENG_FIR_ACTION1_BITS: DMA and Engine FIR Action 1 Register.
50:63	RO	constant = 0b00000000000000

Register Name	DMA and Engine FIR WOF Register
Mnemonic	NX.DBG.NX_DMA_ENG_FIR_WOF
Address	0000000002011108 (SCOM)
Description	DMA and Engine FIR WOF Register

Bits	SCOM	Field Mnemonic: Description
0:49	RWX_WCLRREG	NX_DMA_ENG_FIR_WOF_BITS: DMA and Engine FIR WOF Register.
50:63	RO	constant = 0b00000000000000

Register Name	Debug Multiplexer Control Register
Mnemonic	NX.DBG.NX_DEBUGMUX_CTRL
Address	000000000201110A (SCOM)
Description	Debug Mux Control Register

Bits	SCOM	Field Mnemonic: Description
0:46	RO	constant = 0b00000000000000000000000000000000000000000000000
47:60	RW	NX_DEBUGMUX_CTRL_BITS: NX debug bus selects.
61:63	RO	constant = 0b000

Register Name	Debug Trigger Control Register
Mnemonic	NX.DBG.NX_TRIGGER_CTRL
Address	000000000201110B (SCOM)
Description	Debug Trigger Control Register

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b0000000000000000000000000000000000000000000000000
50:61	RW	NX_TRIGGER_CTRL_BITS: NX trigger select.
62:63	RO	constant = 0b00

Register Name	DMA and Engine Error Injection Control Register
Mnemonic	NX.DBG.NX_ERRORINJ_CTRL
Address	000000000201110C (SCOM)
Description	DMA and Engine Error Injection Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant = 0b00
2	RW	CH0EFT_ERRORINJ_ENA: Channel 0 842 array error inject enable.
3	RW	CH0EFT_ERRORINJ_TYPE: Channel 0 842 array error inject type.
4	RW	CH0EFT_ERRORINJ_ACTION: Channel 0 842 array error inject action.
5:8	RW	CH0EFT_ERRORINJ_SELECT: Channel 0 842 array error inject select.
9	RW	CH1EFT_ERRORINJ_ENA: Channel 1 842 array error inject enable.
10	RW	CH1EFT_ERRORINJ_TYPE: Channel 1 842 array error inject type.
11	RW	CH1EFT_ERRORINJ_ACTION: Channel 1 842 array error inject action.
12:15	RW	CH1EFT_ERRORINJ_SELECT: Channel 1 842 array error inject select.
16:22	RO	constant = 0b0000000
23	RW	DMA_INWR_ERRORINJ_ENA: DMA inbound write error inject enable.
24	RW	DMA_INWR_ERRORINJ_TYPE: DMA inbound write error inject type.
25	RW	DMA_INWR_ERRORINJ_ACTION: DMA inbound write error inject action.
26	RW	DMA_OUTWR_ERRORINJ_ENA: DMA outbound write error inject enable.
27	RW	DMA_OUTWR_ERRORINJ_TYPE: DMA outbound write error inject type.
28	RW	DMA_OUTWR_ERRORINJ_ACTION: DMA outbound write error inject action.
29	RW	DMA_INGARRAY_ERRORINJ_ENA: DMA ingress array error inject enable.
30	RW	DMA_INGARRAY_ERRORINJ_TYPE: DMA ingress array error inject type.
31	RW	DMA_INGARRAY_ERRORINJ_ACTION: DMA ingress array error inject action.
32:35	RW	DMA_INGARRAY_ERRORINJ_SELECT: DMA ingress array error inject select.
36	RW	DMA_EGRARRAY_ERRORINJ_ENA: DMA egress array error inject enable.
37	RW	DMA_EGRARRAY_ERRORINJ_TYPE: DMA egress array error inject type.
38	RW	DMA_EGRARRAY_ERRORINJ_ACTION: DMA egress array error inject action.
39:42	RW	DMA_EGRARRAY_ERRORINJ_SELECT: DMA egress array error inject select.
43	RW	DMA_CRBARRAY_ERRORINJ_ENA: DMA CRB store array error inject enable.
44	RW	DMA_CRBARRAY_ERRORINJ_TYPE: DMA CRB store array error inject type.
45	RW	DMA_CRBARRAY_ERRORINJ_ACTION: DMA CRB store array error inject action.
46	RW	DMA_CRBARRAY_ERRORINJ_SELECT: DMA CRB store array error inject select.
47	RO	constant = 0b0
48	RW	CH4GZIP_ERRORINJ_ENA: CH4 GZIP array error inject enable.
49	RW	CH4GZIP_ERRORINJ_TYPE: CH4 GZIP array error inject type.
50	RW	CH4GZIP_ERRORINJ_ACTION: CH4 GZIP array error inject action.
51:58	RW	CH4GZIP_ERRORINJ_SELECT: CH4 GZIP array error inject select.
59	RW	DMA_OUTWR_QW0_UEINJ_ENA: DMA outbound write CRB QW0 UE inject enable.

Bits	SCOM	Field Mnemonic: Description
60	RW	DMA_OUTWR_QW4_UEINJ_ENA: DMA outbound write CRB QW4 UE inject enable.
61:63	RO	constant = 0b000

Register Name	GZIP Control Register
Mnemonic	NX.CH4.GZIP_CONTROL_REG
Address	0000000002011140 (SCOM)
Description	This register controls GZIP.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_NEAR_HISTORY: Disables near-history matches for GZIP compression.
1	RW	DISABLE_FAR_HISTORY: Disables far-history matches for GZIP compression.
2	RW	DISABLE_EXTRA_HASH_ACCESSES: Disables extra hash table accesses for GZIP compression.
3	RW	DISABLE_EXTRA_FIFO_ACCESSES: Disables extra FIFO accesses for GZIP compression.
4:7	RO	constant = 0b0000
8:15	RW	HASH_SIZE_MASK: Size of hash functions for hash table access in GZIP compression.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	GZIP Address 0 Hash Function Register
Mnemonic	NX.CH4.ADDR_0_HASH_FUNCTION_REG
Address	0000000002011141 (SCOM)
Description	GZIP Address 0 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_0_HASH_FUNCTION: Compression hash function for hash table address bit 0.

Register Name	GZIP Address 1 Hash Function Register
Mnemonic	NX.CH4.ADDR_1_HASH_FUNCTION_REG
Address	0000000002011142 (SCOM)
Description	GZIP Address 1 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_1_HASH_FUNCTION: Compression hash function for hash table address bit 1.

Register Name	GZIP Address 2 Hash Function Register
Mnemonic	NX.CH4.ADDR_2_HASH_FUNCTION_REG
Address	0000000002011143 (SCOM)
Description	GZIP Address 2 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_2_HASH_FUNCTION: Compression hash function for hash table address bit 2.

Register Name	GZIP Address 3 Hash Function Register
Mnemonic	NX.CH4.ADDR_3_HASH_FUNCTION_REG
Address	0000000002011144 (SCOM)
Description	GZIP Address 3 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_3_HASH_FUNCTION: Compression hash function for hash table address bit 3.

Register Name	GZIP Address 4 Hash Function Register
Mnemonic	NX.CH4.ADDR_4_HASH_FUNCTION_REG
Address	0000000002011145 (SCOM)
Description	GZIP Address 4 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_4_HASH_FUNCTION: Compression hash function for hash table address bit 4.

Register Name	GZIP Address 5 Hash Function Register
Mnemonic	NX.CH4.ADDR_5_HASH_FUNCTION_REG
Address	0000000002011146 (SCOM)
Description	GZIP Address 5 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_5_HASH_FUNCTION: Compression hash function for hash table address bit 5.

Register Name	GZIP Address 6 Hash Function Register
Mnemonic	NX.CH4.ADDR_6_HASH_FUNCTION_REG
Address	0000000002011147 (SCOM)
Description	GZIP Address 6 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_6_HASH_FUNCTION: Compression hash function for hash table address bit 6.

Register Name	GZIP Address 7 Hash Function Register
Mnemonic	NX.CH4.ADDR_7_HASH_FUNCTION_REG
Address	0000000002011148 (SCOM)
Description	GZIP Address 7 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_7_HASH_FUNCTION: Compression hash function for hash table address bit 7.

Register Name	GZIP Address 8 Hash Function Register
Mnemonic	NX.CH4.ADDR_8_HASH_FUNCTION_REG
Address	0000000002011149 (SCOM)
Description	GZIP Address 8 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_8_HASH_FUNCTION: Compression hash function for hash table address bit 8.

Register Name	GZIP Address 9 Hash Function Register
Mnemonic	NX.CH4.ADDR_9_HASH_FUNCTION_REG
Address	000000000201114A (SCOM)
Description	GZIP Address 9 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_9_HASH_FUNCTION: Compression hash function for hash table address bit 9.

Register Name	GZIP Address 10 Hash Function Register
Mnemonic	NX.CH4.ADDR_10_HASH_FUNCTION_REG
Address	000000000201114B (SCOM)
Description	GZIP Address 10 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ADDRESS_10_HASH_FUNCTION: Compression hash function for hash table address bit 10.

Register Name	GZIP Tag 0 Hash Function Register
Mnemonic	NX.CH4.DATATAG_0_HASH_FUNCTION_REG
Address	000000000201114C (SCOM)
Description	GZIP Tag 0 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	DATATAG_0_HASH_FUNCTION: Compression hash function for hash table tag 0.

Register Name	GZIP Tag 1 Hash Function Register
Mnemonic	NX.CH4.DATATAG_1_HASH_FUNCTION_REG
Address	000000000201114D (SCOM)
Description	GZIP Tag 1 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	DATATAG_1_HASH_FUNCTION: Compression hash function for hash table tag 1.

Register Name	GZIP Tag 2 Hash Function Register
Mnemonic	NX.CH4.DATATAG_2_HASH_FUNCTION_REG
Address	000000000201114E (SCOM)
Description	GZIP Tag 2 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	DATATAG_2_HASH_FUNCTION: Compression hash function for hash table tag 2.

Register Name	GZIP Tag 3 Hash Function Register
Mnemonic	NX.CH4.DATATAG_3_HASH_FUNCTION_REG
Address	000000000201114F (SCOM)
Description	GZIP Tag 3 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	DATATAG_3_HASH_FUNCTION: Compression hash function for hash table tag 3.

Register Name	GZIP Tag 4 Hash Function Register
Mnemonic	NX.CH4.DATATAG_4_HASH_FUNCTION_REG
Address	0000000002011150 (SCOM)
Description	GZIP Tag 4 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	DATATAG_4_HASH_FUNCTION: Compression hash function for hash table tag 4.

Register Name	GZIP Tag 5 Hash Function Register
Mnemonic	NX.CH4.DATATAG_5_HASH_FUNCTION_REG
Address	0000000002011151 (SCOM)
Description	GZIP Tag 5 Hash Function Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	DATATAG_5_HASH_FUNCTION: Compression hash function for hash table tag 5.

Register Name	GZIP Error Report Hold Register
Mnemonic	NX.CH4.GZIP_ERRRPT_HOLD_REG
Address	0000000002011152 (SCOM)
Description	GZIP Error Report Hold Register

Bits	SCOM	Field Mnemonic: Description
0:11	ROX	GZIP_ERRRPT_HOLD: GZIP engine c_err_rpt_holds.
12:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	Configuration of CC Counters Register
Mnemonic	TP.TCN0.N0.SYNC_CONFIG
Address	0000000002030000 (SCOM)
Description	configuration of CC counters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay incoming SYNC pulse. Default are eight latches: ASYNC 0000 = 8 0001 = 2 0010 = 3 0011 = 4 0100 = 5 0101 = 6 0110 = 7 0111 = 8 1000 = 9 1001 = 10 1010 = 11 1011 = 12 1100 = 13 1101 = 14 1110 = 15 1111 = 16 delay of the reset of the phase counter
4	RW	LISTEN_TO_SYNC_PULSE_DIS: Disables phase counter synchronization by the sync_pulse signal (default is enabled). **Note**: When you enable listen_to_sync, the chiplet is corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: Default is 0. When set to 1, the alternative input of the sync_pulse is used. **Note**: When you toggle the input select, the chiplet is corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: When set, use the OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the chiplet_is_aligned bit.
8	RW	UNIT_REGION_CLKCMD_ENABLE: Enables the unit interface to start/stop one dedicated region. Used for POWER9 cache or core.
9	RW	DISABLE_PCB_ITR: Disables the interrupt generation within CC. The interrupt is sent on each HLD event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enables the VITL align check to compare alignment of the incoming SYNC pulse with 2:1 VITL LCB.
11	RW	SYNC_PULSE_OUT_DIS: Disables the sync_pulse output when set to 1. The master chiplet does not send SYNC pulses to slave chiplets.
12:19	RW	UNUSED1219: Unused.

Register Name	OPCG Align Register
Mnemonic	TP.TCN0.N0.OPCG_ALIGN
Address	0000000002030001 (SCOM)
Description	OPCG ALIGN

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment: 0: none 1: 2:1 2: 3:1 3: 4:1 4: 6:1 5: 8:1 6: 12:1 7: 16:1 8: 24:1 9-15: 48:1
4:7	RW	SNOP_ALIGN: SNOP phase alignment: 0: none 1: 2:1 2: 3:1 3: 4:1 4: 6:1 5: 8:1 6: 12:1 7: 16:1 8: 24:1 9-15: 48:1
8:11	RW	ENOP_ALIGN: ENOP phase alignment: 0: none 1: 2:1 2: 3:1 3: 4:1 4: 6:1 5: 8:1 6: 12:1 7: 16:1 8: 24:1 9-15: 48:1
12:19	RW	INOP_WAIT: INOP cycle delay (0 - 255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0 - 4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0 - 255).
40	RW	INOP_FORCE_SG: INOP: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: SNOP: Set SG high during SNOP.
42	RW	ENOP_FORCE_SG: ENOP: Set SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: When set to 0, a clock change request first waits on the OPCG_WAIT cycles. When set to 1, a clock change request does not wait, when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0: Use the INOPA setting from opcg_reg0 1: Use the rising edge of SYNC pulse 2: Use unit0_sync_lvl to align (for AVP - refresh0) 3: Use unit1_sync_lvl to align (for AVP - refresh1)
46	RW	UNUSED46: Unused.

Bits	SCOM	Field Mnemonic: Description
47:51	RW	SCAN_RATIO: scan_ratio: n = 0 - 15: (n + 1):1 16: 24:1 17: 32:1 18: 48:1 19: 64:1 20: 128:1 Default 4:1 = 00011
52:63	RW	OPCG_WAIT_CYCLES: Old PAD value. Delay at the beginning and end of the OPCG run to allow DC signals to arrive at the correct time (0 4095). Required to be higher than plat depth. Default = 0x020.

Register Name	OPCG Control Register 0
Mnemonic	TP.TCN0.N0.OPCG_REG0
Address	0000000002030002 (SCOM)
Description	OPCG Control Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST mode used for LBIST 1 = RUNN mode used for ABIST/IOBIST
1	RWX	OPCG_GO: OPCG go (start OPCG). Bit is cleared when OPCG is done, Poll for opcg_done in cplt_start reg.
2	RWX	RUN_SCAN0: Run scan0. Overrides all BIST mode settings except the scan_ratio). Starts a scan0 run. The bit is cleared when OPCG is finished. Poll for opcg_done in the cplt_start register.
3	RW	SCAN0_MODE: Sets PRPGs in scan0_mode but does not run the automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, OPCG waits for the master chiplet to start. When Keep_MS_Mode is 0, SLAVE_MODE is cleared after the incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, OPCG sends out a trigger to all slave chiplets. When Keep_MS_MODE = 0, the MASTER_MODE is cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, OPCG in M/S mode bits are not cleared after one incoming OPCG trigger. Default is clear M/S mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: Unit pin used for AVP that can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: Unit pin used for AVP that can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types. Clears the chiplet.
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run SCAN0 on all regions and types. Clears the chiplet at all exclude PLL regions where the PLL is running.
11	RW	RUN_OPCG_ON_UPDATE_DR: Starts the OPCG engine when scan updated (update_dr) is received (set pulse). Cronus requires that this bit be set to 1 for a SETPULSE write.
12	RW	RUN_OPCG_ON_CAPTURE_DR: Starts the OPCG engine when scan updated (update_dr) is received (set pulse). Cronus requires that this bit be set to 1 for a SETPULSE read.
13	RW	STOP_RUNN_ON_XSTOP: RUNN mode. Stops run-n on checkstop.
14	RW	OPCG_STARTS_BIST: rRUNN mode. OPCG engine controls start_bist for ABIST or IOBIST.
15:20	RW	UNUSED1520: Unused.
21:63	RWX	LOOP_COUNT: Loop counter for LBIST and RUNN. Write = target value. Read = current counter value. Counts from zero to the target value.

Register Name	OPCG Control Register 1
Mnemonic	TP.TCN0.N0.OPCG_REG1
Address	0000000002030003 (SCOM)
Description	OPCG Control Register 1

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0 – 4095). runn-mode: start_bist match value (0:11).
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture. runn-mode: start_bist match value (12:23).
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture. runn-mode: start_bist match value (24:35).
36:47	RW	MISR_INIT_WAIT: BIST mode: Delay MISR aperture. MISRs get active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG creates only even and not odd clocks. Used for runn to create only one clock in fast domain. Default is 0.
49	RW	SCAN_CLK_USE_EVEN: Generates scan clock in even cycles instead of odd. Default is 0 = odd for scan.
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: Forces rtim_thold low when not in test_dc mode (must be 0 at all times).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0. Prevents activation of ARY HLD during NSL-fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0. Holds SG high during NSL-fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode. 00: Enables skitter during lbist_ip. 01: Enables skitter when misr_active. 10: skitter OPCG_GO mode. Falling edge = start; rising edge = stop. 11: Unused.
57	RW	MISR_MODE: BIST mode: MISR aperture mode. 0: a - 1 to b - 1 1: Start to a and b to end
58	RW	INFINITE_MODE: Infinite mode. RUNN and LBIST run forever and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode. NSL-fill count (0 - 31).

Register Name	OPCG Control Register 2
Mnemonic	TP.TCN0.N0.OPCG_REG2
Address	0000000002030004 (SCOM)
Description	OPCG Control Register 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: OPCG go for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2 1/4 1/8 1/16 1/2 3/4 7/8 15/16
4:15	RWX	PRPG_VALUE: Set to 0 for PRPG always on, else seed.
16:27	RW	PRPG_A_VAL: a value for PRPG aperture.

Bits	SCOM	Field Mnemonic: Description
28:39	RW	PRPG_B_VAL: b value for PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode: 0: a - 1 to b - 1 1: Start to a and b to end
41:63	RW	UNUSED41_63: Unused.

Register Name	Scan Region and Type Register
Mnemonic	TP.TCN0.N0.SCAN_REGION_TYPE
Address	0000000002030005 (SCOM)
Description	Scan Region and Type

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: Default is 0. When set to 1, the MASK bits in the CMSK chain decide which part is scanned or scan0. MASK = 1: scan0. MASK = 0: Part or scan chain
1:2	RO	constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region VITL (Vital = Clock).
4	RWX	SCAN_REGION_PERV: Scan clock region PERV (Pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region NX.
6	RWX	SCAN_REGION_UNIT2: Scan clock region cxa0 - CAPP.
7	RWX	SCAN_REGION_UNIT3: Scan clock region pbioe0 - PB.
8	RWX	SCAN_REGION_UNIT4: Scan clock region pbioe1 - PB.
9	RWX	SCAN_REGION_UNIT5: Scan clock region pbioe2 - PB.
10	RWX	SCAN_REGION_UNIT6: Scan clock region unused.
11	RWX	SCAN_REGION_UNIT7: Scan clock region unused.
12	RWX	SCAN_REGION_UNIT8: Scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: Scan clock region unused.
14	RWX	SCAN_REGION_UNIT10: Scan clock region reserved.
15:47	RO	constant = 0b00000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain FUNC (functional).
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configuration and debug configuration).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain ccfg / gptr (Pervasive: CC configuration. Others: GPTR).
51	RW	SCAN_TYPE_REGF: Scan chain regf (register files).
52	RW	SCAN_TYPE_LBIST: Scan chain lbst (LBIST).
53	RW	SCAN_TYPE_ABIST: Scan chain abst (ABIST).
54	RW	SCAN_TYPE_REPR: Scan chain repr (array repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (array timing).
56	RW	SCAN_TYPE_BNDY: Scan chain bndy (boundary I/Os).
57	RW	SCAN_TYPE_FARR: Scan chain farr (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain cmsk (LBIST channel mask).

Bits	SCOM	Field Mnemonic: Description
59	RW	SCAN_TYPE_INEX: Scan chain idex (c14 ASIC).
60:63	RO	constant = 0b0000

Register Name	Start/Stop of Clocks Register
Mnemonic	TP.TCN0.N0.CLK_REGION
Address	0000000002030006 (SCOM)
Description	This register starts and stops the clocks.

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00 = NOP 01 = Start 10 = Stop 11 = Pulse (one pulse)
2	RWX	SLAVE_MODE: When selected, the clock command waits for the master chiplet to start. The bit is cleared after the incoming slave trigger and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: When selected, the clock command sends out a trigger to all slave chiplets. The bit is cleared after sending out one master trigger and Keep_MS_Mode_after_trigger is set to 0.
4	RWX	CLOCK_REGION_PERV: For clock region perv (Pervasive).
5	RWX	CLOCK_REGION_UNIT1: For clock region NX.
6	RWX	CLOCK_REGION_UNIT2: For clock region cxa0 - CAPP.
7	RWX	CLOCK_REGION_UNIT3: For clock region pbioe0 - PB.
8	RWX	CLOCK_REGION_UNIT4: For clock region pbioe1 - PB.
9	RWX	CLOCK_REGION_UNIT5: For clock region pbioe2 - PB.
10	RWX	CLOCK_REGION_UNIT6: For clock region unused.
11	RWX	CLOCK_REGION_UNIT7: For clock region unused.
12	RWX	CLOCK_REGION_UNIT8: For clock region unused.
13	RWX	CLOCK_REGION_UNIT9: For clock region unused.
14	RWX	CLOCK_REGION_UNIT10: For clock region reserved.
15:47	RO	constant = 0b00000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Selects SL holds.
49	RWX	SEL_THOLD_NSL: select NSL holds.
50	RWX	SEL_THOLD_ARY: select array holds.
51	RO	constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support. Default for pulse is ODD phase. When this bit is set, the pulse is applied on the even phase.
53:63	RO	constant = 0b00000000000

Register Name	Clocks Running SL Register
Mnemonic	TP.TCN0.N0.CLOCK_STAT_SL
Address	0000000002030008 (SCOM)
Description	This register runs the SL.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: Status of PERV SL HLD. 0 = run 1 = stop
5	ROX	CLOCK_STATUS_UNIT1_SL: Status of NX SL HLD. 0 = run 1 = stop
6	ROX	CLOCK_STATUS_UNIT2_SL: Status of cxa0 - CAPP SL HLD. 0 = run 1 = stop
7	ROX	CLOCK_STATUS_UNIT3_SL: status of PBIOE0 - PB SL HLD 0 = run 1 = stop
8	ROX	CLOCK_STATUS_UNIT4_SL: Status of PBIOE1 - PB SL HLD 0 = run 1 = stop
9	ROX	CLOCK_STATUS_UNIT5_SL: Status of PBIOE2 - PB SL HLD 0 = run 1 = stop
10	ROX	CLOCK_STATUS_UNIT6_SL: Status of unused SL HLD. 0 = run 1 = stop
11	ROX	CLOCK_STATUS_UNIT7_SL: Status of unused SL HLD. 0 = run 1 = stop
12	ROX	CLOCK_STATUS_UNIT8_SL: Status of unused SL HLD. 0 = run 1 = stop
13	ROX	CLOCK_STATUS_UNIT9_SL: Status of unused SL HLD. 0 = run 1 = stop
14	ROX	CLOCK_STATUS_UNIT10_SL: Status of reserved SL HLD. 0 = run 1 = stop
15:63	RO	constant = 0b11111111111111111111111111111111111111111111111111111111111

Register Name	Clocks Running NSL Register
Mnemonic	TP.TCN0.N0.CLOCK_STAT_NSL
Address	0000000002030009 (SCOM)
Description	This register runs the NSL.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: Status of PERV NSL HLD. 0 = run 1 = stop
5	ROX	CLOCK_STATUS_UNIT1_NSL: Status of NX NSL HLD. 0 = run 1 = stop
6	ROX	CLOCK_STATUS_UNIT2_NSL: Status of cxa0 - CAPP NSL HLD. 0 = run 1 = stop
7	ROX	CLOCK_STATUS_UNIT3_NSL: status of PBIOE0 - PB NSL HLD 0 = run 1 = stop

Bits	SCOM	Field Mnemonic: Description
8	ROX	CLOCK_STATUS_UNIT4_NSL: Status of PBIOE1 - PB NSL HLD 0 = run 1 = stop
9	ROX	CLOCK_STATUS_UNIT5_NSL: Status of PBIOE2 - PB NSL HLD 0 = run 1 = stop
10	ROX	CLOCK_STATUS_UNIT6_NSL: Status of unused NSL HLD. 0 = run 1 = stop
11	ROX	CLOCK_STATUS_UNIT7_NSL: Status of unused NSL HLD. 0 = run 1 = stop
12	ROX	CLOCK_STATUS_UNIT8_NSL: Status of unused NSL HLD. 0 = run 1 = stop
13	ROX	CLOCK_STATUS_UNIT9_NSL: Status of unused NSL HLD. 0 = run 1 = stop
14	ROX	CLOCK_STATUS_UNIT10_NSL: Status of reserved NSL HLD. 0 = run 1 = stop
15:63	RO	constant = 0b11111111111111111111111111111111111111111111111111111

Register Name	Clocks Running Array Register
Mnemonic	TP.TCN0.N0.CLOCK_STAT_ARY
Address	000000000203000A (SCOM)
Description	This register runs the array.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: Status of PERV ARY HLD. 0 = run 1 = stop
5	ROX	CLOCK_STATUS_UNIT1_ARY: Status of NX ARY HLD. 0 = run 1 = stop
6	ROX	CLOCK_STATUS_UNIT2_ARY: Status of cxa0 - CAPP ARY HLD. 0 = run 1 = stop
7	ROX	CLOCK_STATUS_UNIT3_ARY: status of PBIOE0 - PB ARY HLD 0 = run 1 = stop
8	ROX	CLOCK_STATUS_UNIT4_ARY: Status of PBIOE1 - PB ARY HLD 0 = run 1 = stop
9	ROX	CLOCK_STATUS_UNIT5_ARY: Status of PBIOE2 - PB ARY HLD 0 = run 1 = stop

Bits	SCOM	Field Mnemonic: Description
10	ROX	CLOCK_STATUS_UNIT6_ARY: Status of unused ARY HLD. 0 = run 1 = stop
11	ROX	CLOCK_STATUS_UNIT7_ARY: Status of unused ARY HLD. 0 = run 1 = stop
12	ROX	CLOCK_STATUS_UNIT8_ARY: Status of unused ARY HLD. 0 = run 1 = stop
13	ROX	CLOCK_STATUS_UNIT9_ARY: Status of unused ARY HLD. 0 = run 1 = stop
14	ROX	CLOCK_STATUS_UNIT10_ARY: Status of reserved ARY HLD. 0 = run 1 = stop
15:63	RO	constant = 0b11111111111111111111111111111111111111111111111111111111

Register Name	ABIST and IOBIST Per Region Register
Mnemonic	TP.TCN0.N0.BIST
Address	000000000203000B (SCOM)
Description	ABIST and IOBIST per region

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this bit 0 during ABIST/IOBIST. Can be used to bypass the RUNN start. When this bit is set, the BIST_START_TEST goes high immediately without waiting for RUNN. BIST starts with the first HLD clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: Selects the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: Selects the ABIST engines for EDRAMs.
3	RW	TC_IOBIST_MODE_DC: Selects the IOBIST engines.
4	RW	BIST_PERV: Region PERV: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
5	RW	BIST_UNIT1: Region NX: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
6	RW	BIST_UNIT2: Region CXA0 - CAPP: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
7	RW	BIST_UNIT3: Region PBIOE0 - PB: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
8	RW	BIST_UNIT4: Region PBIOE1 - PB: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
9	RW	BIST_UNIT5: Region PBIOE2 - PB: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run

Bits	SCOM	Field Mnemonic: Description
10	RW	BIST_UNIT6: Region unused: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
11	RW	BIST_UNIT7: Region unused: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
12	RW	BIST_UNIT8: Region unused: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
13	RW	BIST_UNIT9: Region unused: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
14	RW	BIST_UNIT10: Region reserved: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
15:47	RO	constant = 0b00000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: Enables strobe window only in TE = 1. mode OPCGGO tester pin enables ABIST compare when ABIST is started. Special setup in ABIST engine is required. Default = 0. System mode cannot enable this feature.
49:63	RO	constant = 0b000000000000000

Register Name	Checkstop Per Region 1 Register
Mnemonic	TP.TCN0.N0.XSTOP1
Address	000000000203000C (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: Mask for checkstop to clockstop of select regions (see XSTOP_perv, xstop_unit0..n). 0 = ignore chkstop 1 = stop on chkstop
1	RW	XSTOP1_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP1: Triggers OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, checkstop waits independent from flush. Default is no wait when flush in not set.
4	RW	XSTOP1_PERV: Region PERV: 1 = region is stopped 0 = region keeps running on checkstop
5	RW	XSTOP1_UNIT1: Region NX: 1 = region is stopped 0 = region keeps running on checkstop
6	RW	XSTOP1_UNIT2: Region CXA0 - CAPP: 1 = region is stopped 0 = region keeps running on checkstop
7	RW	XSTOP1_UNIT3: Region PBIOE0 - PB: 1 = region is stopped 0 = region keeps running on checkstop

Bits	SCOM	Field Mnemonic: Description
8	RW	XSTOP1_UNIT4: Region PBIOE1 - PB: 1 = region is stopped 0 = region keeps running on checkstop
9	RW	XSTOP1_UNIT5: Region PBIOE2 - PB: 1 = region is stopped 0 = region keeps running on checkstop
10	RW	XSTOP1_UNIT6: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
11	RW	XSTOP1_UNIT7: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
12	RW	XSTOP1_UNIT8: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
13	RW	XSTOP1_UNIT9: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
14	RW	XSTOP1_UNIT10: Region reserved: 1 = region is stopped 0 = region keeps running on checkstop
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP1_WAIT_CYCLES: Defines how many cycles checkstop waits after dropping flush before Tholds is dropped. 0 - 4095 cycles possible.
60:63	RO	constant = 0b0000

Register Name	Checkstop Per Region 2 Register
Mnemonic	TP.TCN0.N0.XSTOP2
Address	000000000203000D (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: Mask for checkstop to clockstop of select regions (see XSTOP_perv, xstop_unit0..n). 0 = ignore chkstop 1 = stop on chkstop
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: Triggers OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: When set to 1, checkstop waits independent from flush. Default is no wait when flush in not set.
4	RW	XSTOP2_PERV: Region PERV: 1 = region is stopped 0 = region keeps running on checkstop
5	RW	XSTOP2_UNIT1: Region NX: 1 = region is stopped 0 = region keeps running on checkstop
6	RW	XSTOP2_UNIT2: Region CXA0 - CAPP: 1 = region is stopped 0 = region keeps running on checkstop

Bits	SCOM	Field Mnemonic: Description
7	RW	XSTOP2_UNIT3: Region PBIOE0 - PB: 1 = region is stopped 0 = region keeps running on checkstop
8	RW	XSTOP2_UNIT4: Region PBIOE1 - PB: 1 = region is stopped 0 = region keeps running on checkstop
9	RW	XSTOP2_UNIT5: Region PBIOE2 - PB: 1 = region is stopped 0 = region keeps running on checkstop
10	RW	XSTOP2_UNIT6: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
11	RW	XSTOP2_UNIT7: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
12	RW	XSTOP2_UNIT8: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
13	RW	XSTOP2_UNIT9: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
14	RW	XSTOP2_UNIT10: Region reserved: 1 = region is stopped 0 = region keeps running on checkstop
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Defines how many cycles checkstop waits after dropping flush before Tholds is dropped. 0 - 4095 cycles possible.
60:63	RO	constant = 0b0000

Register Name	Checkstop Per Region Register 3
Mnemonic	TP.TCN0.N0.XSTOP3
Address	000000000203000E (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: Mask for checkstop to clockstop of select regions (see XSTOP_perv, xstop_unit0..n). 0 = ignore chkstop 1 = stop on chkstop
1	RW	XSTOP3_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP3: Triggers OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, checkstop waits independent from flush. Default is no wait when flush in not set.
4	RW	XSTOP3_PERV: Region PERV: 1 = region is stopped 0 = region keeps running on checkstop
5	RW	XSTOP3_UNIT1: Region NX: 1 = region is stopped 0 = region keeps running on checkstop

Bits	SCOM	Field Mnemonic: Description
6	RW	XSTOP3_UNIT2: Region CXA0 - CAPP: 1 = region is stopped 0 = region keeps running on checkstop
7	RW	XSTOP3_UNIT3: Region PBIOE0 - PB: 1 = region is stopped 0 = region keeps running on checkstop
8	RW	XSTOP3_UNIT4: Region PBIOE1 - PB: 1 = region is stopped 0 = region keeps running on checkstop
9	RW	XSTOP3_UNIT5: Region PBIOE2 - PB: 1 = region is stopped 0 = region keeps running on checkstop
10	RW	XSTOP3_UNIT6: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
11	RW	XSTOP3_UNIT7: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
12	RW	XSTOP3_UNIT8: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
13	RW	XSTOP3_UNIT9: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
14	RW	XSTOP3_UNIT10: Region reserved: 1 = region is stopped 0 = region keeps running on checkstop
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Defines how many cycles checkstop waits after dropping flush before Tholds is dropped. 0 - 4095 cycles possible.
60:63	RO	constant = 0b0000

Register Name	Error Status of CC Register
Mnemonic	TP.TCN0.N0.ERROR_STATUS
Address	000000000203000F (SCOM)
Description	This register shows the error status of CC.

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: Rrite on read only register.
1	RWX	PCB_READ_NOT_ALLOWED_ERR: Read not allowed. Can be write only register.
2	RWX	PCB_PARITY_ON_CMD_ERR: Parity error on CMD.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: Invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on ADDR.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: Protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on SPCIF.

Bits	SCOM	Field Mnemonic: Description
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: PCB write while OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: Scan read when OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: Clock CMD in progress.
11	RWX	SCAN_COLLISION_ERR: Scan region selected of running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set scan region that is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG gets triggered while OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: Phase counters inside chiplet out of SYNC.
15	RWX	CLOCK_CMD_PREVENTED_ERR: Security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on OPCG state machine.
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on Scan/Clock Region/Type or Clock Status Register.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG registers.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on SYNC Configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on checkstop register.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0, 4, 5, and 6 registers.
22	RWX	CLKCMD_REQUEST_ERR: Region CLKCMD has one request pending, but receives a second CLKCMD.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error. REQ/ACK sequence wrong.
24	RWX	VITL_ALIGN_ERR: VITL Alignment is out of SYNC-to-SYNC pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 SYNC LVL pulses are not in SYNC. AVP is broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on self-boot command state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	**OPCG Control Register Capture 1**
Mnemonic	TP.TCN0.N0.OPCG_CAPT1
Address	0000000002030010 (SCOM)
Description	OPCG Control Register Capture1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000 = 12 cycle 0001 - 1100 = cycle 1-12 1101-1111 = 24 normal, not fast.
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (SL, NSL, ARY, SE, FCE).

Bits	SCOM	Field Mnemonic: Description
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (SL, NSL, ARY, SE, FCE).

Register Name	**OPCG Control Register Capture 2**
Mnemonic	TP.TCN0.N0.OPCG_CAPT2
Address	0000000002030011 (SCOM)
Description	OPCG Control Register Capture 2

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2: Unused.
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1 (even) for fast region or cycle 13 for normal region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1 (odd) for fast region or cycle 14 for normal region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_15_02EVEN: Sequence cycle 2 (even) for fast region or cycle 15 for normal region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_16_02ODD: Sequence cycle 2 (odd) for fast region or cycle 16 for normal region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3 (even) for fast region or cycle 17 for normal region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3 (odd) for fast region or cycle 18 for normal region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4 (even) for fast region or cycle 19 for normal region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4 (odd) for fast region or cycle 20 for normal region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5 (even) for fast region or cycle 21 for normal region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5 (odd) for fast region or cycle 22 for normal region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6 (even) for fast region or cycle 23 for normal region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6 (odd) for fast region or cycle 24 for normal region (SL, NSL, ARY, SE, FCE).

Register Name	**OPCG Control Register Capture 3**
Mnemonic	TP.TCN0.N0.OPCG_CAPT3
Address	0000000002030012 (SCOM)
Description	OPCG Control Register Capture 3

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7 (even) for fast region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_07ODD: Sequence cycle 7 (odd) for fast region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_08EVEN: Sequence cycle 8 (even) for fast region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_08ODD: Sequence cycle 8 (odd) for fast region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_09EVEN: Sequence cycle 9 (even) for fast region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_09ODD: Sequence cycle 9 (odd) for fast region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_10EVEN: Sequence cycle 10 (even) for fast region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_10ODD: Sequence cycle 10 (odd) for fast region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_11EVEN: Sequence cycle 11 (even) for fast region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_11ODD: Sequence cycle 11 (odd) for fast region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_12EVEN: Sequence cycle 12 - even - for fast region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12ODD: Sequence cycle 12 (odd) for fast region (SL, NSL, ARY, SE, FCE).

Register Name	Debug CBS CC Register
Mnemonic	TP.TCN0.N0.DBG_CBS_CC
Address	0000000002030013 (SCOM)
Description	Debug CBS CC Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset endpoint. CC and CTRL in reset state.
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped when enabled. Must have plat-depth cycles to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test enable.
4	ROX	DBG_CBS_REQ: CBS Interface - Request (latched).
5:7	ROX	DBG_CBS_CMD: CBS Interface - Command (latched).
8:12	ROX	DBG_CBS_STATE: CBS command state machine 00000 = idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS protocol error. REQ is raised, but state machine is not in IDLE. Must reset_ep to clear this bit. No impact on IPL.
15	ROX	DBG_PCB_IDLE: PCB interface in IDLE state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: Current/latest OPCG MODE: 0 = NOP 1 = LBIST 2 = ABIST 3 = RUNN 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN w CaptureDR 9 = CLK Change Request 10-15 = Unused

Bits	SCOM	Field Mnemonic: Description
20:23	ROX	DBG_LAST_OPCG_MODE: Previous OPCG mode.
24	ROX	DBG_PCB_ERROR: PCB interface error. Read CC Error Register or set CBS_CMD = 001 to switch FSI CBS. Debug Information to CC error Register.
25	ROX	DBG_PARITY_ERROR: Any parity error, non-PCB parity. Read CC Error Register or set CBS_CMD = 001 to switch FSI CBS. Debug Information to CC error Register.
26	ROX	DBG_CC_ERROR: Any other CC error. Read CC Error Register or set CBS_CMD = 001 to switch FSI CBS. Debug Information to CC error Register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: Value is 1 when the a valid align pulse WS is sent out.
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: Reset clears the bit. The first PCB request sets the bit.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: Rising or falling edge on test enable after reset. Must have reset_ep to clear, no impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on vitl_clkoff, after reset. Must have reset_ep to clear, no impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: Only representation of CC acknowled signal going to FSI.

Register Name	**CC Protect Mode Register**
Mnemonic	TP.TCN0.N0.CC_PROTECT_MODE_REG
Address	00000000020303FE (SCOM)
Description	CC Protect Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enables read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enables write protection.

Register Name	**Atomic Lock Register**
Mnemonic	TP.TCN0.N0.CC_ATOMIC_LOCK_REG
Address	00000000020303FF (SCOM)
Description	Atomic Lock Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	CC_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	**Global Checkstop FIR Register**
Mnemonic	TP.TCN0.N0.XFIR
Address	0000000002040000 (SCOM)
Description	Global checkstop FIR

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any checkstop).
1	RWX	XFIR_IN1: Checkstop broadcast using OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from pervasive unit.

Bits	SCOM	Field Mnemonic: Description
4	RWX	XFIR_IN4: Checkstop from NX0.
5	RWX	XFIR_IN5: Checkstop from NX1.
6	RWX	XFIR_IN6: Checkstop from CXA0 FIR.
7	RWX	XFIR_IN7: Unused.
8	RWX	XFIR_IN8: Checkstop from PBIOE0_0 FIR.
9	RWX	XFIR_IN9: Checkstop from PBIOE0_1 FIR.
10	RWX	XFIR_IN10: Checkstop from PBIOE1_0 FIR.
11	RWX	XFIR_IN11: Checkstop from PBIOE1_1 FIR.
12	RWX	XFIR_IN12: Checkstop from PBIOE2_0 FIR.
13	RWX	XFIR_IN13: Checkstop from PBIOE2_1 FIR.
14:25	RWX	XFIR_IN14: Unused.
26	RWX	XFIR_IN26: Checkstop on debug trigger.

Register Name	Global Recoverable FIR Register
Mnemonic	TP.TCN0.N0.RFIR
Address	0000000002040001 (SCOM)
Description	Global recoverable FIR

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop from NX and CXA0.
1	ROX	LFIR_RECOV_ERR: Recoverable error from pervasive unit.
2	ROX	RFIR_IN4: Recoverable from NX0.
3	ROX	RFIR_IN5: Recoverable from NX1.
4	ROX	RFIR_IN6: Recoverable from CXA0 FIR.
5	ROX	RFIR_IN7: Unused.
6	ROX	RFIR_IN8: Recoverable from PBIOE0_0 FIR.
7	ROX	RFIR_IN9: Recoverable from PBIOE0_1 FIR.
8	ROX	RFIR_IN10: Recoverable from PBIOE1_0 FIR.
9	ROX	RFIR_IN11: Recoverable from PBIOE1_1 FIR.
10	ROX	RFIR_IN12: Recoverable from PBIOE2_0 FIR.
11	ROX	RFIR_IN13: Recoverable from PBIOE2_1 FIR.
12:23	ROX	RFIR_IN14: Unused.

Register Name	FIR Mask Register
Mnemonic	TP.TCN0.N0.FIR_MASK
Address	0000000002040002 (SCOM)
Description	FIR Mask

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR/RFIR summary bit.
1	RW	FIR_MASK_IN1: Mask for XFIR bit received via OOB broadcast.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: Mask for XFIR from pervasive unit.
4	RW	FIR_MASK_IN4: Mask for nx0 XFIR and RFIR.
5	RW	FIR_MASK_IN5: Mask for nx1 XFIR and RFIR.
6	RW	FIR_MASK_IN6: Mask for CXA0 XFIR and RFIR.

Bits	SCOM	Field Mnemonic: Description
7	RW	FIR_MASK_IN7: Unused.
8	RW	FIR_MASK_IN8: Mask for PBIOE0_0 XFIR and RFIR.
9	RW	FIR_MASK_IN9: Mask for PBIOE0_1 XFIR and RFIR.
10	RW	FIR_MASK_IN10: Mask for PBIOE1_0 XFIR and RFIR.
11	RW	FIR_MASK_IN11: Mask for PBIOE1_1 XFIR and RFIR.
12	RW	FIR_MASK_IN12: mask for PBIOE2_0 XFIR and RFIR.
13	RW	FIR_MASK_IN13: Mask for PBIOE2_1 XFIR and RFIR.
14:25	RW	FIR_MASK_IN14: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local checkstop to recoverable error.

Register Name	Special Attention Register
Mnemonic	TP.TCN0.N0.SPATTN
Address	0000000002040004 (SCOM) 0000000002040005 (SCOM1) 0000000002040006 (SCOM2)
Description	Special Attention

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:9	ROX	NCX	NCX	SPATTN_IN: Unused special attentions.

Register Name	Special Attention Mask Register
Mnemonic	TP.TCN0.N0.SPA_MASK
Address	0000000002040007 (SCOM)
Description	Special Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	Mode Register
Mnemonic	TP.TCN0.N0.EPS.FIR.MODE_REG
Address	0000000002040008 (SCOM)
Description	Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop chip TOD on checkstop (unused in POWER9).
5	RW	MODE_IN5: Stop chip TOD on Recoverable (unused in POWER9).

Bits	SCOM	Field Mnemonic: Description
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enables checkstop on special attention.
9	RW	MODE_IN9: mask_direct/local_error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention Register
Mnemonic	TP.TCN0.N0.HOSTATTN
Address	0000000002040009 (SCOM)
Description	Host Attention

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host Attention summary bit.
1	ROX	HOSTATTN_IN1: Unused.
2	ROX	HOSTATTN_IN2: Unused.
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	Local FIR Register
Mnemonic	TP.TCN0.N0.LOCAL_FIR
Address	000000000204000A (SCOM) 000000000204000B (SCOM1) 000000000204000C (SCOM2)
Description	Local FIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Errors from control.
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, and so on).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from Thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from Thermal (PCB error.
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from Thermal (Trip error critical.
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from Thermal (Trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Thermal volt trip error.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from debug (SCOM error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from trace Array0 (SCOM error).
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Local errors from trace Array0.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Local errors from trace Array1 (SCOM error).
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Local errors from trace Array1.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Unused.
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Unused.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Unused.
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Unused.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Unused.
21	RWX	WOX_AND	WOX_OR	FIR_IN21: Unused.
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Unused.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Unused.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Errors from Bsense I/O.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Unused.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Unused.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Unused.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Unused.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Unused.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Unused.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Unused.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Unused.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Unused.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction-alert broadcast using OOB.

Register Name	**Local FIR Mask Register**
Mnemonic	TP.TCN0.N0.EPS.FIR.LOCAL_FIR_MASK
Address	000000000204000D (SCOM) 000000000204000E (SCOM1) 000000000204000F (SCOM2)
Description	Local FIR Mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for LEM error-collection vector.

Register Name	**Local FIR Action0 Register**
Mnemonic	TP.TCN0.N0.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000002040010 (SCOM)
Description	Local FIR Action0

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: Action0 mask.

Register Name	**Local FIR Action1 Register**
Mnemonic	TP.TCN0.N0.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000002040011 (SCOM)
Description	Local FIR Action1

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: Action1 mask.

Register Name	Group Checkstop Mask Register
Mnemonic	TP.TCN0.N0.EPS.FIR.GXSTOP_TRIG_REG
Address	0000000002040013 (SCOM)
Description	Group Checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for type-4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group0 Checkstop Mask Register
Mnemonic	TP.TCN0.N0.EPS.FIR.GXSTOP0_MASK_REG
Address	0000000002040014 (SCOM)
Description	Group0 Checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for recoverable error
2	RW	GXSTP0_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for YYPE 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group1 Checkstop Mask Register
Mnemonic	TP.TCN0.N0.EPS.FIR.GXSTOP1_MASK_REG
Address	0000000002040015 (SCOM)
Description	Group1 Checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for type-4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP1_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group2 Checkstop Mask Register
Mnemonic	TP.TCN0.N0.EPS.FIR.GXSTOP2_MASK_REG
Address	0000000002040016 (SCOM)
Description	Group2 Checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for debug checkstop on Trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	Summary Mask Register
Mnemonic	TP.TCN0.N0.EPS.FIR.SUM_MASK_REG
Address	0000000002040017 (SCOM)
Description	Summary Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type4 host attention summary bit.

Register Name	Local Checkstop Register
Mnemonic	TP.TCN0.N0.LOCAL_XSTOP_ERR
Address	0000000002040018 (SCOM)
Description	Local Checkstop

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit.
1	ROX	LOCAL_XSTOP_IN1: Local checkstop from NX, bit 0.
2	ROX	LOCAL_XSTOP_IN2: Local checkstop from NX, bit 1.
3	ROX	LOCAL_XSTOP_IN3: Local checkstop from CX.
4	ROX	LOCAL_XSTOP_IN4: Unused.
5	ROX	LOCAL_XSTOP_IN5: Unused.
6	ROX	LOCAL_XSTOP_IN6: Unused.
7	ROX	LOCAL_XSTOP_IN7: Unused.
8	ROX	LOCAL_XSTOP_IN8: Unused.
9	ROX	LOCAL_XSTOP_IN9: Unused.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.

Bits	SCOM	Field Mnemonic: Description
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask Register
Mnemonic	TP.TCN0.N0.LOCAL_XSTOP_MASK
Address	0000000002040019 (SCOM)
Description	Local Checkstop Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask Register
Mnemonic	TP.TCN0.N0.HOSTATTN_MASK
Address	000000000204001A (SCOM)
Description	Host Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Thermal Sensor Loop1 Results Register
Mnemonic	TP.TCN0.N0.EPS.THERM.DTS_RESULT0
Address	0000000002050000 (SCOM)
Description	DTS Thermal Sensor loop1 Results

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results Register
Mnemonic	TP.TCN0.N0.EPS.THERM.DTS_TRC_RESULT
Address	0000000002050003 (SCOM)
Description	DTS Trace Results

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with ID 1.

Register Name	CPM & DTS Enables and Controls Register
Mnemonic	TP.TCN0.N0.EPS.THERM.THERM_MODE_REG
Address	000000000205000F (SCOM)
Description	CPM & DTS enables and Controls

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: force tpc_therm_thres_mac clock gating off and activates clocks.
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables. 1xx: trip0 - warning. x1x: trip1 - critical. xx1: trip2 - fatal.
5	RW	THERM_DTS_SAMPLE_ENA: When set to 0, there is no DTS sampling. When set to 1, DTS sampling is enabled and below-counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz, sample pulse is fed into an 18-bit counter. With the therm_sample_pulse_cnt, it is possible to select a high-order bit of the counter to enable a resolutions of sampling DTSS between 2.5 us and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a DTS sample. 0000: 16 ms. 0001: 8 ms. 0010: 4 ms. 0011: 2 ms. 0100: 1 ms. 0101: 0.5 ms. 0110: 250 µs. 0111: 125 µs. 1000: 62 .5 µs. 1001: 31.3 µs. 1010: 15.6 µs. 1011: 7.8 µs. 1100: 3.9 µs. 1101: 2 µs. 1110: 1 µs. 1111: 0.5 µs.
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in threshold unit: 00: Off. 11: Illegal. 10: Maximum mode. 01: Minimum mode.
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: When set to 0, therm_overflow_err is enabled. When set to 1, therm_overflow_err will be disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result is provided with PCB read addr_v(4): 0000: DTS 0. 0001: DTS 1. 0010: DTS 2. 0100: DTS 4. 1111: Worst-case sensor.
20:21	RW	THERM_DTS_ENABLE_L1: Loop1 DTS enables: 1x: DTS 0 available. x1: DTS 1 available.

Bits	SCOM	Field Mnemonic: Description
22:34	RO	constant = 0b0000000000000
35:36	RW	Reserved field.

Register Name	Skitter Control Register
Mnemonic	TP.TCN0.N0.EPS.THERM.SKITTER_MODE_REG
Address	0000000002050010 (SCOM)
Description	Skitter Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold current sample.
1	RW	DISABLE_SKITTER_STICKINESS: When set to 0, accumulation mode. When set to 1, samples new value each cycle and resets the sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0: hold_on_trigger0. bit1: _on_trigger1.
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0: reset_sticky_on_trigger0. bit1: reset_sticky_on_trigger1.
8:9	RW	SKITTER_SAMPLE_GUTS: Selects guts to measure: 00: Guts1. 01: Guts2. 10: Guts3. 11: Guts4.
10:43	RO	constant = 0b00000000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold current sample on the debug trigger. This bit has the highest priority.
45	ROX	SKITTER_DATA_V_LT: When set to 1, the data requested by a skitter force read register has finished and data is present in the skitter data register in the collector macro. The data can be read by any combination of V25/V26/V27 PCB reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TCN0.N0.EPS.THERM.INJECT_REG
Address	0000000002050011 (SCOM)
Description	Error Injection Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00: no injection. 01: Warning trip level injection. 10: Critical trip level injection. 11: Fatal trip level injection.
2:3	RW	THERM_INJECT_MODE: 00: no injection. 01: Injection on the next DTS sample. 10: Solid injection for the next DTS samples till bit setting changes. 11: Not used.

Register Name	Control/Force Reset Register
Mnemonic	TP.TCN0.N0.EPS.THERM.CONTROL_REG
Address	0000000002050012 (SCOM)
Description	Control/Force Reset Register

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved field.
1	WO_1P	Reserved field.
2	WO_1P	Reserved field.
3	WO_1P	Reserved field.
4	WO_1P	Reserved field.
5	WO_1P	Reserved field.
6	WO_1P	Reserved field.
7	WO_1P	Reserved field.
8	WO_1P	Reserved field.
9	WO_1P	Reserved field.
10	WO_1P	Reserved field.
11	WO_1P	Reserved field.
12	WO_1P	Reserved field.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCN0.N0.EPS.THERM.ERR_STATUS_REG
Address	0000000002050013 (SCOM)
Description	Thermal Error Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Thermal Mode Register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter Mode Register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter Force Register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan INIT Version Register parity error mask.
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt Mode Register parity error mask.
22	RO	constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: thres state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Forces skitter read on the hot error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	constant = 0b00000000
40:43	ROX	Reserved field.
44:46	ROX	Reserved field.
47	ROX	Reserved field.
48	ROX	Reserved field.
49:50	ROX	Reserved field.
51:54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCN0.N0.EPS.THERM.SKITTER_FORCE_REG
Address	0000000002050014 (SCOM)
Description	Skitter Force Read Register

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter.

Register Name	Skitter Clock SRC Control Register
Mnemonic	TP.TCN0.N0.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000002050016 (SCOM)
Description	Skitter Clock SRC Control Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects clock to measure: 000: Local mesh clock. 001: External pin skitter_c1_1_in. 010: Local d1clk only if d_mode = 1. 011: External pin skitter_c1_2_in. 100: Local lclk only if d_mode = 1. 101: External pin skitter_c1_3_in. 110: Unused. 111: External pin skitter_c1_4_in.
3:35	RO	constant = 0b00000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: Selects delay to be added between clock source multiplexer and inverter chain (base line delay is 12.2 ps) of skitter0. 00 - No delay. 01 - 0.6 ps. 10 - 1.8 ps. 11 - 5 ps.

Register Name	Skitter Data Register Read Bit 0:63
Mnemonic	TP.TCN0.N0.EPS.THERM.SKITTER_DATA0
Address	0000000002050019 (SCOM)
Description	Skitter Data Register Read Bit0:63

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bit 32:95
Mnemonic	TP.TCN0.N0.EPS.THERM.SKITTER_DATA1
Address	000000000205001A (SCOM)
Description	Skitter Data Register Read Bit32:95

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bit 64:127
Mnemonic	TP.TCN0.N0.EPS.THERM.SKITTER_DATA2
Address	000000000205001B (SCOM)
Description	Skitter Data Register Read Bit 64:127

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Time-Stamp Counter Read Register
Mnemonic	TP.TCN0.N0.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000205001C (SCOM)
Description	Time-Stamp Counter Read

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.

5. PB Chiplet (Nest Chiplet 0 PCB Slave)

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

The POWER9 processor registers are listed in the following tables.

Register Name	**Primary PCB Slave Address Register**
Mnemonic	TP.TPCHIP.NET.PCBSLN0.PRIMARY_ADDRESS_REG
Address	00000000020F0000 (SCOM)
Description	This register contains the PCB slave's primary address.

Bits	SCOM	Field Mnemonic: Description
0:5	RO	Reserved field. This is the primary_address setting.

Register Name	Multicast Group 1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.MULTICAST_GROUP_1
Address	00000000020F0001 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.MULTICAST_GROUP_2
Address	00000000020F0002 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111

Bits	SCOM	Field Mnemonic: Description
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	**Multicast Group 3 Register**
Mnemonic	TP.TPCHIP.NET.PCBSLN0.MULTICAST_GROUP_3
Address	00000000020F0003 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	**Multicast Group 4 Register**
Mnemonic	TP.TPCHIP.NET.PCBSLN0.MULTICAST_GROUP_4
Address	00000000020F0004 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Timeout Select Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.TIMEOUT_REG
Address	00000000020F0010 (SCOM)
Description	This register contains the int_timeout setting.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	Reserved field. This is the int_timeout setting.

Register Name	Assist Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.ASSIST_INTERRUPT_REG
Address	00000000020F0011 (SCOM)
Description	This register contains the attn, recov, and xstop (checkstop) settings.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the attn setting.
1	ROX	Reserved field. This is the recov setting.
2	ROX	Reserved field. This is the xstop setting.

Register Name	Vital Scan Out Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.VITAL_SCAN_OUT
Address	00000000020F0017 (SCOM)
Description	This register contains the vital scan out settings.

Bits	SCOM	Field Mnemonic: Description
0	ROX	RESERVED.

Register Name	Chiplet Heartbeat Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.HEARTBEAT_REG
Address	00000000020F0018 (SCOM)
Description	This register indicates whether a chiplet heartbeat is detected.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: A chiplet heartbeat is not detected.

Register Name	PLL Lock indications Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.PLL_LOCK_REG
Address	00000000020F0019 (SCOM)
Description	This register contains lock indications from the PLLs,

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field. This is the lock setting.

Register Name	Attention Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.ATTN_INTERRUPT_REG
Address	00000000020F001A (SCOM)
Description	This register contains the attn setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the attn setting.

Register Name	Recovery Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.RECOV_INTERRUPT_REG
Address	00000000020F001B (SCOM)
Description	This register contains the recoverable interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the recov setting.

Register Name	Checkstop Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.XSTOP_INTERRUPT_REG
Address	00000000020F001C (SCOM)
Description	This register contains the checkstop interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the xstop setting.

Register Name	Slave Configuration Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.SLAVE_CONFIG_REG
Address	00000000020F001E (SCOM)
Description	This is the slave configuration register.

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: This bit disables the pervasive threshold check.
1	RW	CFG_DISABLE_MALF_PULSE_GEN: This bit disables pulse generation for a malfunction alert. Switch back to level.
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: This bit disables the hang counter stop for a system checkstop.
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: This bit disables the atomic lock for chiplet accesses.
4	RW	CFG_DISABLE_HEARTBEAT: This bit disables the check for voltage and gridclock in the chiplet.
5	RW	CFG_DISABLE_FORCE_TO_ZERO: This bit disables the force to zero for error cases.
6	RW	CFG_PM_DISABLE: This bit disables the power management set/reset interface for net_ctrl registers.
7	RW	CFG_PM_MUX_DISABLE: This bit disables the power-management multiplex request signal.
8:13	RW	ERROR_MASK: These are mask bits for slave error reporting.
14:15	RW	RESERVED.

Register Name	Error Capture Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.ERROR_REG
Address	00000000020F001F (SCOM)
Description	This register is used to capture errors.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on the PCB bus.
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by the chiplet. 000 = No error. 001 = XSCOM command blocked due to pending errors. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address, address error, or bad access type. 101 = Clock error. 110 = Parity error, received unexpected packet, or wrong packet number. 111 = Timeout. This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on the PCB interface.
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in the data buffer.
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in the address buffer.
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in the PCB FSM.
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in the chiplet FSM.
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in the interrupt RX FSM.
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in the interrupt TX FSM.
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type.
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on the chiplet interface.

Bits	SCOM	Field Mnemonic: Description
13	RWX_WCLEAR	INFO_ERROR: Parity error on the chiplet information lines.
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error.
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error on the PCB interface component for the internal endpoint.
17	RWX_WCLEAR	CHIPLET_OFFLINE: A heartbeat check indicated that the chiplet is offline.
18	RWX_WCLEAR	EDRAM_SEQUENCE_ERR: Error in the eDRAM power-up sequence.
19	RWX_WCLEAR	CTRL_REG_PARITY_ERROR: The control register parity is bad.
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: The address register parity is bad.
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: The timeout select register parity is bad.
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: The slave configuration register parity is bad.
23	RWX_WCLEAR	UNUSED_1:
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: The divider register parity is bad.
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: Unlock from the chiplet PLL.

Register Name	Hang Pulse Generation Register 0
Mnemonic	TP.TPCHIP.NET.PCBSLN0.HANG_PULSE_0_REG
Address	00000000020F0020 (SCOM)
Description	This register contains hang pulse 0 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: This field contains the value of hang pulse 0. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 1
Mnemonic	TP.TPCHIP.NET.PCBSLN0.HANG_PULSE_1_REG
Address	00000000020F0021 (SCOM)
Description	This register contains hang pulse 1 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: This field contains the value of hang pulse 1. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 2
Mnemonic	TP.TPCHIP.NET.PCBSLN0.HANG_PULSE_2_REG
Address	00000000020F0022 (SCOM)
Description	This register contains hang pulse 2 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: This field contains the value of hang pulse 2. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 3
Mnemonic	TP.TPCHIP.NET.PCBSLN0.HANG_PULSE_3_REG
Address	00000000020F0023 (SCOM)
Description	This register contains hang pulse 3 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: This field contains the value of hang pulse 3. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 4
Mnemonic	TP.TPCHIP.NET.PCBSLN0.HANG_PULSE_4_REG
Address	00000000020F0024 (SCOM)
Description	This register contains hang pulse 4 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: This field contains the value of hang pulse 4. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 5
Mnemonic	TP.TPCHIP.NET.PCBSLN0.HANG_PULSE_5_REG
Address	00000000020F0025 (SCOM)
Description	This register contains hang pulse 5 information. This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: This field contains the value of hang pulse 5. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 6
Mnemonic	TP.TPCHIP.NET.PCBSLN0.HANG_PULSE_6_REG
Address	00000000020F0026 (SCOM)
Description	This register contains hang pulse 6 information. This hang counter is exclusively used for heartbeat generation.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: This field contains the value of hang pulse 6. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Counter Clock Divider Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.PRE_COUNTER_REG
Address	00000000020F0028 (SCOM)
Description	This register is the divider for the hang counter clock.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: This field is the divider for the hang counter clock. It divides the clock by n + 1. (The default is n = 0).

Register Name	eDRAM Control Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.EDRAM_STATUS
Address	00000000020F0029 (SCOM)
Description	This register contains the eDRAM control status.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	EDRAM_STAT: This field contains the eDRAM control status.

Register Name	NET CTRL0 Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.NET_CTRL0
Address	00000000020F0040 (SCOM) 00000000020F0041 (SCOM1) 00000000020F0042 (SCOM2)
Description	This register contains NET controls. It is not applicable to the pervasive chiplet.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: This bit is set if the chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: The output is ORed to the global EP reset.
2	RWX	RWX_WAND	RWX_WOR	CLK_ASYNC_RESET: POWER9 cache chiplet: EQ skew adjust reset. POWER9 core chiplet: Core duty cycle adjust reset. POWER9 memory chiplet: Memory glitchless multiplexer asynchronous reset.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Test enable for the chiplet PLL.
4	RWX	RWX_WAND	RWX_WOR	PLL_RESET: Reset for the chiplet PLL.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYPASS: Enable bypass for the chiplet PLL.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for the chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8	RWX	RWX_WAND	RWX_WOR	VITAL_PHASE: Phase for the vital domain.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	RWX_WAND	RWX_WOR	FLUSH_ALIGN_OVR: When set to 1, this mechanism overrides automatic control by the clock controller of the flush, flush_nto1, and align signals in the chiplet.
10	RWX	RWX_WAND	RWX_WOR	VITAL_AL: Align for vital domain.
11	RWX	RWX_WAND	RWX_WOR	ACT_DIS: ACT disable control for LCBs in the vital logic.
12	RWX	RWX_WAND	RWX_WOR	MPW1: Modify pulse width 1 (MPW1) control for LCBs in the vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: Modify pulse width 2 (MPW2) control for LCBs in the vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW3: Modify pulse width 3 (MPW3) control for LCBs in the vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for the vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Threshold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FLUSH_SCAN_N: Flush scan control.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for the chiplet.
19	RWX	RWX_WAND	RWX_WOR	CPLT_RCTRL: Chiplet receiver enable.
20	RWX	RWX_WAND	RWX_WOR	CPLT_DCTRL: Chiplet driver enable.
21	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pm_access setting.
22	RWX	RWX_WAND	RWX_WOR	ADJ_FUNC_CLKSEL: POWER9 cache chiplet: Clock select for the skew adjust/duty cycle adjust logic. POWER9 core chiplet: Skew sense to skew adjust fencing.
23:24	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pm_access setting.
25	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the chiplet from the PCB bus. If set, the PCB slave reports “Chiplet Offline.”
26	RWX	RWX_WAND	RWX_WOR	LVLTRANS_FENCE: Fence control for the level translators.
27	RWX	RWX_WAND	RWX_WOR	ARRAY_WRITE_ASSIST_EN: Array write assist.
28	RWX	RWX_WAND	RWX_WOR	HTB_INTEST: HTB intest mode.
29	RWX	RWX_WAND	RWX_WOR	HTB_EXTEST: HTB intest mode.
30	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pm_access setting.
31	RWX	RWX_WAND	RWX_WOR	PLLFORCE_OUT_EN: PLL force out enable.

Register Name	NET CTRL1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.NET_CTRL1
Address	00000000020F0044 (SCOM) 00000000020F0045 (SCOM1) 00000000020F0046 (SCOM2)
Description	This register contains NET controls. It is not applicable to the pervasive chiplet.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	PLL_CLKIN_SEL: PLL clkin select.
1	RWX	RWX_WAND	RWX_WOR	CLK_DCC_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 duty cycle control bypass. POWER9 core chiplet: Core duty cycle control bypass. POWER9 memory chiplet: Memory duty cycle control bypass.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RWX	RWX_WAND	RWX_WOR	CLK_PDLY_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 programmable delay bypass. POWER9 core chiplet: Core programmable delay bypass. POWER9 memory chiplet: Memory programmable delay bypass.
3	RWX	RWX_WAND	RWX_WOR	CLK_DIV_BYPASS_EN: Enable clock divider bypass.
4	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX0_SEL: Select for reference clock mux0.
5	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX1_SEL: Select for reference clock mux1.
6	RWX	RWX_WAND	RWX_WOR	PLL_BNDY_BYPASS_EN: Bypass for IOP PLL.
7	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pcb_access setting.
8:15	RWX	RWX_WAND	RWX_WOR	DPLL_TEST_SEL: DPLL testout multiplexing.
16:19	RWX	RWX_WAND	RWX_WOR	SB_STRENGTH: Sector buffer driver strength.
20	RWX	RWX_WAND	RWX_WOR	ASYNC_TYPE: This is a control signal for testing latches with asynchronous set and reset capabilities.
21	RWX	RWX_WAND	RWX_WOR	ASYNC_OBS: This is a control signal for testing latches with asynchronous set and reset capabilities.
22	RWX	RWX_WAND	RWX_WOR	CPM_CAL_SET: CPM calibrate.
23	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET0: POWER9 cache chiplet: L2-0 duty cycle adjust reset.
24	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET1: POWER9 cache chiplet: L2-1 duty cycle adjust reset.
25	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_EN: Clock pulse mode enable.
26:27	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_MODE: Clock pulse mode setting.
28:31	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pcb_access setting.

Register Name	Protect Mode Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.PROTECT_MODE_REG
Address	00000000020F03FE (SCOM)
Description	This register is used to enable read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection.
1	RW	WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.NET.PCBSLN0.ATOMIC_LOCK_REG
Address	00000000020F03FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable the atomic lock.
1:4	ROX	ATOMIC_ID: This field contains the atomic ID.
5:7	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
8:15	ROX	ATOMIC_ACTIVITY: This is the atomic lock counter.

6. PB Chiplet (Nest Chiplet 1)

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TP.TCN1.N1.CTRL_PROTECT_MODE_REG	0x00000000030003FE	732
TP.TCN1.N1.DBG_CBS_CC	0x0000000003030013	848
TP.TCN1.N1.EPS.DBG.DBG_INST1_COND_REG_1	0x00000000030107C1	773
TP.TCN1.N1.EPS.DBG.DBG_INST1_COND_REG_2	0x00000000030107C2	775
TP.TCN1.N1.EPS.DBG.DBG_INST1_COND_REG_3	0x00000000030107C3	776
TP.TCN1.N1.EPS.DBG.DBG_INST2_COND_REG_1	0x00000000030107C4	777
TP.TCN1.N1.EPS.DBG.DBG_INST2_COND_REG_2	0x00000000030107C5	779
TP.TCN1.N1.EPS.DBG.DBG_INST2_COND_REG_3	0x00000000030107C6	780
TP.TCN1.N1.EPS.DBG.DBG_MODE_REG	0x00000000030107C0	773
TP.TCN1.N1.EPS.DBG.DBG_TRACE_MODE_REG_2	0x00000000030107CF	784
TP.TCN1.N1.EPS.DBG.DBG_TRACE_REG_0	0x00000000030107CD	781
TP.TCN1.N1.EPS.DBG.DBG_TRACE_REG_1	0x00000000030107CE	782
TP.TCN1.N1.EPS.FIR.GXSTOP0_MASK_REG	0x0000000003040014	855
TP.TCN1.N1.EPS.FIR.GXSTOP1_MASK_REG	0x0000000003040015	856
TP.TCN1.N1.EPS.FIR.GXSTOP2_MASK_REG	0x0000000003040016	856
TP.TCN1.N1.EPS.FIR.GXSTOP_TRIG_REG	0x0000000003040013	855
TP.TCN1.N1.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000003040010	854
TP.TCN1.N1.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000003040011	854
TP.TCN1.N1.EPS.FIR.LOCAL_FIR_MASK	0x000000000304000D	854
TP.TCN1.N1.EPS.FIR.MODE_REG	0x0000000003040008	851
TP.TCN1.N1.EPS.FIR.SUM_MASK_REG	0x0000000003040017	857
TP.TCN1.N1.EPS.PSC.PSC.ADDR_TRAP_REG	0x0000000003010003	735
TP.TCN1.N1.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG	0x0000000003010007	736
TP.TCN1.N1.EPS.PSC.PSC.PSCOM_ERROR_MASK	0x0000000003010002	734
TP.TCN1.N1.EPS.PSC.PSC.PSCOM_MODE_REG	0x0000000003010000	732
TP.TCN1.N1.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG	0x0000000003010001	733
TP.TCN1.N1.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG	0x0000000003010008	736
TP.TCN1.N1.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG	0x0000000003010005	735
TP.TCN1.N1.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG	0x0000000003010006	735
TP.TCN1.N1.EPS.THERM.CONTROL_REG	0x0000000003050012	861
TP.TCN1.N1.EPS.THERM.DTS_RESULT0	0x0000000003050000	858
TP.TCN1.N1.EPS.THERM.DTS_TRC_RESULT	0x0000000003050003	858
TP.TCN1.N1.EPS.THERM.ERR_STATUS_REG	0x0000000003050013	861
TP.TCN1.N1.EPS.THERM.INJECT_REG	0x0000000003050011	860
TP.TCN1.N1.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000003050016	863
TP.TCN1.N1.EPS.THERM.SKITTER_DATA0	0x0000000003050019	863
TP.TCN1.N1.EPS.THERM.SKITTER_DATA1	0x000000000305001A	863
TP.TCN1.N1.EPS.THERM.SKITTER_DATA2	0x000000000305001B	863
TP.TCN1.N1.EPS.THERM.SKITTER_FORCE_REG	0x0000000003050014	862
TP.TCN1.N1.EPS.THERM.SKITTER_MODE_REG	0x0000000003050010	860
TP.TCN1.N1.EPS.THERM.THERM_MODE_REG	0x000000000305000F	859
TP.TCN1.N1.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000305001C	864
TP.TCN1.N1.ERROR_STATUS	0x000000000303000F	845
TP.TCN1.N1.FIR_MASK	0x0000000003040002	850
TP.TCN1.N1.HOSTATTN	0x0000000003040009	852
TP.TCN1.N1.HOSTATTN_MASK	0x000000000304001A	858
TP.TCN1.N1.LOCAL_FIR	0x000000000304000A	853
TP.TCN1.N1.LOCAL_XSTOP_ERR	0x0000000003040018	857

Mnemonic	Address	Page
TP.TCN1.N1.LOCAL_XSTOP_MASK	0x0000000003040019	858
TP.TCN1.N1.OPCG_ALIGN	0x0000000003030001	832
TP.TCN1.N1.OPCG_CAPT1	0x0000000003030010	846
TP.TCN1.N1.OPCG_CAPT2	0x0000000003030011	847
TP.TCN1.N1.OPCG_CAPT3	0x0000000003030012	847
TP.TCN1.N1.OPCG_REG0	0x0000000003030002	833
TP.TCN1.N1.OPCG_REG1	0x0000000003030003	834
TP.TCN1.N1.OPCG_REG2	0x0000000003030004	834
TP.TCN1.N1.RFIR	0x0000000003040001	850
TP.TCN1.N1.SCAN_REGION_TYPE	0x0000000003030005	836
TP.TCN1.N1.SPATTN	0x0000000003040004	851
TP.TCN1.N1.SPA_MASK	0x0000000003040007	851
TP.TCN1.N1.SYNC_CONFIG	0x0000000003030000	831
TP.TCN1.N1.TRA0.TR0.TRACE_HI_DATA_REG	0x0000000003010400	736
TP.TCN1.N1.TRA0.TR0.TRACE_LO_DATA_REG	0x0000000003010401	736
TP.TCN1.N1.TRA0.TR0.TRACE_TRCTRL_CONFIG	0x0000000003010402	737
TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x0000000003010403	737
TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x0000000003010404	737
TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_2	0x0000000003010405	738
TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x0000000003010406	738
TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x0000000003010407	738
TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x0000000003010408	738
TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x0000000003010409	738
TP.TCN1.N1.TRA0.TR1.TRACE_HI_DATA_REG	0x0000000003010440	740
TP.TCN1.N1.TRA0.TR1.TRACE_LO_DATA_REG	0x0000000003010441	740
TP.TCN1.N1.TRA0.TR1.TRACE_TRCTRL_CONFIG	0x0000000003010442	740
TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_0	0x0000000003010443	741
TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_1	0x0000000003010444	741
TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_2	0x0000000003010445	741
TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_3	0x0000000003010446	741
TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_4	0x0000000003010447	742
TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_5	0x0000000003010448	742
TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_9	0x0000000003010449	742
TP.TCN1.N1.TRA1.TR0.TRACE_HI_DATA_REG	0x0000000003010480	743
TP.TCN1.N1.TRA1.TR0.TRACE_LO_DATA_REG	0x0000000003010481	744
TP.TCN1.N1.TRA1.TR0.TRACE_TRCTRL_CONFIG	0x0000000003010482	744
TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_0	0x0000000003010483	744
TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_1	0x0000000003010484	745
TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_2	0x0000000003010485	745
TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_3	0x0000000003010486	745
TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_4	0x0000000003010487	745
TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_5	0x0000000003010488	745
TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_9	0x0000000003010489	746
TP.TCN1.N1.TRA1.TR1.TRACE_HI_DATA_REG	0x00000000030104C0	747
TP.TCN1.N1.TRA1.TR1.TRACE_LO_DATA_REG	0x00000000030104C1	747
TP.TCN1.N1.TRA1.TR1.TRACE_TRCTRL_CONFIG	0x00000000030104C2	748
TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_0	0x00000000030104C3	748
TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_1	0x00000000030104C4	748

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TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_2	0x00000000030104C5	748
TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_3	0x00000000030104C6	749
TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_4	0x00000000030104C7	749
TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_5	0x00000000030104C8	749
TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_9	0x00000000030104C9	749
TP.TCN1.N1.TRA2.TR0.TRACE_HI_DATA_REG	0x0000000003010500	751
TP.TCN1.N1.TRA2.TR0.TRACE_LO_DATA_REG	0x0000000003010501	751
TP.TCN1.N1.TRA2.TR0.TRACE_TRCTRL_CONFIG	0x0000000003010502	751
TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_0	0x0000000003010503	752
TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_1	0x0000000003010504	752
TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_2	0x0000000003010505	752
TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_3	0x0000000003010506	752
TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_4	0x0000000003010507	753
TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_5	0x0000000003010508	753
TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_9	0x0000000003010509	753
TP.TCN1.N1.TRA2.TR1.TRACE_HI_DATA_REG	0x0000000003010540	754
TP.TCN1.N1.TRA2.TR1.TRACE_LO_DATA_REG	0x0000000003010541	755
TP.TCN1.N1.TRA2.TR1.TRACE_TRCTRL_CONFIG	0x0000000003010542	755
TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_0	0x0000000003010543	755
TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_1	0x0000000003010544	756
TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_2	0x0000000003010545	756
TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_3	0x0000000003010546	756
TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_4	0x0000000003010547	756
TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_5	0x0000000003010548	756
TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_9	0x0000000003010549	757
TP.TCN1.N1.TRA3.TR0.TRACE_HI_DATA_REG	0x0000000003010580	758
TP.TCN1.N1.TRA3.TR0.TRACE_LO_DATA_REG	0x0000000003010581	758
TP.TCN1.N1.TRA3.TR0.TRACE_TRCTRL_CONFIG	0x0000000003010582	759
TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_0	0x0000000003010583	759
TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_1	0x0000000003010584	759
TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_2	0x0000000003010585	759
TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_3	0x0000000003010586	760
TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_4	0x0000000003010587	760
TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_5	0x0000000003010588	760
TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_9	0x0000000003010589	760
TP.TCN1.N1.TRA3.TR1.TRACE_HI_DATA_REG	0x00000000030105C0	762
TP.TCN1.N1.TRA3.TR1.TRACE_LO_DATA_REG	0x00000000030105C1	762
TP.TCN1.N1.TRA3.TR1.TRACE_TRCTRL_CONFIG	0x00000000030105C2	762
TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_0	0x00000000030105C3	763
TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_1	0x00000000030105C4	763
TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_2	0x00000000030105C5	763
TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_3	0x00000000030105C6	763
TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_4	0x00000000030105C7	764
TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_5	0x00000000030105C8	764
TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_9	0x00000000030105C9	764
TP.TCN1.N1.TRA4.TR0.TRACE_HI_DATA_REG	0x0000000003010600	765
TP.TCN1.N1.TRA4.TR0.TRACE_LO_DATA_REG	0x0000000003010601	766
TP.TCN1.N1.TRA4.TR0.TRACE_TRCTRL_CONFIG	0x0000000003010602	766

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TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_0	0x0000000003010603	766
TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_1	0x0000000003010604	767
TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_2	0x0000000003010605	767
TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_3	0x0000000003010606	767
TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_4	0x0000000003010607	767
TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_5	0x0000000003010608	767
TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_9	0x0000000003010609	768
TP.TCN1.N1.TRA4.TR1.TRACE_HI_DATA_REG	0x0000000003010640	769
TP.TCN1.N1.TRA4.TR1.TRACE_LO_DATA_REG	0x0000000003010641	769
TP.TCN1.N1.TRA4.TR1.TRACE_TRCTRL_CONFIG	0x0000000003010642	770
TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_0	0x0000000003010643	770
TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_1	0x0000000003010644	770
TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_2	0x0000000003010645	770
TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_3	0x0000000003010646	771
TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_4	0x0000000003010647	771
TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_5	0x0000000003010648	771
TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_9	0x0000000003010649	771
TP.TCN1.N1.XFIR	0x0000000003040000	849
TP.TCN1.N1.XSTOP1	0x000000000303000C	841
TP.TCN1.N1.XSTOP2	0x000000000303000D	842
TP.TCN1.N1.XSTOP3	0x000000000303000E	844
VA.VA_NORTH.VA_RG.SCF.VAS_BUFCTL	0x000000000301180C	805
VA.VA_NORTH.VA_RG.SCF.VAS_CAMDATA0	0x0000000003011834	821
VA.VA_NORTH.VA_RG.SCF.VAS_CAMDATA1	0x0000000003011835	821
VA.VA_NORTH.VA_RG.SCF.VAS_CAMDISPCNTL	0x0000000003011833	820
VA.VA_NORTH.VA_RG.SCF.VAS_DBGCONT	0x000000000301182E	819
VA.VA_NORTH.VA_RG.SCF.VAS_DBGNORTH	0x000000000301182D	817
VA.VA_NORTH.VA_RG.SCF.VAS_DBGTRIG	0x000000000301182F	819
VA.VA_NORTH.VA_RG.SCF.VAS_ERRINJNO	0x0000000003011832	820
VA.VA_NORTH.VA_RG.SCF.VAS_FIR_ACTION0_REG	0x0000000003011806	803
VA.VA_NORTH.VA_RG.SCF.VAS_FIR_ACTION1_REG	0x0000000003011807	803
VA.VA_NORTH.VA_RG.SCF.VAS_FIR_MASK_REG	0x0000000003011803	801
VA.VA_NORTH.VA_RG.SCF.VAS_FIR_REG	0x0000000003011800	799
VA.VA_NORTH.VA_RG.SCF.VAS_FIR_WOF_REG	0x0000000003011808	804
VA.VA_NORTH.VA_RG.SCF.VAS_INERRRPT	0x000000000301182B	816
VA.VA_NORTH.VA_RG.SCF.VAS_MISCCTL	0x000000000301180D	805
VA.VA_NORTH.VA_RG.SCF.VAS_MMIOCTL	0x0000000003011829	814
VA.VA_NORTH.VA_RG.SCF.VAS_MMIODATA	0x000000000301182A	816
VA.VA_NORTH.VA_RG.SCF.VAS_MMIOECC	0x0000000003011831	820
VA.VA_NORTH.VA_RG.SCF.VAS_PMCNTL	0x0000000003011830	820
VA.VA_NORTH.VA_RG.SCF.VAS_RGERRRPT	0x000000000301182C	817
VA.VA_NORTH.VA_RG.SCF.VAS_RMABAR	0x000000000301180E	806
VA.VA_NORTH.VA_RG.SCF.VAS_RMABARM	0x000000000301180F	806
VA.VA_NORTH.VA_RG.SCF.VAS_UWMBAR	0x000000000301180B	804
VA.VA_NORTH.VA_RG.SCF.VAS_WCMBAR	0x000000000301180A	804
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON0BAR	0x0000000003011810	806
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON0CMP	0x0000000003011820	810
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON0WID	0x0000000003011818	808

Mnemonic	Address	Page
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON1BAR	0x0000000003011811	806
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON1CMP	0x0000000003011821	811
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON1WID	0x0000000003011819	809
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON2BAR	0x0000000003011812	807
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON2CMP	0x0000000003011822	811
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON2WID	0x000000000301181A	809
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON3BAR	0x0000000003011813	807
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON3CMP	0x0000000003011823	812
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON3WID	0x000000000301181B	809
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON4BAR	0x0000000003011814	807
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON4CMP	0x0000000003011824	812
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON4WID	0x000000000301181C	809
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON5BAR	0x0000000003011815	808
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON5CMP	0x0000000003011825	813
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON5WID	0x000000000301181D	810
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON6BAR	0x0000000003011816	808
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON6CMP	0x0000000003011826	813
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON6WID	0x000000000301181E	810
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON7BAR	0x0000000003011817	808
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON7CMP	0x0000000003011827	814
VA.VA_NORTH.VA_RG.SCF.VAS_WRMON7WID	0x000000000301181F	810
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_CQERRRPT	0x0000000003011848	824
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_DBGSOUTH	0x000000000301184C	827
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_EGERRRPT	0x000000000301184A	826
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_ERRINJSO	0x000000000301184B	826
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PBCFG0	0x000000000301184D	829
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PBCFG1	0x000000000301184E	830
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG1	0x0000000003011841	821
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG2	0x0000000003011842	822
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG3	0x0000000003011843	822
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG4	0x0000000003011844	822
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG5	0x0000000003011845	823
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG6	0x0000000003011846	823
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG7	0x0000000003011847	823
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_SOUTHCTL	0x000000000301184F	830
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_WCBSBAR	0x0000000003011840	821
VA.VA_SOUTH.VA_EG.EG_SCF.VAS_WCERRRPT	0x0000000003011849	825

The POWER9 processor registers are listed in the following tables.

Register Name	Chiplet Control Register 0
Mnemonic	TP.TCN1.N1.CPLT_CTRL0
Address	0000000003000000 (SCOM) 0000000003000010 (SCOM1) 0000000003000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select the ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks are used from a chiplet with ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the synchronous clock for asynchronous latches. (The initial value is 1.)
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode. (The initial value is 1.)
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force an alignment signal to be sent. (The initial value is 1. Drop before dropping flushmode_inh.)
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set the array into write through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: AVP mode. Switches from refresh pulse to phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC:
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC:
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode. For example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of N1L latches. Prevent lock when switching SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC:
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO select.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INT mode for BSC.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Enables delaying the alignment by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into flush state. For DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select. 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM program mode.
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only. Sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. LBIST is controlled by Pin, not by OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	Chiplet Control Register 1
Mnemonic	TP.TCN1.N1.CPLT_CTRL1
Address	0000000003000001 (SCOM) 0000000003000011 (SCOM1) 0000000003000021 (SCOM2)
Description	This register contains the second set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL fence. Protect the VITL region logic from pollution by other regions during LBIST, or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for the pervasive region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for region MCD.
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for regions VA - VAS.
7	RW	WO_OR	WO_CLEAR	TC_REGION3_FENCE: Fence for regions PBIOO0 - PB.
8	RW	WO_OR	WO_CLEAR	TC_REGION4_FENCE: Fence for regions PBIOO1 - PB.
9	RW	WO_OR	WO_CLEAR	TC_REGION5_FENCE: Fence for regions MCS23 - MCU.
10	RW	WO_OR	WO_CLEAR	UNUSED_10B: Unused.
11	RW	WO_OR	WO_CLEAR	UNUSED_11B: Unused.
12	RW	WO_OR	WO_CLEAR	UNUSED_12B: Unused.
13	RW	WO_OR	WO_CLEAR	UNUSED_13B: Unused.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.
15	RW	WO_OR	WO_CLEAR	RESERVED: Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE:
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	UNUSED_20B: Unused.
21	RW	WO_OR	WO_CLEAR	UNUSED_21B: Unused.
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	Chiplet Configuration Register 0
Mnemonic	TP.TCN1.N1.CPLT_CONF0
Address	0000000003000008 (SCOM) 0000000003000018 (SCOM1) 0000000003000028 (SCOM2)
Description	This register contains the first set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 select.
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 select.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 select.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: ABIST overflow/failure indication select.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection. Enables the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from CC or CPLT_CTRL.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in CC, which are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: System ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	**Chiplet Configuration Register 1**
Mnemonic	TP.TCN1.N1.CPLT_CONF1
Address	0000000003000009 (SCOM) 0000000003000019 (SCOM1) 0000000003000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0D: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1D: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2D: Unused.
3	RW	WO_OR	WO_CLEAR	UNUSED_3D: Unused.
4	RW	WO_OR	WO_CLEAR	IOVALID_4D:
5	RW	WO_OR	WO_CLEAR	IOVALID_5D:
6	RW	WO_OR	WO_CLEAR	IOVALID_6D:
7	RW	WO_OR	WO_CLEAR	IOVALID_7D:
8	RW	WO_OR	WO_CLEAR	IOVALID_8D:
9	RW	WO_OR	WO_CLEAR	IOVALID_9D:
10	RW	WO_OR	WO_CLEAR	IOVALID_10D:
11	RW	WO_OR	WO_CLEAR	IOVALID_11D:
12	RW	WO_OR	WO_CLEAR	FREE_USAGE_12D: Free usage.
13	RW	WO_OR	WO_CLEAR	FREE_USAGE_13D: Free usage.
14	RW	WO_OR	WO_CLEAR	FREE_USAGE_14D: Free usage.
15	RW	WO_OR	WO_CLEAR	FREE_USAGE_15D: Free usage.
16	RW	WO_OR	WO_CLEAR	FREE_USAGE_16D: Free usage.
17	RW	WO_OR	WO_CLEAR	FREE_USAGE_17D: Free usage.
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	Chiplet Status Register
Mnemonic	TP.TCN1.N1.CPLT_STAT0
Address	0000000003000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask Register. A mask only masks the interrupt, not the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM and EDRAM ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic out port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic out port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done for LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that the chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	FREE_USAGE_12E: Chiplet specific.
13	ROX	FREE_USAGE_13E: Chiplet specific.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.
16	ROX	FREE_USAGE_16E: Free usage.
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	Chiplet Mask Register
Mnemonic	TP.TCN1.N1.CPLT_MASK0
Address	0000000003000101 (SCOM)
Description	This register masks the interrupt on a bit change of the Chiplet Status Register. It does not mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: This field provides bitwise masking of the Chiplet Status Register.

Register Name	Control Protect Mode Register
Mnemonic	TP.TCN1.N1.CTRL_PROTECT_MODE_REG
Address	00000000030003FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: This bit enables read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: This bit enables write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCN1.N1.CTRL_ATOMIC_LOCK_REG
Address	00000000030003FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: This bit enables an atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: This field contains the atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: This field is an atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCN1.N1.EPS.PSC.PSC.PSCOM_MODE_REG
Address	0000000003010000 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on a PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on a PCB write data parity error.
2	RW	UNUSED_2B. Unused.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on a DL return write data parity error.
4	RW	WATCHDOG_ENABLE: Watchdog enable.

Bits	SCOM	Field Mnemonic: Description
5:6	RW	SCOM_HANG_LIMIT: 0b11 = 256 0b10 = 512 0b01 = 768 0b00 = 1023
7	RW	FORCE_ALL_RINGS: This bit is set to a logical 1 if all rings should be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on statevec parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCN1.N1.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000003010001 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on p2s machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.

Bits	SCOM	Field Mnemonic: Description
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on p2s machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	**PSCOMLE Error Mask Register**
Mnemonic	TP.TCN1.N1.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	0000000003010002 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on the interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on the p2s machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting or ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.

Bits	SCOM	Field Mnemonic: Description
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCN1.N1.EPS.PSC.PSC.ADDR_TRAP_REG
Address	0000000003010003 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: This field contains the PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write, of the last transaction with an error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: Reserved 0.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2 parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit. This bit is set to 1 if no parity error is detected in the satellite number or acknowledgment bits.
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: This bit is set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: This bit is set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: This bit is set if an invalid register address is detected by the satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TCN1.N1.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	0000000003010005 (SCOM)
Description	This register enables the ring lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon write to specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	Write Protect Rings Register
Mnemonic	TP.TCN1.N1.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	0000000003010006 (SCOM)
Description	This register writes ring protect bit maps.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Writes a protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TCN1.N1.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	0000000003010007 (SCOM)
Description	This register provides a bit mask for atomic locking.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: This field provides a bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TCN1.N1.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	0000000003010008 (SCOM)
Description	This register provides a bit mask for ring fencing.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: This field provides a bit mask for ring fencing on a ring-by-ring basis.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000003010400 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000003010401 (SCOM)
Description	Trace array low data register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.

Bits	SCOM	Field Mnemonic: Description
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address pointing to the last entry.

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000003010402 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000003010403 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000003010404 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000003010405 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000003010406 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000003010407 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000003010408 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000003010409 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression. Stores data every cycle.
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.

Bits	SCOM	Field Mnemonic: Description
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: DD1 workaround. Stretches the trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_HI_DATA_REG
Address	0000000003010440 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_LO_DATA_REG
Address	0000000003010441 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address pointing to last entry.

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_TRCTRL_CONFIG
Address	0000000003010442 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enables unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.

Bits	SCOM	Field Mnemonic: Description
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000003010443 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000003010444 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000003010445 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000003010446 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000003010447 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000003010448 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA0.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000003010449 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression (stores data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_HI_DATA_REG
Address	0000000003010480 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_LO_DATA_REG
Address	0000000003010481 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_TRCTRL_CONFIG
Address	0000000003010482 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enables unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000003010483 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000003010484 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000003010485 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000003010486 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000003010487 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000003010488 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA1.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000003010489 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression (stores data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.

Bits	SCOM	Field Mnemonic: Description
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_HI_DATA_REG
Address	00000000030104C0 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_LO_DATA_REG
Address	00000000030104C1 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_TRCTRL_CONFIG
Address	00000000030104C2 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_0
Address	00000000030104C3 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_1
Address	00000000030104C4 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_2
Address	00000000030104C5 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.

Bits	SCOM	Field Mnemonic: Description
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_3
Address	00000000030104C6 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_4
Address	00000000030104C7 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_5
Address	00000000030104C8 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA1.TR1.TRACE_TRDATA_CONFIG_9
Address	00000000030104C9 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression. Stores data every cycle.
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).

Bits	SCOM	Field Mnemonic: Description
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: DD1 workaround. Stretches the trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.

Bits	SCOM	Field Mnemonic: Description
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_HI_DATA_REG
Address	0000000003010500 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_LO_DATA_REG
Address	0000000003010501 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_TRCTRL_CONFIG
Address	0000000003010502 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).

Bits	SCOM	Field Mnemonic: Description
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000003010503 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000003010504 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000003010505 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000003010506 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000003010507 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000003010508 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA2.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000003010509 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression. Stores data every cycle.
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: DD1 workaround. Stretches the trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_HI_DATA_REG
Address	0000000003010540 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_LO_DATA_REG
Address	0000000003010541 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_TRCTRL_CONFIG
Address	0000000003010542 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000003010543 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000003010544 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000003010545 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000003010546 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000003010547 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000003010548 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA2.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000003010549 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression. Stores data every cycle.
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.

Bits	SCOM	Field Mnemonic: Description
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: DD1 workaround. Stretches the trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_HI_DATA_REG
Address	0000000003010580 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_LO_DATA_REG
Address	0000000003010581 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_TRCTRL_CONFIG
Address	0000000003010582 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000003010583 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000003010584 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000003010585 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.

Bits	SCOM	Field Mnemonic: Description
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000003010586 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000003010587 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000003010588 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA3.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000003010589 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression. Stores data every cycle.
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).

Bits	SCOM	Field Mnemonic: Description
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: DD1 workaround. Stretches the trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.

Bits	SCOM	Field Mnemonic: Description
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_HI_DATA_REG
Address	00000000030105C0 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_LO_DATA_REG
Address	00000000030105C1 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_TRCTRL_CONFIG
Address	00000000030105C2 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).

Bits	SCOM	Field Mnemonic: Description
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_0
Address	00000000030105C3 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_1
Address	00000000030105C4 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_2
Address	00000000030105C5 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_3
Address	00000000030105C6 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_4
Address	00000000030105C7 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_5
Address	00000000030105C8 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA3.TR1.TRACE_TRDATA_CONFIG_9
Address	00000000030105C9 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression. Stores data every cycle.
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: DD1 workaround. Stretches the trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_HI_DATA_REG
Address	0000000003010600 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_LO_DATA_REG
Address	0000000003010601 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_TRCTRL_CONFIG
Address	0000000003010602 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000003010603 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000003010604 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000003010605 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000003010606 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000003010607 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000003010608 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA4.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000003010609 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression. Stores data every cycle.
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.

Bits	SCOM	Field Mnemonic: Description
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: DD1 workaround. Stretches the trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_HI_DATA_REG
Address	0000000003010640 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_LO_DATA_REG
Address	0000000003010641 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_TRCTRL_CONFIG
Address	0000000003010642 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000003010643 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000003010644 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000003010645 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.

Bits	SCOM	Field Mnemonic: Description
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000003010646 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000003010647 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000003010648 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN1.N1.TRA4.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000003010649 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disables trace data compression. Stores data every cycle.
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Takes into account (cares about) changes in the error bit for trace data compression (default = 0).

Bits	SCOM	Field Mnemonic: Description
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits (00:23). 0b01 = Debug bus bits (24:47). 0b10 = Debug bus bits (48:71). 0b11 = Debug bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Inverts TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Inverts TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Inverts the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: DD1 workaround. Stretches the trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.

Bits	SCOM	Field Mnemonic: Description
37	RW	Reserved field.

Register Name	Debug Mode Register
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_MODE_REG
Address	00000000030107C0 (SCOM)
Description	This register is debug macro configuration register 0 for the configuration component.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: Global broadcast mode (0 - 2): 100 = dbg_trace_run and dbg_trace_freeze 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze 110 = dbg_triggers_out(0 to 1) 111 = pc_tcdbg_triggers(0 to 1) (from core)
3:5	RW	TRACE_SEL_MODE: Select source for trace_run and bank: 001 = core trace run and bank 010 = tp broadcast run and 0 011 = tc_dbg_inter_brcst latched 100 = tc_dbg_dbg_sync_brcst_rcv else: dbg_trace_run and dbg_trace_bank
6:7	RW	TRIG_SEL_MODE: Select source for tcdbg_trigger(0): 10 = global broadcast 11 = pc_tcdbg_trigger (from core) else: dbg_triggers_out(0:1)
8	RW	STOP_ON_XSTOP_SELECTION: This bit enables a trace stop on a checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: This bit enables a trace stop on a recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: This bit enables a trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select the freeze source: 0 = Local debug freeze. 1 = Via broadcast: tp_tcdbg_glb_brcst(1).
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode; currently unused because obsolete. See trace_sel_mode.
14	RO	constant = 0b0 sync_brcst_mode
15	RO	constant = 0b0
16:31	ROX	DBG_STATUS: Debug status.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000030107C1 (SCOM)
Description	This register is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0): 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst1_dbg_cond1 003 select inst1_dbg_cond2 004 select inst1_dbg_cond3 005 select inst1_dbg_cond2timeout 006 select inst2_dbg_cond1 007 select inst2_dbg_cond2 008 select inst2_dbg_cond3 009 select inst2_dbg_cond2timeout 010 select inst3_dbg_cond1 - unused, tied down 011 select inst3_dbg_cond2 - unused, tied down 012 select inst3_dbg_cond3 - unused, tied down 013 select inst3_dbg_cond2timeout - unused, tied down 014 select inst4_dbg_cond1 - unused, tied down 015 select inst4_dbg_cond2 - unused, tied down 016 select inst4_dbg_cond3 - unused, tied down 017 select inst4_dbg_cond2timeout - unused, tied down 018 select inst1_dbg_trig_sp 019 select inst2_dbg_trig_sp 020 select inst3_dbg_trig_sp - unused, tied down 021 select inst4_dbg_trig_sp - unused, tied down 022 select tctrc_tcdbg_trigger_a(0) 023 select tctrc_tcdbg_trigger_b(0) 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0) 025 select tctrc_tcdbg_trigger_a(1) 026 select tctrc_tcdbg_trigger_b(1) 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1) 028 select tctrc_tcdbg_trigger_a(2) 029 select tctrc_tcdbg_trigger_b(2) 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2) 031 select tctrc_tcdbg_trigger_a(3) 032 select tctrc_tcdbg_trigger_b(3) 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3) 034 select tctrc_tcdbg_trigger_a(4) 035 select tctrc_tcdbg_trigger_b(4) 036 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4) 037 select tctrc_tcdbg_trigger_a(5) 038 select tctrc_tcdbg_trigger_b(5) 039 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5) 040 select tctrc_tcdbg_trigger_a(6) 041 select tctrc_tcdbg_trigger_b(6) 042 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6) 043 select tctrc_tcdbg_trigger_a(7) 044 select tctrc_tcdbg_trigger_b(7) 045 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7) 046 select tctrc_tcdbg_trigger_a(8) 047 select tctrc_tcdbg_trigger_b(8) 048 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8) 049 select tctrc_tcdbg_trigger_a(9) 050 select tctrc_tcdbg_trigger_b(9) 051 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9) 052 select tctrc_tcdbg_trigger_a(10) 053 select tctrc_tcdbg_trigger_b(10) 054 select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10) 055 select tctrc_tcdbg_trigger_a(11) 056 select tctrc_tcdbg_trigger_b(11) 057 select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11) 058 select tctrc_tcdbg_trigger_a(12) 059 select tctrc_tcdbg_trigger_b(12)

Bits	SCOM	Field Mnemonic: Description
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Front-end instance 1, counter 1 in-a-row mode.
33	RW	INST1_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST1_UNUSED_1: Unused.
39	RW	INST1_C2_INAROW_MODE: Front-end instance 1, counter 2 in-a-row mode.
40	RW	INST1_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST1_UNUSED_2: Unused
46	RW	INST1_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST1_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST1_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST1_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: Instance 1 condition 1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: Instance 1 condition 2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front-end instance 1: reset condition 3 for reset_c3_on_c0: 0b100 = dbg_cross_couple_triggers(4) 0b101 = dbg_cross_couple_triggers(12) 0b110 = dbg_cross_couple_triggers(20) 0b111 = dbg_cross_couple_triggers(28)

Register Name	Debug Instance 1 Condition 2 Register
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_INST1_COND_REG_2
Address	00000000030107C2 (SCOM)
Description	This is debug macro configuration register 2 for front-end 1 component

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same of all selectors: 00000 - Selects inst1_cond1_trig_a. 00001 - Selects inst1_cond1_trig_b. 00010 - Selects inst1_cond2_trig_a. 00011 - Selects inst1_cond2_trig_b. 00100 - Selects inst1_condition1. 00101 - Selects inst1_condition2. 00110 - Selects inst1_condition3. 00111 - Selects inst1_cond2_timeout. 01000 - Selects inst2_cond1_trig_a. 01001 - Selects inst2_cond1_trig_b. 01010 - Selects inst2_cond2_trig_a. 01011 - Selects inst2_cond2_trig_b. 01100 - Selects inst2_condition1. 01101 - Selects inst2_condition2. 01110 - Selects inst2_condition3. 01111 - Selects inst2_cond2_timeout. 10000 - Selects inst3_cond1_trig_a. 10001 - Selects inst3_cond1_trig_b. 10010 - Selects inst3_cond2_trig_a. 10011 - Selects inst3_cond2_trig_b. 10100 - Selects inst3_condition1. 10101 - Selects inst3_condition2. 10110 - Selects inst3_condition3. 10111 - Selects inst3_cond2_timeout. 11000 - Selects inst4_cond1_trig_a. 11001 - Selects inst4_cond1_trig_b. 11010 - Selects inst4_cond2_trig_a. 11011 - Selects inst4_cond2_trig_b. 11100 - Selects inst4_condition1. 11101 - Selects inst4_condition2. 11110 - Selects inst4_condition3. 11111 - Selects inst4_cond2_timeout.
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: Instance 1 cross couple select 1 b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: Instance 1 cross couple select 2 a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: Instance 1 cross couple select 2 b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate to compare without an actual compare.

Register Name	Debug Instance 1 Condition 3 Register
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_INST1_COND_REG_3
Address	00000000030107C3 (SCOM)
Description	This is debug macro configuration register 3 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to compare the value for dbg_cond_comp_1.

Register Name	**Debug Instance 2 Condition 1 Register**
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000030107C4 (SCOM)
Description	This is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst2_dbg_cond1. 003 select inst2_dbg_cond2. 004 select inst2_dbg_cond3. 005 select inst2_dbg_cond2timeout. 006 select inst2_dbg_cond1. 007 select inst2_dbg_cond2. 008 select inst2_dbg_cond3. 009 select inst2_dbg_cond2timeout. 010 select inst3_dbg_cond1 - Unused, tied down. 011 select inst3_dbg_cond2 - Unused, tied down. 012 select inst3_dbg_cond3 - Unused, tied down. 013 select inst3_dbg_cond2timeout - Unused, tied down. 014 select inst4_dbg_cond1 - Unused, tied down. 015 select inst4_dbg_cond2 - Unused, tied down. 016 select inst4_dbg_cond3 - Unused, tied down. 017 select inst4_dbg_cond2timeout - Unused, tied down. 018 select inst2_dbg_trig_sp. 019 select inst2_dbg_trig_sp. 020 select inst3_dbg_trig_sp - Unused, tied down. 021 select inst4_dbg_trig_sp - Unused, tied down. 022 select tctrc_tcdbg_trigger_a(0). 023 select tctrc_tcdbg_trigger_b(0). 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 select tctrc_tcdbg_trigger_a(1). 026 select tctrc_tcdbg_trigger_b(1). 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 select tctrc_tcdbg_trigger_a(2). 029 select tctrc_tcdbg_trigger_b(2). 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 select tctrc_tcdbg_trigger_a(3). 032 select tctrc_tcdbg_trigger_b(3). 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 select tctrc_tcdbg_trigger_a(4). 035 select tctrc_tcdbg_trigger_b(4). 026 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 027 select tctrc_tcdbg_trigger_a(5). 028 select tctrc_tcdbg_trigger_b(5). 029 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 030 select tctrc_tcdbg_trigger_a(6). 031 select tctrc_tcdbg_trigger_b(6). 032 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 033 select tctrc_tcdbg_trigger_a(7). 034 select tctrc_tcdbg_trigger_b(7). 035 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 036 select tctrc_tcdbg_trigger_a(8). 037 select tctrc_tcdbg_trigger_b(8). 038 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 039 select tctrc_tcdbg_trigger_a(9). 040 select tctrc_tcdbg_trigger_b(9). 041 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 042 select xstop_err. 043 select recov_err. 044 select spattn. 045 select fir_dbg_local_xstop_err. 046 select tc_dbg_inter_brcst(0). 047 select tc_dbg_inter_brcst(1). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare.

Bits	SCOM	Field Mnemonic: Description
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Front-end instance 1 counter 1 in-a-row mode.
33	RW	INST2_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition1.
36:38	RWX	INST2_UNUSED_1: Unused.
39	RW	INST2_C2_INAROW_MODE: Front-end instance 1 counter 2 in-a-row mode.
40	RW	INST2_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST2_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST2_UNUSED_2: Unused.
46	RW	INST2_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST2_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST2_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST2_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: Instance 2 condition 1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: Instance 2 condition 2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front-end instance 1, reset condition 3 for reset_c3_on_c0: 0b100 = dbg_cross_couple_triggers(4). 0b101 = dbg_cross_couple_triggers(12). 0b110 = dbg_cross_couple_triggers(20). 0b111 = dbg_cross_couple_triggers(28).

Register Name	**Debug Instance 2 Condition 2 Register**
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000030107C5 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same of all selectors: 00000 - Selects inst2_cond1_trig_a. 00001 - Selects inst2_cond1_trig_b. 00010 - Selects inst2_cond2_trig_a. 00011 - Selects inst2_cond2_trig_b. 00100 - Selects inst2_condition1. 00101 - Selects inst2_condition2. 00110 - Selects inst2_condition3. 00111 - Selects inst2_cond2_timeout. 01000 - Selects inst2_cond1_trig_a. 01001 - Selects inst2_cond1_trig_b. 01010 - Selects inst2_cond2_trig_a. 01011 - Selects inst2_cond2_trig_b. 01100 - Selects inst2_condition1. 01101 - Selects inst2_condition2. 01110 - Selects inst2_condition3. 01111 - Selects inst2_cond2_timeout. 10000 - Selects inst3_cond1_trig_a. 10001 - Selects inst3_cond1_trig_b. 10010 - Selects inst3_cond2_trig_a. 10011 - Selects inst3_cond2_trig_b. 10100 - Selects inst3_condition1. 10101 - Selects inst3_condition2. 10110 - Selects inst3_condition3. 10111 - Selects inst3_cond2_timeout. 11000 - Selects inst4_cond1_trig_a. 11001 - Selects inst4_cond1_trig_b. 11010 - Selects inst4_cond2_trig_a. 11011 - Selects inst4_cond2_trig_b. 11100 - Selects inst4_condition1. 11101 - Selects inst4_condition2. 11110 - Selects inst4_condition3. 11111 - Selects inst4_cond2_timeout.
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: Instance 2 cross couple select 1 b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: Instance 2 cross couple select 2 a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: Instance 2 cross couple select 2 b.
20:43	RW	INST2_TO_CMP_LT: Compares the value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Forces test mode to indicate compare without actual compare.

Register Name	Debug Instance 2 Condition 3 Register
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_INST2_COND_REG_3
Address	00000000030107C6 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_TRACE_REG_0
Address	00000000030107CD (SCOM)
Description	This is debug macro configuration register 0 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: Enable of instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: Enable of instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: Enable slow LFSR mode of front-end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: Enable slow LFSR mode of front-end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: Select Instance 1 condition 1 for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
10:11	RW	INST1_CONDITION2_TRIG_SEL: Select Instance 1 condition 2 for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: Select instance 1 condition 2 time-out counter for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
14:15	RW	INST2_CONDITION1_TRIG_SEL: Select instance 2 condition 1 for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
16:17	RW	INST2_CONDITION2_TRIG_SEL: Select instance 2 condition 2 trigger for output (external) triggers: 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: Select inst2 c2 time-out counter for output (external) triggers. 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
20:31	RO	constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: Enables trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: Enables trigger on freeze.
34:38	RW	CORE_RAS0_TRIG_SEL:

Bits	SCOM	Field Mnemonic: Description
39:43	RW	CORE_RAS1_TRIG_SEL:
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(0). Note: Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)
54:57	RW	TRIG1_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(1). Note: Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)
58:63	RO	constant = 0b000000

Register Name	Debug Trace 1 Register
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_TRACE_REG_1
Address	00000000030107CE (SCOM)
Description	This is debug macro configuration register 1 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Instance 1 action selection, condition 1: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles

Bits	SCOM	Field Mnemonic: Description
2:3	RW	INST1_CONDITION2_ACTION_DO: Instance 1 action selection, condition 2: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Instance 1 action selection, c2_timeout: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
6:7	RW	INST2_CONDITION1_ACTION_DO: Instance 2 action selection, condition 1: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
8:9	RW	INST2_CONDITION2_ACTION_DO: Instance 2 action selection, condition 2: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Instance 2 action selection, c2_timeout: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
12:23	RO	constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For wait-N.
25	RW	INST1_CONDITION2_ACTION_WAITN: For wait-N.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For wait-N.
27	RW	INST2_CONDITION1_ACTION_WAITN: For wait-N.
28	RW	INST2_CONDITION2_ACTION_WAITN: For wait-N.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For wait-N.
30:35	RO	constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (inst1, condition1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (inst1, condition2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (instance 2, condition1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (instance 2, condition2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 2, c2_timeout).
42:47	RO	constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt 001 = inst1_condition2_lt 010 = inst1_condition3_lt 011 = inst1_cond2_timeout_lt 1XX = disable checkstop_mode

Bits	SCOM	Field Mnemonic: Description
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: Enable_fir_trig_xstop: Enable checkstop on debug trigger: 0 = disable checkstop on debug trigger 1 = enable checkstop on debug trigger
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt 001 = inst2_condition2_lt 010 = inst2_condition3_lt 011 = inst2_cond2_timeout_lt 1XX = disable checkstop_mode
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: enable_fir_error_xstop: Enable checkstop on FIR error: 0 = Disable checkstop on FIR error. 1 = Enable checkstop on FIR error.
56:63	RO	constant = 0b00000000

Register Name	Debug Trace Mode 2 Register
Mnemonic	TP.TCN1.N1.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000030107CF (SCOM)
Description	This is debug macro configuration register 2 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the run-N counter used in trace modes run-N and wait-N.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on run-N match.
19	RW	FORCE_TEST_MODE: Force the run-N condition to be true.
20	RW	ACCUM_HIST_MODE: Accumulate history mode; do not clear history mode when trace_run is active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	Pervasive FIR Register
Mnemonic	MCD0.MCC_FIR_REG
Address	0000000003011000 (SCOM) 0000000003011001 (SCOM1) 0000000003011002 (SCOM2)
Description	This is the local fault-isolation register for the memory coherency directory.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MCD_ARRAY_ECC_UE_ERR: MCD array ECC uncorrectable error.
1	RWX	WOX_AND	WOX_OR	MCD_ARRAY_ECC_CE_ERR: MCD array ECC uncorrectable error.
2	RWX	WOX_AND	WOX_OR	MCD_PB_ADDR_PARITY_ERR: MCD processor bus address parity error.
3	RWX	WOX_AND	WOX_OR	MCD_SM_OR_CASE_ERR: MCD invalid state error.
4	RWX	WOX_AND	WOX_OR	MCD_CL_PROBE_PB_HANG_ERR: Hang poll timer expired on cl_probe.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	MCD_CRESP_ADDR_ERR: Processor bus address error CRESP received.
6	RWX	WOX_AND	WOX_OR	MCD_UNSOLICITED_CRESP_ERR: MCD received a unsolicited CRESP.
7	RWX	WOX_AND	WOX_OR	MCD_TTAG_PARITY_ERR: MCD processor bus TTAG parity error.
8	RWX	WOX_AND	WOX_OR	MCD_FIR_REG_UPDATE_ERR: MCD SCOM register update error.
9	RWX	WOX_AND	WOX_OR	MCD_ACK_DEAD_CRESP_ERR: MCD received an ack_dead_cresp.
10	RWX	WOX_AND	WOX_OR	MCD_SCOM_ERR: PBEH CENT FIR_SCOM error.
11	RWX	WOX_AND	WOX_OR	MCD_SCOM_ERR_DUP: PBEH CENT FIR_SCOM error duplicate.
12:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Pervasive FIR Mask Register
Mnemonic	MCD0.MCD_FIR_MASK_REG
Address	0000000003011003 (SCOM) 0000000003011004 (SCOM1) 0000000003011005 (SCOM2)
Description	Error mask register (Action0, Action1, Mask) = Action select (0, 1, 0) = Recoverable error (0, 0, 0) = Checkstop error (1, 0, 0) = Special attention (x, x, 1) = Masked

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MCD_ARRAY_ECC_UE_MASK: Mask MCD array ECC uncorrectable error.
1	RW	WO_AND	WO_OR	MCD_ARRAY_ECC_CE_MASK: Mask MCD array ECC uncorrectable error.
2	RW	WO_AND	WO_OR	MCD_PB_ADDR_PARITY_MASK: Mask MCD processor bus address parity error.
3	RW	WO_AND	WO_OR	MCD_SM_OR_CASE_MASK: Mask MCD invalid state error.
4	RW	WO_AND	WO_OR	MCD_CL_PROBE_PB_HANG_MASK: Mask hang poll timer expired on cl_probe.
5	RW	WO_AND	WO_OR	MCD_CRESP_ADDR_MASK: Mask processor bus address error CRESP received.
6	RW	WO_AND	WO_OR	MCD_UNSOLICITED_CRESP_MASK: Mask MCD received an unsolicited CRESP.
7	RW	WO_AND	WO_OR	MCD_TTAG_PARITY_MASK: Mask MCD processor bus TTAG parity error.
8	RW	WO_AND	WO_OR	MCD_FIR_REG_UPDATE_ERR_MASK: Mask MCD SCOM register update error.
9	RW	WO_AND	WO_OR	MCD_ACK_DEAD_CRESP_MASK: Mask MCD SCOM register update error.
10	RW	WO_AND	WO_OR	MCD_SCOM_ERR_MASK: PBEH CENT FIR_SCOM error mask.
11	RW	WO_AND	WO_OR	MCD_SCOM_ERR_MASK_DUP: PBEH CENT FIR_SCOM error mask duplicate.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
12:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	Pervasive FIR Action 0 Register
Mnemonic	MCD0.MCD_FIR_ACTION0_REG
Address	0000000003011006 (SCOM)
Description	Action select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:11	RW	FIR_ACTION0: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action Select. (0, 1, 0) = Recoverable error (0, 0, 0) = Checkstop error (1, 0, 0) = Special attention (x, x, 1) = Masked
12:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	Pervasive FIR Action 1 Register
Mnemonic	MCD0.MCD_FIR_ACTION1_REG
Address	0000000003011007 (SCOM)
Description	Action select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:11	RW	FIR_ACTION1: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action Select. (0, 1, 0) = Recoverable error (0, 0, 0) = Checkstop error (1, 0, 0) = Special attention (x, x, 1) = Masked
12:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	MCD TOP (mcd_cn0) Configuration Register
Mnemonic	MCD0.BANK0_MCD_TOP
Address	000000000301100A (SCOM)
Description	MCD TOP (mcd_cn0) Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	BANK0_MCD_TOP_VALID: MCD_TOP valid.
1	RW	BANK0_MCD_TOP_CPG: MCD_TOP group address with other bank.
2	RW	BANK0_MCD_TOP_GRP_MBR_ID: MCD_TOP group member identification.
3	RW	BANK0_MCD_TOP_ALWAYS_RTY: MCD_TOP disable array array access and force rty_dinc response.
4:12	RO	constant = 0b000000000
13:29	RW	BANK0_MCD_TOP_GRP_SIZE: MCD_TOP group size.

Bits	SCOM	Field Mnemonic: Description
30:32	RO	constant = 0b000
33:63	RW	BANK0_MCD_TOP_GRP_BASE: MCD_TOP base address.

Register Name	MCD STR (mcd_cn1) Configuration Register
Mnemonic	MCD0.BANK0_MCD_STR
Address	000000000301100B (SCOM)
Description	MCD STR (mcd_cn1) Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	BANK0_MCD_STR_VALID: MCD_str valid.
1	RW	BANK0_MCD_STR_CPG: MCD_str group address with other bank.
2	RW	BANK0_MCD_STR_GRP_MBR_ID: MCD_str group member identification.
3	RW	BANK0_MCD_STR_ALWAYS_RTY: MCD_str disable array array access and force rty_dinc response.
4:12	RO	constant = 0b000000000
13:29	RW	BANK0_MCD_STR_GRP_SIZE: MCD_str group size.
30:32	RO	constant = 0b000
33:63	RW	BANK0_MCD_STR_GRP_BASE: MCD_str base address.

Register Name	MCD bot (mcd_cn2) Configuration Register
Mnemonic	MCD0.BANK0_MCD_BOT
Address	000000000301100C (SCOM)
Description	MCD bot (mcd_cn2) Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	BANK0_MCD_BOT_VALID: MCD_bot valid.
1	RW	BANK0_MCD_BOT_CPG: MCD_bot group address with other bank.
2	RW	BANK0_MCD_BOT_GRP_MBR_ID: MCD_bot group member identification.
3	RW	BANK0_MCD_BOT_ALWAYS_RTY: MCD_bot disable array array access and force rty_dinc response.
4:12	RO	constant = 0b000000000
13:29	RW	BANK0_MCD_BOT_GRP_SIZE: MCD_bot group size.
30:32	RO	constant = 0b000
33:63	RW	BANK0_MCD_BOT_GRP_BASE: MCD_bot base address.

Register Name	MCD cha (mcd_cn3) Configuration Register
Mnemonic	MCD0.BANK0_MCD_CHA
Address	000000000301100D (SCOM)
Description	MCD cha (mcd_cn3) Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	BANK0_MCD_CHA_VALID: MCD_cha valid.
1	RW	BANK0_MCD_CHA_CPG: MCD_cha group address with other bank.
2	RW	BANK0_MCD_CHA_GRP_MBR_ID: MCD_cha group member identification.
3	RW	BANK0_MCD_CHA_ALWAYS_RTY: MCD_cha disable array array access and force rty_dinc response.
4:12	RO	constant = 0b000000000
13:29	RW	BANK0_MCD_CHA_GRP_SIZE: MCD_cha group size.
30:32	RO	constant = 0b000
33:63	RW	BANK0_MCD_CHA_GRP_BASE: MCD_cha base address.

Register Name	MCD Command Decode Configuration Register
Mnemonic	MCD0.BANK0_MCD_CMD
Address	000000000301100E (SCOM)
Description	MCD command decode configuration register

Bits	SCOM	Field Mnemonic: Description
0:18	RW	BANK0_MCD_CHECK_CMDS: Check commands.
19:30	RO	constant = 0b000000000000
31	RW	BANK0_MCD_CHECK_CMDS_EN: Enable override of check commands.
32:50	RW	BANK0_MCD_SET_CMDS: Set commands.
51:62	RO	constant = 0b000000000000
63	RW	BANK0_MCD_SET_CMDS_EN: Enable override of set commands.

Register Name	MCD Direct Read Write Register
Mnemonic	MCD0.BANK0_MCD_RW
Address	000000000301100F (SCOM)
Description	MCD direct read write register

Bits	SCOM	Field Mnemonic: Description
0	RWX	BANK0_MCD_RDWR_ACCESS_EN: MCD direct read/write access enable.
1	RW	BANK0_MCD_RDWR_WR_ENABLE: MCD direct write enable. Reads when off.
2	RO	constant = 0b0
3	ROX	BANK0_MCD_RDWR_REQ_PEND: MCD direct read/write access pending.
4	ROX	BANK0_MCD_RDWR_READ_STATUS: MCD direct read data is valid.
5	RW	BANK0_MCD_RDWR_WRITE_MODE: MCD write mode: 0 = OR 1 = and
6	ROX	BANK0_MCD_RDWR_WRITE_STATUS: MCD direct write has completed.
7:16	RO	constant = 0b0000000000
17:31	RW	BANK0_MCD_RDWR_ADDR: MCD direct access address.
32:63	RWX	BANK0_MCD_RDWR_RDWR_DATA: MCD read/write data based on wr_enable setting.

Register Name	MCD Recovery Control Register
Mnemonic	MCD0.BANK0_MCD_REC
Address	0000000003011010 (SCOM)
Description	MCD recovery control register

Bits	SCOM	Field Mnemonic: Description
0	RWX	BANK0_MCD_REC_ENABLE: MCD recovery access enable.
1	ROX	BANK0_MCD_REC_DONE: MCD recovery done.
2	RW	BANK0_MCD_REC_CONTINUOUS: MCD recovery continuous setting.
3:4	RO	constant = 0b00
5	ROX	BANK0_MCD_REC_STATUS: MCD recovery status: 0 = idle 1 = running
6:7	RO	constant = 0b00
8:19	RW	BANK0_MCD_REC_PACE: MCD recovery pace between new cache lines.
20	ROX	BANK0_MCD_REC_ADDR_ERROR: MCD recovery has received an address error CRESP.
21:35	RW	BANK0_MCD_REC_ADDR: MCD recovery start address.
36:39	RO	constant = 0b0000
40:43	RW	BANK0_MCD_REC_RTY_COUNT: MCD recovery retries before failure.
44:48	RO	constant = 0b00000
49:63	RW	BANK0_MCD_REC_VG_COUNT: MCD recovery vector groups to recovery.

Register Name	MCD Vector Group Configuration Register
Mnemonic	MCD0.BANK0_MCD_VGC
Address	0000000003011011 (SCOM)
Description	MCD vector group configuration register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	BANK0_MCD_AVAIL_GROUPS: Available groups, for ECC.
16:31	RO	constant = 0b0000000000000000
32	RW	BANK0_MCD_4X4_MODE: Enable Brazos 4x4.
33	RW	BANK0_MCD_HANG_POLL_ENABLE: Enables hang_poll.
34	RW	BANK0_MCD_RND_BACKOFF_ENABLE: Enables rnd_backoff.
35	RW	BANK0_MCD_DROP_PRIORITY_MODE: Reduces drop_priority: 0 = high 1 = low
36	RW	BANK0_MCD_MASK_AGV_DISABLE_MODE: Reduce mask_agv_disable: 0 = mask 1 = not mask
37	RW	BANK0_MCD_XLATE_TO_ADDR_ID_ENABLE: Reduces mask_agv_disable: 0 = mask 1 = not mask

Bits	SCOM	Field Mnemonic: Description
38:63	RO	constant = 0b00000000000000000000000000

Register Name	MCD ECC Error Capture Register
Mnemonic	MCD0.MCD_ECAP
Address	0000000003011012 (SCOM)
Description	MCD ECC Error Capture Register

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	MCD_ECAP_ECC_CLEAR: Write of 1 clears ECC capture data.
1	RO	constant = 0b0
2	ROX	MCD_ECAP_ECC_UE: ECC capture data is for an uncorrectable error.
3	ROX	MCD_ECAP_ECC_CE: ECC capture data is for a correctable error.
4:7	ROX	MCD_ECAP_ECC_ERROR_COUNT: Number of ECC errors detected. Clamps to 0xF.
8:9	RO	constant = 0b00
10:23	ROX	MCD_ECAP_ECC_ERROR_ADDR: Line (0 - 9) and array (10 - 13) of last captured ECC error.
24:31	ROX	MCD_ECAP_ECC_SYNDROME: Syndrome of last captured ECC error.
32	RO	constant = 0b0
33	ROX	MCD_ECAP_SLICE0_CFG_ECC_UE_ERR:
34	ROX	MCD_ECAP_SLICE0_CFG_ECC_CE_ERR:
35	ROX	MCD_ECAP_SLICE1_CFG_ECC_UE_ERR:
36	ROX	MCD_ECAP_SLICE1_CFG_ECC_CE_ERR:
37	ROX	MCD_ECAP_SLICE2_CFG_ECC_UE_ERR:
38	ROX	MCD_ECAP_SLICE2_CFG_ECC_CE_ERR:
39	ROX	MCD_ECAP_SLICE3_CFG_ECC_UE_ERR:
40	ROX	MCD_ECAP_SLICE3_CFG_ECC_CE_ERR:
41	ROX	MCD_ECAP_PRESP_RTY_OTHER:
42	ROX	MCD_ECAP_REC_SM_ERROR_ERR:
43	ROX	MCD_ECAP_REC_PB_SM_ERROR_ERR:
44	ROX	MCD_ECAP_ADDR_ERROR_PULSE:
45	ROX	MCD_ECAP_RCMD0_ADDR_PARITY_ERROR:
46	ROX	MCD_ECAP_RCMD1_ADDR_PARITY_ERROR:
47	ROX	MCD_ECAP_RCMD2_ADDR_PARITY_ERROR:
48	ROX	MCD_ECAP_RCMD3_ADDR_PARITY_ERROR:
49	ROX	MCD_ECAP_WARB_INVALID_CASE_ERROR:
50	ROX	MCD_ECAP_INVALID_CRESP_ERROR:
51	ROX	MCD_ECAP_TTAG_PARITY_ERROR:
52	ROX	MCD_ECAP_RDADDR_ARB_BAD_HAND:
53	ROX	MCD_RDWR_UPDATE_ERROR: MCD direct access register update error.
54	ROX	MCD_REC_UPDATE_ERROR: MCD direct access register update error.

Bits	SCOM	Field Mnemonic: Description
55	ROX	MCD_REC_ACK_DEAD_ERROR: MCD received an ack_dead cResp.
56:63	RO	constant = 0b00000000

Register Name	MCD Debug Configuration Register
Mnemonic	MCD0.MCD_DBG
Address	0000000003011013 (SCOM)
Description	MCD Debug Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b000
3	RW	MCD_DBG_TRACE_ENABLE:
4:7	RW	MCD_DBG_TRACE_SELECT:
8	RW	MCD_DBG_ERR_INJ_ENABLE: MCD Array error inject enable.
9	RW	MCD_DBG_ERR_INJ_TYPE: MCD Array error inject type. 0 : CE 1 : UE
10	RW	MCD_DBG_ERR_INJ_ACTION: MCD Array error inject action. 0 : single 1 : continuous
11:14	RW	MCD_DBG_ERR_INJ_ARRAY_SEL: MCD Array error inject select. 0000 - 1111.
15	RWX_WCLRPART	MCD_DBG_ERR_INJ_STATUS: MCD Array error inject status. 1: success.
16:18	RO	constant = 0b000
19	RW	MCD_DBG_PMU_ENABLE:
20:22	RW	MCD_DBG_PMU_SELECT_LOW:
23:25	RW	MCD_DBG_PMU_SELECT_HIGH:
26:31	RO	constant = 0b000000
32:47	RW	MCD_DBG_PMU_BUS_ENABLE:
48:63	RO	constant = 0b0000000000000000

Register Name	Pervasive FIR Register
Mnemonic	MCD1.MCC_FIR_REG
Address	0000000003011400 (SCOM) 0000000003011401 (SCOM1) 0000000003011402 (SCOM2)
Description	Local FIR register for MCD

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MCD_ARRAY_ECC_UE_ERR: MCD array ECC uncorrectable error.
1	RWX	WOX_AND	WOX_OR	MCD_ARRAY_ECC_CE_ERR: MCD array ECC uncorrectable error.
2	RWX	WOX_AND	WOX_OR	MCD_PB_ADDR_PARITY_ERR: MCD processor bus address Parity error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	MCD_SM_OR_CASE_ERR: MCD invalid state error.
4	RWX	WOX_AND	WOX_OR	MCD_CL_PROBE_PB_HANG_ERR: Hang poll timer expired on cl_probe.
5	RWX	WOX_AND	WOX_OR	MCD_CRESP_ADDR_ERR: Processor bus address error cresp received.
6	RWX	WOX_AND	WOX_OR	MCD_UNSOLICITED_CRESP_ERR: MCD received an unsolicited CRESP.
7	RWX	WOX_AND	WOX_OR	MCD_TTAG_PARITY_ERR: MCD processor bus ttag parity error.
8	RWX	WOX_AND	WOX_OR	MCD_FIR_REG_UPDATE_ERR: MCD SCOM register update error.
9	RWX	WOX_AND	WOX_OR	MCD_ACK_DEAD_CRESP_ERR: MCD received an ack_dead_cresp.
10	RWX	WOX_AND	WOX_OR	MCD_SCOM_ERR: PBEH CENT FIR SCOM error.
11	RWX	WOX_AND	WOX_OR	MCD_SCOM_ERR_DUP: PBEH CENT FIR SCOM error duplicate.
12:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Pervasive FIR Mask Register
Mnemonic	MCD1.MCD_FIR_MASK_REG
Address	0000000003011403 (SCOM) 0000000003011404 (SCOM1) 0000000003011405 (SCOM2)
Description	Error mask register (Action0, Action1, Mask) = Action Select (0, 1, 0) = Recoverable Error (0, 0, 0) = Checkstop Error (1, 0, 0) = Special_attention (x, x, 1) = MASKED

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MCD_ARRAY_ECC_UE_MASK: Mask MCD array ECC uncorrectable error.
1	RW	WO_AND	WO_OR	MCD_ARRAY_ECC_CE_MASK: Mask MCD array ECC uncorrectable error.
2	RW	WO_AND	WO_OR	MCD_PB_ADDR_PARITY_MASK: Mask MCD processor bus address parity error.
3	RW	WO_AND	WO_OR	MCD_SM_OR_CASE_MASK: Mask MCD invalid state error.
4	RW	WO_AND	WO_OR	MCD_CL_PROBE_PB_HANG_MASK: Mask Hang poll timer expired on cl_probe.
5	RW	WO_AND	WO_OR	MCD_CRESP_ADDR_MASK: Mask processor bus address error CRESP received.
6	RW	WO_AND	WO_OR	MCD_UNSOLICITED_CRESP_MASK: Mask MCD received an unsolicited CRESP.
7	RW	WO_AND	WO_OR	MCD_TTAG_PARITY_MASK: Mask MCD processor bus TTAG parity error.
8	RW	WO_AND	WO_OR	MCD_FIR_REG_UPDATE_ERR_MASK: Mask MCD SCOM register update error.
9	RW	WO_AND	WO_OR	MCD_ACK_DEAD_CRESP_MASK: Mask MCD SCOM register update error.
10	RW	WO_AND	WO_OR	MCD_SCOM_ERR_MASK: PBEH CENT FIR_SCOM error mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
11	RW	WO_AND	WO_OR	MCD_SCOM_ERR_MASK_DUP: PBEH CENT FIR_SCOM error mask duplicate.
12:63	RO	RO	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Pervasive FIR Action 0 Register
Mnemonic	MCD1.MCD_FIR_ACTION0_REG
Address	0000000003011406 (SCOM)
Description	Action Select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:11	RW	FIR_ACTION0: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action select. (0, 1, 0) = Recoverable error. (0, 0, 0) = Checkstop error. (1, 0, 0) = Special attention. (x, x, 1) = Masked.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Pervasive FIR Action 1 Register
Mnemonic	MCD1.MCD_FIR_ACTION1_REG
Address	0000000003011407 (SCOM)
Description	Action Select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:11	RW	FIR_ACTION1: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action select. (0, 1, 0) = Recoverable error. (0, 0, 0) = Checkstop error. (1, 0, 0) = Special attention. (x, x, 1) = Masked.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	MCD TOP (mcd_cn0) Configuration Register
Mnemonic	MCD1.BANK0_MCD_TOP
Address	000000000301140A (SCOM)
Description	MCD TOP (mcd_cn0) Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	BANK0_MCD_TOP_VALID: MCD_TOP valid.
1	RW	BANK0_MCD_TOP_CPG: MCD_TOP group address with other bank.
2	RW	BANK0_MCD_TOP_GRP_MBR_ID: MCD_TOP group member identification.
3	RW	BANK0_MCD_TOP_ALWAYS_RTY: MCD_TOP disable array array access and force rty_dinc response.

Bits	SCOM	Field Mnemonic: Description
4:12	RO	constant = 0b000000000
13:29	RW	BANK0_MCD_TOP_GRP_SIZE: MCD_TOP group size.
30:32	RO	constant = 0b000
33:63	RW	BANK0_MCD_TOP_GRP_BASE: MCD_TOP base address.

Register Name	MCD STR (mcd_cn1) Configuration Register
Mnemonic	MCD1.BANK0_MCD_STR
Address	000000000301140B (SCOM)
Description	MCD STR (mcd_cn1) Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	BANK0_MCD_STR_VALID: MCD_str valid.
1	RW	BANK0_MCD_STR_CPG: MCD_str group address with other bank.
2	RW	BANK0_MCD_STR_GRP_MBR_ID: MCD_str group member identification.
3	RW	BANK0_MCD_STR_ALWAYS_RTY: MCD_str disable array array access and force rty_dinc response.
4:12	RO	constant = 0b000000000
13:29	RW	BANK0_MCD_STR_GRP_SIZE: MCD_str group size.
30:32	RO	constant = 0b000
33:63	RW	BANK0_MCD_STR_GRP_BASE: MCD_str base address.

Register Name	MCD bot (mcd_cn2) Configuration Register
Mnemonic	MCD1.BANK0_MCD_BOT
Address	000000000301140C (SCOM)
Description	MCD bot (mcd_cn2) Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	BANK0_MCD_BOT_VALID: MCD_bot valid.
1	RW	BANK0_MCD_BOT_CPG: MCD_bot group address with other bank.
2	RW	BANK0_MCD_BOT_GRP_MBR_ID: MCD_bot group member identification.
3	RW	BANK0_MCD_BOT_ALWAYS_RTY: MCD_bot disable array array access and force rty_dinc response.
4:12	RO	constant = 0b000000000
13:29	RW	BANK0_MCD_BOT_GRP_SIZE: MCD_bot group size.
30:32	RO	constant = 0b000
33:63	RW	BANK0_MCD_BOT_GRP_BASE: MCD_bot base address.

Register Name	MCD cha (mcd_cn3) Configuration Register
Mnemonic	MCD1.BANK0_MCD_CHA
Address	000000000301140D (SCOM)
Description	MCD cha (mcd_cn3) Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	BANK0_MCD_CHA_VALID: MCD_cha valid.
1	RW	BANK0_MCD_CHA_CPG: MCD_cha group address with other bank.
2	RW	BANK0_MCD_CHA_GRP_MBR_ID: MCD_cha group member identification.
3	RW	BANK0_MCD_CHA_ALWAYS_RTY: MCD_cha disable array array access and force rty_dinc response.
4:12	RO	constant = 0b000000000
13:29	RW	BANK0_MCD_CHA_GRP_SIZE: MCD_cha group size.
30:32	RO	constant = 0b000
33:63	RW	BANK0_MCD_CHA_GRP_BASE: MCD_cha base address.

Register Name	MCD Command Decode Configuration Register
Mnemonic	MCD1.BANK0_MCD_CMD
Address	000000000301140E (SCOM)
Description	MCD command decode Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:18	RW	BANK0_MCD_CHECK_CMDS: Check commands.
19:30	RO	constant = 0b000000000000
31	RW	BANK0_MCD_CHECK_CMDS_EN: Enable override of check commands.
32:50	RW	BANK0_MCD_SET_CMDS: Set commands.
51:62	RO	constant = 0b000000000000
63	RW	BANK0_MCD_SET_CMDS_EN: Enable override of set commands.

Register Name	MCD Direct Read Write Register
Mnemonic	MCD1.BANK0_MCD_RW
Address	000000000301140F (SCOM)
Description	MCD direct read write Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	BANK0_MCD_RDWR_ACCESS_EN: MCD direct read/write access enable.
1	RW	BANK0_MCD_RDWR_WR_ENABLE: MCD direct write enable. Reads when off.
2	RO	constant = 0b0
3	ROX	BANK0_MCD_RDWR_REQ_PEND: MCD direct read/write access pending.
4	ROX	BANK0_MCD_RDWR_READ_STATUS: MCD direct read data is valid.

Bits	SCOM	Field Mnemonic: Description
5	RW	BANK0_MCD_RDWR_WRITE_MODE: MCD write mode. 0 = OR 1 = and
6	ROX	BANK0_MCD_RDWR_WRITE_STATUS: MCD direct write has completed.
7:16	RO	constant = 0b0000000000
17:31	RW	BANK0_MCD_RDWR_ADDR: MCD direct access address.
32:63	RWX	BANK0_MCD_RDWR_RDWR_DATA: MCD read/write data based on the wr_enable setting.

Register Name	MCD Recovery Control Register
Mnemonic	MCD1.BANK0_MCD_REC
Address	0000000003011410 (SCOM)
Description	MCD recovery control Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	BANK0_MCD_REC_ENABLE: MCD recovery access enable.
1	ROX	BANK0_MCD_REC_DONE: MCD recovery done.
2	RW	BANK0_MCD_REC_CONTINUOUS: MCD recovery continuous setting.
3:4	RO	constant = 0b00
5	ROX	BANK0_MCD_REC_STATUS: MCD recovery status. 0 = idle 1 = running
6:7	RO	constant = 0b00
8:19	RW	BANK0_MCD_REC_PACE: MCD recovery pace between new cache lines.
20	ROX	BANK0_MCD_REC_ADDR_ERROR: MCD recovery has received an address error CRESP.
21:35	RW	BANK0_MCD_REC_ADDR: MCD recovery start address.
36:39	RO	constant = 0b0000
40:43	RW	BANK0_MCD_REC_RTY_COUNT: MCD recovery retries before failure.
44:48	RO	constant = 0b00000
49:63	RW	BANK0_MCD_REC_VG_COUNT: MCD recovery vector groups to recovery.

Register Name	MCD Vector Group Configuration Register
Mnemonic	MCD1.BANK0_MCD_VGC
Address	0000000003011411 (SCOM)
Description	MCD vector group Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	BANK0_MCD_AVAIL_GROUPS: Available groups for ECC.
16:31	RO	constant = 0b0000000000000000
32	RW	BANK0_MCD_4X4_MODE: Enable Brazos 4x4.
33	RW	BANK0_MCD_HANG_POLL_ENABLE: Enable hang_poll.
34	RW	BANK0_MCD_RND_BACKOFF_ENABLE: Enable rnd_backoff.

Bits	SCOM	Field Mnemonic: Description
35	RW	BANK0_MCD_DROP_PRIORITY_MODE: Reduce drop_priority. 0 = high 1 = low
36	RW	BANK0_MCD_MASK_AGV_DISABLE_MODE: Reduce mask_agv_disable. 0 = mask 1 = not mask
37	RW	BANK0_MCD_XLATE_TO_ADDR_ID_ENABLE: Reduce mask_agv_disable. 0 = mask 1 = not mask
38:63	RO	constant = 0b00000000000000000000000000

Register Name	MCD ECC Error Capture Register
Mnemonic	MCD1.MCD_ECAP
Address	0000000003011412 (SCOM)
Description	MCD ECC Error Capture Register

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	MCD_ECAP_ECC_CLEAR: Write of 1 clears ECC capture data.
1	RO	constant = 0b0
2	ROX	MCD_ECAP_ECC_UE: ECC capture data is for an uncorrectable error.
3	ROX	MCD_ECAP_ECC_CE: ECC capture data is for a correctable error.
4:7	ROX	MCD_ECAP_ECC_ERROR_COUNT: Number of ECC errors detected. Clamps to 0xF.
8:9	RO	constant = 0b00
10:23	ROX	MCD_ECAP_ECC_ERROR_ADDR: Line (0 - 9) and array(10 - 13) of last captured ECC error.
24:31	ROX	MCD_ECAP_ECC_SYNDROME: Syndrome of last captured ECC error.
32	RO	constant = 0b0
33	ROX	MCD_ECAP_SLICE0_CFG_ECC_UE_ERR:
34	ROX	MCD_ECAP_SLICE0_CFG_ECC_CE_ERR:
35	ROX	MCD_ECAP_SLICE1_CFG_ECC_UE_ERR:
36	ROX	MCD_ECAP_SLICE1_CFG_ECC_CE_ERR:
37	ROX	MCD_ECAP_SLICE2_CFG_ECC_UE_ERR:
38	ROX	MCD_ECAP_SLICE2_CFG_ECC_CE_ERR:
39	ROX	MCD_ECAP_SLICE3_CFG_ECC_UE_ERR:
40	ROX	MCD_ECAP_SLICE3_CFG_ECC_CE_ERR:
41	ROX	MCD_ECAP_PRESP_RTY_OTHER:
42	ROX	MCD_ECAP_REC_SM_ERROR_ERR:
43	ROX	MCD_ECAP_REC_PB_SM_ERROR_ERR:
44	ROX	MCD_ECAP_ADDR_ERROR_PULSE:
45	ROX	MCD_ECAP_RCMD0_ADDR_PARITY_ERROR:
46	ROX	MCD_ECAP_RCMD1_ADDR_PARITY_ERROR:
47	ROX	MCD_ECAP_RCMD2_ADDR_PARITY_ERROR:

Bits	SCOM	Field Mnemonic: Description
48	ROX	MCD_ECAP_RCMD3_ADDR_PARITY_ERROR:
49	ROX	MCD_ECAP_WARB_INVALID_CASE_ERROR:
50	ROX	MCD_ECAP_INVALID_CRESP_ERROR:
51	ROX	MCD_ECAP_TTAG_PARITY_ERROR:
52	ROX	MCD_ECAP_RDADDR_ARB_BAD_HAND:
53	ROX	MCD_RDWR_UPDATE_ERROR: MCD direct access register update error.
54	ROX	MCD_REC_UPDATE_ERROR: MCD direct access register update error.
55	ROX	MCD_REC_ACK_DEAD_ERROR: MCD received an ack_dead cResp.
56:63	RO	constant = 0b00000000

Register Name	MCD Debug Configuration Register
Mnemonic	MCD1.MCD_DBG
Address	0000000003011413 (SCOM)
Description	MCD Debug Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b000
3	RW	MCD_DBG_TRACE_ENABLE:
4:7	RW	MCD_DBG_TRACE_SELECT:
8	RW	MCD_DBG_ERR_INJ_ENABLE: MCD Array error inject enable.
9	RW	MCD_DBG_ERR_INJ_TYPE: MCD Array error inject type. 0 : CE 1 : UE
10	RW	MCD_DBG_ERR_INJ_ACTION: MCD Array error inject action. 0 : single 1 : continuous
11:14	RW	MCD_DBG_ERR_INJ_ARRAY_SEL: MCD Array error inject select. 0000 - 1111.
15	RWX_WCLRPART	MCD_DBG_ERR_INJ_STATUS: MCD Array error inject status. 1: success.
16:18	RO	constant = 0b000
19	RW	MCD_DBG_PMU_ENABLE:
20:22	RW	MCD_DBG_PMU_SELECT_LOW:
23:25	RW	MCD_DBG_PMU_SELECT_HIGH:
26:31	RO	constant = 0b000000
32:47	RW	MCD_DBG_PMU_BUS_ENABLE:
48:63	RO	constant = 0b0000000000000000

Register Name	VAS Unit FIR Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_FIR_REG
Address	0000000003011800 (SCOM) 0000000003011801 (SCOM1) 0000000003011802 (SCOM2)
Description	Local FIR register for the VAS unit logic

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	EG_LOGIC_HW_ERROR: Hardware error detected in egress logic.
1	RWX	WOX_AND	WOX_OR	IN_LOGIC_HW_ERROR: Hardware error detected in ingress logic.
2	RWX	WOX_AND	WOX_OR	CQ_LOGIC_HW_ERROR: Hardware error detected in CQ logic.
3	RWX	WOX_AND	WOX_OR	WC_LOGIC_HW_ERROR: Hardware error detected in WC logic.
4	RWX	WOX_AND	WOX_OR	RG_LOGIC_HW_ERROR: Hardware error detected in RG logic.
5	RWX	WOX_AND	WOX_OR	CQ_PB_PARITY_ERROR: processor bus parity error detected on CQ logic interface.
6	RWX	WOX_AND	WOX_OR	CQ_PB_RD_ADDR_ERROR: CQ logic detected processor bus address error on CRESP from a read operation.
7	RWX	WOX_AND	WOX_OR	CQ_PB_WR_ADDR_ERROR: CQ logic detected processor bus address error on CRESP from a write operation.
8	RWX	WOX_AND	WOX_OR	EG_ECC_CE_ERROR: Correctable ECC error detected in egress logic.
9	RWX	WOX_AND	WOX_OR	IN_ECC_CE_ERROR: Correctable ECC error detected in ingress logic.
10	RWX	WOX_AND	WOX_OR	CQ_ECC_CE_ERROR: Correctable ECC error detected in CQ logic.
11	RWX	WOX_AND	WOX_OR	WC_ECC_CE_ERROR: Correctable ECC error detected in WC logic.
12	RWX	WOX_AND	WOX_OR	RG_ECC_CE_ERROR: Correctable ECC error detected in RG logic.
13	RWX	WOX_AND	WOX_OR	CQ_PB_OB_CE_ERROR: ECC Correctable Error detected on CQ outbound processor bus interface.
14	RWX	WOX_AND	WOX_OR	CQ_PB_OB_UE_ERROR: ECC uncorrectable Error detected on CQ outbound processor bus interface.
15	RWX	WOX_AND	WOX_OR	CQ_PB_MASTER_FSM_HANG: processor bus state machine hang detected in CQ logic.
16	RWX	WOX_AND	WOX_OR	EG_ECC_UE_ERROR: Uncorrectable ECC error detected in egress logic.
17	RWX	WOX_AND	WOX_OR	IN_ECC_UE_ERROR: Uncorrectable ECC error detected in ingress logic.
18	RWX	WOX_AND	WOX_OR	CQ_ECC_UE_ERROR: Uncorrectable ECC error detected in CQ logic.
19	RWX	WOX_AND	WOX_OR	WC_ECC_UE_ERROR: Uncorrectable ECC error detected in WC logic.
20	RWX	WOX_AND	WOX_OR	RG_ECC_UE_ERROR: Uncorrectable ECC error detected in RG logic.
21	RWX	WOX_AND	WOX_OR	IN_PARITY_ERROR: Parity error detected in Ingress logic.
22	RWX	WOX_AND	WOX_OR	IN_SW_CAST_ERROR: Software cast error detected in Ingress logic.
23	RWX	WOX_AND	WOX_OR	Reserved field.
24	RWX	WOX_AND	WOX_OR	EG_ECC_SUE_ERROR: ECC sue error detected in egress logic.
25	RWX	WOX_AND	WOX_OR	IN_ECC_SUE_ERROR: ECC sue error detected in ingress logic.
26	RWX	WOX_AND	WOX_OR	CQ_ECC_SUE_ERROR: ECC sue error detected in CQ logic.
27	RWX	WOX_AND	WOX_OR	WC_ECC_SUE_ERROR: ECC sue error detected in WC logic.
28	RWX	WOX_AND	WOX_OR	RG_ECC_SUE_ERROR: ECC sue error detected in RG logic.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
29	RWX	WOX_AND	WOX_OR	CQ_PB_RD_LINK_ERROR: processor bus link error detected on read operation in CQ logic.
30	RWX	WOX_AND	WOX_OR	CQ_PB_WR_LINK_ERROR: processor bus link error detected on write operation in CQ logic.
31	RWX	WOX_AND	WOX_OR	CQ_PB_LINK_ABORT: processor bus link abort operation received in CQ logic.
32	RWX	WOX_AND	WOX_OR	MMIO_HYP_RD_ADDR_ERR: Address error detected on hypervisor MMIO read.
33	RWX	WOX_AND	WOX_OR	MMIO_OS_RD_ADDR_ERR: Address error detected on OS MMIO read.
34	RWX	WOX_AND	WOX_OR	MMIO_HYP_WR_ADDR_ERR: Address error detected on hypervisor MMIO write.
35	RWX	WOX_AND	WOX_OR	MMIO_OS_WR_ADDR_ERR: Address error detected on OS MMIO write.
36	RWX	WOX_AND	WOX_OR	MMIO_NON8B_HYP_ERR: non-8-Byte MMIO detected by hypervisor.
37	RWX	WOX_AND	WOX_OR	MMIO_NON8B_OS_ERR: non-8-Byte MMIO detected by user or OS.
38	RWX	WOX_AND	WOX_OR	WM_WIN_NOT_OPEN_ERR: Write monitor operation attempted on a window that is not open.
39	RWX	WOX_AND	WOX_OR	WM_MULTIHIT_ERR: Multiple write monitor registers match the same snooped PB operation.
40	RWX	WOX_AND	WOX_OR	PG_MIG_DISABLED_ERR: Page Migration Register is not valid.
41	RWX	WOX_AND	WOX_OR	PG_MIG_SIZE_MISMATCH_ERR: Page Migration Register size does not match corresponding FIFO.
42	RWX	WOX_AND	WOX_OR	NOTIFY_FAILED_ERR: ASB_Notify sent but not claimed and interrupts were disabled in window context.
43	RWX	WOX_AND	WOX_OR	WR_MON_NOT_DISABLED_ERR: Write monitor operation hit a window which has notification disabled.
44	RWX	WOX_AND	WOX_OR	VAS_REJECTED_PASTE_CMD: VAS rejected a PB paste command. See window status register for details.
45	RWX	WOX_AND	WOX_OR	DATA_HANG_DETECTED: VAS hung waiting for data from processor bus.
46	RWX	WOX_AND	WOX_OR	INCOMING_PB_PARITY_ERR: Incoming processor bus parity error.
47	RWX	WOX_AND	WOX_OR	SCOM1_SAT_ERR: HW error from SCOM Satellite 1.
48	RWX	WOX_AND	WOX_OR	NX_LOCAL_XSTOP: NX local checkstop.
49	RWX	WOX_AND	WOX_OR	SCOM_MMIO_ADDR_ERR: SCOM MMIO address offset error. SCOM-initiated MMIO address did not decode to valid address.
50	RWX	WOX_AND	WOX_OR	UNUSED50: Unused bit.
51	RWX	WOX_AND	WOX_OR	UNUSED51: Unused bit.
52	RWX	WOX_AND	WOX_OR	SCOMFIR_INT_ERR_0: FIR/SCOM satellite parity error.
53	RWX	WOX_AND	WOX_OR	SCOMFIR_INT_ERR_1: FIR/SCOM satellite parity error duplicate.
54:63	RO	RO	RO	constant = 0b0000000000

Register Name	**VAS FIR Mask Register**
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_FIR_MASK_REG
Address	0000000003011803 (SCOM) 0000000003011804 (SCOM1) 0000000003011805 (SCOM2)
Description	Error mask register (Action0, Action1, Mask) = Action select (0, 0, 0) = System checkstop error (0, 1, 0) = Recoverable error (1, 0, 0) = Not used (1, 1, 0) = Local checkstop error (x, x, 1) = Masked

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	EG_LOGIC_HW_ERROR_MASK: Mask for hardware error detected in egress logic.
1	RW	WO_AND	WO_OR	IN_LOGIC_HW_ERROR_MASK: Mask for hardware error detected in ingress logic.
2	RW	WO_AND	WO_OR	CQ_LOGIC_HW_ERROR_MASK: Mask for hardware error detected in CQ logic.
3	RW	WO_AND	WO_OR	WC_LOGIC_HW_ERROR_MASK: Mask for hardware error detected in WC logic.
4	RW	WO_AND	WO_OR	RG_LOGIC_HW_ERROR_MASK: Mask for hardware error detected in RG logic.
5	RW	WO_AND	WO_OR	CQ_PB_PARITY_ERROR_MASK: Mask for processor bus parity error detected on CQ logic interface.
6	RW	WO_AND	WO_OR	CQ_PB_RD_ADDR_ERROR_MASK: Mask for processor bus address error detected by CQ logic on CRESP from a read operation.
7	RW	WO_AND	WO_OR	CQ_PB_WR_ADDR_ERROR_MASK: Mask for processor bus address error detected by CQ logic on CRESP from a write operation.
8	RW	WO_AND	WO_OR	EG_ECC_CE_ERROR_MASK: Mask for correctable ECC error detected in Egress logic.
9	RW	WO_AND	WO_OR	IN_ECC_CE_ERROR_MASK: Mask for correctable ECC error detected in Ingress logic.
10	RW	WO_AND	WO_OR	CQ_ECC_CE_ERROR_MASK: Mask for correctable ECC error detected in CQ logic.
11	RW	WO_AND	WO_OR	WC_ECC_CE_ERROR_MASK: Mask for correctable ECC error detected in WC logic.
12	RW	WO_AND	WO_OR	RG_ECC_CE_ERROR_MASK: Mask for correctable ECC error detected in RG logic.
13	RW	WO_AND	WO_OR	CQ_PB_OB_CE_ERROR_MASK: Mask for ECC correctable error detected on CQ outbound processor bus interface.
14	RW	WO_AND	WO_OR	CQ_PB_OB_UE_ERROR_MASK: Mask for ECC uncorrectable Error detected on CQ outbound processor bus interface.
15	RW	WO_AND	WO_OR	CQ_PB_MASTER_FSM_HANG_MASK: Mask for processor bus state machine hang detected in CQ logic.
16	RW	WO_AND	WO_OR	EG_ECC_UE_ERROR_MASK: Mask for uncorrectable ECC error detected in egress logic.
17	RW	WO_AND	WO_OR	IN_ECC_UE_ERROR_MASK: Mask for uncorrectable ECC error detected in ingress logic.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RW	WO_AND	WO_OR	CQ_ECC_UE_ERROR_MASK: Mask for uncorrectable ECC error detected in CQ logic.
19	RW	WO_AND	WO_OR	WC_ECC_UE_ERROR_MASK: Mask for uncorrectable ECC error detected in WC logic.
20	RW	WO_AND	WO_OR	RG_ECC_UE_ERROR_MASK: Mask for uncorrectable ECC error detected in RG logic.
21	RW	WO_AND	WO_OR	IN_PARITY_ERROR_MASK: Mask for parity error detected in Ingress logic.
22	RW	WO_AND	WO_OR	IN_SW_CAST_ERROR_MASK: Mask for software cast error detected in Ingress logic.
23	RW	WO_AND	WO_OR	Reserved field.
24	RW	WO_AND	WO_OR	EG_ECC_SUE_ERROR_MASK: Mask for ECC sue error detected in Egress logic.
25	RW	WO_AND	WO_OR	IN_ECC_SUE_ERROR_MASK: Mask for ECC sue error detected in Ingress logic.
26	RW	WO_AND	WO_OR	CQ_ECC_SUE_ERROR_MASK: Mask for ECC sue error detected in CQ logic.
27	RW	WO_AND	WO_OR	WC_ECC_SUE_ERROR_MASK: Mask for ECC sue error detected in WC logic.
28	RW	WO_AND	WO_OR	RG_ECC_SUE_ERROR_MASK: Mask for ECC sue error detected in RG logic.
29	RW	WO_AND	WO_OR	CQ_PB_RD_LINK_ERROR_MASK: Mask for processor bus link error detected on read operation in CQ logic.
30	RW	WO_AND	WO_OR	CQ_PB_WR_LINK_ERROR_MASK: Mask for processor bus link error detected on write operation in CQ logic.
31	RW	WO_AND	WO_OR	CQ_PB_LINK_ABORT_MASK: Mask for processor bus link abort operation received in CQ logic.
32	RW	WO_AND	WO_OR	MMIO_HYP_RD_ADDR_ERR_MASK: Mask for address error detected on hypervisor MMIO read.
33	RW	WO_AND	WO_OR	MMIO_OS_RD_ADDR_ERR_MASK: Mask for address error detected on OS MMIO read.
34	RW	WO_AND	WO_OR	MMIO_HYP_WR_ADDR_ERR_MASK: Mask for address error detected on hypervisor MMIO write.
35	RW	WO_AND	WO_OR	MMIO_OS_WR_ADDR_ERR_MASK: Mask for address error detected on OS MMIO write.
36	RW	WO_AND	WO_OR	MMIO_NON8B_HYP_ERR_MASK: Mask for non-8-Byte MMIO detected by hypervisor.
37	RW	WO_AND	WO_OR	MMIO_NON8B_OS_ERR_MASK: Mask for non-8-Byte MMIO detected by user or OS.
38	RW	WO_AND	WO_OR	WM_WIN_NOT_OPEN_ERR_MASK: Mask for write monitor operation attempted on a window that is not open.
39	RW	WO_AND	WO_OR	WM_MULTIHIT_ERR_MASK: Mask for multiple write monitor registers which match the same snooped PB operation.
40	RW	WO_AND	WO_OR	PG_MIG_DISABLED_ERR_MASK: Mask for Page Migration Register which is not valid.
41	RW	WO_AND	WO_OR	PG_MIG_SIZE_MISMATCH_ERR_MASK: Mask for Page Migration Register whose size does not match corresponding FIFO.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
42	RW	WO_AND	WO_OR	NOTIFY_FAILED_ERR_MASK: Mask for ASB_Notify sent but not claimed and interrupts were disabled in window context.
43	RW	WO_AND	WO_OR	WR_MON_NOT_DISABLED_ERR_MASK: Mask for write monitor operation hit a window which has notification disabled.
44	RW	WO_AND	WO_OR	VAS_REJECTED_PASTE_CMD_MASK: Mask for VAS rejecting a PB paste command.
45	RW	WO_AND	WO_OR	DATA_HANG_DETECTED_MASK: Mask for VAS hang waiting for data from processor bus.
46	RW	WO_AND	WO_OR	INCOMING_PB_PARITY_ERR_MASK: Mask for incoming processor bus parity error.
47	RW	WO_AND	WO_OR	SCOM1_SAT_ERR_MASK: Mask for HW error from SCOM Satellite 1.
48	RW	WO_AND	WO_OR	NX_LOCAL_XSTOP_MASK: Mask for NX Local Checkstop.
49	RW	WO_AND	WO_OR	SCOM_MMIO_ADDR_ERR_MASK: Mask for SCOM MMIO address offset error.
50	RW	WO_AND	WO_OR	UNUSED50_MASK: Unused bit.
51	RW	WO_AND	WO_OR	UNUSED51_MASK: Unused bit.
52	RW	WO_AND	WO_OR	SCOMFIR_INT_ERR_0_MASK: Mask for FIR/SCOM satellite parity error.
53	RW	WO_AND	WO_OR	SCOMFIR_INT_ERR_1_MASK: Mask for FIR/SCOM satellite parity error duplicate.
54:63	RO	RO	RO	constant = 0b0000000000

Register Name	VAS FIR Action 0 Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_FIR_ACTION0_REG
Address	0000000003011806 (SCOM)
Description	Action Select 0 for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:53	RW	VAS_FIR_ACTION0: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action select (0, 0, 0) = System checkstop error (0, 1, 0) = Recoverable error (1, 0, 0) = Not used (1, 1, 0) = Local checkstop error (x, x, 1) = Masked
54:63	RO	constant = 0b0000000000

Register Name	VAS FIR Action 1 Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_FIR_ACTION1_REG
Address	0000000003011807 (SCOM)
Description	Action Select 1 for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:53	RW	VAS_FIR_ACTION1: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action select (0, 0, 0) = System checkstop error (0, 1, 0) = Recoverable error (1, 0, 0) = Not used (1, 1, 0) = Local checkstop error (x, x, 1) = Masked
54:63	RO	constant = 0b0000000000

Register Name	VAS FIR WOF Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_FIR_WOF_REG
Address	0000000003011808 (SCOM)
Description	The “Who's on first” (WOF) register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:53	RWX_WCLRREG	VAS_FIR_WOF: WOF Register locks on first error.
54:63	RO	constant = 0b0000000000

Register Name	Window Context MMIO Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WCMBAR
Address	000000000301180A (SCOM)
Description	Window Context MMIO Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:38	RW	WCMBAR_BASE_ADDR: Base address for the start of the MMIOable registers.
39:63	RO	constant = 0b00000000000000000000000000

Register Name	OS/User Window Context MMIO Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_UWMBAR
Address	000000000301180B (SCOM)
Description	OS/User Window Context MMIO Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:35	RW	UWMBAR_BASE_ADDR: Base address for the start of the OS/user MMIOable registers.
36:63	RO	constant = 0b0000000000000000000000000000

Register Name	Buffer Control Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_BUFCTL
Address	000000000301180C (SCOM)
Description	Buffer Control Register

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	TOTAL_FREE_BUF_COUNT: Total number of buffers in the free pool.
56	RO	constant = 0b0
57:63	ROX	CONSUMED_BUF_COUNT: Number of free pool buffers that VAS is actively using.

Register Name	Miscellaneous Status and North Control Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_MISCCTL
Address	000000000301180D (SCOM)
Description	Miscellaneous Status and North Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MISC_CTL_4VS64: 4 K vs 64 K striding of window ID bits in paste commands.
1	RW	MISC_CTL_ACCEPT_PASTE: When this bit is asserted, VAS snoops for and accepts paste commands.
2	RW	MISC_CTL_ENABLE_WRMON: Assert this bit to enable the write monitoring function in VAS.
3	RW	MISC_CTL_DISABLE_PUSH2MEM_LIMIT: Disable the push-to-memory credit limit (default limit is one push-to-mem operation at a time).
4	RW	MISC_CTL_QUIESCE_REQUEST: Quiesce requested. VAS logic stops accepting work and quiesces when in-progress work is done.
5	RW	MISC_CTL_PREFETCH_DISABLE: Prefetch disable switch. Tells ingress logic to turn off RCV window prefetching for SND window requests.
6:7	RW	MISC_CTL_UNUSED_BITS: Unused bits.
8:46	RO	constant = 0b00000000000000000000000000000000000000000000
47	WOX	MISC_CTL_INVALIDATE_CAM_LOC: Assert this bit to invalidate the CAM location specified in bits 49:55. Hardware clears this bit.
48	RW	MISC_CTL_INVALIDATE_CAM_ALL: Assert this bit to invalidate the entire CAM. All entries are forced back to memory and marked invalid.
49:55	RW	MISC_CTL_CAM_LOCATION: This location in the CAM is invalidated when bit 47 is asserted.
56	ROX	MISC_CTL_CAM_INVAL_DONE: CAM invalidate done Bit: This bit is asserted when a CAM invalidate operation is completed.
57	RW	MISC_CTL_UNUSED_BITS2: Unused bit.
58	ROX	MISC_CTL_HMI_ACTIVE: HMI Active Bit: This bit indicates that VAS experienced a local checkstop and set the HMI FIR.
59	ROX	MISC_CTL_RG_IS_IDLE: When this bit is asserted ,VAS RG logic is currently idle.
60:63	RO	constant = 0b0000

Register Name	Remote Memory Access Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_RMABAR
Address	000000000301180E (SCOM)
Description	Remote Memory Access Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:51	RW	RMA_BAR: Remote memory access base address register.
52:63	RO	constant = 0b000000000000

Register Name	Remote Memory Access Base Address Mask Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_RMABARM
Address	000000000301180F (SCOM)
Description	Remote Memory Access Base Address Mask Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:51	RW	RMA_BAR_MASK: Remote memory access base address mask register.
52:63	RO	constant = 0b000000000000

Register Name	Write Monitor 0 Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON0BAR
Address	0000000003011810 (SCOM)
Description	Write Monitor 0 Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	RW	WRMON_BAR0_BA: Write monitor 0 base address register.
57:59	RO	constant = 0b000
60:63	RW	WRMON_BAR0_SIZE: Write monitor 0 base address size compare.

Register Name	Write Monitor 1 Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON1BAR
Address	0000000003011811 (SCOM)
Description	Write Monitor 1 Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	RW	WRMON_BAR1_BA: Write monitor 1 base address register.
57:59	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
60:63	RW	WRMON_BAR1_SIZE: Write monitor 1 base address size compare.

Register Name	Write Monitor 2 Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON2BAR
Address	0000000003011812 (SCOM)
Description	Write Monitor 2 Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	RW	WRMON_BAR2_BA: Write monitor 2 base address register.
57:59	RO	constant = 0b000
60:63	RW	WRMON_BAR2_SIZE: Write monitor 2 base address size compare.

Register Name	Write Monitor 3 Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON3BAR
Address	0000000003011813 (SCOM)
Description	Write Monitor 3 Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	RW	WRMON_BAR3_BA: Write monitor 3 base address register.
57:59	RO	constant = 0b000
60:63	RW	WRMON_BAR3_SIZE: Write monitor 3 base address size compare.

Register Name	Write Monitor 4 Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON4BAR
Address	0000000003011814 (SCOM)
Description	Write Monitor 4 Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	RW	WRMON_BAR4_BA: Write monitor 4 base address register.
57:59	RO	constant = 0b000
60:63	RW	WRMON_BAR4_SIZE: Write monitor 4 base address size compare.

Register Name	Write Monitor 5 Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON5BAR
Address	0000000003011815 (SCOM)
Description	Write Monitor 5 Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	RW	WRMON_BAR5_BA: Write monitor 5 base address register.
57:59	RO	constant = 0b000
60:63	RW	WRMON_BAR5_SIZE: Write monitor 5 base address size compare.

Register Name	Write Monitor 6 Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON6BAR
Address	0000000003011816 (SCOM)
Description	Write Monitor 6 Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	RW	WRMON_BAR6_BA: Write monitor 6 base address register.
57:59	RO	constant = 0b000
60:63	RW	WRMON_BAR6_SIZE: Write monitor 6 base address size compare.

Register Name	Write Monitor 7 Base Address Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON7BAR
Address	0000000003011817 (SCOM)
Description	Write Monitor 7 Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	RW	WRMON_BAR7_BA: Write monitor 7 base address register.
57:59	RO	constant = 0b000
60:63	RW	WRMON_BAR7_SIZE: Write monitor 7 base address size compare.

Register Name	Write Monitor 0 Window ID Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON0WID
Address	0000000003011818 (SCOM)
Description	Write Monitor 0 Window ID Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRMON_WID0: Write monitor 0 receive window ID.

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Write Monitor 1 Window ID Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON1WID
Address	0000000003011819 (SCOM)
Description	Write Monitor 1 Window ID Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRMON_WID1: Write monitor 1 receive window ID.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Write Monitor 2 Window ID Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON2WID
Address	000000000301181A (SCOM)
Description	Write Monitor 2 Window ID Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRMON_WID2: Write monitor 2 receive window ID.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Write Monitor 3 Window ID Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON3WID
Address	000000000301181B (SCOM)
Description	Write Monitor 3 Window ID Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRMON_WID3: Write monitor 3 receive window ID.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Write Monitor 4 Window ID Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON4WID
Address	000000000301181C (SCOM)
Description	Write Monitor 4 Window ID Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRMON_WID4: Write monitor 4 receive window ID.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Write Monitor 5 Window ID Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON5WID
Address	000000000301181D (SCOM)
Description	Write Monitor 5 Window ID Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRMON_WID5: Write monitor 5 receive window ID.
16:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Write Monitor 6 Window ID Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON6WID
Address	000000000301181E (SCOM)
Description	Write Monitor 6 Window ID Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRMON_WID6: Write monitor 6 receive window ID.
16:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Write Monitor 7 Window ID Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON7WID
Address	000000000301181F (SCOM)
Description	Write Monitor 7 Window ID Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRMON_WID7: Write monitor 7 receive window ID.
16:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Write Monitor 0 TType Compare Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON0CMP
Address	0000000003011820 (SCOM)
Description	Write Monitor 0 TType Compare Register

Bits	SCOM	Field Mnemonic: Description
0	RW	WRMON_CMP0_VAL: Write monitor 0. 0: Valid/Enable
1:6	RW	WRMON_CMP0_TTYPEDIS: Write monitor 0. 0: TType disable bits
7	RW	WRMON_CMP0_UNUSED: Unused bit.
8	RW	WRMON_CMP0_ENADTTYPE: Write monitor 0. 0: Enable additional TType to monitor
9:15	RW	WRMON_CMP0_TTYPE: Write monitor 0. 0: TType

Bits	SCOM	Field Mnemonic: Description
16:23	RW	WRMON_CMP0_TSIZE: Write monitor 0. 0: TSize
24:30	RW	WRMON_CMP0_TTYPEMSK: Write monitor 0. 0: TType mask
31:38	RW	WRMON_CMP0_TSIZEMSK: Write monitor 0. 0: TSize mask
39:63	RO	constant = 0b00000000000000000000000000

Register Name	Write Monitor 1 TType Compare Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON1CMP
Address	0000000003011821 (SCOM)
Description	Write Monitor 1 TType Compare Register

Bits	SCOM	Field Mnemonic: Description
0	RW	WRMON_CMP1_VAL: Write monitor. 0: Valid/Enable
1:6	RW	WRMON_CMP1_TTYPEDIS: Write monitor 1. 0: TType disable bits
7	RW	WRMON_CMP1_UNUSED: Unused bit 1.
8	RW	WRMON_CMP1_ENADTTYPE: Write monitor 1. 0: Enable additional TType to monitor
9:15	RW	WRMON_CMP1_TTYPE: Write monitor 1. 0: TType
16:23	RW	WRMON_CMP1_TSIZE: Write monitor 1. 0: TSize
24:30	RW	WRMON_CMP1_TTYPEMSK: Write monitor 1. 0: TType mask
31:38	RW	WRMON_CMP1_TSIZEMSK: Write monitor 1. 0: TSize mask
39:63	RO	constant = 0b00000000000000000000000000

Register Name	Write Monitor 2 TType Compare Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON2CMP
Address	0000000003011822 (SCOM)
Description	Write Monitor 2 TType Compare Register

Bits	SCOM	Field Mnemonic: Description
0	RW	WRMON_CMP2_VAL: Write monitor 2. 0: Valid/Enable
1:6	RW	WRMON_CMP2_TTYPEDIS: Write monitor 2. 0: TType disable bits
7	RW	WRMON_CMP2_UNUSED: Unused bit 2.
8	RW	WRMON_CMP2_ENADTTYPE: Write monitor 2. 0: Enable additional TType to monitor

Bits	SCOM	Field Mnemonic: Description
9:15	RW	WRMON_CMP2_TTYPE: Write monitor 2. 0: TType
16:23	RW	WRMON_CMP2_TSIZE: Write monitor 2. 0: TSize
24:30	RW	WRMON_CMP2_TTYPEMSK: Write monitor 2. 0: TType mask
31:38	RW	WRMON_CMP2_TSIZEMSK: Write monitor 2. 0: TSize mask
39:63	RO	constant = 0b00000000000000000000000

Register Name	Write Monitor 3 TType Compare Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON3CMP
Address	0000000003011823 (SCOM)
Description	Write Monitor 3 TType Compare Register

Bits	SCOM	Field Mnemonic: Description
0	RW	WRMON_CMP3_VAL: Write monitor 3. 0: Valid/Enable
1:6	RW	WRMON_CMP3_TTYPEDIS: Write monitor 3. 0: TType disable bits
7	RW	WRMON_CMP3_UNUSED: Unused bit.
8	RW	WRMON_CMP3_ENADTTYPE: Write monitor 3. 0: Enable additional TType to monitor
9:15	RW	WRMON_CMP3_TTYPE: Write monitor 3. 0: TType
16:23	RW	WRMON_CMP3_TSIZE: Write monitor 3. 0: TSize
24:30	RW	WRMON_CMP3_TTYPEMSK: Write monitor 3. 0: TType mask
31:38	RW	WRMON_CMP3_TSIZEMSK: Write monitor 3. 0: TSize mask
39:63	RO	constant = 0b00000000000000000000000

Register Name	Write Monitor 4 TType Compare Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON4CMP
Address	0000000003011824 (SCOM)
Description	Write Monitor 4 TType Compare Register

Bits	SCOM	Field Mnemonic: Description
0	RW	WRMON_CMP4_VAL: Write monitor 4. 0: Valid/Enable
1:6	RW	WRMON_CMP4_TTYPEDIS: Write monitor 4. 0: TType disable bits
7	RW	WRMON_CMP4_UNUSED: Unused bit.

Bits	SCOM	Field Mnemonic: Description
8	RW	WRMON_CMP4_ENADTTYPE: Write monitor 4. 0: Enable additional TType to monitor
9:15	RW	WRMON_CMP4_TTYPE: Write monitor 4. 0: TType
16:23	RW	WRMON_CMP4_TSIZE: Write monitor 4. 0: TSize
24:30	RW	WRMON_CMP4_TTYPEMSK: Write monitor 4. 0: TType mask
31:38	RW	WRMON_CMP4_TSIZEMSK: Write monitor 4. 0: TSize mask
39:63	RO	constant = 0b00000000000000000000000000

Register Name	**Write Monitor 5 TType Compare Register**
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON5CMP
Address	0000000003011825 (SCOM)
Description	Write Monitor 5 TType Compare Register

Bits	SCOM	Field Mnemonic: Description
0	RW	WRMON_CMP5_VAL: Write monitor 5. 0: Valid/Enable
1:6	RW	WRMON_CMP5_TTYPEDIS: Write monitor 5. 0: TType disable bits
7	RW	WRMON_CMP5_UNUSED: Unused bit.
8	RW	WRMON_CMP5_ENADTTYPE: Write monitor 5. 0: Enable additional TType to monitor
9:15	RW	WRMON_CMP5_TTYPE: Write monitor 5. 0: TType
16:23	RW	WRMON_CMP5_TSIZE: Write monitor 5. 0: TSize
24:30	RW	WRMON_CMP5_TTYPEMSK: Write monitor 5. 0: TType mask
31:38	RW	WRMON_CMP5_TSIZEMSK: Write monitor 5. 0: TSize mask
39:63	RO	constant = 0b00000000000000000000000000

Register Name	**Write Monitor 6 TType Compare Register**
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON6CMP
Address	0000000003011826 (SCOM)
Description	Write Monitor 6 TType Compare Register

Bits	SCOM	Field Mnemonic: Description
0	RW	WRMON_CMP6_VAL: Write monitor 6. 0: Valid/Enable

Bits	SCOM	Field Mnemonic: Description
1:6	RW	WRMON_CMP6_TTYPEDIS: Write monitor 6. 0: TType disable bits
7	RW	WRMON_CMP6_UNUSED: Unused bit.
8	RW	WRMON_CMP6_ENADTTYPE: Write monitor 6. 0: Enable additional TType to monitor
9:15	RW	WRMON_CMP6_TTYPE: Write monitor 6. 0: TType
16:23	RW	WRMON_CMP6_TSIZE: Write monitor 6. 0: TSize
24:30	RW	WRMON_CMP6_TTYPEMSK: Write monitor 6. 0: TType mask
31:38	RW	WRMON_CMP6_TSIZEMSK: Write monitor 6. 0: TSize mask
39:63	RO	constant = 0b00000000000000000000000000

Register Name	**Write Monitor 7 TType Compare Register**
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_WRMON7CMP
Address	0000000003011827 (SCOM)
Description	Write Monitor 7 TType Compare Register

Bits	SCOM	Field Mnemonic: Description
0	RW	WRMON_CMP7_VAL: Write monitor 7. 0: Valid/Enable
1:6	RW	WRMON_CMP7_TTYPEDIS: Write monitor 7. 0: TType disable bits
7	RW	WRMON_CMP7_UNUSED: Unused bit.
8	RW	WRMON_CMP7_ENADTTYPE: Write monitor 7. 0: Enable additional TType to monitor
9:15	RW	WRMON_CMP7_TTYPE: Write monitor 7. 0: TType
16:23	RW	WRMON_CMP7_TSIZE: Write monitor 7. 0: TSize
24:30	RW	WRMON_CMP7_TTYPEMSK: Write monitor 7. 0: TType mask
31:38	RW	WRMON_CMP7_TSIZEMSK: Write monitor 7. 0: TSize mask
39:63	RO	constant = 0b00000000000000000000000000

Register Name	**Window ID MMIO Control Register**
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_MMIOCTL
Address	0000000003011829 (SCOM)
Description	Window ID MMIO Control Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	MMIO_CTL_INIT: Initiate MMIO Operation. SW asserts this bit to start MMIO. HW clears bit when MMIO is done.
1	RWX	MMIO_CTL_COMP: MMIO Complete. HW asserts this bit when MMIO operation is complete. SW must clear bit before reuse.
2	RW	MMIO_CTL_OPTYPE: Operation type load/store. 0 = MMIO Store 1 = MMIO Load
3	RW	MMIO_CTL_ACTYPE: Window Cache Access Type: 0 = Normal MMIO read/write 1 = Raw read of WC array contents
4	RWX	MMIO_CTL_OP_ERR: Error Indicator: 0 = No error 1 = Operation completed with error (typically bad address offset).
5:7	RW	MMIO_CTL_UNUSED: Window ID MMIO Control Register unused bits.
8:35	RO	constant = 0b00000000000000000000000000000000
36:47	RW	MMIO_CTL_OFFSET: Register offset. This field specifies the register to be read or written. Not used for raw array content display operation.

Bits	SCOM	Field Mnemonic: Description
48:63	RW	MMIO_CTL_WINID: Window ID. Specifies which of the 64 K window IDs should be read or written.

Register Name	Window ID MMIO Data Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_MMIODATA
Address	000000000301182A (SCOM)
Description	Window ID MMIO Data Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	MMIO_DATA: Data for MMIO write or read operation. ECC for read operation is in the Window ID MMIO ECC Register.

Register Name	IN Error Capture Contents Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_INERRRPT
Address	000000000301182B (SCOM)
Description	IN Error Capture Contents Register

Bits	SCOM	Field Mnemonic: Description
0	WOX	IN_CERR_RESET: c_err_rpt (Error capture) reset bit for IN logic. Asserting this bit resets the error capture keeper latches.
1:3	RO	constant = 0b000
4	ROX	IN_CERR_BIT4: ECC Correctable error (CE) in Window Cache Data0.
5	ROX	IN_CERR_BIT5: ECC Correctable error (CE) in Window Cache Data1.
6	ROX	IN_CERR_BIT6: ECC uncorrectable error (UE) in Window Cache Data0.
7	ROX	IN_CERR_BIT7: ECC uncorrectable error (UE) in Window Cache Data1.
8	ROX	IN_CERR_BIT8: ECC special uncorrectable Error (SUE) in Window Cache Data0.
9	ROX	IN_CERR_BIT9: ECC special uncorrectable Error (SUE) in Window Cache Data1.
10	ROX	IN_CERR_BIT10: Parity error on CAM data fields while doing a castout.
11	ROX	IN_CERR_BIT11: Parity error on CAM data fields while doing an MMIO operation.
12	ROX	IN_CERR_BIT12: Parity error on CAM lookup send data fields for a paste command.
13	ROX	IN_CERR_BIT13: Parity error on CAM lookup receive data fields for a paste command.
14	ROX	IN_CERR_BIT14: Parity error on CAM WINID field.
15	ROX	IN_CERR_BIT15: Software tried to castout an entry that was still in use.
16	ROX	IN_CERR_BIT16: VAS received a paste command for a WINID that is being castout by software.
17	ROX	IN_CERR_BIT17: Hardware rejected an RMA (read or write) command arriving on RCMD bus 1, 2, or 3.
18	ROX	IN_CERR_BIT18: Hardware rejected a paste command received on bus0 due to L=1 (length not zero) or command was an RMA read.
19	ROX	IN_CERR_BIT19: Hardware rejected a paste command due to send window being closed.
20	ROX	IN_CERR_BIT20: Hardware rejected a paste command due to receive window being closed.
21	ROX	IN_CERR_BIT21: Hardware rejected a paste command because (send) fault window had no credits.
22	ROX	IN_CERR_BIT22: Hardware rejected a paste command because send window had no credits (and HW is configured to do this).

Bits	SCOM	Field Mnemonic: Description
23	ROX	IN_CERR_BIT23: Hardware rejected a paste command because receive(fault) window had no credits.
24	ROX	IN_CERR_BIT24: Hardware rejected a paste command because receive window had no credits (and HW is configured to do this).
25	ROX	IN_CERR_BIT25: Multihit detected in CAM during a send window lookup.
26	ROX	IN_CERR_BIT26: Multihit detected in CAM during a receive window lookup.
27	ROX	IN_CERR_BIT27: Multihit detected in CAM during an MMIO lookup.
28	ROX	IN_CERR_BIT28: Combined response hit multiple entries in ingress cResp logic.
29	ROX	IN_CERR_BIT29: State machine entered an invalid state in the castout logic.
30	ROX	IN_CERR_BIT30: Data arrived for send window context, but no CAM slot was reserved for prefetching receive window context.
31	ROX	IN_CERR_BIT31: Unused bit.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	RG Error Capture Contents Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_RGERRRPT
Address	000000000301182C (SCOM)
Description	RG Error Capture Contents Register

Bits	SCOM	Field Mnemonic: Description
0	WOX	RG_CERR_RESET: c_err_rpt (Error capture) reset bit for RG logic. Asserting this bit resets the error capture keeper latches.
1:3	RO	constant = 0b000
4	ROX	RG_CERR_BIT4: RCMD Bus 0 Address parity error.
5	ROX	RG_CERR_BIT5: RCMD Bus 1 Address parity error.
6	ROX	RG_CERR_BIT6: RCMD Bus 2 Address parity error.
7	ROX	RG_CERR_BIT7: RCMD Bus 3 Address parity error.
8	ROX	RG_CERR_BIT8: RCMD Bus 0 TTAG parity error.
9	ROX	RG_CERR_BIT9: RCMD Bus 1 TTAG parity error.
10	ROX	RG_CERR_BIT10: RCMD Bus 2 TTAG parity error.
11	ROX	RG_CERR_BIT11: RCMD Bus 3 TTAG parity error.
12	ROX	RG_CERR_BIT12: Parity error detected on the current state of the MMIO state machine.
13	ROX	RG_CERR_BIT13: MMIO state machine has entered an invalid state.
14:23	ROX	RG_CERR_UNUSED_BITS: Unused bits.
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	Debug Bus IN/RG and Group Trace/PMU Selection Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_DBGNORTH
Address	000000000301182D (SCOM)
Description	Debug Bus IN/RG and Group Trace/PMU Selection Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	SEL_RG_TRACE_DATA_LO: Trace data selection for bits 00 - 43: 0b00 = pass ingress data 0b01 = pass CQ data 0b10 = pass RG internal data
2:3	RW	SEL_RG_TRACE_DATA_HI: Trace data selection for bits 44 - 87: 0b00 = pass ingress data 0b01 = pass CQ data 0b10 = pass RG internal data
4:5	RW	SEL_RG_TRIGGERS_01: Trigger selection for triggers 0, 1: 0b00 = pass Ingress triggers 0b01 = pass CQ triggers 0b10 = pass RG internal triggers
6:7	RW	SEL_RG_TRIGGERS_23: Trigger selection for triggers 2, 3: 0b00 = pass Ingress triggers 0b01 = pass CQ triggers 0b10 = pass RG internal triggers
8:10	RW	IN_TRACE_GROUP_SEL_LO: Select Ingress internal trace groups for bits 0:43, 0b000 = group0, 0b001 = group1, ... , 0b111 = group7.
11:13	RW	IN_TRACE_GROUP_SEL_HI: Select Ingress internal trace groups for bits 44:87, 0b000 = group0, 0b001 = group1, ... , 0b111 = group7.
14:16	RW	IN_TRACE_TRIGGER_SEL_01: Select Ingress internal trigger group for triggers 0, 1 0b000 = group0, 0b001 = group1, ... , 0b111 = group7.
17:19	RW	IN_TRACE_TRIGGER_SEL_23: Select Ingress internal trigger group for triggers 2, 3 0b000 = group0, 0b001 = group1, ... , 0b111 = group7.
20:22	RW	RG_TRACE_GROUP_SEL_LO: Select RG internal trace groups for bits 0:43 0b000 = group0, 0b001 = group1, ... , 0b111 = group7.
23:25	RW	RG_TRACE_GROUP_SEL_HI: Select RG internal trace groups for bits 44:87 0b000 = group0, 0b001 = group1, ... , 0b111 = group7.
26:28	RW	RG_TRACE_TRIGGER_SEL_01: Select RG internal trigger group for triggers 0, 1 0b000 = group0, 0b001 = group1, ... , 0b111 = group7.
29:31	RW	RG_TRACE_TRIGGER_SEL_23: Select RG internal trigger group for triggers 2, 3 0b000 = group0, 0b001 = group1, ... , 0b111 = group7.
32	RW	ENABLE_IN_TRACE: Enable Ingress trace logic. Must be asserted to trace ingress data.
33	RW	ENABLE_RG_TRACE: Enable RG trace logic. Must be asserted to trace RG data, or pass ingress, CQ, WC, or EG data.
34:35	RW	DBG_NORTH_UNUSED_BITS0: Unused bits.

Bits	SCOM	Field Mnemonic: Description
36	RW	SEL_RG_PMU_DATA: Select PMU data out, bits 0-31: 0b0 = pass Ingress/RG data, 0b1 = pass EG/CQ data.
37:39	RW	DBG_NORTH_UNUSED_BITS1: Unused bits.
40	RW	ENABLE_IN_PMU_COUNTING: Enable ingress PMU counting. Must be asserted to count ingress events.
41	RW	ENABLE_RG_PMU_COUNTING: Enable RG PMU counting. Must be asserted to count RG events, or pass Ingress, CQ, WC, or EG events.
42	RW	IN_TRACE_INT_DATA_LO: Select Lower(0:43) or Upper(44:87) Half of IN trace data for bits 0:43.
43	RW	IN_TRACE_INT_DATA_HI: Select Lower(0:43) or Upper(44:87) Half of IN trace data for bits 44:87.
44	RW	EG_TRACE_INT_DATA_LO: Select Lower(0:43) or Upper(44:87) Half of EG trace data for bits 0:43.
45	RW	EG_TRACE_INT_DATA_HI: Select Lower(0:43) or Upper(44:87) Half of EG trace data for bits 44:87.
46	RW	RG_TRACE_INT_DATA_LO: Select Lower(0:43) or Upper(44:87) Half of RG trace data for bits 0:43.
47	RW	RG_TRACE_INT_DATA_HI: Select Lower(0:43) or Upper(44:87) Half of RG trace data for bits 44:87.
48	RW	IN_TRACE_INT_TRIG_01: Select Lower(0:1) or Upper(2:3) Half of IN trace triggers for bits 0:1.
49	RW	IN_TRACE_INT_TRIG_23: Select Lower(0:1) or Upper(2:3) Half of IN trace triggers for bits 2:3.
50	RW	EG_TRACE_INT_TRIG_01: Select Lower(0:1) or Upper(2:3) Half of EG trace triggers for bits 0:1.
51	RW	EG_TRACE_INT_TRIG_23: Select Lower(0:1) or Upper(2:3) Half of EG trace triggers for bits 2:3.
52	RW	RG_TRACE_INT_TRIG_01: Select Lower(0:1) or Upper(2:3) Half of RG trace triggers for bits 0:1.
53	RW	RG_TRACE_INT_TRIG_23: Select Lower(0:1) or Upper(2:3) Half of RG trace triggers for bits 2:3.
54:63	RO	constant = 0b0000000000

Register Name	Debug Bus Data Contents Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_DBGCONT
Address	000000000301182E (SCOM)
Description	This register contains bits 0 – 63 of the trace/debug bus.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_BUS_BITS_0_63: This dial contains bits 0 - 63 of the trace/debug bus.

Register Name	Debug Bus Data and Trigger Contents Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_DBGTRIG
Address	000000000301182F (SCOM)
Description	This register contains bits 64 – 87 of the trace/debug bus and bits 0 – 3 of the trace/trigger bus.

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	TRACE_BUS_BITS_64_87: This dial contains bits 64 - 87 of the trace/debug bus.
24:27	ROX	TRACE_BUS_TRIGGER_BITS: This dial contains trigger bits 0 - 3 of the trace/trigger bus.
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	Performance Monitor Control Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_PMCNTL
Address	0000000003011830 (SCOM)
Description	This register is used to enable performance counter bits.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	PU_BIT_ENABLES: Each bit of this dial is used to enable the associated performance counter bit and send it to the PMU.
32:35	RW	PU_CNTL_UNUSED: Unused bits.
36:63	RO	constant = 0b00000000000000000000000000000

Register Name	Window ID MMIO ECC Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_MMIOECC
Address	0000000003011831 (SCOM)
Description	This register contains an error correction code (ECC) for MMIO data.

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	MMIO_ECC: This field contains an ECC for MMIO data returned by an MMIO read operation. The data itself is in the Window ID MMIO Data Register.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	North ECC Error Injection Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_ERRINJNO
Address	0000000003011832 (SCOM)
Description	This register is used to control ECC error injection.

Bits	SCOM	Field Mnemonic: Description
0	RW	ECC_ERR_INJ_NORTH_WC_ENA: This bit enables ECC error injection in the MMIO logic.
1	RW	ECC_ERR_INJ_NORTH_WC_TYP: This bit selects the ECC error-injection type for the MMIO logic: 0 = Single-bit errors. 1 = Double-bit errors.
2	RW	ECC_ERR_INJ_NORTH_WC_FRQ: This bit selects the ECC error-injection frequency for the MMIO logic: 0 = Single shot. 1 = Continuous errors.
3:7	RW	ECC_ERR_INJ_NORTH_WC_UNUSED: Unused bits.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	CAM Display Control Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_CAMDISPCNTL
Address	0000000003011833 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0	RO	Not implemented.
1	WOX	RESERVED.
2:15	RO	Not implemented.
16:31	WOX	RESERVED.
32:63	RO	Not implemented.

Register Name	CAM Display Data 0 Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_CAMDATA0
Address	0000000003011834 (SCOM)
Description	This register contains bit 0 – 63 of the content-addressable memory (CAM) Display 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	CAM_DISPLAY_REG_0: This dial contains bits 0 - 63 of the CAM Display 0 Register.

Register Name	CAM Display Data 1 Register
Mnemonic	VA.VA_NORTH.VA_RG.SCF.VAS_CAMDATA1
Address	0000000003011835 (SCOM)
Description	This register contains bit 0 – 63 of the CAM Display 1 Register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	CAM_DISPLAY_REG_1: This dial contains bits 0 - 63 of the CAM Display 1 Register.

Register Name	Window Context Backing Store Base Address Register
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_WCBSBAR
Address	0000000003011840 (SCOM)
Description	This is the Window Context Backing Store Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:40	RW	WC_BS_BAR: Window Context Backing Store Base Address Register.
41:63	RO	constant = 0b00000000000000000000000

Register Name	Page Migration Register 1
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG1
Address	0000000003011841 (SCOM)
Description	This register is used to control page migration 1.

Bits	SCOM	Field Mnemonic: Description
0	RW	PGMIGR1_VAL: This bit indicates that page migration 1 is valid or enabled.

Bits	SCOM	Field Mnemonic: Description
1:7	RO	constant = 0b0000000
8:53	RW	PGMIGR1_BAR: This field contains the page migration 1 base real address.
54:59	RO	constant = 0b000000
60:63	RW	PGMIGR1_PGSZ: This field contains the page migration 1 page size.

Register Name	Page Migration Register 2
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG2
Address	0000000003011842 (SCOM)
Description	This register is used to control page migration 2.

Bits	SCOM	Field Mnemonic: Description
0	RW	PGMIGR2_VAL: This bit indicates that page migration 2 is valid or enabled.
1:7	RO	constant = 0b0000000
8:53	RW	PGMIGR2_BAR: This field contains the page migration 2 base real address.
54:59	RO	constant = 0b000000
60:63	RW	PGMIGR2_PGSZ: This field contains the page migration 2 page size.

Register Name	Page Migration Register 3
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG3
Address	0000000003011843 (SCOM)
Description	This register is used to control page migration 3.

Bits	SCOM	Field Mnemonic: Description
0	RW	PGMIGR3_VAL: This bit indicates that page migration 3 is valid or enabled.
1:7	RO	constant = 0b0000000
8:53	RW	PGMIGR3_BAR: This field contains the page migration 3 base real address.
54:59	RO	constant = 0b000000
60:63	RW	PGMIGR3_PGSZ: This field contains the page migration 3 page size.

Register Name	Page Migration Register 4
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG4
Address	0000000003011844 (SCOM)
Description	This register is used to control page migration 4.

Bits	SCOM	Field Mnemonic: Description
0	RW	PGMIGR4_VAL: This bit indicates that page migration 4 is valid or enabled.
1:7	RO	constant = 0b0000000
8:53	RW	PGMIGR4_BAR: This field contains the page migration 4 base real address.
54:59	RO	constant = 0b000000

Bits	SCOM	Field Mnemonic: Description
60:63	RW	PGMIGR4_PGSZ: This field contains the page migration 4 page size.

Register Name	Page Migration Register 5
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG5
Address	0000000003011845 (SCOM)
Description	This register is used to control page migration 5.

Bits	SCOM	Field Mnemonic: Description
0	RW	PGMIGR5_VAL: This bit indicates that page migration 5 is valid or enabled.
1:7	RO	constant = 0b0000000
8:53	RW	PGMIGR5_BAR: This field contains the page migration 5 base real address.
54:59	RO	constant = 0b000000
60:63	RW	PGMIGR5_PGSZ: This field contains the page migration 5 page size.

Register Name	Page Migration Register 6
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG6
Address	0000000003011846 (SCOM)
Description	This register is used to control page migration 6.

Bits	SCOM	Field Mnemonic: Description
0	RW	PGMIGR6_VAL: This bit indicates that page migration 6 is valid or enabled.
1:7	RO	constant = 0b0000000
8:53	RW	PGMIGR6_BAR: This field contains the page migration 6 base real address.
54:59	RO	constant = 0b000000
60:63	RW	PGMIGR6_PGSZ: This field contains the page migration 6 page size.

Register Name	Page Migration Register 7
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PGMIG7
Address	0000000003011847 (SCOM)
Description	This register is used to control page migration 7.

Bits	SCOM	Field Mnemonic: Description
0	RW	PGMIGR7_VAL: This bit indicates that page migration 7 is valid or enabled.
1:7	RO	constant = 0b0000000
8:53	RW	PGMIGR7_BAR: This field contains the page migration 7 base real address.
54:59	RO	constant = 0b000000
60:63	RW	PGMIGR7_PGSZ: This field contains the page migration 7 page size.

Register Name	CQ Error Capture Contents Register
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_CQERRRPT
Address	0000000003011848 (SCOM)
Description	This register contains common queue (CQ) error information.

Bits	SCOM	Field Mnemonic: Description
0	WOX	CQ_CERR_RESET: This is the error capture (c_err_rpt) reset bit for the CQ logic. Asserting this bit resets the error-capture keeper latches.
1:3	RO	constant = 0b000
4	ROX	CQ_CERR_BIT4: Parity error on MMIO data RTAG.
5	ROX	CQ_CERR_BIT5: Parity error on the RTAG for combined response bus 0.
6	ROX	CQ_CERR_BIT6: Parity error on the RTAG for combined response bus 1.
7	ROX	CQ_CERR_BIT7: Parity error on the RTAG for combined response bus 2.
8	ROX	CQ_CERR_BIT8: Parity error on the RTAG for combined response bus 3.
9	ROX	CQ_CERR_BIT9: Parity error on the address provided for a write operation.
10	ROX	CQ_CERR_BIT10: Parity error on the address provided for a read operation.
11	ROX	CQ_CERR_BIT11: Parity error on the RTAG for an incoming data payload into CQ.
12	ROX	CQ_CERR_BIT12: Parity error on the combined response TTAG for bus 0.
13	ROX	CQ_CERR_BIT13: Parity error on the combined response TTAG for bus 1.
14	ROX	CQ_CERR_BIT14: Parity error on the combined response TTAG for bus 2.
15	ROX	CQ_CERR_BIT15: Parity error on the combined response TTAG for bus 3.
16	ROX	CQ_CERR_BIT16: Parity error on the ATAG for combined response bus 0.
17	ROX	CQ_CERR_BIT17: Parity error on the ATAG for combined response bus 1.
18	ROX	CQ_CERR_BIT18: Parity error on the ATAG for combined response bus 2.
19	ROX	CQ_CERR_BIT19: Parity error on the ATAG for combined response bus 3.
20	ROX	CQ_CERR_BIT20: Hang detected on a write machine (write machine waiting for data for a write read push protocol, for example).
21	ROX	CQ_CERR_BIT21: Hang detected on a read machine (read machine waiting for data for a read operation).
22	ROX	CQ_CERR_BIT22: ACK dead combined response (cRESP) received for a read operation occurring on a write machine.
23	ROX	CQ_CERR_BIT23: ACK dead cRESP received for a read operation occurring on a read machine.
24	ROX	CQ_CERR_BIT24: Abort operation received for a write machine.
25	ROX	CQ_CERR_BIT25: Abort operation received for a read machine.
26	ROX	CQ_CERR_BIT26: Write machine entered an undefined state (hardware error).
27	ROX	CQ_CERR_BIT27: Read machine entered an undefined state (hardware error).
28	ROX	CQ_CERR_BIT28: Undefined cRESP received for a read machine.
29	ROX	CQ_CERR_BIT29: cRESP received for a read machine before transition to wait for cRESP state (for example, command not yet mastered).
30	ROX	CQ_CERR_BIT30: Data received before the read machine expects it.
31	ROX	CQ_CERR_BIT31: Attempt made to start an active read machine.
32	ROX	CQ_CERR_BIT32: Undefined cRESP received for a write machine.

Bits	SCOM	Field Mnemonic: Description
33	ROX	CQ_CERR_BIT33: cRESP received for a write machine before the transition to wait for cRESP state (for example, command not yet mastered).
34	ROX	CQ_CERR_BIT34: Data received before the write machine expects it.
35	ROX	CQ_CERR_BIT35: Attempt made to start an active write machine.
36	ROX	CQ_CERR_BIT36: Unused bit.
37	ROX	CQ_CERR_BIT37: Unused bit.
38	ROX	CQ_CERR_BIT38: Unused bit.
39	ROX	CQ_CERR_BIT39: Unused bit.
40:63	RO	constant = 0b00000000000000000000000

Register Name	WC Error Capture Contents Register
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_WCERRRPT
Address	0000000003011849 (SCOM)
Description	This register contains write control (WC) error information.

Bits	SCOM	Field Mnemonic: Description
0	WOX	WC_CERR_RESET: Error capture (c_err_rpt) reset bit for the WC logic. Asserting this bit resets the error capture keeper latches.
1:3	RO	constant = 0b000
4	ROX	WC_CERR_BIT4: Correctable ECC error (CE) from WC array bank 0 or 2.
5	ROX	WC_CERR_BIT5: Correctable ECC error (CE) from WC array bank 1 or 3.
6	ROX	WC_CERR_BIT6: Uncorrectable ECC error (UE) from WC array bank 0 or 2.
7	ROX	WC_CERR_BIT7: Uncorrectable ECC error (UE) from WC array bank 1 or 3.
8	ROX	WC_CERR_BIT8: Special uncorrectable ECC error (SUE) from WC array bank 0 or 2.
9	ROX	WC_CERR_BIT9: Special uncorrectable ECC error (SUE) from WC array bank 1 or 3.
10	ROX	WC_CERR_BIT10: WC logic received an unexpected castout request.
11	ROX	WC_CERR_BIT11: WC logic sent a new command to the CQ without waiting for a castout ACK from a previous command.
12	ROX	WC_CERR_BIT12: Overflow detected in the WC send FIFO.
13	ROX	WC_CERR_BIT13: Read error detected in the WC send FIFO (tried to read an empty FIFO).
14	ROX	WC_CERR_BIT14: Overflow detected in the WC fill FIFO.
15	ROX	WC_CERR_BIT15: Read error detected in the WC fill FIFO (tried to read an empty FIFO).
16	ROX	WC_CERR_BIT16: Overflow detected in the WC castout FIFO.
17	ROX	WC_CERR_BIT17: Read error detected in the WC castout FIFO (tried to read an empty FIFO).
18	ROX	WC_CERR_BIT18: Parity check detected an invalid (non-hot1) state in the send FIFO FSM.
19	ROX	WC_CERR_BIT19: Parity check detected an invalid (non-hot1) state in the fill FIFO FSM.
20	ROX	WC_CERR_BIT20: Parity check detected an invalid (non-hot1) state in the castout FIFO FSM.
21	ROX	WC_CERR_BIT21: Parity check detected an invalid (non-hot1) state in the WC scrubber FSM.
22	ROX	WC_CERR_BIT22: Parity check detected an invalid (non-hot1) state in the WC write FSM.
23	ROX	WC_CERR_BIT23: Parity check detected an invalid (non-hot1) state in the WC read FSM.

Bits	SCOM	Field Mnemonic: Description
24:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	EG Error Capture Contents Register
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_EGERRRPT
Address	0000000003011844A (SCOM)
Description	EG Error Capture Contents Register

Bits	SCOM	Field Mnemonic: Description
0	WOX	EG_CERR_RESET: c_err_rpt (Error capture) reset bit for EG logic. Asserting this bit resets the error capture keeper latches.
1:3	RO	constant = 0b000
4	ROX	EG_CERR_BIT4: EG unloader state machine parity error.
5	ROX	EG_CERR_BIT5: EG data buffer state machine parity error.
6	ROX	EG_CERR_BIT6: EG data flow ECC correctable error (CE) detected in array 0.
7	ROX	EG_CERR_BIT7: EG data flow ECC CE detected in array 1.
8	ROX	EG_CERR_BIT8: EG data flow ECC uncorrectable error (UE) detected in array 0.
9	ROX	EG_CERR_BIT9: EG data flow ECC UE detected in array 1.
10	ROX	EG_CERR_BIT10: EG data flow ECC special uncorrectable error (SUE) detected in array 0.
11	ROX	EG_CERR_BIT11: EG data flow ECC S SUE detected in array 1.
12:19	ROX	EG_CERR_UNUSEDBITS: Unused bits.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	South ECC Error Injection Register
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_ERRINJSO
Address	0000000003011845B (SCOM)
Description	South ECC Error Injection Register

Bits	SCOM	Field Mnemonic: Description
0	RW	ECC_ERR_INJ_SOUTH_WC_ENA: Enable ECC error injection in Window Cache (WC) logic.
1	RW	ECC_ERR_INJ_SOUTH_WC_TYP: ECC error injection type for WC logic: 0 = Single-bit errors. 1 = Double-bit errors.
2	RW	ECC_ERR_INJ_SOUTH_WC_FRQ: ECC error injection frequency for WC logic: 0 = Single shot. 1 = Continuous errors.
3:4	RW	ECC_ERR_INJ_SOUTH_WC_SEL: Array selection for WC arrays: 0b00 = array0 0b01 = array1 0b10 = array2 0b11 = array3
5	RW	ECC_ERR_INJ_SOUTH_EG_ENA: Enable ECC error injection in egress (EG) logic.

Bits	SCOM	Field Mnemonic: Description
6	RW	ECC_ERR_INJ_SOUTH_EG_TYP: ECC error injection type for EG logic: 0 = single-bit errors 1 = double bit errors
7	RW	ECC_ERR_INJ_SOUTH_EG_FRQ: ECC error injection frequency for EG logic: 0 = single shot 1 = continuous errors
8	RW	ECC_ERR_INJ_SOUTH_EG_SEL: Array selection for EG arrays: 0b0 = array0 0b1 = array1
9:11	RW	ECC_ERR_INJ_SOUTH_UNUSED: Unused bits.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Debug Bus EG/WC/CQ and Group Trace/PMU Selection Register
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_DBGSOUTH
Address	000000000301184C (SCOM)
Description	Debug Bus EG/WC/CQ and Group Trace/PMU Selection Register

Bits	SCOM	Field Mnemonic: Description
0	RW	PASS_WC_INT_TRACE_DATA_LO: Select trace data bits 0:43. 0 = pass EG data to CQ, 1 = pass WC internal data to CQ.
1	RW	PASS_WC_INT_TRACE_DATA_HI: Select trace data bits 44:87. 0 = pass EG data to CQ, 1 = pass WC internal data to CQ.
2	RW	PASS_CQ_INT_TRACE_DATA_LO: Select trace data bits 0:43. 0 = pass WC data to RG, 1 = pass CQ internal data to RG.
3	RW	PASS_CQ_INT_TRACE_DATA_HI: Select trace data bits 44:87. 0 = pass WC data to RG, 1 = pass CQ internal data to RG.
4	RW	PASS_WC_INT_TRACE_TRIG_01: Select trace triggers 0,1. 0 = pass EG triggers to CQ, 1 = pass WC internal triggers to CQ.
5	RW	PASS_WC_INT_TRACE_TRIG_23: Select trace triggers 2,3. 0 = pass EG triggers to CQ, 1 = pass WC internal triggers to CQ.
6	RW	PASS_CQ_INT_TRACE_TRIG_01: Select trace triggers 0,1. 0 = pass WC triggers to RG, 1 = pass CQ internal triggers to RG.
7	RW	PASS_CQ_INT_TRACE_TRIG_23: Select trace triggers 2,3. 0 = pass WC triggers to RG, 1 = pass CQ internal triggers to RG.
8:11	RW	EG_TRACE_GROUP_SEL_LO: Select EG internal trace groups for bits 0:43. 0b0000=group0 0b0001=group1 ... 0b1111=group15

Bits	SCOM	Field Mnemonic: Description
12:15	RW	EG_TRACE_GROUP_SEL_HI: Select EG internal trace groups for bits 44:87. 0b0000 = group0 0b0001 = group1, ... 0b1111 = group15
16:17	RW	EG_TRACE_TRIGGER_SEL_01: Select EG internal trigger group for triggers 0,1. 0b00 = group0 0b01 = group1 ... 0b11 = group3
18:19	RW	EG_TRACE_TRIGGER_SEL_23: Select EG internal trigger group for triggers 2,3. 0b00 = group0 0b01 = group1 ... 0b11 = group3
20:22	RW	WC_TRACE_GROUP_SEL_LO: Select WC internal trace groups for bits 0:43. 0b000 = group0 0b001 = group1 ... 0b111 = group7
23:25	RW	WC_TRACE_GROUP_SEL_HI: Select WC internal trace groups for bits 44:87. 0b000 = group0 0b001 = group1 ... 0b111 = group7
26:28	RW	WC_TRACE_TRIGGER_SEL_01: Select WC internal trigger group for triggers 0,1. 0b000 = group0 0b001 = group1 ... 0b111 = group7
29:31	RW	WC_TRACE_TRIGGER_SEL_23: Select WC internal trigger group for triggers 2,3. 0b000 = group0 0b001 = group1 ... 0b111 = group7
32:34	RW	CQ_TRACE_GROUP_SEL_LO: Select CQ internal trace groups for bits 0:43. 0b000 = group0, 0b001 = group1 ... 0b111 = group7
35:37	RW	CQ_TRACE_GROUP_SEL_HI: Select CQ internal trace groups for bits 44:87. 0b000 = group0 0b001 = group1 ... 0b111 = group7
38:40	RW	CQ_TRACE_TRIGGER_SEL_01: Select CQ internal trigger group for triggers 0,1. 0b000 = group0 0b001 = group1 ... 0b111 = group7
41:43	RW	CQ_TRACE_TRIGGER_SEL_23: Select CQ internal trigger group for triggers 2,3. 0b000 = group0 0b001 = group1 ... 0b111 = group7
44	RW	ENABLE_EG_TRACE: Enable EG trace logic. Must be asserted to trace EG data.
45	RW	ENABLE_WC_TRACE: Enable WC trace logic. Must be asserted to trace WC data, or pass EG data.
46	RW	ENABLE_CQ_TRACE: Enable CQ trace logic. Must be asserted to trace CQ data, or pass EG or WC data.
47	RW	WC_TRACE_INT_DATA_LO: Select Lower(0:43) or Upper(44:87) Half of WC trace data for bits 0:43.
48	RW	WC_TRACE_INT_DATA_HI: Select Lower(0:43) or Upper(44:87) Half of WC trace data for bits 44:87.
49	RW	EG_TRACE_INT_DATA_LO: Select Lower(0:43) or Upper(44:87) Half of EG trace data for bits 0:43.

Bits	SCOM	Field Mnemonic: Description
50	RW	PASS_CQ_INT_PMU_DATA_LO: Select PMU data bits 0:7 at CQ: 0 = pass WC data to RG 1 = pass CQ internal data to RG
51	RW	PASS_CQ_INT_PMU_DATA_HI: Select PMU data bits 8:15 at CQ: 0 = pass WC data to RG 1 = pass CQ internal data to RG
52	RW	ENABLE_EG_PMU_COUNTING: Enable EG PMU counting. Must be asserted to count EG events.
53	RW	EG_TRACE_INT_DATA_HI: Select Lower(0:43) or Upper(44:87) Half of EG trace data for bits 44:87.
54	RW	ENABLE_CQ_PMU_COUNTING: Enable CQ PMU counting. Must be asserted to count CQ events, or pass EG or WC events.
55	RW	CQ_TRACE_INT_DATA_LO: Select Lower(0:43) or Upper(44:87) Half of CQ trace data for bits 0:43.
56	RW	CQ_TRACE_INT_DATA_HI: Select Lower(0:43) or Upper(44:87) Half of CQ trace data for bits 44:87.
57	RW	WC_TRACE_INT_TRIG_01: Select Lower(0:1) or Upper(2:3) Half of WC trace triggers for bits 0:1.
58	RW	WC_TRACE_INT_TRIG_23: Select Lower(0:1) or Upper(2:3) Half of WC trace triggers for bits 2:3.
59	RW	EG_TRACE_INT_TRIG_01: Select Lower(0:1) or Upper(2:3) Half of EG trace triggers for bits 0:1.
60	RW	EG_TRACE_INT_TRIG_23: Select Lower(0:1) or Upper(2:3) Half of EG trace triggers for bits 2:3.
61	RW	CQ_TRACE_INT_TRIG_01: Select Lower(0:1) or Upper(2:3) Half of CQ trace triggers for bits 0:1.
62	RW	CQ_TRACE_INT_TRIG_23: Select Lower(0:1) or Upper(2:3) Half of CQ trace triggers for bits 2:3.
63	RO	constant = 0b0

Register Name	Processor Bus Configuration 0 Register
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PBCFG0
Address	000000000301184D (SCOM)
Description	Processor bus Configuration 0

Bits	SCOM	Field Mnemonic: Description
0:6	RW	PBCFG_0_EPSILON: Epsilon configuration value.
7:10	RW	PBCFG_0_HANG_POLL_MAX_CNT: CQ SCOM hang poll maximum count.
11:14	RW	PBCFG_0_UNUSED1: CQ Unused Controls.
15:18	RW	PBCFG_0_HANG_NX_MAX_CNT: CQ SCOM hang NX maximum count.
19	RW	PBCFG_0_DISABLE_WR_RD_PUSH: Disable write-read-push protocol.
20	RW	PBCFG_0_INJ_CE: Inject correctable error (CE) into PBCQ arrays.
21	RW	PBCFG_0_INJ_UE: Inject uncorrectable error (UE) into PBCQ arrays.
22	RW	PBCFG_0_INJ_SUE: Inject special uncorrectable error (SUE) into PBCQ arrays.
23	RW	PBCFG_0_INJ_ARRAY_SEL: Select array for error injection: 0 = CRA0 1 = CRA1
24	RW	PBCFG_0_INJ_FREQ: Error injection frequency: 0 = inject once 1 = inject continuously
25:31	RW	PBCFG_0_UNUSED2: CQ unused controls.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Processor Bus Configuration 1 Register
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_PBCFG1
Address	000000000301184E (SCOM)
Description	processor bus Configuration 1

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_LN_WR: Disable Ln write.
1	RW	DISABLE_G_WR: Disable G write.
2	RW	DISABLE_VG_WR: Disable Vg write.
3	RW	DISABLE_NN_WR: Disable Nn Rn write.
4	RW	DISABLE_LN_RD: Disable Ln read.
5	RW	DISABLE_G_RD: Disable G read.
6	RW	DISABLE_VG_RD: Disable Vg read.
7	RW	DISABLE_NN_RD: Disable Nn Rn read.
8:11	RW	PBCFG_1_UNUSED1: CQ VACQ unused configuration bits.
12	RW	RD_GO_M_QOS: Quality of Service bit for rd_go_m commands.
13	RW	ADDR_BAR_MODE: Addr_bar_mode: 0 = for large system address map 1 = for small system address map
14	RW	SKIP_G: Scope mode control when chip equals group.
15	RW	HANG_SM_ON_ARE: Hang state machine when address error combined response received.
16	RW	HANG_SM_ON_LINK_FAIL: Hang state machine when link fail combined response received.
17	RW	CFG_PUMP_MODE: Random backoff control.
18	RW	DMA_WR_NOT_INJ: When set, do not issue cl_dma_inj. Issue cl_dma_w.
19	RW	DMA_PART_WR_NOT_INJ: When set do not issue dma_pr_injj. Issue dma_pr_w.
20:27	RW	DMA_RD_VG_RST_TMASK: Mask to control when to reset read Vg scope predictor.
28:35	RW	DMA_WR_VG_RST_TMASK: Mask to control when to reset write Vg scope predictor.
36:51	RW	PBCFG_1_UNUSED2: CQ VACQ unused configuration bits.
52:63	RO	constant = 0b000000000000

Register Name	Miscellaneous Status and South Control Register
Mnemonic	VA.VA_SOUTH.VA_EG.EG_SCF.VAS_SOUTHCTL
Address	000000000301184F (SCOM)
Description	Miscellaneous Status and South Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SOUTH_CTL_DISABLE_WC_SCRUB: Disables the window cache scrubbing when this bit is asserted.
1	RW	SOUTH_CTL_DISABLE_WC_ECC: Disables the window cache ECC correction when this bit is asserted.
2	RW	SOUTH_CTL_EG_SINGLE_THREAD: Single thread all paste commands in EG when this bit is asserted.
3	RW	SOUTH_CTL_EG_WM_CTX_UPDATE_MODE: EG write monitor context update mode. Skips updating some fields when this bit is asserted.

Bits	SCOM	Field Mnemonic: Description
4	RW	SOUTH_CTL_EG_STAMP_DEBUG: EG stamp debug mode. Injects buffer number to stamp payload.
5	RW	SOUTH_CTL_EN_FAST_SCRUB: Enables fast scrub of window cache arrays: 0 = normal scrub 1 = continuous scrubbing.
6	RW	SOUTH_CTL_DIS_SIMULT_RD_WR: Disables simultaneous read and write in window cache arrays: 0 = normal operation 1 = non-overlapping read and writes
7	RW	SOUTH_CTL_ENA_NOTIFY_ORDER: Enables notification ordering within CQ.
8	ROX	SOUTH_CTL_WC_IDLE_BIT: Window cache (WC) logic is idle. This bit is read-only. It is set by the hardware.
9	ROX	SOUTH_CTL_CQ_IDLE_BIT: Common queue (CQ) logic is idle. This bit is read-only. It is set by the hardware.
10	ROX	SOUTH_CTL_EG_IDLE_BIT: Egress (EG) logic is idle. This bit is read-only. It is set by the hardware.
11:15	RW	SOUTH_CTL_UNUSED: Unused bits.
16:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	Configuration of CC Counters Register
Mnemonic	TP.TCN1.N1.SYNC_CONFIG
Address	0000000003030000 (SCOM)
Description	configuration of CC counters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay incoming SYNC pulse. Default are eight latches: ASYNC 0000 = 8 0001 = 2 0010 = 3 0011 = 4 0100 = 5 0101 = 6 0110 = 7 0111 = 8 1000 = 9 1001 = 10 1010 = 11 1011 = 12 1100 = 13 1101 = 14 1110 = 15 1111 = 16 delay of the reset of the phase counter
4	RW	LISTEN_TO_SYNC_PULSE_DIS: Disables phase counter synchronization by the sync_pulse signal (default is enabled). Note: When you enable listen_to_sync, the chiplet is corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: Default is 0. When set to 1, the alternative input of the sync_pulse is used. Note: When you toggle the input select, the chiplet is corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: When set, use the OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the chiplet_is_aligned bit.
8	RW	UNIT_REGION_CLKCMD_ENABLE: Enables the unit interface to start/stop one dedicated region. Used for POWER9 cache or core.

Bits	SCOM	Field Mnemonic: Description
9	RW	DISABLE_PCB_ITR: Disables the interrupt generation within CC. The interrupt is sent on each HLD event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enables the VITL align check to compare alignment of the incoming SYNC pulse with 2:1 VITL LCB.
11	RW	SYNC_PULSE_OUT_DIS: Disables the sync_pulse output when set to 1. The master chiplet does not send SYNC pulses to slave chiplets.
12:19	RW	UNUSED1219: Unused.

Register Name	OPCG Align Register
Mnemonic	TP.TCN1.N1.OPCG_ALIGN
Address	0000000003030001 (SCOM)
Description	OPCG ALIGN

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment: 0: none 1: 2:1 2: 3:1 3: 4:1 4: 6:1 5: 8:1 6: 12:1 7: 16:1 8: 24:1 9 - 15: 48:1
4:7	RW	SNOP_ALIGN: SNOP phase alignment: 0: none 1: 2:1 2: 3:1 3: 4:1 4: 6:1 5: 8:1 6: 12:1 7: 16:1 8: 24:1 9 - 15: 48:1
8:11	RW	ENOP_ALIGN: ENOP phase alignment: 0: none 1: 2:1 2: 3:1 3: 4:1 4: 6:1 5: 8:1 6: 12:1 7: 16:1 8: 24:1 9 - 15: 48:1
12:19	RW	INOP_WAIT: INOP cycle delay (0 - 255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0 - 4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0 - 255).
40	RW	INOP_FORCE_SG: INOP: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: SNOP: Set SG high during SNOP.

Bits	SCOM	Field Mnemonic: Description
42	RW	ENOP_FORCE_SG: ENOP: Set SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: When set to 0, a clock change request first waits on the OPCG_WAIT cycles. When set to 1, a clock change request does not wait, when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0: Use the INOPA setting from opcg_reg0 1: Use the rising edge of SYNC pulse 2: Use unit0_sync_lvl to align (for AVP - refresh0) 3: Use unit1_sync_lvl to align (for AVP - refresh1)
46	RW	UNUSED46: Unused.
47:51	RW	SCAN_RATIO: scan_ratio: n = 0 - 15: (n + 1):1 16: 24:1 17: 32:1 18: 48:1 19: 64:1 20: 128:1 Default 4:1 = 00011
52:63	RW	OPCG_WAIT_CYCLES: Old PAD value. Delay at the beginning and end of the OPCG run to allow DC signals to arrive at the correct time (0 4095). Required to be higher than plat depth. Default = 0x020.

Register Name	OPCG Control Register 0
Mnemonic	TP.TCN1.N1.OPCG_REG0
Address	0000000003030002 (SCOM)
Description	OPCG Control Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST mode used for LBIST 1 = RUNN mode used for ABIST/IOBIST
1	RWX	OPCG_GO: OPCG go (start OPCG). Bit is cleared when OPCG is done, Poll for opcg_done in cplt_start reg.
2	RWX	RUN_SCAN0: Run scan0. Overrides all BIST mode settings except the scan_ratio. Starts a scan0 run. The bit is cleared when OPCG is finished. Poll for opcg_done in the cplt_start register.
3	RW	SCAN0_MODE: Sets PRPGs in scan0_mode but does not run the automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, OPCG waits for the master chiplet to start. When Keep_MS_Mode is 0, SLAVE_MODE is cleared after the incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, OPCG sends out a trigger to all slave chiplets. When Keep_MS_MODE = 0, the MASTER_MODE is cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, OPCG in M/S mode bits are not cleared after one incoming OPCG trigger. Default is clear M/S mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: Unit pin used for AVP that can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: Unit pin used for AVP that can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types. Clears the chiplet.
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run SCAN0 on all regions and types. Clears the chiplet at all exclude PLL regions where the PLL is running.
11	RW	RUN_OPCG_ON_UPDATE_DR: Starts the OPCG engine when scan updated (update_dr) is received (set pulse). Cronus requires that this bit be set to 1 for a SETPULSE write.

Bits	SCOM	Field Mnemonic: Description
12	RW	RUN_OPCG_ON_CAPTURE_DR: Starts the OPCG engine when scan updated (update_dr) is received (set pulse). Cronus requires that this bit be set to 1 for a SETPULSE read.
13	RW	STOP_RUNN_ON_XSTOP: RUNN mode. Stops run-n on checkstop.
14	RW	OPCG_STARTS_BIST: RUNN mode. OPCG engine controls start_bist for ABIST or IOBIST.
15:20	RW	UNUSED1520: Unused.
21:63	RWX	LOOP_COUNT: Loop counter for LBIST and RUNN. Write = target value. Read = current counter value. Counts from zero to the target value.

Register Name	**OPCG Control Register 1**
Mnemonic	TP.TCN1.N1.OPCG_REG1
Address	0000000003030003 (SCOM)
Description	OPCG Control Register 1

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0 – 4095). runn-mode: start_bist match value (0:11).
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture. runn-mode: start_bist match value (12:23).
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture. runn-mode: start_bist match value (24:35).
36:47	RW	MISR_INIT_WAIT: BIST mode: Delay MISR aperture. MISRs get active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG creates only even and not odd clocks. Used for runn to create only one clock in fast domain. Default is 0.
49	RW	SCAN_CLK_USE_EVEN: Generates scan clock in even cycles instead of odd. Default is 0 = odd for scan.
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: Forces rtim_thold low when not in test_dc mode (must be 0 at all times).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0. Prevents activation of ARY HLD during NSL-fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0. Holds SG high during NSL-fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode. 00: Enables skitter during lbist_ip. 01: Enables skitter when misr_active. 10: skitter OPCG_GO mode. Falling edge = start; rising edge = stop. 11: Unused.
57	RW	MISR_MODE: BIST mode: MISR aperture mode. 0: a - 1 to b - 1 1: Start to a and b to end
58	RW	INFINITE_MODE: Infinite mode. RUNN and LBIST run forever and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode. NSL-fill count (0 - 31).

Register Name	**OPCG Control Register 2**
Mnemonic	TP.TCN1.N1.OPCG_REG2
Address	0000000003030004 (SCOM)
Description	OPCG Control Register 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: OPCG go for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2 1/4 1/8 1/16 1/2 3/4 7/8 15/16
4:15	RWX	PRPG_VALUE: Set to 0 for PRPG always on, else seed.
16:27	RW	PRPG_A_VAL: a value for PRPG aperture.

Bits	SCOM	Field Mnemonic: Description
28:39	RW	PRPG_B_VAL: b value for PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode: 0: a - 1 to b - 1 1: Start to a and b to end
41:63	RW	UNUSED41_63: Unused.

Register Name	Scan Region and Type Register
Mnemonic	TP.TCN1.N1.SCAN_REGION_TYPE
Address	0000000003030005 (SCOM)
Description	Scan Region and Type

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: Default is 0. When set to 1, the MASK bits in the CMSK chain decide which part is scanned or scan0. MASK = 1: scan0. MASK = 0: Part or scan chain
1:2	RO	constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region VITL (Vital = Clock).
4	RWX	SCAN_REGION_PERV: Scan clock region PERV (Pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region MCD.
6	RWX	SCAN_REGION_UNIT2: Scan clock region VA - VAS.
7	RWX	SCAN_REGION_UNIT3: Scan clock region PBIOO0 - PB.
8	RWX	SCAN_REGION_UNIT4: Scan clock region PBIOO1 - PB.
9	RWX	SCAN_REGION_UNIT5: Scan clock region MCS23 - MCU.
10	RWX	SCAN_REGION_UNIT6: Scan clock region unused.
11	RWX	SCAN_REGION_UNIT7: Scan clock region unused.
12	RWX	SCAN_REGION_UNIT8: Scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: Scan clock region unused.
14	RWX	SCAN_REGION_UNIT10: Scan clock region reserved.
15:47	RO	constant = 0b00000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain FUNC (functional).
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configuration and debug configuration).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain CCFG/GPTR (Pervasive: CC configuration. Others: GPTR).
51	RW	SCAN_TYPE_REGF: Scan chain regf (register files).
52	RW	SCAN_TYPE_LBIST: Scan chain lbst (LBIST).
53	RW	SCAN_TYPE_ABIST: Scan chain abst (ABIST).
54	RW	SCAN_TYPE_REPR: Scan chain repr (array repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (array timing).
56	RW	SCAN_TYPE_BNDY: Scan chain bndy (boundary I/Os).
57	RW	SCAN_TYPE_FARR: Scan chain farr (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain cmsk (LBIST channel mask).

Bits	SCOM	Field Mnemonic: Description
59	RW	SCAN_TYPE_INEX: Scan chain index (c14 ASIC).
60:63	RO	constant = 0b0000

Register Name	Start/Stop of Clocks Register
Mnemonic	TP.TCN1.N1.CLK_REGION
Address	0000000003030006 (SCOM)
Description	This register starts and stops the clocks.

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00 = NOP 01 = Start 10 = Stop 11 = Pulse (one pulse)
2	RWX	SLAVE_MODE: When selected, the clock command waits for the master chiplet to start. The bit is cleared after the incoming slave trigger and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: When selected, the clock command sends out a trigger to all slave chiplets. The bit is cleared after sending out one master trigger and Keep_MS_Mode_after_trigger is set to 0.
4	RWX	CLOCK_REGION_PERV: For clock region perv (Pervasive).
5	RWX	CLOCK_REGION_UNIT1: For clock region MCD.
6	RWX	CLOCK_REGION_UNIT2: For clock region VA - VAS.
7	RWX	CLOCK_REGION_UNIT3: For clock region PBIOO0 - PB.
8	RWX	CLOCK_REGION_UNIT4: For clock region PBIOO1 - PB.
9	RWX	CLOCK_REGION_UNIT5: For clock region MCS23 - MCU.
10	RWX	CLOCK_REGION_UNIT6: For clock region unused.
11	RWX	CLOCK_REGION_UNIT7: For clock region unused.
12	RWX	CLOCK_REGION_UNIT8: For clock region unused.
13	RWX	CLOCK_REGION_UNIT9: For clock region unused.
14	RWX	CLOCK_REGION_UNIT10: For clock region reserved.
15:47	RO	constant = 0b00000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Selects SL holds.
49	RWX	SEL_THOLD_NSL: select NSL holds.
50	RWX	SEL_THOLD_ARY: select array holds.
51	RO	constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support. Default for pulse is ODD phase. When this bit is set, the pulse is applied on the even phase.
53:63	RO	constant = 0b00000000000

Register Name	Clocks Running SL Register
Mnemonic	TP.TCN1.N1.CLOCK_STAT_SL
Address	0000000003030008 (SCOM)
Description	This register runs the SL.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: Status of PERV SL HLD. 0 = run 1 = stop
5	ROX	CLOCK_STATUS_UNIT1_SL: Status of MCD SL HLD. 0 = run 1 = stop
6	ROX	CLOCK_STATUS_UNIT2_SL: Status of VA - VAS SL HLD. 0 = run 1 = stop
7	ROX	CLOCK_STATUS_UNIT3_SL: status of PBIOO0 - PB SL HLD 0 = run 1 = stop
8	ROX	CLOCK_STATUS_UNIT4_SL: Status of PBIOO1 - PB SL HLD 0 = run 1 = stop
9	ROX	CLOCK_STATUS_UNIT5_SL: Status of MCS23 - MCU SL HLD 0 = run 1 = stop
10	ROX	CLOCK_STATUS_UNIT6_SL: Status of unused SL HLD. 0 = run 1 = stop
11	ROX	CLOCK_STATUS_UNIT7_SL: Status of unused SL HLD. 0 = run 1 = stop
12	ROX	CLOCK_STATUS_UNIT8_SL: Status of unused SL HLD. 0 = run 1 = stop
13	ROX	CLOCK_STATUS_UNIT9_SL: Status of unused SL HLD. 0 = run 1 = stop
14	ROX	CLOCK_STATUS_UNIT10_SL: Status of reserved SL HLD. 0 = run 1 = stop
15:63	RO	constant = 0b111111111111111111111111111111111111111111111111111111111

Register Name	Clocks Running NSL Register
Mnemonic	TP.TCN1.N1.CLOCK_STAT_NSL
Address	0000000003030009 (SCOM)
Description	This register runs the NSL.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: Status of PERV NSL HLD. 0 = run 1 = stop
5	ROX	CLOCK_STATUS_UNIT1_NSL: Status of MCD NSL HLD. 0 = run 1 = stop
6	ROX	CLOCK_STATUS_UNIT2_NSL: Status of VA - VAS NSL HLD. 0 = run 1 = stop
7	ROX	CLOCK_STATUS_UNIT3_NSL: status of PBIOO0 - PB NSL HLD 0 = run 1 = stop
8	ROX	CLOCK_STATUS_UNIT4_NSL: Status of PBIOO1 - PB NSL HLD 0 = run 1 = stop
9	ROX	CLOCK_STATUS_UNIT5_NSL: Status of MCS23 - MCU NSL HLD 0 = run 1 = stop
10	ROX	CLOCK_STATUS_UNIT6_NSL: Status of unused NSL HLD. 0 = run 1 = stop
11	ROX	CLOCK_STATUS_UNIT7_NSL: Status of unused NSL HLD. 0 = run 1 = stop
12	ROX	CLOCK_STATUS_UNIT8_NSL: Status of unused NSL HLD. 0 = run 1 = stop
13	ROX	CLOCK_STATUS_UNIT9_NSL: Status of unused NSL HLD. 0 = run 1 = stop
14	ROX	CLOCK_STATUS_UNIT10_NSL: Status of reserved NSL HLD. 0 = run 1 = stop
15:63	RO	constant = 0b11111111111111111111111111111111111111111111111111111111

Register Name	Clocks Running Array Register
Mnemonic	TP.TCN1.N1.CLOCK_STAT_ARY
Address	000000000303000A (SCOM)
Description	This register runs the array.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: Status of PERV ARY HLD. 0 = run 1 = stop

Bits	SCOM	Field Mnemonic: Description
5	ROX	CLOCK_STATUS_UNIT1_ARY: Status of MCD ARY HLD. 0 = run 1 = stop
6	ROX	CLOCK_STATUS_UNIT2_ARY: Status of VA - VAS ARY HLD. 0 = run 1 = stop
7	ROX	CLOCK_STATUS_UNIT3_ARY: status of PBIOO0 - PB ARY HLD 0 = run 1 = stop
8	ROX	CLOCK_STATUS_UNIT4_ARY: Status of PBIOO1 - PB ARY HLD 0 = run 1 = stop
9	ROX	CLOCK_STATUS_UNIT5_ARY: Status of MCS23 - MCU ARY HLD 0 = run 1 = stop
10	ROX	CLOCK_STATUS_UNIT6_ARY: Status of unused ARY HLD. 0 = run 1 = stop
11	ROX	CLOCK_STATUS_UNIT7_ARY: Status of unused ARY HLD. 0 = run 1 = stop
12	ROX	CLOCK_STATUS_UNIT8_ARY: Status of unused ARY HLD. 0 = run 1 = stop
13	ROX	CLOCK_STATUS_UNIT9_ARY: Status of unused ARY HLD. 0 = run 1 = stop
14	ROX	CLOCK_STATUS_UNIT10_ARY: Status of reserved ARY HLD. 0 = run 1 = stop
15:63	RO	constant = 0b11111111111111111111111111111111111111111111111111111

Register Name	**ABIST and IOBIST Per Region Register**
Mnemonic	TP.TCN1.N1.BIST
Address	0000000003030008 (SCOM)
Description	ABIST and IOBIST per region

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this bit 0 during ABIST/IOBIST. Can be used to bypass the RUNN start. When this bit is set, the BIST_START_TEST goes high immediately without waiting for RUNN. BIST starts with the first HLD clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: Selects the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: Selects the ABIST engines for eDRAMs.
3	RW	TC_IOBIST_MODE_DC: Selects the IOBIST engines.
4	RW	BIST_PERV: Region PERV: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run

Bits	SCOM	Field Mnemonic: Description
5	RW	BIST_UNIT1: Region MCD: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
6	RW	BIST_UNIT2: Region VA - VAS: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
7	RW	BIST_UNIT3: Region PBIOO0 - PB: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
8	RW	BIST_UNIT4: Region PBIOO1 - PB: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
9	RW	BIST_UNIT5: Region MCS23 - MCU: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
10	RW	BIST_UNIT6: Region unused: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
11	RW	BIST_UNIT7: Region unused: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
12	RW	BIST_UNIT8: Region unused: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
13	RW	BIST_UNIT9: Region unused: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
14	RW	BIST_UNIT10: Region reserved: 1 = BIST_START_TEST for this region is triggered 0 = Region not part of the ABIST/IOBIST run
15:47	RO	constant = 0b00000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: Enables strobe window only in TE = 1 mode OPCGGO tester pin enables ABIST compare when ABIST is started. Special setup in ABIST engine is required. Default = 0. System mode cannot enable this feature.
49:63	RO	constant = 0b000000000000000

Register Name	Checkstop Per Region 1 Register
Mnemonic	TP.TCN1.N1.XSTOP1
Address	000000000303000C (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: Mask for checkstop to clockstop of select regions (see XSTOP_perv, xstop_unit0..n). 0 = ignore checkstop 1 = stop on checkstop
1	RW	XSTOP1_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP1: Triggers OPCG on checkstop instead of performing clockstop.

Bits	SCOM	Field Mnemonic: Description
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, checkstop waits independent from flush. Default is no wait when flush in not set.
4	RW	XSTOP1_PERV: Region PERV: 1 = region is stopped 0 = region keeps running on checkstop
5	RW	XSTOP1_UNIT1: Region MCD: 1 = region is stopped 0 = region keeps running on checkstop
6	RW	XSTOP1_UNIT2: Region VA - VAS: 1 = region is stopped 0 = region keeps running on checkstop
7	RW	XSTOP1_UNIT3: Region PBIOO0 - PB: 1 = region is stopped 0 = region keeps running on checkstop
8	RW	XSTOP1_UNIT4: Region PBIOO1 - PB: 1 = region is stopped 0 = region keeps running on checkstop
9	RW	XSTOP1_UNIT5: Region MCS23 - MCU: 1 = region is stopped 0 = region keeps running on checkstop
10	RW	XSTOP1_UNIT6: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
11	RW	XSTOP1_UNIT7: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
12	RW	XSTOP1_UNIT8: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
13	RW	XSTOP1_UNIT9: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
14	RW	XSTOP1_UNIT10: Region reserved: 1 = region is stopped 0 = region keeps running on checkstop
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP1_WAIT_CYCLES: Defines how many cycles checkstop waits after dropping flush before Tholds is dropped. 0 - 4095 cycles possible.
60:63	RO	constant = 0b0000

Register Name	**Checkstop Per Region 2 Register**
Mnemonic	TP.TCN1.N1.XSTOP2
Address	000000000303000D (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: Mask for checkstop to clockstop of select regions (see XSTOP_perv, xstop_unit0..n). 0 = ignore checkstop 1 = stop on checkstop
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: Triggers OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: When set to 1, checkstop waits independent from flush. Default is no wait when flush in not set.
4	RW	XSTOP2_PERV: Region PERV: 1 = region is stopped 0 = region keeps running on checkstop
5	RW	XSTOP2_UNIT1: Region MCD: 1 = region is stopped 0 = region keeps running on checkstop
6	RW	XSTOP2_UNIT2: Region VA - VAS: 1 = region is stopped 0 = region keeps running on checkstop
7	RW	XSTOP2_UNIT3: Region PBIOO0 - PB: 1 = region is stopped 0 = region keeps running on checkstop
8	RW	XSTOP2_UNIT4: Region PBIOO1 - PB: 1 = region is stopped 0 = region keeps running on checkstop
9	RW	XSTOP2_UNIT5: Region MCS23 - MCU: 1 = region is stopped 0 = region keeps running on checkstop
10	RW	XSTOP2_UNIT6: Region unused: 1 = region is stopped 0 = region keeps running on checkstop

Bits	SCOM	Field Mnemonic: Description
11	RW	XSTOP2_UNIT7: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
12	RW	XSTOP2_UNIT8: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
13	RW	XSTOP2_UNIT9: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
14	RW	XSTOP2_UNIT10: Region reserved: 1 = region is stopped 0 = region keeps running on checkstop
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Defines how many cycles checkstop waits after dropping flush before Tholds is dropped. 0 - 4095 cycles possible.
60:63	RO	constant = 0b0000

Register Name	Checkstop Per Region Register 3
Mnemonic	TP.TCN1.N1.XSTOP3
Address	000000000303000E (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: Mask for Checkstop to clockstop of select regions (see XSTOP_perv, xstop_unit0..n). 0 = ignore checkstop 1 = stop on checkstop
1	RW	XSTOP3_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP3: Triggers OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, checkstop waits independent from flush. Default is no wait when flush in not set.
4	RW	XSTOP3_PERV: Region PERV: 1 = region is stopped 0 = region keeps running on checkstop
5	RW	XSTOP3_UNIT1: Region MCD: 1 = region is stopped 0 = region keeps running on checkstop
6	RW	XSTOP3_UNIT2: Region VA - VAS: 1 = region is stopped 0 = region keeps running on checkstop
7	RW	XSTOP3_UNIT3: Region PBIOO0 - PB: 1 = region is stopped 0 = region keeps running on checkstop
8	RW	XSTOP3_UNIT4: Region PBIOO1 - PB: 1 = region is stopped 0 = region keeps running on checkstop
9	RW	XSTOP3_UNIT5: Region MCS23 - MCU: 1 = region is stopped 0 = region keeps running on checkstop

Bits	SCOM	Field Mnemonic: Description
10	RW	XSTOP3_UNIT6: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
11	RW	XSTOP3_UNIT7: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
12	RW	XSTOP3_UNIT8: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
13	RW	XSTOP3_UNIT9: Region unused: 1 = region is stopped 0 = region keeps running on checkstop
14	RW	XSTOP3_UNIT10: Region reserved: 1 = region is stopped 0 = region keeps running on checkstop
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Defines how many cycles checkstop waits after dropping flush before Tholds is dropped. 0 - 4095 cycles possible.
60:63	RO	constant = 0b0000

Register Name	Error Status of CC Register
Mnemonic	TP.TCN1.N1.ERROR_STATUS
Address	000000000303000F (SCOM)
Description	This register shows the error status of CC.

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: Write on read-only register.
1	RWX	PCB_READ_NOT_ALLOWED_ERR: Read not allowed. Can be write-only register.
2	RWX	PCB_PARITY_ON_CMD_ERR: Parity error on CMD.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: Invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on ADDR.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: Protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on SPCIF.
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: PCB write while OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: Scan read when OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: Clock CMD in progress.
11	RWX	SCAN_COLLISION_ERR: Scan region selected of running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set scan region that is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG gets triggered while OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: Phase counters inside chiplet out of SYNC.
15	RWX	CLOCK_CMD_PREVENTED_ERR: Security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on OPCG state machine.

Bits	SCOM	Field Mnemonic: Description
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on Scan/Clock Region/Type or Clock Status Register.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG registers.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on SYNC Configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on checkstop register.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0, 4, 5, and 6 registers.
22	RWX	CLKCMD_REQUEST_ERR: Region CLKCMD has one request pending, but receives a second CLKCMD.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error. REQ/ACK sequence wrong.
24	RWX	VITL_ALIGN_ERR: VITL Alignment is out of SYNC-to-SYNC pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 SYNC LVL pulses are not in SYNC. AVP is broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on self-boot command state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	**OPCG Control Register Capture 1**
Mnemonic	TP.TCN1.N1.OPCG_CAPT1
Address	0000000003030010 (SCOM)
Description	OPCG Control Register Capture1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000 = 12 cycle 0001 - 1100 = cycle 1-12 1101-1111 = 24 normal, not fast.
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (SL, NSL, ARY, SE, FCE).

Register Name	OPCG Control Register Capture 2
Mnemonic	TP.TCN1.N1.OPCG_CAPT2
Address	0000000003030011 (SCOM)
Description	OPCG Control Register Capture 2

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2: Unused.
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1 (even) for fast region or cycle 13 for normal region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1 (odd) for fast region or cycle 14 for normal region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_15_02EVEN: Sequence cycle 2 (even) for fast region or cycle 15 for normal region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_16_02ODD: Sequence cycle 2 (odd) for fast region or cycle 16 for normal region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3 (even) for fast region or cycle 17 for normal region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3 (odd) for fast region or cycle 18 for normal region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4 (even) for fast region or cycle 19 for normal region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4 (odd) for fast region or cycle 20 for normal region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5 (even) for fast region or cycle 21 for normal region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5 (odd) for fast region or cycle 22 for normal region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6 (even) for fast region or cycle 23 for normal region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6 (odd) for fast region or cycle 24 for normal region (SL, NSL, ARY, SE, FCE).

Register Name	OPCG Control Register Capture 3
Mnemonic	TP.TCN1.N1.OPCG_CAPT3
Address	0000000003030012 (SCOM)
Description	OPCG Control Register Capture 3

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7 (even) for fast region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_07ODD: Sequence cycle 7 (odd) for fast region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_08EVEN: Sequence cycle 8 (even) for fast region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_08ODD: Sequence cycle 8 (odd) for fast region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_09EVEN: Sequence cycle 9 (even) for fast region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_09ODD: Sequence cycle 9 (odd) for fast region (SL, NSL, ARY, SE, FCE).

Bits	SCOM	Field Mnemonic: Description
34:38	RW	SEQ_10EVEN: Sequence cycle 10 (even) for fast region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_10ODD: Sequence cycle 10 (odd) for fast region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_11EVEN: Sequence cycle 11 (even) for fast region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_11ODD: Sequence cycle 11 (odd) for fast region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_12EVEN: Sequence cycle 12 (even) for fast region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12ODD: Sequence cycle 12 (odd) for fast region (SL, NSL, ARY, SE, FCE).

Register Name	Debug CBS CC Register
Mnemonic	TP.TCN1.N1.DBG_CBS_CC
Address	0000000003030013 (SCOM)
Description	Debug CBS CC Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset endpoint. CC and CTRL in reset state.
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped when enabled. Must have plat-depth cycles to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test enable.
4	ROX	DBG_CBS_REQ: CBS Interface - Request (latched).
5:7	ROX	DBG_CBS_CMD: CBS Interface - Command (latched).
8:12	ROX	DBG_CBS_STATE: CBS command state machine 00000 = idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS protocol error. REQ is raised, but state machine is not in IDLE. Must reset_ep to clear this bit. No impact on IPL.
15	ROX	DBG_PCB_IDLE: PCB interface in IDLE state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: Current/latest OPCG MODE: 0 = NOP 1 = LBIST 2 = ABIST 3 = RUNN 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN w CaptureDR 9 = CLK Change Request 10-15 = Unused
20:23	ROX	DBG_LAST_OPCG_MODE: Previous OPCG mode.
24	ROX	DBG_PCB_ERROR: PCB interface error. Read CC Error Register or set CBS_CMD = 001 to switch FSI CBS. Debug Information to CC error Register.
25	ROX	DBG_PARITY_ERROR: Any parity error, non-PCB parity. Read CC Error Register or set CBS_CMD = 001 to switch FSI CBS. Debug Information to CC error Register.
26	ROX	DBG_CC_ERROR: Any other CC error. Read CC Error Register or set CBS_CMD = 001 to switch FSI CBS. Debug Information to CC error Register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: Value is 1 when the a valid align pulse WS is sent out.

Bits	SCOM	Field Mnemonic: Description
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: Reset clears the bit. The first PCB request sets the bit.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: Rising or falling edge on test enable after reset. Must have reset_ep to clear, no impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on vitl_clkoff, after reset. Must have reset_ep to clear, no impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: Only representation of CC acknowledged signal going to FSI.

Register Name	CC Protect Mode Register
Mnemonic	TP.TCN1.N1.CC_PROTECT_MODE_REG
Address	00000000030303FE (SCOM)
Description	CC Protect Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enables read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enables write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCN1.N1.CC_ATOMIC_LOCK_REG
Address	00000000030303FF (SCOM)
Description	Atomic Lock Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	CC_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	Global Checkstop FIR Register
Mnemonic	TP.TCN1.N1.XFIR
Address	0000000003040000 (SCOM)
Description	Global checkstop FIR

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any checkstop).
1	RWX	XFIR_IN1: Checkstop broadcast using OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from pervasive unit.
4	RWX	XFIR_IN4: Checkstop from MCS23_0.
5	RWX	XFIR_IN5: Checkstop from MCS23_1.
6	RWX	XFIR_IN6: Checkstop from MCD0 FIR.

Bits	SCOM	Field Mnemonic: Description
7	RWX	XFIR_IN7: Checkstop from MCD1 FIR.
8	RWX	XFIR_IN8: Checkstop from VA FIR.
9	RWX	XFIR_IN9: Checkstop from PBIOO_0 FIRP.
10	RWX	XFIR_IN10: Checkstop from PBIOO_1 FIR.
11:25:00 AM	RWX	XFIR_IN11: Unused.
26	RWX	XFIR_IN26: Checkstop on debug trigger.

Register Name	Global Recoverable FIR Register
Mnemonic	TP.TCN1.N1.RFIR
Address	0000000003040001 (SCOM)
Description	Global recoverable FIR

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Unused.
1	ROX	LFIR_RECOV_ERR: Recoverable error from pervasive unit.
2	ROX	RFIR_IN4: Recoverable from MCS23_0.
3	ROX	RFIR_IN5: Recoverable from MCS23_1.
4	ROX	RFIR_IN6: Recoverable from MCD0 FIR.
5	ROX	RFIR_IN7: Recoverable from MCD1 FIR.
6	ROX	RFIR_IN8: Recoverable from VA FIR.
7	ROX	RFIR_IN9: Recoverable from PBIOO_0 FIR.
8	ROX	RFIR_IN10: Recoverable from PBIOO_1 FIR.
09:23:00 AM	ROX	RFIR_IN11: Unused.

Register Name	FIR Mask Register
Mnemonic	TP.TCN1.N1.FIR_MASK
Address	0000000003040002 (SCOM)
Description	FIR Mask

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR summary bit (any checkstop).
1	RW	FIR_MASK_IN1: Mask for XFIR bit received from other chiplets.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: Mask for XFIR from pervasive unit.
4	RW	FIR_MASK_IN4: Mask for MCS23_0 XFIR and RFIR.
5	RW	FIR_MASK_IN5: Mask for MCS23_1 XFIR and RFIR.
6	RW	FIR_MASK_IN6: Mask for MCD0 XFIR and RFIR.
7	RW	FIR_MASK_IN7: Mask for MCD1 XFIR and RFIR.

Bits	SCOM	Field Mnemonic: Description
8	RW	FIR_MASK_IN8: Mask for VA XFIR and RFIR.
9	RW	FIR_MASK_IN9: Mask for PBIOO_0 XFIR and RFIR.
10	RW	FIR_MASK_IN10: Mask for PBIOO_1 XFIR and RFIR.
11:25	RW	FIR_MASK_IN11: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local checkstop to recoverable error.

Register Name	Special Attention Register
Mnemonic	TP.TCN1.N1.SPATTN
Address	0000000003040004 (SCOM) 0000000003040005 (SCOM1) 0000000003040006 (SCOM2)
Description	Special Attention

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Special attention from MCS23_0.
1	ROX	NCX	NCX	SPATTN_IN1: Special attention from MCS23_1.
2	ROX	NCX	NCX	SPATTN_IN2: Special attention from MCD0.
3	ROX	NCX	NCX	SPATTN_IN3: Special attention from MCD1.
4:9	ROX	NCX	NCX	SPATTN_IN4: Unused special attentions.

Register Name	Special Attention Mask Register
Mnemonic	TP.TCN1.N1.SPA_MASK
Address	0000000003040007 (SCOM)
Description	Special Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	Mode Register
Mnemonic	TP.TCN1.N1.EPS.FIR.MODE_REG
Address	0000000003040008 (SCOM)
Description	Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop chip TOD on checkstop (unused in POWER9).
5	RW	MODE_IN5: Stop chip TOD on Recoverable (unused in POWER9).

Bits	SCOM	Field Mnemonic: Description
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enables checkstop on special attention.
9	RW	MODE_IN9: mask_direct/local_error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	**Host Attention Register**
Mnemonic	TP.TCN1.N1.HOSTATTN
Address	0000000003040009 (SCOM)
Description	Host Attention

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host Attention summary bit.
1	ROX	HOSTATTN_IN1: Host attention error from MCS23, bit 0.
2	ROX	HOSTATTN_IN2: Host attention error from MCS23, bit 1.
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	**Local FIR Register**
Mnemonic	TP.TCN1.N1.LOCAL_FIR
Address	000000000304000A (SCOM) 000000000304000B (SCOM1) 000000000304000C (SCOM2)
Description	Local FIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Errors from GPIO (PCB error).
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, and so on).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from thermal (trip error critical).
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from thermal (trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Thermal volt trip error.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from debug (SCOM error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from trace Array0 (SCOM error).
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Local errors from trace Array0.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Local errors from trace Array1 (SCOM error).
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Local errors from trace Array1.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: local errors from trace Array2 (SCOM error).
17	RWX	WOX_AND	WOX_OR	FIR_IN17: local errors from trace Array2.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: local errors from trace Array3 (SCOM error).
19	RWX	WOX_AND	WOX_OR	FIR_IN19: local errors from trace Array3.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: local errors from trace Array4 (SCOM error).
21	RWX	WOX_AND	WOX_OR	FIR_IN21: local errors from trace Array4.
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Unused.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Unused.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Errors from Bsense I/O.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Unused.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Unused.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Unused.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Unused.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Unused.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Unused.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Unused.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Unused.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Unused.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction alert broadcast using OOB.

Register Name	**Local FIR Mask Register**
Mnemonic	TP.TCN1.N1.EPS.FIR.LOCAL_FIR_MASK
Address	000000000304000D (SCOM) 000000000304000E (SCOM1) 000000000304000F (SCOM2)
Description	Local FIR Mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for LEM error-collection vector.

Register Name	**Local FIR Action0 Register**
Mnemonic	TP.TCN1.N1.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000003040010 (SCOM)
Description	Local FIR Action0

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: Action0 mask.

Register Name	**Local FIR Action1 Register**
Mnemonic	TP.TCN1.N1.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000003040011 (SCOM)
Description	Local FIR Action1

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: Action1 mask.

Register Name	Group Checkstop Mask Register
Mnemonic	TP.TCN1.N1.EPS.FIR.GXSTOP_TRIG_REG
Address	0000000003040013 (SCOM)
Description	Group Checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for type-4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group0 Checkstop Mask Register
Mnemonic	TP.TCN1.N1.EPS.FIR.GXSTOP0_MASK_REG
Address	0000000003040014 (SCOM)
Description	Group0 Checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for recoverable error
2	RW	GXSTP0_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for YYPE 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group1 Checkstop Mask Register
Mnemonic	TP.TCN1.N1.EPS.FIR.GXSTOP1_MASK_REG
Address	0000000003040015 (SCOM)
Description	Group1 Checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for type-4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP1_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group2 Checkstop Mask Register
Mnemonic	TP.TCN1.N1.EPS.FIR.GXSTOP2_MASK_REG
Address	0000000003040016 (SCOM)
Description	Group2 Checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for OOB sys_checkstop input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for OOB sys_checkstop input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	Summary Mask Register
Mnemonic	TP.TCN1.N1.EPS.FIR.SUM_MASK_REG
Address	0000000003040017 (SCOM)
Description	Summary Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type4 host attention summary bit.

Register Name	Local Checkstop Register
Mnemonic	TP.TCN1.N1.LOCAL_XSTOP_ERR
Address	0000000003040018 (SCOM)
Description	Local Checkstop

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit.
1	ROX	LOCAL_XSTOP_IN1: Local checkstop from MCS23, bit 0.
2	ROX	LOCAL_XSTOP_IN2: Local checkstop from MCS23, bit 1.
3	ROX	LOCAL_XSTOP_IN3: Unused.
4	ROX	LOCAL_XSTOP_IN4: Local checkstop from VA.
5	ROX	LOCAL_XSTOP_IN5: Unused.
6	ROX	LOCAL_XSTOP_IN6: Unused.
7	ROX	LOCAL_XSTOP_IN7: Unused.
8	ROX	LOCAL_XSTOP_IN8: Unused.
9	ROX	LOCAL_XSTOP_IN9: Unused.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.

Bits	SCOM	Field Mnemonic: Description
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask Register
Mnemonic	TP.TCN1.N1.LOCAL_XSTOP_MASK
Address	0000000003040019 (SCOM)
Description	Local Checkstop Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask Register
Mnemonic	TP.TCN1.N1.HOSTATTN_MASK
Address	000000000304001A (SCOM)
Description	Host Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Thermal Sensor Loop1 Results Register
Mnemonic	TP.TCN1.N1.EPS.THERM.DTS_RESULT0
Address	0000000003050000 (SCOM)
Description	DTS Thermal Sensor loop1 Results

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results Register
Mnemonic	TP.TCN1.N1.EPS.THERM.DTS_TRC_RESULT
Address	0000000003050003 (SCOM)
Description	DTS Trace Results

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with ID 1.

Register Name	CPM and DTS Enables and Controls Register
Mnemonic	TP.TCN1.N1.EPS.THERM.THERM_MODE_REG
Address	000000000305000F (SCOM)
Description	CPM and DTS enables and controls

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: force tpc_therm_thres_mac clock gating off and activates clocks.
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables. 1xx: trip0 - warning. x1x: trip1 - critical. xx1: trip2 - fatal.
5	RW	THERM_DTS_SAMPLE_ENA: When set to 0, there is no DTS sampling. When set to 1, DTS sampling is enabled and below-counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz, sample pulse is fed into an 18-bit counter. With the therm_sample_pulse_cnt, it is possible to select a high-order bit of the counter to enable a resolutions of sampling DTSS between 2.5 us and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a DTS sample. 0000: 16 ms. 0001: 8 ms. 0010: 4 ms. 0011: 2 ms. 0100: 1 ms. 0101: 0.5 ms. 0110: 250 ms. 0111: 125 ms. 1000: 62 .5 ms. 1001: 31.3 ms. 1010: 15.6 ms. 1011: 7.8 ms. 1100: 3.9 ms. 1101: 2 ms. 1110: 1 ms. 1111: 0.5 ms.
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in threshold unit: 00: Off. 11: Illegal. 10: Maximum mode. 01: Minimum mode.
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: When set to 0, therm_overflow_err is enabled. When set to 1, therm_overflow_err will be disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result is provided with PCB read addr_v(4): 0000: DTS 0. 0001: DTS 1. 0010: DTS 2. 0100: DTS 4. 1111: Worst-case sensor.
20:21	RW	THERM_DTS_ENABLE_L1: Loop1 DTS enables: 1x: DTS 0 available. x1: DTS 1 available.

Bits	SCOM	Field Mnemonic: Description
22:34	RO	constant = 0b0000000000000
35:36	RW	Reserved field.

Register Name	Skitter Control Register
Mnemonic	TP.TCN1.N1.EPS.THERM.SKITTER_MODE_REG
Address	0000000003050010 (SCOM)
Description	Skitter Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold current sample.
1	RW	DISABLE_SKITTER_STICKINESS: When set to 0, accumulation mode. When set to 1, samples new value each cycle and resets the sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0: hold_on_trigger0. bit1: _on_trigger1.
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0: reset_sticky_on_trigger0. bit1: reset_sticky_on_trigger1.
8:9	RW	SKITTER_SAMPLE_GUTS: Selects guts to measure: 00: Guts1. 01: Guts2. 10: Guts3. 11: Guts4.
10:43	RO	constant = 0b00000000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold current sample on the debug trigger. This bit has the highest priority.
45	ROX	SKITTER_DATA_V_LT: When set to 1, the data requested by a skitter force read register has finished and data is present in the skitter data register in the collector macro. The data can be read by any combination of V25/V26/V27 PCB reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TCN1.N1.EPS.THERM.INJECT_REG
Address	0000000003050011 (SCOM)
Description	Error Injection Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00: no injection. 01: Warning trip level injection. 10: Critical trip level injection. 11: Fatal trip level injection.
2:3	RW	THERM_INJECT_MODE: 00: no injection. 01: Injection on the next DTS sample. 10: Solid injection for the next DTS samples till bit setting changes. 11: Not used.

Register Name	Control/Force Reset Register
Mnemonic	TP.TCN1.N1.EPS.THERM.CONTROL_REG
Address	0000000003050012 (SCOM)
Description	Control/Force Reset Register

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved field.
1	WO_1P	Reserved field.
2	WO_1P	Reserved field.
3	WO_1P	Reserved field.
4	WO_1P	Reserved field.
5	WO_1P	Reserved field.
6	WO_1P	Reserved field.
7	WO_1P	Reserved field.
8	WO_1P	Reserved field.
9	WO_1P	Reserved field.
10	WO_1P	Reserved field.
11	WO_1P	Reserved field.
12	WO_1P	Reserved field.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCN1.N1.EPS.THERM.ERR_STATUS_REG
Address	0000000003050013 (SCOM)
Description	Thermal Error Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Thermal Mode Register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter Mode Register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter Force Register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan INIT Version Register parity error mask.
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt Mode Register parity error mask.
22	RO	constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: Threshold state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Forces skitter read on the hot error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	constant = 0b00000000
40:43	ROX	Reserved field.
44:46	ROX	Reserved field.
47	ROX	Reserved field.
48	ROX	Reserved field.
49:50	ROX	Reserved field.
51:54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCN1.N1.EPS.THERM.SKITTER_FORCE_REG
Address	0000000003050014 (SCOM)
Description	Skitter Force Read Register

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter.

Register Name	Skitter Clock SRC Control Register
Mnemonic	TP.TCN1.N1.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000003050016 (SCOM)
Description	Skitter Clock SRC Control Register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects clock to measure: 000: Local mesh clock. 001: External pin skitter_c1_1_in. 010: Local d1clk only if d_mode = 1. 011: External pin skitter_c1_2_in. 100: Local lclk only if d_mode = 1. 101: External pin skitter_c1_3_in. 110: Unused. 111: External pin skitter_c1_4_in.
3:35	RO	constant = 0b00000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: Selects delay to be added between clock source multiplexer and inverter chain (base line delay is 12.2 ps) of skitter0. 00 - No delay. 01 - 0.6 ps. 10 - 1.8 ps. 11 - 5 ps.

Register Name	Skitter Data Register Read Bits 0:63 Register
Mnemonic	TP.TCN1.N1.EPS.THERM.SKITTER_DATA0
Address	0000000003050019 (SCOM)
Description	Skitter Data Register Read Bit0:63

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bits 32:95 Register
Mnemonic	TP.TCN1.N1.EPS.THERM.SKITTER_DATA1
Address	000000000305001A (SCOM)
Description	Skitter Data Register Read Bit32:95

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bits 64:127 Register
Mnemonic	TP.TCN1.N1.EPS.THERM.SKITTER_DATA2
Address	000000000305001B (SCOM)
Description	Skitter Data Register Read Bit 64:127

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Time-Stamp Counter Read Register
Mnemonic	TP.TCN1.N1.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000305001C (SCOM)
Description	Time-Stamp Counter Read

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.

7. PB Chiplet (Nest Chiplet 2)

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
CAPP1.CXA_TOP.APC_ERRINJ	0x0000000004010810	913
CAPP1.CXA_TOP.CXA_APC0.APCFG	0x0000000004010819	919
CAPP1.CXA_TOP.CXA_APC0.APCLCO	0x0000000004010821	922
CAPP1.CXA_TOP.CXA_APC0.APCRDFSMMASK	0x0000000004010823	922
CAPP1.CXA_TOP.CXA_APC0.APCTL	0x0000000004010818	917
CAPP1.CXA_TOP.CXA_APC0.FLUSHSHUE	0x000000000401080F	913
CAPP1.CXA_TOP.CXA_APC1.APC_ARRY_ADDR	0x000000000401082A	926
CAPP1.CXA_TOP.CXA_APC1.APC_ARRY_RDDATA	0x000000000401082B	926
CAPP1.CXA_TOP.CXA_APC1.APC_ARRY_WRDATA	0x0000000004010842	927
CAPP1.CXA_TOP.CXA_APC1.APC_PMUSEL	0x0000000004010816	917
CAPP1.CXA_TOP.CXA_APC1.DFSUOP1	0x0000000004010843	927
CAPP1.CXA_TOP.CXA_APC1.ERRRPT	0x000000000401080B	908
CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ARRAY_ADDR_REG	0x0000000004010828	925
CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ARRAY_READ_REG	0x0000000004010829	925
CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ARRAY_WRITE_REG	0x0000000004010841	927
CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_CAPI_CFG_REG	0x000000000401081A	919
CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_CNTL_REG	0x000000000401081B	920
CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ERROR_REPORT_REG	0x000000000401080A	908
CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_PHB_TTAG_FILTER_REG	0x0000000004010831	927
CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_PMU_EVENTS_SELECT_REG	0x0000000004010817	917
CAPP1.CXA_TOP.CXA_TRIGCTL	0x0000000004010812	915
CAPP1.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE0	0x0000000004010846	928
CAPP1.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE1	0x0000000004010847	928
CAPP1.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE2	0x0000000004010848	928
CAPP1.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE3	0x0000000004010849	929
CAPP1.CXA_TOP.CXA_XPT.XPT_EPT.CAPP_EPOCH_AND_RECOVERY_TMR_CONTROL	0x000000000401082C	926
CAPP1.CXA_TOP.CXA_XPT.XPT_EPT.CAPP_ERR_STATUS_CONTROL	0x000000000401080E	912
CAPP1.CXA_TOP.CXA_XPT.XPT_PMULET.PMU_CNTRA_REG	0x0000000004010815	916
CAPP1.CXA_TOP.CXA_XPT.XPT_PMULET.PMU_CNTRB_REG	0x0000000004010825	924
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.DEBUG_CONTROL	0x0000000004010811	914
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_ACTION0_REG	0x0000000004010806	908
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_ACTION1_REG	0x0000000004010807	908
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_MASK_REG	0x0000000004010803	905
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_REG	0x0000000004010800	903
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.PMU_CNTRA_CFG	0x0000000004010814	915
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.PMU_CNTRB_CFG	0x0000000004010824	923
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.TLBI_ERROR_REPORT	0x000000000401080D	912
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.XPT_CONTROL	0x000000000401081C	920
CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.XPT_PMU_EVENTS_SEL	0x0000000004010822	922
CAPP1.CXA_TOP.CXA_XPT.XPT_TOD.TFMR	0x0000000004010827	924
CAPP1.CXA_TOP.CXA_XPT.XPT_TOD.TOD_SYNC000	0x0000000004010826	924
CAPP1.CXA_TOP.ERR_RPT_CLR	0x0000000004010813	915

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PE0.PB0.PBCQ.PEPBREGS.DRPPRICTL_REG	0x0000000004010C01	931
PE0.PB0.PBCQ.PEPBREGS.NESTTRC_REG	0x0000000004010C03	932
PE0.PB0.PBCQ.PEPBREGS.PBCQEINJ_REG	0x0000000004010C02	932
PE0.PB0.PBCQ.PEPBREGS.PBCQHWCFG_REG	0x0000000004010C00	929
PE0.PB0.PBCQ.PEPBREGS.PECAPP_CNTL_REG	0x0000000004010C07	934
PE0.PB0.PBCQ.PEPBREGS.PMONCTL_REG	0x0000000004010C04	933
PE0.PB0.PBCQ.PEPBREGS.PREDV_REG	0x0000000004010C06	934
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.BARE_REG	0x0000000004010C54	939
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.CERR_RPT0_REG	0x0000000004010C4A	936
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.CERR_RPT1_REG	0x0000000004010C4B	936
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.CQSTAT_REG	0x0000000004010C4C	936
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.INTBAR_REG	0x0000000004010C53	938
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR0_MASK_REG	0x0000000004010C4F	937
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR0_REG	0x0000000004010C4E	937
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR1_MASK_REG	0x0000000004010C51	938
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR1_REG	0x0000000004010C50	938
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIRACTION0_REG	0x0000000004010C46	935
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIRACTION1_REG	0x0000000004010C47	935
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIRMASK_REG	0x0000000004010C43	935
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIRWOF_REG	0x0000000004010C48	936
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIR_REG	0x0000000004010C40	935
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.PBCQMODE_REG	0x0000000004010C4D	937
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.PE_DFREEZE_REG	0x0000000004010C55	939
PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.PHBBAR_REG	0x0000000004010C52	938
PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.BARE_REG	0x0000000004010C94	943
PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.CERR_RPT0_REG	0x0000000004010C8A	941
PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.CERR_RPT1_REG	0x0000000004010C8B	941
PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.CQSTAT_REG	0x0000000004010C8C	941
PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.INTBAR_REG	0x0000000004010C93	943
PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR0_MASK_REG	0x0000000004010C8F	942
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PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR1_MASK_REG	0x0000000004010C91	942
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PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.PHBBAR_REG	0x0000000004010C92	943
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PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.CERR_RPT0_REG	0x0000000004010CCA	945
PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.CERR_RPT1_REG	0x0000000004010CCB	946
PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.CQSTAT_REG	0x0000000004010CCC	946
PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.INTBAR_REG	0x0000000004010CD3	948
PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_MASK_REG	0x0000000004010CCF	947

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PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_REG	0x0000000004010CCE	946
PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_MASK_REG	0x0000000004010CD1	947
PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_REG	0x0000000004010CD0	947
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PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION1_REG	0x0000000004010CC7	945
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PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.NFIR_REG	0x0000000004010CC0	944
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PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.PE_DFREEZE_REG	0x0000000004010CD5	948
PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.PHBBAR_REG	0x0000000004010CD2	947
PE0.PB0.PBCQ.PEPBREGS.TUNNEL_BAR_REG	0x0000000004010C05	934
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PE1.PB1.PBCQ.PEPBREGS.PBCQEINJ_REG	0x0000000004011002	951
PE1.PB1.PBCQ.PEPBREGS.PBCQHWCFG_REG	0x0000000004011000	949
PE1.PB1.PBCQ.PEPBREGS.PECAPP_CNTL_REG	0x0000000004011007	954
PE1.PB1.PBCQ.PEPBREGS.PMONCTL_REG	0x0000000004011004	952
PE1.PB1.PBCQ.PEPBREGS.PREDV_REG	0x0000000004011006	953
PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.BARE_REG	0x0000000004011054	958
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PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.CERR_RPT1_REG	0x000000000401104B	956
PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.CQSTAT_REG	0x000000000401104C	956
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PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR0_MASK_REG	0x000000000401104F	957
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PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.CERR_RPT0_REG	0x000000000401108A	960
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PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR0_REG	0x000000000401108E	961
PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR1_MASK_REG	0x0000000004011091	962
PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR1_REG	0x0000000004011090	962
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PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.NFIRACTION1_REG	0x0000000004011087	959
PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.NFIRMASK_REG	0x0000000004011083	959

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PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.CERR_RPT1_REG	0x00000000040110CB	965
PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.CQSTAT_REG	0x00000000040110CC	965
PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.INTBAR_REG	0x00000000040110D3	967
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PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_REG	0x00000000040110CE	966
PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_MASK_REG	0x00000000040110D1	966
PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_REG	0x00000000040110D0	966
PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION0_REG	0x00000000040110C6	964
PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION1_REG	0x00000000040110C7	964
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PE1.PB1.PBCQ.PEPBREGS.TUNNEL_BAR_REG	0x0000000004011005	953
PE2.PB2.PBCQ.PEPBREGS.DRPPRICTL_REG	0x0000000004011401	970
PE2.PB2.PBCQ.PEPBREGS.NESTTRC_REG	0x0000000004011403	971
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PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.PHBBAR_REG	0x0000000004011492	981
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PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.CQSTAT_REG	0x00000000040114CC	984
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.INTBAR_REG	0x00000000040114D3	986
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_MASK_REG	0x00000000040114CF	985
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_REG	0x00000000040114CE	985
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PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_REG	0x00000000040114D0	985
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION0_REG	0x00000000040114C6	983
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION1_REG	0x00000000040114C7	983
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIRMASK_REG	0x00000000040114C3	983
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIRWOF_REG	0x00000000040114C8	983
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIR_REG	0x00000000040114C0	982
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.PBCQMODE_REG	0x00000000040114CD	984
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.PE_DFREEZE_REG	0x00000000040114D5	987
PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.PHBBAR_REG	0x00000000040114D2	986
PE2.PB2.PBCQ.PEPBREGS.TUNNEL_BAR_REG	0x0000000004011405	972
PSI.PSI.PSI_MAC.PSI_SCOM.FIR_ACTION0_REG	0x0000000004011806	988
PSI.PSI.PSI_MAC.PSI_SCOM.FIR_ACTION1_REG	0x0000000004011807	988
PSI.PSI.PSI_MAC.PSI_SCOM.FIR_MASK_REG	0x0000000004011803	987
PSI.PSI.PSI_MAC.PSI_SCOM.FIR_REG	0x0000000004011800	987
PSI.PSI.PSI_MAC.PSI_SCOM.FIR_WOF_REG	0x0000000004011808	988
PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.RX_PSI_CNTL	0x0000000004011820	988
PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.RX_PSI_MODE	0x0000000004011821	989
PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.RX_PSI_STATUS	0x0000000004011822	990
PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.TX_PSI_CNTL	0x0000000004011830	990
PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.TX_PSI_MODE	0x0000000004011831	991
PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.TX_PSI_STATUS	0x0000000004011832	992
TP.TCN2.N2.BIST	0x000000000403000B	999
TP.TCN2.N2.CC_ATOMIC_LOCK_REG	0x00000000040303FF	1007
TP.TCN2.N2.CC_PROTECT_MODE_REG	0x00000000040303FE	1007

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TP.TCN2.N2.CLK_REGION	0x0000000004030006	996
TP.TCN2.N2.CLOCK_STAT_ARY	0x000000000403000A	998
TP.TCN2.N2.CLOCK_STAT_NSL	0x0000000004030009	998
TP.TCN2.N2.CLOCK_STAT_SL	0x0000000004030008	997
TP.TCN2.N2.CPLT_CONF0	0x0000000004000008	875
TP.TCN2.N2.CPLT_CONF1	0x0000000004000009	876
TP.TCN2.N2.CPLT_CTRL0	0x0000000004000000	872
TP.TCN2.N2.CPLT_CTRL1	0x0000000004000001	874
TP.TCN2.N2.CPLT_MASK0	0x0000000004000101	878
TP.TCN2.N2.CPLT_STAT0	0x0000000004000100	877
TP.TCN2.N2.CTRL_ATOMIC_LOCK_REG	0x00000000040003FF	878
TP.TCN2.N2.CTRL_PROTECT_MODE_REG	0x00000000040003FE	878
TP.TCN2.N2.DBG_CBS_CC	0x0000000004030013	1006
TP.TCN2.N2.EPS.DBG.DBG_INST1_COND_REG_1	0x00000000040107C1	891
TP.TCN2.N2.EPS.DBG.DBG_INST1_COND_REG_2	0x00000000040107C2	893
TP.TCN2.N2.EPS.DBG.DBG_INST1_COND_REG_3	0x00000000040107C3	894
TP.TCN2.N2.EPS.DBG.DBG_INST2_COND_REG_1	0x00000000040107C4	895
TP.TCN2.N2.EPS.DBG.DBG_INST2_COND_REG_2	0x00000000040107C5	897
TP.TCN2.N2.EPS.DBG.DBG_INST2_COND_REG_3	0x00000000040107C6	898
TP.TCN2.N2.EPS.DBG.DBG_MODE_REG	0x00000000040107C0	890
TP.TCN2.N2.EPS.DBG.DBG_TRACE_MODE_REG_2	0x00000000040107CF	902
TP.TCN2.N2.EPS.DBG.DBG_TRACE_REG_0	0x00000000040107CD	899
TP.TCN2.N2.EPS.DBG.DBG_TRACE_REG_1	0x00000000040107CE	901
TP.TCN2.N2.EPS.FIR.GXSTOP0_MASK_REG	0x0000000004040014	1013
TP.TCN2.N2.EPS.FIR.GXSTOP1_MASK_REG	0x0000000004040015	1013
TP.TCN2.N2.EPS.FIR.GXSTOP2_MASK_REG	0x0000000004040016	1014
TP.TCN2.N2.EPS.FIR.GXSTOP_TRIG_REG	0x0000000004040013	1012
TP.TCN2.N2.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000004040010	1012
TP.TCN2.N2.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000004040011	1012
TP.TCN2.N2.EPS.FIR.LOCAL_FIR_MASK	0x000000000404000D	1012
TP.TCN2.N2.EPS.FIR.MODE_REG	0x0000000004040008	1009
TP.TCN2.N2.EPS.FIR.SUM_MASK_REG	0x0000000004040017	1014
TP.TCN2.N2.EPS.PSC.PSC.ADDR_TRAP_REG	0x0000000004010003	881
TP.TCN2.N2.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG	0x0000000004010007	882
TP.TCN2.N2.EPS.PSC.PSC.PSCOM_ERROR_MASK	0x0000000004010002	880
TP.TCN2.N2.EPS.PSC.PSC.PSCOM_MODE_REG	0x0000000004010000	879
TP.TCN2.N2.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG	0x0000000004010001	879
TP.TCN2.N2.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG	0x0000000004010008	882
TP.TCN2.N2.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG	0x0000000004010005	882
TP.TCN2.N2.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG	0x0000000004010006	882
TP.TCN2.N2.EPS.THERM.CONTROL_REG	0x0000000004050012	1018
TP.TCN2.N2.EPS.THERM.DTS_RESULT0	0x0000000004050000	1016
TP.TCN2.N2.EPS.THERM.DTS_TRC_RESULT	0x0000000004050003	1016
TP.TCN2.N2.EPS.THERM.ERR_STATUS_REG	0x0000000004050013	1019
TP.TCN2.N2.EPS.THERM.INJECT_REG	0x0000000004050011	1018
TP.TCN2.N2.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000004050016	1020
TP.TCN2.N2.EPS.THERM.SKITTER_DATA0	0x0000000004050019	1021
TP.TCN2.N2.EPS.THERM.SKITTER_DATA1	0x000000000405001A	1021

Mnemonic	Address	Page
TP.TCN2.N2.EPS.THERM.SKITTER_DATA2	0x000000000405001B	1021
TP.TCN2.N2.EPS.THERM.SKITTER_FORCE_REG	0x0000000004050014	1020
TP.TCN2.N2.EPS.THERM.SKITTER_MODE_REG	0x0000000004050010	1017
TP.TCN2.N2.EPS.THERM.THERM_MODE_REG	0x000000000405000F	1016
TP.TCN2.N2.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000405001C	1022
TP.TCN2.N2.ERROR_STATUS	0x000000000403000F	1003
TP.TCN2.N2.FIR_MASK	0x0000000004040002	1008
TP.TCN2.N2.HOSTATTN	0x0000000004040009	1010
TP.TCN2.N2.HOSTATTN_MASK	0x000000000404001A	1016
TP.TCN2.N2.LOCAL_FIR	0x000000000404000A	1010
TP.TCN2.N2.LOCAL_XSTOP_ERR	0x0000000004040018	1015
TP.TCN2.N2.LOCAL_XSTOP_MASK	0x0000000004040019	1015
TP.TCN2.N2.OPCG_ALIGN	0x0000000004030001	993
TP.TCN2.N2.OPCG_CAPT1	0x0000000004030010	1004
TP.TCN2.N2.OPCG_CAPT2	0x0000000004030011	1004
TP.TCN2.N2.OPCG_CAPT3	0x0000000004030012	1005
TP.TCN2.N2.OPCG_REG0	0x0000000004030002	994
TP.TCN2.N2.OPCG_REG1	0x0000000004030003	994
TP.TCN2.N2.OPCG_REG2	0x0000000004030004	995
TP.TCN2.N2.RFIR	0x0000000004040001	1008
TP.TCN2.N2.SCAN_REGION_TYPE	0x0000000004030005	995
TP.TCN2.N2.SPATTN	0x0000000004040004	1009
TP.TCN2.N2.SPA_MASK	0x0000000004040007	1009
TP.TCN2.N2.SYNC_CONFIG	0x0000000004030000	992
TP.TCN2.N2.TRA0.TR0.TRACE_HI_DATA_REG	0x0000000004010400	882
TP.TCN2.N2.TRA0.TR0.TRACE_LO_DATA_REG	0x0000000004010401	883
TP.TCN2.N2.TRA0.TR0.TRACE_TRCTRL_CONFIG	0x0000000004010402	883
TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x0000000004010403	883
TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x0000000004010404	884
TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_2	0x0000000004010405	884
TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x0000000004010406	884
TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x0000000004010407	884
TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x0000000004010408	885
TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x0000000004010409	885
TP.TCN2.N2.TRA0.TR1.TRACE_HI_DATA_REG	0x0000000004010440	886
TP.TCN2.N2.TRA0.TR1.TRACE_LO_DATA_REG	0x0000000004010441	887
TP.TCN2.N2.TRA0.TR1.TRACE_TRCTRL_CONFIG	0x0000000004010442	887
TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_0	0x0000000004010443	887
TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_1	0x0000000004010444	888
TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_2	0x0000000004010445	888
TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_3	0x0000000004010446	888
TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_4	0x0000000004010447	888
TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_5	0x0000000004010448	889
TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_9	0x0000000004010449	889
TP.TCN2.N2.XFIR	0x0000000004040000	1007
TP.TCN2.N2.XSTOP1	0x000000000403000C	1000
TP.TCN2.N2.XSTOP2	0x000000000403000D	1001
TP.TCN2.N2.XSTOP3	0x000000000403000E	1002

The POWER9 processor registers are listed in the following tables.

Register Name	Chiplet Control Register 0
Mnemonic	TP.TCN2.N2.CPLT_CTRL0
Address	0000000004000000 (SCOM) 0000000004000010 (SCOM1) 0000000004000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select the ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks are used from a chiplet with ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the synchronous clock for asynchronous latches. (The initial value is 1.)
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode. (The initial value is 1.)
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force an alignment signal to be sent. (The initial value is 1. Drop before dropping flushmode_inh.)
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set the array into write-through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: AVP mode. Switches from the refresh pulse to the phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC: Unused.
11	RW	WO_OR	WO_CLEAR	Reserved_11A: Reserved.
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC: Enables skitter to be used functionally during the BIST. When set to 1, the scan chain is bypassed and scan enable (SE) is degated.
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode. For example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of N1L latches. Prevents lock when switching SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC: Enables test-only logic and latches to increase the test coverage.
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	Reserved_18A: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
19	RW	WO_OR	WO_CLEAR	Reserved_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO selected.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INTEST instruction support (INT) mode for BSC. The IEEE 1149.1 INTEST instruction can be triggered through JTAG or through this register.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	Reserved_33A: Reserved.
34	RW	WO_OR	WO_CLEAR	Reserved_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	Reserved_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Enables delaying the alignment by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into flush state. Used for DFT only.
38	RW	WO_OR	WO_CLEAR	Reserved_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	Reserved_39A: Reserved.
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select. 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	Reserved_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	Reserved_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: Test enable (TE) = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM program mode.
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only. Sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. LBIST is controlled by PIN, and not by OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	**Chiplet Control Register 1**
Mnemonic	TP.TCN2.N2.CPLT_CTRL1
Address	0000000004000001 (SCOM) 0000000004000011 (SCOM1) 0000000004000021 (SCOM2)
Description	This register contains the second set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	Unused_0B: Unused.
1	RW	WO_OR	WO_CLEAR	Unused_1B: Unused.
2	RW	WO_OR	WO_CLEAR	Unused_2B: Unused.
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL fence. Protect the VITL region logic from pollution by other regions during LBIST, or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for the pervasive region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for region CXA1 to CAPP.
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for region PCI Slave 0 (PCIS0) to PCI.
7	RW	WO_OR	WO_CLEAR	TC_REGION3_FENCE: Fence for region PCI Slave 1 (PCIS1) to PCI.
8	RW	WO_OR	WO_CLEAR	TC_REGION4_FENCE: Fence for region PCI Slave 2 (PCIS2) to PCI.
9	RW	WO_OR	WO_CLEAR	Unused_9B: Unused.
10	RW	WO_OR	WO_CLEAR	Unused_10B: Unused.
11	RW	WO_OR	WO_CLEAR	Unused_11B: Unused.
12	RW	WO_OR	WO_CLEAR	Unused_12B: Unused.
13	RW	WO_OR	WO_CLEAR	Unused_13B: Unused.
14	RW	WO_OR	WO_CLEAR	Unused_14B: Unused.
15	RW	WO_OR	WO_CLEAR	Reserved_15B: Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE: Fence logic that is indeterminate at any frequency.
17	RW	WO_OR	WO_CLEAR	Unused_17B: Unused.
18	RW	WO_OR	WO_CLEAR	Unused_18B: Unused.
19	RW	WO_OR	WO_CLEAR	Unused_19B: Unused.
20	RW	WO_OR	WO_CLEAR	Unused_20B: Unused.
21	RW	WO_OR	WO_CLEAR	Unused_21B: Unused.
22	RW	WO_OR	WO_CLEAR	Unused_22B: Unused.
23	RW	WO_OR	WO_CLEAR	Unused_23B: Unused.
24	RW	WO_OR	WO_CLEAR	Unused_24B: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
25	RW	WO_OR	WO_CLEAR	Unused_25B: Unused.
26	RW	WO_OR	WO_CLEAR	Unused_26B: Unused.
27	RW	WO_OR	WO_CLEAR	Unused_27B: Unused.
28	RW	WO_OR	WO_CLEAR	Unused_28B: Unused.
29	RW	WO_OR	WO_CLEAR	Unused_29B: Unused.
30	RW	WO_OR	WO_CLEAR	Unused_30B: Unused.
31	RW	WO_OR	WO_CLEAR	Unused_31B: Unused.

Register Name	Chiplet Configuration Register 0
Mnemonic	TP.TCN2.N2.CPLT_CONF0
Address	0000000004000008 (SCOM) 0000000004000018 (SCOM1) 0000000004000028 (SCOM2)
Description	This register contains the first set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 selected.
6	RW	WO_OR	WO_CLEAR	Reserved_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	Reserved_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 selected.
14	RW	WO_OR	WO_CLEAR	Reserved_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	Reserved_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 selected.
22	RW	WO_OR	WO_CLEAR	Reserved_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	Reserved_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3 selected.
30	RW	WO_OR	WO_CLEAR	Reserved_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	Reserved_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: Selects an ABIST overflow or failure indication.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection and the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.
35	RW	WO_OR	WO_CLEAR	Reserved_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	Reserved_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	Reserved_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	Reserved_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	Reserved_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from the CC or chiplet control.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in the CC that are not PCB related.
42	RW	WO_OR	WO_CLEAR	Reserved_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	Reserved_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	Reserved_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: System ID.
61	RW	WO_OR	WO_CLEAR	Reserved_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	Reserved_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	Reserved_ID_63C: Reserved ID.

Register Name	Chiplet Configuration Register 1
Mnemonic	TP.TCN2.N2.CPLT_CONF1
Address	0000000004000009 (SCOM) 0000000004000019 (SCOM1) 0000000004000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	Unused_0D: Unused.
1	RW	WO_OR	WO_CLEAR	Unused_1D: Unused.
2	RW	WO_OR	WO_CLEAR	Unused_2D: Unused.
3	RW	WO_OR	WO_CLEAR	Unused_3D: Unused.
4	RW	WO_OR	WO_CLEAR	IOVALID_4D: Unused.
5	RW	WO_OR	WO_CLEAR	IOVALID_5D: Unused.
6	RW	WO_OR	WO_CLEAR	IOVALID_6D: Unused.
7	RW	WO_OR	WO_CLEAR	IOVALID_7D: Unused.
8	RW	WO_OR	WO_CLEAR	IOVALID_8D: Unused.
9	RW	WO_OR	WO_CLEAR	IOVALID_9D: Unused.
10	RW	WO_OR	WO_CLEAR	TC_PSI_IOVALID_DC: Enables the interface logic of this I/O.
11	RW	WO_OR	WO_CLEAR	IOVALID_11D: Unused.
12	RW	WO_OR	WO_CLEAR	FREE_USAGE_12D: Free usage.
13	RW	WO_OR	WO_CLEAR	FREE_USAGE_13D: Free usage.
14	RW	WO_OR	WO_CLEAR	FREE_USAGE_14D: Free usage.
15	RW	WO_OR	WO_CLEAR	FREE_USAGE_15D: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
16	RW	WO_OR	WO_CLEAR	FREE_USAGE_16D: Free usage.
17	RW	WO_OR	WO_CLEAR	FREE_USAGE_17D: Free usage.
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	Chiplet Status Register
Mnemonic	TP.TCN2.N2.CPLT_STAT0
Address	0000000004000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask Register. A mask only masks the interrupt, not the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM and eDRAM ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	Reserved_2E: Reserved.
3	ROX	Reserved_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic output port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic output port.
6	ROX	Reserved_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done. Used for LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that the chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	FREE_USAGE_12E: Free usage.
13	ROX	FREE_USAGE_13E: Free usage.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.

Bits	SCOM	Field Mnemonic: Description
16	ROX	FREE_USAGE_16E: Free usage.
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	**Chiplet Mask Register**
Mnemonic	TP.TCN2.N2.CPLT_MASK0
Address	0000000004000101 (SCOM)
Description	This register masks an interrupt when a bit changes in the Chiplet Status Register. It does not mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: This field provides bitwise masking of the chiplet status register.

Register Name	**CTRL Protect Mode Register**
Mnemonic	TP.TCN2.N2.CTRL_PROTECT_MODE_REG
Address	00000000040003FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: This bit enables read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: This bit enables write protection.

Register Name	**Atomic Lock Register**
Mnemonic	TP.TCN2.N2.CTRL_ATOMIC_LOCK_REG
Address	00000000040003FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: This bit enables an atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: This field contains the atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: This field is an atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCN2.N2.EPS.PSC.PSC.PSCOM_MODE_REG
Address	0000000004010000 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on a PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on a PCB write data parity error.
2	RW	UNUSED_2B: Unused.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on a DL return write data parity error.
4	RW	WATCHDOG_ENABLE: Watchdog enable.
5:6	RW	SCOM_HANG_LIMIT: 0b11 = 256 0b10 = 512 0b01 = 768 0b00 = 1023
7	RW	FORCE_ALL_RINGS: This bit is set to a logical 1 if all rings should be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on statevec parity error enable.
9:11	RW	Reserved_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCN2.N2.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000004010001 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on the interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on the parallel-to-serial (p2S) machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated time out while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated time out while waiting for DLDCH_return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated time out while waiting for ULDCH.

Bits	SCOM	Field Mnemonic: Description
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address is invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid_register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped download return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on p2s machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD .
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD .
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address is invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	PSCOMLE Error Mask Register
Mnemonic	TP.TCN2.N2.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	0000000004010002 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.

Bits	SCOM	Field Mnemonic: Description
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on the interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on the parallel-to-serial (p2s) machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting for ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NLVD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NLVD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCN2.N2.EPS.PSC.PSC.ADDR_TRAP_REG
Address	0000000004010003 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: This field contains the PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write of the last transaction with an error.
17	ROX	Reserved_ADDR_LAST_TRAP_LT: Reserved.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial-to-parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit. This bit is set to 1 if no parity error is detected in the satellite number or acknowledgment bits. This applies to the parity of the satellite response excluding read data.
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: This bit is set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: This bit is set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: This bit is set if an invalid register address is detected by the satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TCN2.N2.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	0000000004010005 (SCOM)
Description	This register enables the ring lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon a write to a specific ring.
1	RW	Reserved_RING_LOCKING: Reserved.

Register Name	Write Protection Rings Register
Mnemonic	TP.TCN2.N2.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	0000000004010006 (SCOM)
Description	This register writes ring-protect bit maps.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Writes a protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TCN2.N2.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	0000000004010007 (SCOM)
Description	This register provides a bit mask for atomic locking.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: This field provides a bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TCN2.N2.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	0000000004010008 (SCOM)
Description	This register provides a bit mask for ring fencing.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: This field provides a bit mask for ring fencing on a ring-by-ring basis.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000004010400 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000004010401 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-tun indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000004010402 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store-on-trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace is run.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000004010403 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000004010404 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000004010405 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match pattern A 0 – 23. Pattern A is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERNB: Pattern match pattern B 0 – 23. Pattern B is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000004010406 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match pattern C 0 – 23. Pattern C is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERND: Pattern match pattern D 0 – 23. Pattern D is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000004010407 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A. When set to '1', masks off bits from Pattern A. This field is used to mask off individual bits of Pattern A so that they are "don't care" for the data compare match function.
24:47	RW	MASKB: Mask B. When set to '1', masks off bits from Pattern B. This field is used to mask off individual bits of Pattern B so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000004010408 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C. When set to '1', masks off bits from Pattern C. This field is used to mask off individual bits of Pattern C so that they are "don't care" for the data compare match function.
24:47	RW	MASKD: Mask D. When set to '1', masks off bits from Pattern D. This field is used to mask off individual bits of Pattern D so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN2.N2.TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000004010409 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes

Bits	SCOM	Field Mnemonic: Description
10:13	RW	TRIG0_OR_MASK: Note: The OR of all selected MATCHes is ORed with result of TRIG0_AND: 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes
14:17	RW	TRIG0_AND_MASK: Note: The AND of the following selected MATCHes is ORed with result of TRIG0_OR: 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0
18:21	RW	TRIG1_OR_MASK: Note: The OR of all selected MATCHes is ORed with result of TRIG1_AND: 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1
22:25	RW	TRIG1_AND_MASK: Note: The AND of following selected MATCHes is ORed with result of TRIG1_OR: 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a TRIGger: 0b1000 inverts MATCHA 0b0100 inverts MATCHB 0b0010 inverts MATCHC 0b0001 inverts MATCHD
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_HI_DATA_REG
Address	0000000004010440 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_LO_DATA_REG
Address	0000000004010441 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_TRCTRL_CONFIG
Address	0000000004010442 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store-on-trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace is run.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace date pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000004010443 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000004010444 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000004010445 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match pattern A 0 – 23. Pattern A is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERNB: Pattern match pattern B 0 – 23. Pattern B is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000004010446 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match pattern C 0 – 23. Pattern C is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERND: Pattern match pattern D 0 – 23. Pattern D is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000004010447 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A. When set to '1', masks off bits from Pattern A. This field is used to mask off individual bits of Pattern A so that they are "don't care" for the data compare match function.
24:47	RW	MASKB: Mask B. When set to '1', masks off bits from Pattern B. This field is used to mask off individual bits of Pattern B so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000004010448 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C. When set to '1', masks off bits from Pattern C. This field is used to mask off individual bits of Pattern C so that they are "don't care" for the data compare match function.
24:47	RW	MASKD: Mask D. When set to '1', masks off bits from Pattern D. This field is used to mask off individual bits of Pattern D so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN2.N2.TRA0.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000004010449 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23) 0b01 = Debug bus bits(24:47) 0b10 = Debug bus bits(48:71) 0b11 = Debug bus bits(72:87) | 8 zeroes
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG0_AND: 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes

Bits	SCOM	Field Mnemonic: Description
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG0_OR: 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG1_AND: 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG1_OR: 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a TRIGger: 0b1000 inverts MATCHA 0b0100 inverts MATCHB 0b0010 inverts MATCHC 0b0001 inverts MATCHD
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	**Debug Mode Register**
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_MODE_REG
Address	00000000040107C0 (SCOM)
Description	This is debug macro configuration register 0 for the configuration component.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: Global broadcast mode (0 - 2): 100 = dbg_trace_run and dbg_trace_freeze 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze 110 = dbg_triggers_out(0 to 1) 111 = pc_tcdbg_triggers(0 to 1) (from core)
3:5	RW	TRACE_SEL_MODE: Select source for trace_run and bank: 001 = core trace run and bank 010 = tp broadcast run and 0 011 = tc_dbg_inter_brcst latched 100 = tc_dbg_dbg_sync_brcst_rcv else: dbg_trace_run and dbg_trace_bank
6:7	RW	TRIG_SEL_MODE: Select source for tcdbg_trigger(0): 10 = global broadcast 11 = pc_tcdbg_trigger (from core) else: dbg_triggers_out(0:1)

Bits	SCOM	Field Mnemonic: Description
8	RW	STOP_ON_XSTOP_SELECTION: This bit enables a trace stop on a checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: This bit enables a trace stop on a recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: This bit enables a trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select freeze source: 0 = local debug freeze. 1 = via broadcast: tp_tcdbg_glb_brcst(1)
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode; currently unused because obsolete. See TRACE_SEL_MODE.
14	RO	constant = 0b0 See SYNC_BRCST_MODE.
15	RO	constant = 0b0
16:31	ROX	DBG_STATUS: Read-only debug status bits.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000040107C1 (SCOM)
Description	This is debug macro configuration register 1 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0): 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst1_dbg_cond1 003 select inst1_dbg_cond2 004 select inst1_dbg_cond3 005 select inst1_dbg_cond2timeout 006 select inst2_dbg_cond1 007 select inst2_dbg_cond2 008 select inst2_dbg_cond3 009 select inst2_dbg_cond2timeout 010 select inst3_dbg_cond1 - Unused, tied down 011 select inst3_dbg_cond2 - Unused, tied down 012 select inst3_dbg_cond3 - Unused, tied down 013 select inst3_dbg_cond2timeout - Unused, tied down 014 select inst4_dbg_cond1 - Unused, tied down 015 select inst4_dbg_cond2 - Unused, tied down 016 select inst4_dbg_cond3 - Unused, tied down 017 select inst4_dbg_cond2timeout - Unused, tied down 018 select inst1_dbg_trig_sp 019 select inst2_dbg_trig_sp 020 select inst3_dbg_trig_sp - Unused, tied down 021 select inst4_dbg_trig_sp - Unused, tied down 022 select tctrc_tcdbg_trigger_a(0) 023 select tctrc_tcdbg_trigger_b(0) 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0) 025 select tctrc_tcdbg_trigger_a(1) 026 select tctrc_tcdbg_trigger_b(1) 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1) 028 select tctrc_tcdbg_trigger_a(2) 029 select tctrc_tcdbg_trigger_b(2) 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2) 031 select tctrc_tcdbg_trigger_a(3) 032 select tctrc_tcdbg_trigger_b(3) 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3) 034 select tctrc_tcdbg_trigger_a(4) 035 select tctrc_tcdbg_trigger_b(4) 036 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4) 037 select tctrc_tcdbg_trigger_a(5) 038 select tctrc_tcdbg_trigger_b(5) 039 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5) 040 select tctrc_tcdbg_trigger_a(6) 041 select tctrc_tcdbg_trigger_b(6) 042 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6) 043 select tctrc_tcdbg_trigger_a(7) 044 select tctrc_tcdbg_trigger_b(7) 045 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7) 046 select tctrc_tcdbg_trigger_a(8). 047 select tctrc_tcdbg_trigger_b(8). 048 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8) 049 select tctrc_tcdbg_trigger_a(9) 050 select tctrc_tcdbg_trigger_b(9) 051 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9) 052 select tctrc_tcdbg_trigger_a(10) 053 select tctrc_tcdbg_trigger_b(10) 054 select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10) 055 select tctrc_tcdbg_trigger_a(11) 056 select tctrc_tcdbg_trigger_b(11) 057 select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11) 058 select tctrc_tcdbg_trigger_a(12) 059 select tctrc_tcdbg_trigger_b(12)

Bits	SCOM	Field Mnemonic: Description
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Counter 1 in-a-row mode for front-end instance (or component) 1.
33	RW	INST1_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST1_Unused_1: Unused.
39	RW	INST1_C2_INAROW_MODE: Counter 2 in-a-row mode for front-end instance (or component) 1.
40	RW	INST1_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode 2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST1_Unused_2: Unused.
46	RW	INST1_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST1_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST1_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST1_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: Instance 1 condition 1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: Instance 1 condition 2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front-end instance 1 reset condition 3 for reset_c3_on_c0: 0b100 = dbg_cross_couple_triggers(4) 0B101 = dbg_cross_couple_triggers(12) 0B110 = dbg_cross_couple_triggers(20) 0B111 = dbg_cross_couple_triggers(28)

Register Name	**Debug Instance 1 Condition 2 Register**
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_INST1_COND_REG_2
Address	00000000040107C2 (SCOM)
Description	This is debug macro configuration register 2 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same of all selectors: 00000 - selects inst1_cond1_trig_a 00001 - selects inst1_cond1_trig_b 00010 - selects inst1_cond2_trig_a 00011 - selects inst1_cond2_trig_b 00100 - selects inst1_condition1 00101 - selects inst1_condition2 00110 - selects inst1_condition3 00111 - selects inst1_cond2_timeout 01000 - selects inst2_cond1_trig_a 01001 - selects inst2_cond1_trig_b 01010 - selects inst2_cond2_trig_a 01011 - selects inst2_cond2_trig_b 01100 - selects inst2_condition1 01101 - selects inst2_condition2 01110 - selects inst2_condition3 01111 - selects inst2_cond2_timeout 10000 - selects inst3_cond1_trig_a 10001 - selects inst3_cond1_trig_b 10010 - selects inst3_cond2_trig_a 10011 - selects inst3_cond2_trig_b 10100 - selects inst3_condition1 10101 - selects inst3_condition2 10110 - selects inst3_condition3 10111 - selects inst3_cond2_timeout 11000 - selects inst4_cond1_trig_a 11001 - selects inst4_cond1_trig_b 11010 - selects inst4_cond2_trig_a 11011 - selects inst4_cond2_trig_b 11100 - selects inst4_condition1 11101 - selects inst4_condition2 11110 - selects inst4_condition3 11111 - selects inst4_cond2_timeout
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: Instance 1 cross couple select 1 b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: Instance 1 cross couple select 2 a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: Instance 1 cross couple select 2 b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate to compare without an actual compare.

Register Name	Debug Instance 1 Condition 3 Register
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_INST1_COND_REG_3
Address	00000000040107C3 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	**Debug Instance 2 Condition 1 Register**
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000040107C4 (SCOM)
Description	This is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0): 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst2_dbg_cond1 003 select inst2_dbg_cond2 004 select inst2_dbg_cond3 005 select inst2_dbg_cond2timeout 006 select inst2_dbg_cond1 007 select inst2_dbg_cond2 008 select inst2_dbg_cond3 009 select inst2_dbg_cond2timeout 010 select inst3_dbg_cond1 - Unused, tied down 011 select inst3_dbg_cond2 - Unused, tied down 012 select inst3_dbg_cond3 - Unused, tied down 013 select inst3_dbg_cond2timeout - Unused, tied down 014 select inst4_dbg_cond1 - Unused, tied down 015 select inst4_dbg_cond2 - Unused, tied down 016 select inst4_dbg_cond3 - Unused, tied down 017 select inst4_dbg_cond2timeout - Unused, tied down 018 select inst2_dbg_trig_sp 019 select inst2_dbg_trig_sp 020 select inst3_dbg_trig_sp - Unused, tied down 021 select inst4_dbg_trig_sp - Unused, tied down 022 select tctrc_tcdbg_trigger_a(0) 023 select tctrc_tcdbg_trigger_b(0) 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0) 025 select tctrc_tcdbg_trigger_a(1) 026 select tctrc_tcdbg_trigger_b(1) 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1) 028 select tctrc_tcdbg_trigger_a(2) 029 select tctrc_tcdbg_trigger_b(2) 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2) 031 select tctrc_tcdbg_trigger_a(3) 032 select tctrc_tcdbg_trigger_b(3) 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3) 034 select tctrc_tcdbg_trigger_a(4) 035 select tctrc_tcdbg_trigger_b(4) 026 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4) 027 select tctrc_tcdbg_trigger_a(5) 028 select tctrc_tcdbg_trigger_b(5) 029 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5) 030 select tctrc_tcdbg_trigger_a(6) 031 select tctrc_tcdbg_trigger_b(6) 032 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6) 033 select tctrc_tcdbg_trigger_a(7) 034 select tctrc_tcdbg_trigger_b(7) 035 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7) 036 select tctrc_tcdbg_trigger_a(8) 037 select tctrc_tcdbg_trigger_b(8) 038 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8) 039 select tctrc_tcdbg_trigger_a(9) 040 select tctrc_tcdbg_trigger_b(9) 041 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9) 042 select xstop_err 043 select recov_err 044 select spattn 045 select fir_dbg_local_xstop_err 046 select tc_dbg_inter_brcst(0) 047 select tc_dbg_inter_brcst(1) -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare

Bits	SCOM	Field Mnemonic: Description
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Counter 1 in-a-row mode for front-end instance (or component) 2.
33	RW	INST2_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST2_Unused_1: Unused.
39	RW	INST2_C2_INAROW_MODE: Counter 2 in-a-row mode for front-end instance (or component) 2.
40	RW	INST2_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode 2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST2_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST2_Unused_2: Unused.
46	RW	INST2_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST2_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST2_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST2_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: Instance 2 condition1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: Instance 2 condition 2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front-end instance 1, reset condition 3 for reset_c3_on_c0: 0b100 = dbg_cross_couple_triggers(4) 0b101 = dbg_cross_couple_triggers(12) 0b110 = dbg_cross_couple_triggers(20) 0b111 = dbg_cross_couple_triggers(28)

Register Name	Debug Instance 2 Condition 2 Register
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000040107C5 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same of all selectors: 00000 selects inst2_cond1_trig_a 00001 selects inst2_cond1_trig_b 00010 selects inst2_cond2_trig_a 00011 selects inst2_cond2_trig_b 00100 selects inst2_condition1 00101 selects inst2_condition2 00110 selects inst2_condition3 00111 selects inst2_cond2_timeout 01000 selects inst2_cond1_trig_a 01001 selects inst2_cond1_trig_b 01010 selects inst2_cond2_trig_a 01011 selects inst2_cond2_trig_b 01100 selects inst2_condition1 01101 selects inst2_condition2 01110 selects inst2_condition3 01111 selects inst2_cond2_timeout 10000 selects inst3_cond1_trig_a 10001 selects inst3_cond1_trig_b 10010 selects inst3_cond2_trig_a 10011 selects inst3_cond2_trig_b 10100 selects inst3_condition1 10101 selects inst3_condition2 10110 selects inst3_condition3 10111 selects inst3_cond2_timeout 11000 selects inst4_cond1_trig_a 11001selects inst4_cond1_trig_b 11010 selects inst4_cond2_trig_a 11011 selects inst4_cond2_trig_b 11100 selects inst4_condition1 11101 selects inst4_condition2 11110 selects inst4_condition3 11111 selects inst4_cond2_timeout
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: Instance 2 cross couple select 1 b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: Instance 2 cross couple select 2 a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: Instance 2 cross couple select 2 b.
20:43	RW	INST2_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Force test mode to indicate to compare without actual compare.

Register Name	Debug Instance 2 Condition 3 Register
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_INST2_COND_REG_3
Address	00000000040107C6 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_TRACE_REG_0
Address	00000000040107CD (SCOM)
Description	This is debug macro configuration register 0 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: This bit enables of instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: This bit enables of instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: This bit enables slow LFSR mode of front-end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: This bit enables slow LFSR mode of front-end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: This field selects instance 1 condition1 for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
10:11	RW	INST1_CONDITION2_TRIG_SEL: This field selects instance 1 condition 2 for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: This field selects instance1 condition 2 time-out counter for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
14:15	RW	INST2_CONDITION1_TRIG_SEL: This field selects instance 2 condition1 for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
16:17	RW	INST2_CONDITION2_TRIG_SEL: This field selects instance 2 condition 2 trigger for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: This field selects instance 2 condition 2 time-out counter for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
20:31	RO	constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: This bit enables trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: This bit enables trigger on freeze.

Bits	SCOM	Field Mnemonic: Description
34:38	RW	CORE_RAS0_TRIG_SEL: This field selects which debug event of the debug front-end components is used for dbg_triggers_out(3) of the debug back-end component. 00001 = inst1_condition1_lt 00010 = inst1_cond2_3_event 00100 = inst1_cond2_timeout 01001 = inst2_condition1_lt 01010 = inst2_cond2_3_event 01100 = inst2_cond2_timeout 10001 = inst3_condition1_lt unused 10010 = inst3_cond2_3_event unused 10100 = inst3_cond2_timeout unused 11001 = inst4_condition1_lt unused 11010 = inst4_cond2_3_event unused 11100 = inst4_cond2_timeout unused
39:43	RW	CORE_RAS1_TRIG_SEL: This field selects which debug event of the debug front-end components is multiplexed to dbg_triggers_out(4) of the debug back-end component ' 00001 = inst1_condition1_lt 00010 = inst1_cond2_3_event 00100 = inst1_cond2_timeout 01001 = inst2_condition1_lt 01010 = inst2_cond2_3_event 01100 = inst2_cond2_timeout 10001 = inst3_condition1_lt unused 10010 = inst3_cond2_3_event unused 10100 = inst3_cond2_timeout unused 11001 = inst4_condition1_lt unused 11010 = inst4_cond2_3_event unused 11100 = inst4_cond2_timeout unused
44:45	RW	PC_TP_TRIG_SEL: This field selects which debug event of the debug front-end components is multiplexed to dbg_triggers_out(5 to 6) of the debug back-end component. 00 = triggers_out_lt(0) & triggers_out_lt(1) 01 = triggers_out_lt(0) & triggers_out_lt(2) 10 = triggers_out_lt(1) & triggers_out_lt(2) 11 = Unused
46:49	RW	DBG_ARM_SEL: This field selects which debug event is multiplexed to dbg_wat_arm (unused). XXXX = don't care, unused.
50:53	RW	TRIG0_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(0): Note: Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)

Bits	SCOM	Field Mnemonic: Description
54:57	RW	TRIG1_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(1). Note: Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)
58:63	RO	constant = 0b000000

Register Name	Debug Trace 1 Register
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_TRACE_REG_1
Address	00000000040107CE (SCOM)
Description	This is debug macro configuration register 1 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Instance1 action selection, condition1: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
2:3	RW	INST1_CONDITION2_ACTION_DO: Instance1 action selection, condition 2: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Instance1 action selection, c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
6:7	RW	INST2_CONDITION1_ACTION_DO: Instance 2 action selection, condition 1: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
8:9	RW	INST2_CONDITION2_ACTION_DO: Instance 2 action selection, condition 2: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)

Bits	SCOM	Field Mnemonic: Description
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Instance 2 action selection, c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
12:23	RO	constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For wait-N.
25	RW	INST1_CONDITION2_ACTION_WAITN: For wait-N.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For wait-N.
27	RW	INST2_CONDITION1_ACTION_WAITN: For wait-N.
28	RW	INST2_CONDITION2_ACTION_WAITN: For wait-N.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For wait-N.
30:35	RO	constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (instance 1, condition 1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (instance 1, condition 2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (instance 2, condition 1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (instance 2, condition 2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 2, c2_timeout).
42:47	RO	constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select an additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt 001 = inst1_condition2_lt 010 = inst1_condition3_lt 011 = inst1_cond2_timeout_lt 1XX = Disable checkstop_mode
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: Enable_fir_trig_xstop: Enable a checkstop on the debug trigger: 0 = Disable a checkstop on the debug trigger 1 = Enable a checkstop on the debug trigger
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select an additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt 001 = inst2_condition2_lt 010 = inst2_condition3_lt 011 = inst2_cond2_timeout_lt 1XX = Disable checkstop_mode
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: Enable_fir_error_xstop: Enable a checkstop on a FIR error: 0 = Disable a checkstop on a FIR error 1 = Enable a checkstop on a FIR error
56:63	RO	constant = 0b00000000

Register Name	**Debug Trace 2 Register**
Mnemonic	TP.TCN2.N2.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000040107CF (SCOM)
Description	This is debug macro configuration register 2 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the run-N counter used in trace modes run-N and wait-N.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on a checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on run-N match.
19	RW	FORCE_TEST_MODE: Force the run-N condition to be true.
20	RW	ACCUM_HIST_MODE: Accumulate history mode; do not clear history mode when trace run is active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	**CXA FIR Register**
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_REG
Address	0000000004010800 (SCOM) 0000000004010801 (SCOM1) 0000000004010802 (SCOM2)
Description	This is the local FIR register for the CAPP.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	BAR_PE: Informational PE. Generic bucket for errors that are informational.
1	RWX	WOX_AND	WOX_OR	REGISTER_PE: System checkstop PE. Generic bucket for errors that are system checkstop.
2	RWX	WOX_AND	WOX_OR	MASTER_ARRAY_CE: Correctable error on the master array; includes micro-operation (uOP) and combined response (CRESP) arrays.
3	RWX	WOX_AND	WOX_OR	MASTER_ARRAY_UE: Uncorrectable error on the master array, includes uOP and CRESP arrays.
4	RWX	WOX_AND	WOX_OR	TIMER_EXPIRED_RECOV_ERROR: Precise directory epoch timeout. Coarse directory epoch timeout. rtagPool epoxh data hang timeout. Recovery sequencer hang detection.
5	RWX	WOX_AND	WOX_OR	TIMER_EXPIRED_XSTOP_ERROR: Recovery sequencer hang detection.
6	RWX	WOX_AND	WOX_OR	PSL_CMD_UE: The XPT detected an uncorrectable error on the processor bus data that is determined to be a PSL command. The PSL command does not propagate past XPT.
7	RWX	WOX_AND	WOX_OR	PSL_CMD_SUE: XPT detected special uncorrectable error on processor bus data determined to be a PSL command. The PSL command does not propagate past XPT.
8	RWX	WOX_AND	WOX_OR	SNOOP_ARRAY_CE: Correctable error on the snooper array. Includes the precise directory, coarse directory, and uOP.
9	RWX	WOX_AND	WOX_OR	SNOOP_ARRAY_UE: Uncorrectable error on the snooper array. Includes the precise directory, coarse directory, and uOP.
10	RWX	WOX_AND	WOX_OR	RECOVERY_FAILED: CAPP recovery failed.
11	RWX	WOX_AND	WOX_OR	ILLEGAL_LPC_BAR_ACCESS: Illegal LPC BAR access. An error was detected when a snooper or master write operation attempted to access directories in LPC-only mode or when the operation hits the LPC BAR region in LPC-disjoint mode. Also fires if a directory hit is found on a read operation within the LPC BAR range.
12	RWX	WOX_AND	WOX_OR	XPT_RECOVERABLE_ERROR: Recoverable errors detected in transport.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
13	RWX	WOX_AND	WOX_OR	MASTER_RECOVERABLE_ERROR: Recoverable errors detected in the master.
14	RWX	WOX_AND	WOX_OR	SNOOPER_RECOVERABLE_ERROR: Spare FIR bits allocated for future use.
15	RWX	WOX_AND	WOX_OR	SECURE_SCOM_ERROR: Error detected in the secure SCOM satellite.
16	RWX	WOX_AND	WOX_OR	MASTER_SYS_XSTOP_ERROR: System checkstop errors detected in the master (invalid state, control checker).
17	RWX	WOX_AND	WOX_OR	SNOOPER_SYS_XSTOP_ERROR: System checkstop errors detected in the snooper (invalid state, control checker).
18	RWX	WOX_AND	WOX_OR	XPT_SYS_XSTOP_ERROR: System checkstop errors detected in transport (invalid state, control checker).
19	RWX	WOX_AND	WOX_OR	MUOP_ERROR_1: Master uOP FIR 1.
20	RWX	WOX_AND	WOX_OR	MUOP_ERROR_2: Master uOP FIR 2.
21	RWX	WOX_AND	WOX_OR	MUOP_ERROR_3: Master uOP FIR 3.
22	RWX	WOX_AND	WOX_OR	SUOP_ERROR_1: Snooper uOP FIR 1.
23	RWX	WOX_AND	WOX_OR	SUOP_ERROR_2: Snooper uOP FIR 2.
24	RWX	WOX_AND	WOX_OR	SUOP_ERROR_3: Snooper uOP FIR 3.
25	RWX	WOX_AND	WOX_OR	POWERBUS_MISC_ERROR: Miscellaneous informational processor bus errors including unsolicited processor bus data and unsolicited CRESP.
26	RWX	WOX_AND	WOX_OR	POWERBUS_INTERFACE_PE: Parity error on power bus interface (address/aTag/tTaag/rTag APC, SNP TLBI).
27	RWX	WOX_AND	WOX_OR	POWERBUS_DATA_HANG_ERROR: Any processor bus data hang poll error.
28	RWX	WOX_AND	WOX_OR	POWERBUS_HANG_ERROR: Any processor bus command hang error (domestic address range).
29	RWX	WOX_AND	WOX_OR	LD_CLASS_CMD_ADDR_ERR: Processor bus address error detected by the APC on a load-class command.
30	RWX	WOX_AND	WOX_OR	ST_CLASS_CMD_ADDR_ERR: Processor bus address error detected by the APC on a store-class command.
31	RWX	WOX_AND	WOX_OR	PHB_LINK_DOWN: The PHB0 or PHB1 interface asserted link down.
32	RWX	WOX_AND	WOX_OR	LD_CLASS_CMD_FOREIGN_LINK_FAIL: The APC received ack_dead or ack_ed_dead from the foreign interface on a load-class command.
33	RWX	WOX_AND	WOX_OR	FOREIGN_LINK_HANG_ERROR: Any processor bus command hang error (foreign address range).
34	RWX	WOX_AND	WOX_OR	XPT_POWERBUS_CE: A CE on data received from the processor bus and destined for either the XPT data array (and back to the processor bus) or a PSL command or link delay response packet.
35	RWX	WOX_AND	WOX_OR	XPT_POWERBUS_UE: A UE on data received from the processor bus and destined for the XPT data array (and back to the processor bus) or a link delay response packet.
36	RWX	WOX_AND	WOX_OR	XPT_POWERBUS_SUE: An SUE on data received from the processor bus and destined for the XPT data array (and back to the processor bus) or a link delay response packet.
37	RWX	WOX_AND	WOX_OR	TLBI_TIMEOUT: TLBI timeout error. TLBI needs a re-IPL to recover.
38	RWX	WOX_AND	WOX_OR	TLBI_SOT_ERR: Illegal SOT operation detected in P8BC mode.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
39	RWX	WOX_AND	WOX_OR	TLBI_BAD_OP_ERR: TLBI bad operation error. TLBI needs a re-IPL to recover.
40	RWX	WOX_AND	WOX_OR	TLBI_SEQ_NUM_PARITY_ERR: Parity error detected on the TLBI sequence number.
41	RWX	WOX_AND	WOX_OR	ST_CLASS_CMD_FOREIGN_LINK_FAIL: The APC received ack_dead or ack_ed_dead from the foreign interface on a store-class command.
42	RWX	WOX_AND	WOX_OR	TIME_BASE_ERR: An error occurred with the timebase. This is an indication that the timebase value can no longer be assumed to be correct.
43	RWX	WOX_AND	WOX_OR	TRANSPORT_INFORMATIONAL_ERR: Transport informational error.
44	RWX	WOX_AND	WOX_OR	APC_ARRAY_CMD_CE_ERPT: A CE on the PSL command queue array in the APC.
45	RWX	WOX_AND	WOX_OR	APC_ARRAY_CMD_UE_ERPT: A UE on the PSL command queue array in the APC.
46	RWX	WOX_AND	WOX_OR	PSL_CREDIT_TIMEOUT_ERR: PSL credit timeout error.
47	RWX	WOX_AND	WOX_OR	SPARE_2: Spare FIR bits allocated for future use.
48	RWX	WOX_AND	WOX_OR	HYPERVISOR: Hypervisor.
49	RWX	WOX_AND	WOX_OR	SPARE_3: Spare FIR bits allocated for future use.
50	RWX	WOX_AND	WOX_OR	SCOM_ERR2: Local FIR parity error RAS duplicate.
51	RWX	WOX_AND	WOX_OR	SCOM_ERR: Local FIR parity error of ACTION/MASK registers.
52:63	RO	RO	RO	constant = 0b000000000000

Register Name	CXA FIR Mask Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_MASK_REG
Address	0000000004010803 (SCOM) 0000000004010804 (SCOM1) 0000000004010805 (SCOM2)
Description	Error mask register. (Action0, Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked (1,x) = Checkstop Error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	BAR_PE_MASK: Informational PE mask. This is a generic bucket for errors that are informational.
1	RW	WO_AND	WO_OR	REGISTER_PE_MASK: System checkstop PE mask. This is a generic bucket for errors that are a system checkstop.
2	RW	WO_AND	WO_OR	MASTER_ARRAY_CE_MASK: Correctable error on the master array. Includes uOP and CRESP arrays mask.
3	RW	WO_AND	WO_OR	MASTER_ARRAY_UE_MASK: Uncorrectable error on the master array. Includes uOP and CRESO arrays mask.
4	RW	WO_AND	WO_OR	TIMER_EXPIRED_RECOV_ERROR_MASK: Precise directory epoch timeout mask. Coarse directory epoch timeout mask. rtagPool epoxh data hang timeout mask. Recovery sequencer hang detection mask.
5	RW	WO_AND	WO_OR	TIMER_EXPIRED_XSTOP_ERROR_MASK: Recovery sequencer hang detection mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6	RW	WO_AND	WO_OR	PSL_CMD_UE_MASK: XPT detected uncorrectable error on power-bus data determined to be a PSL command mask. The PSL command does not propagate past the XPT.
7	RW	WO_AND	WO_OR	PSL_CMD_SUE_MASK: XPT detected special uncorrectable error on processor bus data determined to be a PSL command mask. The PSL command does not propagate past the XPT.
8	RW	WO_AND	WO_OR	SNOOP_ARRAY_CE_MASK: Correctable error on the snooper array. Includes the precise directory, coarse directory, and uOP mask.
9	RW	WO_AND	WO_OR	SNOOP_ARRAY_UE_MASK: Uncorrectable error on the snooper array. Includes the precise directory, coarse directory, and uOP mask.
10	RW	WO_AND	WO_OR	RECOVERY_FAILED_MASK: CAPP recovery failed mask.
11	RW	WO_AND	WO_OR	ILLEGAL_LPC_BAR_ACCESS_MASK: Illegal LPC BAR access mask. Error detected when a snooper or master write operation is attempted to access directories in LPC-only mode or when the operation hits the LPC BAR region in LPC disjoint mode. Also fires if a directory hit is found on a read operation within the LPC BAR range.
12	RW	WO_AND	WO_OR	XPT_RECOVERABLE_ERROR_MASK: Recoverable errors detected in the XPT mask.
13	RW	WO_AND	WO_OR	MASTER_RECOVERABLE_ERROR_MASK: Recoverable errors detected in the master mask.
14	RW	WO_AND	WO_OR	SNOOPER_RECOVERABLE_ERROR_MASK: Spare FIR bits allocated for future use mask.
15	RW	WO_AND	WO_OR	SECURE_SCOM_ERROR_MASK: Error detected in the secure SCOM satellite mask.
16	RW	WO_AND	WO_OR	MASTER_SYS_XSTOP_ERROR_MASK: System checkstop errors detected in the master (invalid state, control checker) mask.
17	RW	WO_AND	WO_OR	SNOOPER_SYS_XSTOP_ERROR_MASK: System checkstop errors detected in snooper (invalid state, control checker) mask.
18	RW	WO_AND	WO_OR	XPT_SYS_XSTOP_ERROR_MASK: System checkstop errors detected in the transport (invalid state, control checker) mask.
19	RW	WO_AND	WO_OR	MUOP_ERROR_1_MASK: Master uOP FIR 1 mask.
20	RW	WO_AND	WO_OR	MUOP_ERROR_2_MASK: Master uOP FIR 2 mask.
21	RW	WO_AND	WO_OR	MUOP_ERROR_3_MASK: Master uOP FIR 3 mask.
22	RW	WO_AND	WO_OR	SUOP_ERROR_1_MASK: Snooper uOP FIR 1 mask.
23	RW	WO_AND	WO_OR	SUOP_ERROR_2_MASK: Snooper uOP FIR 2 mask.
24	RW	WO_AND	WO_OR	SUOP_ERROR_3_MASK: Snooper uOP FIR 3 mask.
25	RW	WO_AND	WO_OR	POWERBUS_MISC_ERROR_MASK: Miscellaneous informational processor bus errors mask including unsolicited processor bus data and unsolicited CRESP.
26	RW	WO_AND	WO_OR	POWERBUS_INTERFACE_PE_MASK: Parity error on the processor bus interface (address/aTag/tTag/rTag APC, SNP TLBI) mask.
27	RW	WO_AND	WO_OR	POWERBUS_DATA_HANG_ERROR_MASK: Any processor bus data hang poll error mask.
28	RW	WO_AND	WO_OR	POWERBUS_HANG_ERROR_MASK: Any processor bus command hang error (domestic address range) mask.
29	RW	WO_AND	WO_OR	LD_CLASS_CMD_ADDR_ERR_MASK: Processor bus address error detected by the APC on a load-class command mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
30	RW	WO_AND	WO_OR	ST_CLASS_CMD_ADDR_ERR_MASK: Processor bus address error detected by the APC on a store-class command mask.
31	RW	WO_AND	WO_OR	PHB_LINK_DOWN_MASK: The PHB0 or PHB1 interface asserted a link down mask.
32	RW	WO_AND	WO_OR	LD_CLASS_CMD_FOREIGN_LINK_FAIL_MASK: APC received ack_dead or ack_ed_dead from the foreign interface on a load-class command mask.
33	RW	WO_AND	WO_OR	FOREIGN_LINK_HANG_ERROR_MASK: Any processor bus command hang error (foreign address range) mask.
34	RW	WO_AND	WO_OR	XPT_POWERBUS_CE_MASK: CE on data received from the processor bus and destined for either the XPT data array (and back to the processor bus) or a PSL command or link-delay response packet mask.
35	RW	WO_AND	WO_OR	XPT_POWERBUS_UE_MASK: UE on data received from the processor bus and destined for the XPT data array (and back to the processor bus) or a link-delay response packet mask.
36	RW	WO_AND	WO_OR	XPT_POWERBUS_SUE_MASK: SUE on data received from the processor bus and destined for the XPT data array (and back to the processor bus) or a link-delay response packet mask.
37	RW	WO_AND	WO_OR	TLBI_TIMEOUT_MASK: TLBI timeout error. TLBI needs a re-IPL to recover mask.
38	RW	WO_AND	WO_OR	TLBI_SOT_ERR_MASK: Illegal SOT operation detected in P8BC mode. TLBI needs a re-IPL to recover mask.
39	RW	WO_AND	WO_OR	TLBI_BAD_OP_ERR_MASK: TLBI bad operation error. TLBI needs a re-IPL to recover mask.
40	RW	WO_AND	WO_OR	TLBI_SEQ_NUM_PARITY_ERR_MASK: Parity error detected on a TLBI sequence number mask.
41	RW	WO_AND	WO_OR	ST_CLASS_CMD_FOREIGN_LINK_FAIL_MASK: APC received ack_dead or ack_ed_dead from the foreign interface on a store-class command mask.
42	RW	WO_AND	WO_OR	TIME_BASE_ERR_MASK: Mask for an error that occurred with the timebase. This is an indication that the timebase value can no longer assumed to be correct.
43	RW	WO_AND	WO_OR	TRANSPORT_INFORMATIONAL_ERR_MASK: Transport informational error mask.
44	RW	WO_AND	WO_OR	APC_ARRAY_CMD_CE_ERPT_MASK: CE on the PSL command queue array in APC mask.
45	RW	WO_AND	WO_OR	APC_ARRAY_CMD_UE_ERPT_MASK: UE on the PSL command queue array in APC mask.
46	RW	WO_AND	WO_OR	PSL_CREDIT_TIMEOUT_ERR_MASK: PSL credit timeout error mask.
47	RW	WO_AND	WO_OR	SPARE_2_MASK: Spare FIR bits allocated for future use mask.
48	RW	WO_AND	WO_OR	SPARE_3_MASK: Spare FIR bits allocated for future use mask.
49	RW	WO_AND	WO_OR	HYPERVISOR_MASK: Hypervisor mask.
50	RW	WO_AND	WO_OR	SCOM_ERR2_MASK: Local FIR parity error RAS duplicate mask.
51	RW	WO_AND	WO_OR	SCOM_ERR_MASK: Local FIR parity error of ACTION/MASK registers mask.
52:63	RO	RO	RO	constant = 0b000000000000

Register Name	Pervasive FIR Action 0 Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_ACTION0_REG
Address	0000000004010806 (SCOM)
Description	This register contains the action select for the FIR bits.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	FIR_ACTION0: MSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable (1,0) = Recoverable Interrupt (1,1) = Machine Check

Register Name	Pervasive FIR Action 1 Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.FIR_ACTION1_REG
Address	0000000004010807 (SCOM)
Description	This register contains the second bit of action select if necessary.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	FIR_ACTION1: LSB of action select for corresponding bit in FIR. (Action0,Action1,Mask) = Action Select (x,x,1) = Masked (0,0,0) = Checkstop (0,1,0) = Recoverable Error (1,0,0) = Recoverable Interrupt (1,1,0) = Machine Check

Register Name	Snoop Error Report Register
Mnemonic	CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ERROR_REPORT_REG
Address	000000000401080A (SCOM)
Description	SCOM access of SNP c_err_rpt latches.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	CXA_SNP_C_ERR_RPT_HOLD_DATA: SNP c_err_report_hold value.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	APC Master Error Report Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC1.ERRRPT
Address	000000000401080B (SCOM)
Description	Output of APC cerr_rpt hold latches.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	Reserved field.
17	ROX	Reserved field.
18	ROX	Reserved field.
19	ROX	Reserved field.
20	ROX	Reserved field.
21	ROX	Reserved field.
22	ROX	Reserved field.
23	ROX	Reserved field.
24	ROX	Reserved field.
25	ROX	Reserved field.
26	ROX	Reserved field.
27	ROX	Reserved field.
28	ROX	Reserved field.
29	ROX	Reserved field.
30	ROX	Reserved field.
31	ROX	Reserved field.
32	ROX	Reserved field.
33	ROX	Reserved field.
34	ROX	Reserved field.
35	ROX	Reserved field.
36	ROX	Reserved field.
37	ROX	Reserved field.
38	ROX	Reserved field.
39	ROX	Reserved field.
40	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
41	ROX	Reserved field.
42	ROX	Reserved field.
43	ROX	Reserved field.
44	ROX	Reserved field.
45	ROX	Reserved field.
46:63	RO	constant = 0b0000000000000000000

Register Name	Transport Error Hold Register
Mnemonic	CAPP1.CXA_TOP.XPT_ERROR_REPORT
Address	0000000004010800C (SCOM)
Description	The XPT error report register contains hold latches for the conditions that result in FIR errors.

Bits	SCOM	Field Mnemonic: Description
0	ROX	XPT_PSL_CMD_UE_ERRHOLD: PSL command uncorrectable error.
1	ROX	XPT_PSL_CMD_SUE_ERRHOLD: PSL command special uncorrectable error.
2	ROX	XPT_SC_RDATA_PARITY_ERRHOLD: EPT register read data parity error.
3	ROX	APC_SC_RDATA_PARITY_ERRHOLD: APC register read data parity error.
4	ROX	SN_SC_RDATA_PARITY_ERRHOLD: Snoop register read data parity error.
5	ROX	NX_DATA_RTAG_PARITY_ERRHOLD: Power bus RTAG parity error.
6	ROX	NXPBXPT_PBRCV_ECC_CE_ERRHOLD: Power bus data or PSL command correctable error.
7	ROX	NXPBXPT_PBRCV_ECC_UE_ERRHOLD: Power bus data uncorrectable error.
8	ROX	NXPBXPT_PBRCV_ECC_SUE_ERRHOLD: Power bus data special uncorrectable error.
9	ROX	XPT_DBG_CTL_REG_PARITY_ERRHOLD: Debug bus MUX control register write data parity error.
10	ROX	XPT_CFG_REG_PARITY_ERRHOLD: Transport control register write data parity error.
11	ROX	CAPP_ERR_STAT_CTL_REG_PARITY_ERRHOLD: CAPP error status and control register write data parity error.
12	ROX	PMU_CNTRA_CFG_REG_PARITY_ERRHOLD: PMU counter configuration register 0 write data parity error.
13	ROX	PMU_CNTRB_CFG_REG_PARITY_ERRHOLD: PMU counter configuration register 1 write data parity error.
14	ROX	XPT_PMU_EVENT_SEL_REG_PARITY_ERRHOLD: XPT PMU event select register write data parity error.
15	ROX	PE0_CXA_LINKDOWN_ERRHOLD: PE0 link down.
16	ROX	PE1_CXA_LINKDOWN_ERRHOLD: PE1 link down.
17	ROX	SB_SCOM_ERRHOLD: Secure SCOM internal error.
18	ROX	PBXMIT_MSGQ_SEQ_ERRHOLD: Transport message queue sequencer not one hot error.
19	ROX	PBXMIT_DXMIT_SEQ_ERRHOLD: Transport transmit queue sequencer not one hot error.
20	ROX	EPH_REC_TMR_CNTL_REG_PARITY_ERRHOLD: Epoch and recovery timers control register write data parity error.
21	ROX	RCS_RECOVERY_FAILED_ERRHOLD: CAPP recovery failed.
22	ROX	RCS_STATE_MACHINE_ERRHOLD: Recovery sequencer FSM invalid state.
23	ROX	NXPBXPT_PBRCV_LNK_RSP_ECC_UE_ERRHOLD: Secure link response packet UE.

Bits	SCOM	Field Mnemonic: Description
24	ROX	NXPBXPT_PBRCV_LNK_RSP_ECC_SUE_ERRHOLD: Secure link response packet SUE.
25	ROX	LNK_RSP_PKT_DISCARDED_ERRHOLD: Secure link response packet discarded.
26	ROX	SECURE_LNK_RSP_PKT_NOT_VALID_ERRHOLD: Secure link response packet not valid.
27	ROX	SECURE_LNK_SCOM_CONFLICT_ERRHOLD: Secure link response packet conflict with SCOM access.
28	ROX	UNSOLICITED_DATA_RCV_ERROR_ERRHOLD: Unsolicited data received.
29	ROX	AS_RCMD0_PARITY_ERR_ERRHOLD: AS as endpoint rcmd0 parity error.
30	ROX	AS_REGS_PARITY_ERR_ERRHOLD: AS as endpoint register parity error.
31	ROX	AS_SM_ERROR_ERRHOLD: AS as endpoint state machine error.
32	ROX	AS_REG_RDATA_PERR_ERRHOLD: AS as endpoint register read data parity error.
33	ROX	DFS_SM_ERROR_ERRHOLD: DFS State machine error.
34	ROX	TB_XPT_ERROR_FIR_ERR_ERRHOLD: Time base error.
35	ROX	TB_CMD_DISCARDED_ERRHOLD: Timebase command discarded.
36	ROX	TB_REG_RDATA_PERR_ERRHOLD: Timebase command discarded.
37	ROX	RNG_WR_ENBL_REG_PERR_ERRHOLD: RNG write enable configuration register parity error.
38	ROX	SSA_ECC_HI_UE_ERRHOLD: Message queue high UE.
39	ROX	SSA_ECC_HI_CE_ERRHOLD: Message queue high CE.
40	ROX	SSA_ECC_HI_SUE_ERRHOLD: Message queue high SUE.
41	ROX	SSA_ECC_LO_SUE_ERRHOLD: Message queue low SUE.
42	ROX	SSA_ECC_LO_CE_ERRHOLD: Message queue low CE.
43	ROX	SSA_ECC_LO_UE_ERRHOLD: Message queue low UE.
44	ROX	CXACQPB_MUX_ECC_CE_ERRHOLD: CQ MUX CE.
45	ROX	CXACQPB_MUX_ECC_UE_ERRHOLD: CQ MUX UE.
46	ROX	APC0_SC_RDATA_PARITY_ERRHOLD: APC0 register parity error.
47	ROX	CREDIT_TIMEOUT_ERRHOLD: CAPP credit timeout.
48	ROX	TLBI_SC_RDATA_PARITY_ERRHOLD: TLBI SCOM parity error.
49	ROX	TLBI_REGS_PARITY_ERRHOLD: TLBI register parity error.
50	ROX	RCS_RECOVERY_TIMEOUT_ERRHOLD: CAPP recovery timeout.
51	ROX	TBST0_BADIN_ERRHOLD: Timebase state machine in state 0 and SCOM TFMR write of bit (18) move_chip_tod_to_tb.
52	ROX	TBST6_BADIN_ERRHOLD: Timebase state machine in State 6 and SCOM TFMR write of 1 bit (18) move_chip_tod_to_tb.
53	ROX	TBST7_BADIN_ERRHOLD: Timebase state machine in State 7 and SCOM TFMR write of 1 bit (16) load_tod_mod or (18) move_chip_tod_to_tb.
54	ROX	TWO_TFMRCMDS_ERR_ERRHOLD: SCOM tfmr write of 1 to both bits (16) load_tod_mod and bit (18) move_chip_tod_to_tb.
55	ROX	TB_MISSING_SYNC_ERRHOLD: Indicates a synch pulse was not received in the time specified by the sync_bit_sel control bits.
56	ROX	TB_MISSING_STEP_ERRHOLD: Indicates that a step pulse was not received in the time specified by the max_cyc_bet_steps control bits.
57	ROX	TB_RESIDUE_ERR_ERRHOLD: Indicates a parity or residue error has compromised the integrity of the timebase.
58	ROX	TX_TFMR_CORRUPT_ERRHOLD: Indicates a parity error has been detected on the TFMR register.

Bits	SCOM	Field Mnemonic: Description
59	ROX	TBST_CORRUPT_ERRHOLD: Indicates a TFMR invalid TB state machine state.
60	ROX	TBST9_BADIN_ERRHOLD: Timebase state machine in state 9 and SCOM TFMR write of 1 bit (16) load_tod_mod or (18) move_chip_tod_to_tb.
61:63	RO	constant = 0b000

Register Name	TLBI Error Hold Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.TLBI_ERROR_REPORT
Address	000000000401080D (SCOM)
Description	The TLBI error report register contains hold latches for the conditions that result in FIR errors.

Bits	SCOM	Field Mnemonic: Description
0	ROX	TLBI_IN_TIMEOUT: Data hang timeout.
1	ROX	TLBI_IN_SEQ_ERR: Error in TLBI internal sequencers.
2	ROX	TLBI_IN_SEQ_PERR: TLBI sequence number parity error.
3	ROX	TLBI_IN_BAD_OP_ERR: TLBI bad operation error.
4	ROX	TLBI_IN_SNP_ADDR_PERR: TLBI snoop address parity error.
5	ROX	TLBI_IN_SNP_TTAG_PERR: TLBI snoop TTAG parity error.
6:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	CAPP Error Status and Control Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_EPT.CAPP_ERR_STATUS_CONTROL
Address	000000000401080E (SCOM)
Description	The CAPP error status and control register contains status and controls for the error recovery process.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	ERROR_RECOVERY_INITIATED: If this bit is set (=1) a recoverable error has been detected and the CAPP recovery process has been initiated. Once set, this bit remains set until cleared by the firmware or POR.
1	RWX_WCLRPART	ERROR_RECOVERY_COMPLETE: If error recovery initiated is 1 and this bit is 0, the CAPP recovery process is in progress. If error recovery initiated is 1 and this bit is 1, the CAPP recovery process has completed. If error recovery initiated is 0, error recovery complete = 1 is not meaningful. Once set, this bit remains set until cleared by the firmware or POR.
2	RO	constant = 0b0
3	RWX	TLBI_PSL_DEAD: This bit is set by hardware when error recovery initiated is set, asserting the core_is_dead signal to the TLBI macro informing it that PSL must be considered non-operational, possibly with outstanding TLBI requests. When core_is_dead = 1, the snoop machine in TLBI stops waiting for not_my_lpar_id or TLBI response command from PSL. TLBI acts as if PSL has returned something and goes back to idle. When error recovery is complete and the firmware wants to re-initialize the TLBI, it writes this bit and TLBI fence to 0 in the same SCOM write operation.
4	RWX	TLBI_FENCE: This bit is set by hardware when error recovery initiated is set. This bit drives the tlbie_fence_lvl signal to the TLBI macro, which normally informs the macro that the core is going to sleep but here is used as part of error initiation and recovery. The tlbie_fence_lvl tell the macro to start ignoring the new TLBIs, but still finish up the TLBIs received before tlbie_fence_lvl went high. When recovery is complete and the firmware wants to re-initialize the TLBI, it writes this bit and the TLBI PSL is dead to 0 in the same SCOM write operation.

Bits	SCOM	Field Mnemonic: Description
5	RWX_WCLRPART	RECOVERY_FAILED: Recovery did not complete successfully. Bits 6 through 9 specify the reason for the failure.
6	RWX_WCLRPART	RTAGFLUSH_FAILED: During recovery an error was detected while trying to flush the rTagPool.
7	RWX_WCLRPART	PRECISE_DIR_FLUSH_FAILED: During recovery an error was detected while trying to flush the precise directory.
8	RWX_WCLRPART	COURSE_DIR_FLUSH_FAILED: During recovery an error was detected while trying to flush the course directory.
9	RWX_WCLRPART	RECOVERY_HANG_DETECTED: The recovery actions timed out and a hang was declared.
10:11	RWX_WCLRPART	EPOCH_VALUE: Epoch value captured when error recovery is initiated.
12:13	RO	constant = 0b00
14	WO_1P	FORCE_QUIESCE: Force CAPP to quiesce.
15	ROX	QUIESCE_DONE: 1 = Force quiesce in progress, 0 = Quiesce has completed.
16:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	Flush SUE State Map Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC0.FLUSHSHUE
Address	000000000401080F (SCOM)
Description	1 bit per state decode. 1 = Requires flush with SUE during directory flush.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	FLUSH_SUE_STATE_MAP: Directory flush SUE state map, 1 bit per state decode.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Error Inject Register
Mnemonic	CAPP1.CXA_TOP.APC_ERRINJ
Address	0000000004010810 (SCOM)
Description	Error inject register controls error injection.

Bits	SCOM	Field Mnemonic: Description
0	RW	APC_ERRINJ_ENABLE: APC master error inject enable.
1	RW	APC_ERRINJ_DBLERR: APC master: 0 = Inject 1 bit ECC error 1 = Inject 2 bit ECC error
2	RW	APC_ERRINJ_CONTINUOUS: APC master: 0 = Inject error once 1 = Inject error continuously
3:6	RO	constant = 0b0000
7:11	RW	APC_ERRINJ_TARGET: APC master error inject target selection.
12	RW	SNP_ERROR_INJECT_ENABLE: SNP master error inject enable.

Bits	SCOM	Field Mnemonic: Description
13	RW	SNP_INJECT_DBL_ECC_ERROR: SNP master: 0 = Inject 1 bit ECC error 1 = Inject 2 bit ECC error
14	RW	SNP_INJECT_CONTINOUS_ERROR: SNP master: 0 = Inject error once 1 = Inject error continuously
15:16	RO	constant = 0b00
17:23	RW	SNP_ERROR_INJECT_TARGET: SNP master error inject target selection.
24:31	RO	constant = 0b00000000
32	RW	XPT_ERROR_INJECT_ENABLE: XPT master error inject enable.
33:34	RW	XPT_ERROR_TYPE: XPT Error type: 00 = Inject CE 01 = Inject UE 10 = Inject SUE 11 = Reserved
35	RW	XPT_INJECT_CONTINUOUS_ERROR: XPT continuous mode: 1 = Continuously inject the error 0 = Inject on the next operation
36:39	RW	XPT_ERROR_INJECT_TARGET: XPT Error inject target: 0000 = Write buffer array 0 0001 = Write buffer array 1 0010 – 1111 = Reserved
40:63	RO	constant = 0b000000000000000000000000

Register Name	Debug Bus MUX Control Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.DEBUG_CONTROL
Address	0000000004010811 (SCOM)
Description	The debug bus MUX control register selects which unit drives and which port of its 16-1 MUX drives the bus.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	BLOCK_MUX_PORT_SEL: Selects 1 of up to 16 block internal debug buses to source the block debug bus output.
4:11	RW	BLOCK_SEL: One-hot bit vector that selects the block to drive the debug bus. Bit block: 4 = APC0 5 = APC1 6 = SNPFE 7 = snpfe_dir 8 = SBPBE 9 = snpbe_uop 10 = TLBI 11 = XPT If all block select bits are 0, the debug bus is de-gated and no switching on the main trunk of the debug bus occurs.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Trigger Bus MUX Control Register
Mnemonic	CAPP1.CXA_TOP.CXA_TRIGCTL
Address	0000000004010812 (SCOM)
Description	Trigger bus MUX control register. selects and enables trigger events.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CXA_TRIGCTL_PORTSEL: APC Master trigger selection.
4	RW	CXA_TRIGCTL_APC0_ENABLE: APC Master trigger enable for APC0.
5	RW	CXA_TRIGCTL_APC1_ENABLE: APC Master trigger enable for APC1.
6	RW	SNPFE_TRIGGER_ENABLE: SNP FE trigger enable.
7	RW	SNPFE_DIR_TRIGGER_ENABLE: SNP FE DIR trigger enable.
8	RW	SNPBE_TRIGGER_ENABLE: SNP BE trigger enable.
9	RW	SNPBE_UOP_TRIGGER_ENABLE: SNP BE uOP trigger enable.
10	RW	Reserved field.
11	RW	Reserved field.
12:15	RW	SNP_MUX_PORT_SEL: Selects 1 of up to 16 block internal trigger conditions to source the SNP trigger bus bit 1.
16:19	RW	Reserved field.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	Error Report Clear Register
Mnemonic	CAPP1.CXA_TOP.ERR_RPT_CLR
Address	0000000004010813 (SCOM)
Description	A write to this register clears all the CAPP c_err_rpt error hold latches.

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved.
1:63	RO	Not implemented.

Register Name	PMU Counter A Configuration Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.PMU_CNTRA_CFG
Address	0000000004010814 (SCOM)
Description	The PMU counter A configuration register controls the configuration of the PMU counters.

Bits	SCOM	Field Mnemonic: Description
0	RW	PMUA_COUNTER0_ENABLE: When = 1 this bit enables PMU counter 0.
1	RW	PMUA_COUNTER1_ENABLE: When = 1 this bit enables PMU counter 1.
2	RW	PMUA_COUNTER2_ENABLE: When = 1 this bit enables PMU counter 2.
3	RW	PMUA_COUNTER3_ENABLE: When = 1 this bit enables PMU counter 3.
4:6	RW	PMUA_PRESCALER_SELECT: Determines which, if any, prescaler counter to apply to all 16 bit PMU counters.

Bits	SCOM	Field Mnemonic: Description
7	RW	PMUA_COUNTER_FREEZE_MODE: Indicates a counter should freeze on overflow: 0 = Free running 1 = Freeze on overflow
8	RW	PMUA_COUNTER_RESET_MODE: Indicates how the counter should be reset: 0 = Free running 1 = Reset on SCOM read
9:12	RW	PMUA_COUNTER0_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter 0.
13	RW	PMUA_COUNTER0_POSEDGE_SELECT: If this bit is 1, the PMU only counts the event rising edge. If this bit is 0, the PMU counts every cycle the event is asserted (high).
14:15	RW	PMUA_COUNTER0_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
16:19	RW	PMUA_COUNTER1_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter 1.
20	RW	PMUA_COUNTER1_POSEDGE_SELECT: If this bit is 1, the PMU only counts the event rising edge. If this bit is 0, the PMU counts every cycle the event is asserted (high).
21:22	RW	PMUA_COUNTER1_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
23:26	RW	PMUA_COUNTER2_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter 2.
27	RW	PMUA_COUNTER2_POSEDGE_SELECT: If this bit is 1, the PMU only counts the event rising edge. If this bit is 0, the PMU counts every cycle the event is asserted (high).
28:29	RW	PMUA_COUNTER2_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
30:33	RW	PMUA_COUNTER3_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter 3.
34	RW	PMUA_COUNTER3_POSEDGE_SELECT: If this bit is 1, the PMU only counts the event rising edge. If this bit is 0, the PMU counts every cycle the event is asserted (high).
35:36	RW	PMUA_COUNTER3_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
37:38	RW	PMUA_PMU_PORT_SELECT: Chooses final PMU events to feed to the counters.
39:63	RO	constant = 0b00000000000000000000000000

Register Name	PMU Counters A Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_PMULET.PMU_CNTRA_REG
Address	0000000004010815 (SCOM)
Description	The PMU counters A register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PMU_COUNTERA_0: PMU Counter 0.
16:31	ROX	PMU_COUNTERA_1: PMU Counter 1.
32:47	ROX	PMU_COUNTERA_2: PMU Counter 2.
48:63	ROX	PMU_COUNTERA_3: PMU Counter 3.

Register Name	APC Master PMU Events Select Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC1.APC_PMUSEL
Address	0000000004010816 (SCOM)
Description	Controls APC performance monitor event selections.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	APC_PMUSEL_GRPSEL: APC master PMU events group selection, valid values of 0 - 4.
4:5	RO	constant = 0b00
6:11	RW	APC_PMUSEL_FSMJ_EVENT_SEL: APC master PMU events FSMJ event selection, valid values of 0 - 9.
12	RO	constant = 0b0
13:19	RW	APC_PMUSEL_FSMJ_FSM_SEL: APC master PMU FSMJ FSM selection: Valid values of 0, 1, 8, 9, 16, 17, 24, and 25 for read FSMs. Valid values of 64, 65, 72, 73, 80, 81, 88, and 89 for write FSMs.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	Snoop PMU Events Select Register
Mnemonic	CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_PMU_EVENTS_SELECT_REG
Address	0000000004010817 (SCOM)
Description	Used for which group of events that will go on the CXA SNP PMON bus . This bus is sent to the PMU input bus MUX in XPT where further bit selection is performed on input to the PMU counters.

Bits	SCOM	Field Mnemonic: Description
0:3	WO	CXA_SNP_PMU_GROUP_SELECT: Selects which one of four snoop PMU event groups is sent. Only values 0 to 3 are used .
4:5	RO	constant = 0b00
6:11	WO	CXA_SNP_PMU_FSMJ_EVENT_SELECT: Selects which one of eight FSMJ events gets routed to the FAMJ event. Only values 0 to 7 are used.
12:13	RO	constant = 0b00
14:19	WO	CXA_SNP_PMU_FSMJ_FSM_SELECT: Selects which one of four snoop state machines will be used for FSMJ event counting. Only values of 0, 1, 2, and 3 are used.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	APC Master Power Bus Control Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC0.APCTL
Address	0000000004010818 (SCOM)
Description	Controls Power bus operations.

Bits	SCOM	Field Mnemonic: Description
0	RW	APCCTL_ENB_CRESP_EXAM: Enables APC master examining CRESPs for it. When disabled, prevents false assertion of unexpected CRESP FIR when CRESPs for PHB are seen. (APC RD FSM spoofs PHB unit ID)
1	RW	APCCTL_ADR_BAR_MODE: addr_bar_mode is set to 1 when chip = group. Small system address map. Reduces the number of group ID bits to 2 and eliminates the chip ID bits. All chips have an ID of 0. Nn scope is not available in this mode.

Bits	SCOM	Field Mnemonic: Description
2	RW	APCCTL_DISABLE_NN_RN: Disable nn_rn scope.
3	RW	APCCTL_DISABLE_VG_NOT_SYS: Disable vg_not_sys scope.
4	RW	APCCTL_DISABLE_G: Disable group scope.
5	RW	APCCTL_DISABLE_LN: Disable LN scope.
6	RW	APCCTL_SKIP_G: Skip increment to group scope. Only used by read machines.
7	RW	APCCTL_HANG_ARE: Hang on address error.
8	RW	APCCTL_HANG_DEAD: Hang on Ack_*dead.
9	RW	APCCTL_CFG_BKILL_INC: This configuration bit controls the increase of scope when a combined response of *bk_inc is received. If this bit is 0, when the scope of the command is group or remote group scope (RGS), the scope of the background kill is unchanged and the command used is bkill_inc. When the scope of the command is nodal, the scope is increased to group and the command used is bkill_inc. Otherwise, the scope of the command is unlimited, the scope is unchanged, and the command used is bkill. Note: The combined response equations do not provide an *inc combined response directive when the command scope is unlimited. If this bit is 1, the command scope used for background kill is always increased. When the new scope is group, the command used is bkill_inc. Otherwise, the command used is bkill. Initialize to 0.
10	RW	Reserved field.
11	RW	Reserved field.
12	RW	APCCTL_DISABLE_PSL_CMDQUEUE: Disable PSL command queue: 0 = PSL command queue enabled. Order of commands is restored in queue using queue. ID as write pointer. 1 = PSL command queue is disabled/bypassed. PSL can only have one command outstanding per APC machine.
13	RW	APCCTL_ENABLE_MASTER_RETRY_BACKOFF: Enable master retry backoff: 0 = Master retry backoff due to excessive rty_lpc_only is disabled 1 = Master retry backoff due to excessive rty_lpc_only is enabled
14:16	RW	SCPTGT_LFSR_MODE: Mode for LFSRs used in scope target counter logic selects count of average number of clocks before LFSR will rollover: 0 = On average every 64K clocks 1 = On average every 32K clocks 2 = On average every 16K clocks 3 = On average every 8K clocks 4 = On average every 4K clocks 5 = On average every 2K clocks 6 = On average every 1K clocks 7 = On average every 512 clocks
17	RW	APCCTL_ENABLE_RD_VG_SCOPE_PREDICT: Enable rd_vg_scope_predict: 0 = rd_vg_scope_predictor is disabled 1 = rd_vg_scope_predictor is enabled.
18	RW	Reserved field.
19:38	RO	constant = 0b00000000000000000000
39:45	RW	WR_EPSILON_VALUE: Write epsilon value.
46:55	RO	constant = 0b0000000000
56:63	RW	APCCTL_MAX_RETRY: Max Retry count. 0 = Retry forever.

Register Name	**APC Master Configuration Register**
Mnemonic	CAPP1.CXA_TOP.CXA_APC0.APCFG
Address	0000000004010819 (SCOM)
Description	Controls PHB selection, hang_poll_scale, speculative HPC state, POWER8/POWER9 mode, and addr(8:13).

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1	RW	Reserved field.
2:3	RW	APCCTL_PHB_SEL: PHB Select: 01 = PHB 10 = Alink
4:7	RW	HANG_POLL_SCALE: How many hang polls that need to be detected to indicate a hang poll to the logic.
8:12	RW	SPEC_HPC_DIR_STATE: Speculative HPC DIR state value.
13	RW	Reserved field.
14	RW	APCCTL_P9_MODE: 0 = POWER8 backwards compatibility mode, 1 = POWER9 mode.
15:20	RW	APCCTL_SYSADDR: Used for address bits 8:13 in PB commands and SNP DIR compares.
21	RW	APCCTL_MEM_SEL_MODE: Memory select mode as defined in PB Arch V4: 0 = Memory select mode 0 1 = Memory select mode 1
22	RW	APCCTL_ENB_FRC_ADDR13: Enables forcing of addr(13)=1 when P8BC mode AND mem_sel_mode=0 AND pslcmd.rfs_class != 0: 0 = Disabled 1 = Enabled
23:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	**Snoop CAPI Configuration Register**
Mnemonic	CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_CAPI_CFG_REG
Address	000000000401081A (SCOM)
Description	This register controls the configuration of the precise and coarse directories and controls other snooper functions whose setup is dependent on the discovered CAPI device.

Bits	SCOM	Field Mnemonic: Description
0	RW	CXA_SNP_ENABLE_TTYPE_DECODE: When = 1 this bit enables tType decode in the snoop pipeline. When = 0, tTypes are not decoded and the snoop pipelines are disabled.
1	RO	constant = 0b0
2:3	RW	CXA_SNP_PRECISE_DIR_SIZE: These bits control the size of the precise directory. Directory size can be further reduced by not allocating entries to a particular way.
4	RW	CXA_SNP_COARSE_DIR_ENABLE: The coarse directory must be enabled to participate in the memory coherence protocol. If the coarse directory is disabled, the effect is as if the coarse directory always misses on a search access and the results of reads and writes to coarse directory entries is unpredictable.
5	RW	CXA_SNP_COARSE_DIR_SECTORS: Coarse directory sector configuration varies under control of this bit allowing the capacity of memory covered by the directory to be either 8MB or 256MB.
6	RW	CXA_SNP_MCD_CHICKEN_SWITCH: This chicken switch is to be used only if the MCD cannot be configured to cover the address space specified by the BHR address range.

Bits	SCOM	Field Mnemonic: Description
7:11	RW	CXA_SNP_BHR_DIR_STATE: This is the directory state value used to indicate that the remote address BAR has been hit (BHR BAR hit remote).
12:13	RW	CXA_SNP_LPC_MODE: Set this field to 00. Other functions are not supported.
14:31	RO	constant = 0b0000000000000000000
32:37	RW	CXA_SNP_CT_COMPARE_VECTOR: Used to compare the CT field of COP request commands, bits 30 to 35 of address for match.
38:39	RW	CXA_SNP_PHB_FILTER_CNTL: Reserved.
40:63	RW	CXA_SNP_EPOCH_TEST_VECTOR: Used to determine epoch time outs when there are multiple way hits on the directory.

Register Name	Snoop Control Register
Mnemonic	CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_CNTL_REG
Address	000000000401081B (SCOM)
Description	This register contains CAPI device independent snooper controls and parameters.

Bits	SCOM	Field Mnemonic: Description
0	RW	CXA_SNP_READ_EPSILON_MODE: Controls which read epsilon tier is loaded into the read epsilon counter for read commands of various scopes.
1:2	RO	constant = 0b00
3:11	RW	CXA_SNP_READ_EPSILON_TIER0: Read epsilon mode controls whether this value loads the read epsilon counter tier 0.
12:14	RO	constant = 0b000
15:23	RW	CXA_SNP_READ_EPSILON_TIER1: Read epsilon mode controls whether this value loads the read epsilon counter tier 1.
24	RO	constant = 0b0
25:35	RW	CXA_SNP_READ_EPSILON_TIER2: Read epsilon mode controls whether this value loads the read epsilon counter tier 2.
36:44	RO	constant = 0b000000000
45:47	RW	CXA_SNP_ADDRESS_PIPELINE_MASTERWAIT_COUNT: Maximum number of cycles an APC master can wait before swapping the arbitration priority between APC and snooper.
48:51	RW	CXA_SNP_DATA_HANG_POLL_SCALE: Number of dhang_polls it takes to increment the dhang counter in snoop. Actual count is scale + 1. Value of 0000 = decimal 1 counts.
52:63	RO	constant = 0b000000000000

Register Name	Transport Control Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.XPT_CONTROL
Address	000000000401081C (SCOM)
Description	The transport control register contains configuration and threshold values.

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SEND_PACKET_TIMER_VALUE: The send packet timer, which is used to determine when the XPT has waited long enough for a next message to pack, is loaded from this field. The timer is used in conjunction with the CI store buffer threshold field and expires when the number of cycles specified by that field has passed. When the CI store buffer threshold is set to '11'x, the timer starts when a message is loaded into an empty buffer. When the CI store buffer threshold timer is not set to '11'x, the timer is started when a new message is loaded into a buffer and the number of CI store buffers in use is greater than the value specified by the CI store buffer threshold. When a message packet is sent, the timer is reset and is not running and the buffer is marked empty. A send packet timer value of x'000' specifies 1024 cycles.
10:13	RW	CI_STORE_BUFFER_THRESHOLD: The number of PHB0 CI store buffers in use must exceed CI store buffer threshold before the send message timer affects when XPT sends message packets (see send packet timer value). The values of this field apply as follows: 000 - 101 = Message packet is delayed until either the packet is full or the timer has expired when the number of CI store buffers in use exceeds this value. When the number of buffers in use does not exceed this value, then the message packet is not delayed and can be sent as soon as there is a break in the message send requests from the APC, Snooper, or TLBI units. 11x = Message packet is delayed until either the packet is full or the timer has expired. To disable this function set the threshold to a value of `101'. With this setting, the timer is active only when the number of in use buffers is 6, which is all of them, stopping additional packets to be sent until the CI store buffers clear out.
14:17	RW	MAX_LPC_DATA_PBH0_CI_STORE_BUFFERS: This field is the maximum number of PHB port 0 CI store buffers that can be used for LPC data packets. Six CI store buffers are available and a minimum of two are reserved for message data packets. 00 4 buffers can be used, 01 1 buffer can be used, 10 2 buffers can be used, and 11 3 buffers can be used.
18:21	RW	TLBI_DATA_POLL_PULSE_DIV: Number of data polls received before signaling TLBI hang detection timer expired.
22:25	RW	SN_WRT_DBUF_MAX_CREDIT: Defines the maximum number of snooper write data cache lines that can be sent to PSL without return of credit (LPC mode). This configuration is for the number of credits available per snooper data queue in the PSL. There is one snooper data queue per snooper in CAPP. For each snooper data queue there is a counter tracking the number of credits available. For each full or partial cache line sent, a counter is incremented for the data queue specified by the snooper sending the data. When the counter reaches the value in this field, no more cache lines can be sent and are allowed to back up into the snoopers and eventually back up onto the processor bus (no snoopers to dispatch). A value of 0 in this field means 16 credits per snooper data queue.
26:27	RW	Reserved: Reserved.
28:36	RW	SN_MSG_MAX_CREDIT: Defines the maximum number of messages (SN_snoop, SN_write, tlbi_set, ASE, APC credit consumer) that can be sent to PSL without return of credit. For each message sent requiring a credit, a counter is incremented. When the counter reaches the value in this field, no more messages can be sent which require credits. A value of 0 in this field means 512 credits. Initialized to 32.
37	RW	BENIGN_PTR_DATA: Used to indicate the format of the line sent during rTagPool flush sequence when the rfs_class = '10': 0 = Send a line of all 0 1 = Send a line of all 1
38	RW	TLBIE_STALL_EN: Enables CAPP stalling the PSL if CAPP is overflowing with TLBIs.
39:41	RW	TLBIE_STALL_THRESHOLD: The number of TLBIS pending needed before the CAPP will start the stall count. Minimum is 1 and maximum is 7.

Bits	SCOM	Field Mnemonic: Description
42:45	RW	TLBIE_STALL_CMPLT_CNT: The number of TLBIs to be completed before CAPP stops stalling the PSL. Minimum that should be set is 1 and the maximum that should be set is 8.
46:53	RW	TLBIE_STALL_DELAY_CNT: The number of cycles CAPP will wait while over threshold before actually stalling the PSL. This count is in increments of 128 cycles, up to 32K. A value of zero is invalid.
54:57	RO	constant = 0b0000
58:61	RW	XPT_CI_BUFF_MIN: Determines the lowest value CI store buffer used in the PHB.
62	RW	CI_BUFF_AVAIL: The number of CI store buffers available in the PHB: 0 = 6 buffers 1 = 14 buffers
63	WO	LOAD_CI_BUFF: Initial setup of the lowest CI store buffer used counter and PHB rtag generation.

Register Name	APC Master LCO Target Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC0.APCLCO
Address	0000000004010821 (SCOM)
Description	Controls LCO target selection.

Bits	SCOM	Field Mnemonic: Description
0:11	RW	APCLCO_TARGET_VALID: List of valid LCO targets.
12	RW	APCLCO_TARGET_ID0: Used for bit 0 of LCO target Id.
13:15	RW	APCLCO_TARGET_MIN: Minimum number of eligible LCO targets. Must be greater than or equal to the sum of valid targets.
16:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	XPT PMU Events Select Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.XPT_PMU_EVENTS_SEL
Address	0000000004010822 (SCOM)
Description	The PMU counter configuration register selects which of the 64 events will be on each bit of the PMU output bus.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	XPT_PMON_GROUP_SELECT: Selects which one of 64 XPT PMU events sources bit 0 of the 8b XPT PMU output bus.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	APC FSM Read Machine Mask Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC0.APCRDFSMMASK
Address	0000000004010823 (SCOM)
Description	Controls RD FSM that can be used in CAPP. Must match values used in PHB configuration register (TBD), CAPP Snoop PHB tTag Filter Mask Register, and PSL machine allocation register (TBD).

Bits	SCOM	Field Mnemonic: Description
0:47	RW	APC_RDFSM_MASK: List of RD FSMs used by APC.

Bits	SCOM	Field Mnemonic: Description
48:63	RO	constant = 0b0000000000000000

Register Name	PMU Counter B Configuration Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_SCOMFIR.PMU_CNTRB_CFG
Address	0000000004010824 (SCOM)
Description	The PMU counter B configuration register controls the configuration of the PMU counters.

Bits	SCOM	Field Mnemonic: Description
0	RW	PMUB_COUNTER0_ENABLE: When = 1 this bit enables PMU counter 0.
1	RW	PMUB_COUNTER1_ENABLE: When = 1 this bit enables PMU counter 1.
2	RW	PMUB_COUNTER2_ENABLE: When = 1 this bit enables PMU counter 2.
3	RW	PMUB_COUNTER3_ENABLE: When = 1 this bit enables PMU counter 3.
4:6	RW	PMUB_PRESCALER_SELECT: Determines which, if any, prescaler counter to apply to all 16bit PMU counters.
7	RW	PMUB_COUNTER_FREEZE_MODE: Indicates a counter should freeze on overflow: 0 = Free running 1 = Freeze on overflow
8	RW	PMUB_COUNTER_RESET_MODE: Indicates how counter should reset: 0 = Free running 1 = Reset on SCOM read
9:12	RW	PMUB_COUNTER0_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter 0.
13	RW	PMUB_COUNTER0_POSEDGE_SELECT: If this bit is 1, the PMU only counts the event rising edge. If this bit is 0, the PMU counts every cycle the event is asserted (high).
14:15	RW	PMUB_COUNTER0_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
16:19	RW	PMUB_COUNTER1_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter 1.
20	RW	PMUB_COUNTER1_POSEDGE_SELECT: If this bit is 1, the PMU only counts the event rising edge. If this bit is 0, the PMU counts every cycle the event is asserted (high).
21:22	RW	PMUB_COUNTER1_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
23:26	RW	PMUB_COUNTER2_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter 2.
27	RW	PMUB_COUNTER2_POSEDGE_SELECT: If this bit is 1, the PMU only counts the event rising edge. If this bit is 0, the PMU counts every cycle the event is asserted (high).
28:29	RW	PMUB_COUNTER2_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
30:33	RW	PMUB_COUNTER3_EVENT_SELECT: Indication of which of the four event pairs (eight total events) to count in counter 3.
34	RW	PMUB_COUNTER3_POSEDGE_SELECT: If this bit is 1, the PMU only counts the event rising edge. If this bit is 0, the PMU counts every cycle the event is asserted (high).
35:36	RW	PMUB_COUNTER3_BIT_PAIR_SELECT: Indicates how the event pairs should be combined to increment this PMU counter.
37:38	RW	PMUB_PMU_PORT_SELECT: Chooses final PMU events to feed to the counters.

Bits	SCOM	Field Mnemonic: Description
39:63	RO	constant = 0b00000000000000000000000000

Register Name	PMU Counters B Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_PMULET.PMU_CNTRB_REG
Address	0000000004010825 (SCOM)
Description	The PMU counters B register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PMU_COUNTERB_0: PMU counter 0.
16:31	ROX	PMU_COUNTERB_1: PMU counter 1.
32:47	ROX	PMU_COUNTERB_2: PMU counter 2.
48:63	ROX	PMU_COUNTERB_3: PMU counter 3.

Register Name	Time of Day Synchronization Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_TOD.TOD_SYNC000
Address	0000000004010826 (SCOM)
Description	Time of day synchronization register.

Bits	SCOM	Field Mnemonic: Description
0:54	RWX	TIMEBASE: Timebase register.
55:59	ROX	TIMEBASE: Timebase register.
60:63	WO	CHIP_TOD_STATUS: Chip time of day status.

Register Name	CAPP Timebase Control Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_TOD.TFMR
Address	0000000004010827 (SCOM)
Description	Time facility management register (TFMR)

Bits	SCOM	Field Mnemonic: Description
0:7	RW	Reserved field.
8:9	RW	Reserved field.
10	RW	Reserved field.
11:13	RW	Reserved field.
14	RW	Reserved field.
15	RW	Reserved field.
16	RWX	Reserved field.
17	RWX	Reserved field.
18	RWX	Reserved field.
19	RWX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
20	RWX	Reserved field.
21	RWX	Reserved field.
22	RWX	Reserved field.
23	RWX	Reserved field.
24	WOX	Reserved field.
25:26	RO	constant = 0b00
27	WOX_CLEAR	Reserved field.
28:31	ROX	Reserved field.
32:35	ROX	Reserved field.
36:39	RO	constant = 0b0000
40	ROX	Reserved field.
41	ROX	Reserved field.
42	ROX	Reserved field.
43	WOX_CLEAR	Reserved field.
44	WOX_CLEAR	Reserved field.
45	WOX_CLEAR	Reserved field.
46	WOX_CLEAR	Reserved field.
47:50	ROX	CHIP_TOD_STATUS: Chip time of day status.
51	ROX	Reserved field.
52:59	RO	constant = 0b00000000
60	WOX_CLEAR	Reserved field.

Register Name	Snoop Array Address Register
Mnemonic	CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ARRAY_ADDR_REG
Address	0000000004010828 (SCOM)
Description	Used to SCOM read and write of the SNP arrays.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RWX	CXA_SNP_ARRAY_ADDRESS: SNP SCOM array address.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Snoop Array Read Register
Mnemonic	CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ARRAY_READ_REG
Address	0000000004010829 (SCOM)
Description	Holds data read via SCOM of the SNP arrays.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	CXA_SNP_ARRAY_READ_DATA: SNP SCOM array read data.

Register Name	APC Master Array Address Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC1.APC_ARRY_ADDR
Address	000000000401082A (SCOM)
Description	Holds the address for array access 2 instances of CRESP arrays to get the four read ports. A write to either instance writes to both. A read only reads from one instance. encd_array_select: CRESP read copy0/write copies 0-1 for decodes = 0x0 through 0x5. uOP read/write for decode = 0x6. CRESP read copy1/write copies 0-1 for decodes = 0x8 through 0xC. array_address: address for selected array. This register increments on each access initiated by read.write to apc_arry_data register.

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant = 0b00
2:11	RWX	APCARY_ADDRESS: Address for APC master array access. Note: Due to the number of ports required, there are two identical copies of the CRESP arrays. The bits are parsed according to the range as follows: 0x000 – 0x15F: CRESP arrays (writes both copies, reads copy 0). 2:5 Array select. 6:11 Row address. 0x160 – 0x17F: Reserved (instantiated but unused). 0x180 – 0x1BF: APC master uOP table array. 2:5 Array select (= 0110). 6:11 Row address; this is the psl_ttype(0:5). 0x1C0 – 0x1FF: Reserved. 0x200 – 0x35F: CRESP arrays (writes both copies, reads copy 1). 2:5 Array select. 6:11 Row address. 0x360 – 0x37F: Reserved (instantiated but unused). 0x380 – 0x3FF: Reserved.
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	APC Master Array Read Data Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC1.APC_ARRY_RDDATA
Address	000000000401082B (SCOM)
Description	Holds read data for array access. Read from array reads data from this register. Address used is in register apc_arry_addr. Address is auto-incremented when write/read operation completes.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	APCARY_RDDATA: Read data for APC master array access.

Register Name	CAPP Epoch and Recovery Timers Control Register
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_EPT.CAPP_EPOCH_AND_RECOVERY_TMR_CONTROL
Address	000000000401082C (SCOM)
Description	The epoch and recovery timers control register contains the enables and period controls for the epoch and recovery timers.

Bits	SCOM	Field Mnemonic: Description
0	RW	EPOCH_TIMER_ENABLE: When = 1, the epoch timer is enabled, otherwise it is disabled.
1	RW	RECOVERY_TIMER_ENABLE: When = 1, the recovery timer is enabled, otherwise it is disabled.

Bits	SCOM	Field Mnemonic: Description
2:31	RO	constant = 0b00000000000000000000000000000000
32:47	RW	EPOCH_TIMER_PERIOD_MASK: The mask determines the timer period. The mask and timer incrementers are bitwise ORed and AND reduced. When the output of the AND is 1, the timer has expired. By filling in the mask with ones from the most-significant bit toward the least, the timer pulse is divided by powers of 2. If zeros are placed between ones in the mask, the timer divider will be non-uniform.
48:63	RW	RECOVERY_TIMER_PERIOD_MASK: The mask determines the timer period. The mask and timer incrementers are bitwise ORed and AND reduced. When the output of the AND is 1, the timer has expired. By filling in the mask with ones from the most-significant bit toward the least, the timer pulse is divided by powers of 2. If zeros are placed between ones in the mask, the timer divider will be non-uniform.

Register Name	PHB TTAG Filter Register
Mnemonic	CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_PHB_TTAG_FILTER_REG
Address	0000000004010831 (SCOM)
Description	This register is used to define which of the 48 APC FSMs read machines are available for use and therefore which TTAGs to care about.

Bits	SCOM	Field Mnemonic: Description
0:47	RW	CXA_SNP_PHB_TTAG_FILTER: For APC FSMs 0 to 47, set each bit to 1 for each queue that is available to CAPP for use .
48:63	RO	constant = 0b0000000000000000

Register Name	Snoop Array Write Register
Mnemonic	CAPP1.CXA_TOP.CXA_SNPFE.SNP_REGS.CXA_SNP_ARRAY_WRITE_REG
Address	0000000004010841 (SCOM)
Description	SCOM write data for SNP arrays.

Bits	SCOM	Field Mnemonic: Description
0:63	WO	CXA_SNP_ARRAY_WRITE_DATA: SNP SCOM array write data.

Register Name	APC Master Array Write Data Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC1.APC_ARRY_WRDATA
Address	0000000004010842 (SCOM)
Description	Holds write data for array access write to array writes data to this register. Address used is in register apc_arry_addr. Address is auto-incremented when write/read operation completes.

Bits	SCOM	Field Mnemonic: Description
0:63	WOX	APCARY_WRDATA: Write data for APC master array access.

Register Name	Flush uOP Configuration Register
Mnemonic	CAPP1.CXA_TOP.CXA_APC1.DFSUOP1
Address	0000000004010843 (SCOM)
Description	UOP1 word used during directory flush.

Bits	SCOM	Field Mnemonic: Description
0:55	RW	DFSUOP1_WORD: UOP1 word used during directory flush.
56:63	RO	constant = 0b00000000

Register Name	AS Endpoint Tuple Register 0
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE0
Address	0000000004010846 (SCOM)
Description	AS endpoint tuple register 0 .

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RWX	ASE_TUPLE0_LPID: lpid(0:11) for ASE tuple0 register.
16:19	RO	constant = 0b0000
20:39	RWX	ASE_TUPLE0_PID: pid(0:15) for ASE tuple0 register .
40:43	RO	constant = 0b0000
44:59	RWX	ASE_TUPLE0_TID: tid(0:15) for ASE tuple0 register .
60:62	RO	constant = 0b000
63	RWX	ASE_TUPLE0_VALID: Valid for ASE tuple0 register.

Register Name	AS Endpoint Tuple Register 1
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE1
Address	0000000004010847 (SCOM)
Description	AS endpoint tuple register 1.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RWX	ASE_TUPLE1_LPID: lpid(0:11) for ASE tuple1 register.
16:19	RO	constant = 0b0000
20:39	RWX	ASE_TUPLE1_PID: pid(0:15) for ASE tuple1 register.
40:43	RO	constant = 0b0000
44:59	RWX	ASE_TUPLE1_TID: tid(0:15) for ASE tuple1 register.
60:62	RO	constant = 0b000
63	RWX	ASE_TUPLE1_VALID: Valid for ASE tuple1 register.

Register Name	AS Endpoint Tuple Register 2
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE2
Address	0000000004010848 (SCOM)
Description	AS endpoint tuple register 2.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RWX	ASE_TUPLE2_LPID: lpid(0:11) for ASE tuple2 register.
16:19	RO	constant = 0b0000
20:39	RWX	ASE_TUPLE2_PID: pid(0:15) for ASE tuple2 register.
40:43	RO	constant = 0b0000
44:59	RWX	ASE_TUPLE2_TID: tid(0:15) for ASE tuple2 register.
60:62	RO	constant = 0b000
63	RWX	ASE_TUPLE2_VALID: valid for ASE tuple2 register.

Register Name	AS Endpoint Tuple Register 3
Mnemonic	CAPP1.CXA_TOP.CXA_XPT.XPT_AS.ASE_TUPLE3
Address	0000000004010849 (SCOM)
Description	AS endpoint tuple register 3.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:15	RWX	ASE_TUPLE3_LPID: lpid(0:11) for ASE tuple3 register.
16:19	RO	constant = 0b0000
20:39	RWX	ASE_TUPLE3_PID: pid(0:15) for ASE tuple3 register.
40:43	RO	constant = 0b0000
44:59	RWX	ASE_TUPLE3_TID: tid(0:15) for ASE tuple3 register.
60:62	RO	constant = 0b000
63	RWX	ASE_TUPLE3_VALID: Valid for ASE tuple3 register.

Register Name	PCI PBCQ Hardware Configuration Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.PBCQHWCFG_REG
Address	0000000004010C00 (SCOM)
Description	PCI PBCQ hardware configuration register.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	HANG_POLL_SCALE: How many hang polls that need to be detected to indicate a hang poll to the logic.
4:7	RW	HANG_DATA_SCALE: How many data polls that need to be detected to indicate a data poll to the logic.
8:11	RW	HANG_PE_SCALE: How many data polls that need to be detected to indicate a PE poll to the logic. A PE poll is created by the PCIi unit to detect hangs of SMs while waiting on exchanges with the PCI logic.
12	RW	PE_BLOCK_CQPB_PB_INIT: When set, PCI to PB data movement ignores the PB initial signal. When not set, PCI to PB data movement will stop on cache line boundaries.
13	RW	DISABLE_RCMD_CLKGATE: Chicken switch to turn off the clock gating that occurs on a rcmd when the command is not for the PE.
14	RW	PE_HANG_SM_ON_ARE: Controls processor bus master state machines when an ARE is received.
15	RW	PE_DISABLE_PCI_CLK_CHECK: Disables the logic that checks valid PCI clocks (FIR bit 15).

Bits	SCOM	Field Mnemonic: Description
16	RW	LFSR_ARB_MODE: 1=use LFSR in outbound arbitration.
17	RW	PE_ENABLE_DMAR_IOPACING: Allow I/O pacing scheme for DMA read operations.
18	RW	PE_ENABLE_DMAW_IOPACING: Allow I/O pacing scheme for DMA write operations.
19	RW	PE_ADR_BAR_MODE: Address mode register for PE unit.
20	RW	PE_STQ_ALLOCATION: Queue allocation between stores and p2p: 0 = stq_1_reserved for each type, the rest floating 1 = stq_1_only Only one queue used for all traffic. The remaining seven are unused.
21	RW	DISABLE_LPC_CMDS: Disable LPC acknowledgment for commands that the PE does not service.
22	RW	PE_DISABLE_OOO_MODE: PE order OOO type CI stores like a normal CI store command.
23:26	RW	PE_OSMB_EARLY_START: Determines how much overlap of reading/writing the OSMB allows: 0b0000 = Most conservative, full packet written in before signaling PCI side 0b0001 = Most conservative, full packet written in before signaling PCI side 0b0010 = Start 2 writes from the end of the packet 0b0011 = Start 3 writes from the end of the packet 0b0100 = Start 4 writes from the end of the packet 0b0101 = Start 5 writes from the end of the packet 0b0110 = Start 6 writes from the end of the packet 0b0111 = Start 7 writes from the end of the packet 0b1000 = Most aggressive, start 8 writes from the end of the packet, before any data written 0b1111 = Extra aggressive, start before any data written (that is, when the command is written
27:28	RW	PE_QFIFO_HOLD_MODE: Determines how much overlap of reading/writing the OSMB allows: 0b00 = Stop sending outbound commands when QFIFO is full(default) 0b01 = Stop sending outbound commands when QFIFO has 1 entry empty 0b10 = Stop sending outbound commands when QFIFO has 3 entry empty 0b11 = Ignore QFIFO count when sending outbound packets
29:31	RW	Reserved field.
32	RW	PE_WR_STRICT_ORDER_MODE: Strictly order inbound write commands, independent of node ID.
33	RW	PE_CHANNEL_STREAMING_EN: Enable processor bus channel streaming operations.
34:35	RW	PE_WR_CACHE_INJECT_MODE: Mode bits for controlling processor bus cCache inject: DisableCacheInj(00) = Disable all cache injections(debug only) LegacyCacheInj(01) = Cache inject after a addr_hpc_ack combined response TLPHintCacheInj(10) = Start with cache inject if TLP hints indicate cache inject (TLP hints non-zero) P9ModetCacheInj(11) = Start with cache inject unconditionally
36	RW	PE_ENABLE_NEW_FLOW_CACHE_INJECT: Start new flows on PE to send cache inject commands.
37	RW	PE_DISABLE_INJ_ON_RESEND: Controls cache inject on resends when other cache inject modes are disabled.
38	RW	PE_FORCE_DISABLED_CTAG_TO_FOLLOW_FLOW: When CTAGs are disable, forces DMA writes to still use flows for non-ordering reasons.
39	RW	PE_ENABLE_ENH_FLOW: Controls cache inject on resends when other cache inject modes are disabled.
40	RW	Reserved field.
41	RW	PE_DISABLE_WR_VG: Force all DMA write requests to system scope when they progress to VG scope.
42	RW	PE_DISABLE_WR_SCOPE_GROUP: Disable group scope on DMA write requests.
43	RW	PE_DISABLE_INTWR_VG: Force all initial write requests to system scope when they progress to VG scope.
44	RW	PE_DISABLE_INTWR_SCOPE_GROUP: Disable group scope on initial write requests.
45	RW	PE_DISABLE_INTWR_SCOPE_NODE: Disable node scope on initial write requests.
46:47	RW	Reserved field.

Bits	SCOM	Field Mnemonic: Description
48:49	RW	PE_RD_WRITE_ORDERING: Ordering modes for reads verses writes: NodeMatch(110) = All non-write commands wait behind all writes that match its node AnyNode(111) = All non-write commands wait behind all writes All others are reserved.
50	RW	PE_DISABLE_RD_SCOPE_NODAL: Disable nodal scope on non-TCE DMA read requests.
51	RW	PE_DISABLE_RD_SCOPE_GROUP: Disable group scope on non-TCE DMA read requests.
52	RW	PE_DISABLE_RD_SCOPE_RNNN: Disable RN and Nn scopes on non-TCE DMA read requests.
53	RW	PE_ENABLE_RD_SKIP_GROUP: Skip group scope on non-TCE DMA read requests.
54	RW	PE_DISABLE_RD_VG: Use VG(sys) when at VG scope.
55	RW	PE_DISABLE_TCE_SCOPE_NODAL: Disable nodal scope on non-TCE DMA read requests.
56	RW	PE_DISABLE_TCE_SCOPE_GROUP: Disable group scope on non-TCE DMA read requests.
57	RW	PE_DISABLE_TCE_SCOPE_RNNN: Disable RnNn scopes on non-TCE DMA read requests.
58	RW	PE_ENABLE_TCE_SKIP_GROUP: Skip group scope on TCE DMA read requests.
59	RW	PE_DISABLE_TCE_VG: Use Vg(sys) when at VG scope.
60	RW	PE_DISABLE_TCE_ARBITRATION: Disable preferential TCE read request arbitration.
61	RW	PE_DISABLE_CQ_TCE_ARBITRATION: Disable preferential TCE read response arbitration.
62	RW	PE_DISABLE_MC_PREFETCH: Disable setting PADE bits in cl_rd_nc requests.
63	RW	PE_IGNORE_SFSTAT: Controls DMA read state machine behavior when receiving SFSTAT.

Register Name	Drop Priority Control Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.DRPPRICTL_REG
Address	0000000004010C01 (SCOM)
Description	Drop priority control register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	PE_DROPPRIORITYMASK: Mask value to determine when a rty_drp will cause the priority to increment on the next request (enable_IO_cmd_pacing = 0) or the DropPaceCounter will be incremented based on dep(enable_IO_cmd_pacing = 1). When LSFR bits match mask drop priority, one of these two actions will be taken (DMA write commands only).
6	RW	PE_ENABLE_CTAG_DROP_PRIORITY: Allow commands in a CTAG stream to take the priority of previous rty_drp commands in the stream. If not set, each commands priority is sent independently.
7	RW	PE_ENABLE_IO_CMD_PACING: When a rty_drop CRESP is received, keep drop priority constant and lower command rate until the pacing count is reached. Pacing counter is incremented instead. When not set, drop priority is raised when DropPriorityMask = LSFR value.
8:16	RW	PE_DROPPACECOUNT: Value to use when determining if drop priority should be increased when I/O command pacing is enabled. When the drop priority counter reaches this value, the drop priority is increased (enable_IO_cmd_pacing = 1). Not used when enable_IO_cmd_pacing = 0.
17:22	RW	PE_DROPPACEINC: Value to use when determining how much drop pace count should increase when a retry drop CRESP occurs. Not used when enable_IO_cmd_pacing = 0.

Bits	SCOM	Field Mnemonic: Description
23:25	RW	PE_RTYDROPDIVIDER: Value used to divide down rty_drp combined responses before invoking drop priority: 000/001 = 1st retry drop combined response will invoke drop priority mechanism 010 = 2nd retry drop combined response will invoke drop priority mechanism 011 = 3rd retry drop combined response will invoke drop priority mechanism 100 = 4th retry drop combined response will invoke drop priority mechanism 101 = 5th retry drop combined response will invoke drop priority mechanism 110 = 6th retry drop combined response will invoke drop priority mechanism 111 = 7th retry drop combined response will invoke drop priority mechanism
26:63	RO	constant = 0b00000000000000000000000000000000000000000

Register Name	PBCQ Error Inject Control Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.PBCQEINJ_REG
Address	0000000004010C02 (SCOM)
Description	PBCQ error inject control register.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PE_ECC_INJECT_TYPE: Determines the type of ECC error injected: 01 = Correctable error/Parity error 10 = Uncorrectable error 11 = Special uncorrectable error
2	RW	PE_CQ_ECC_INJECT_ENABLE: Enable ECC inject on CQ arrays.
3:6	RW	PE_CQ_SRAM_ARRAY: Determines which CQ SRAM array to force the ECC error into: 0000 = CI store 00:63 0001 = CI store 64:127 0010 = DMA read 00:63 0011 = DMA read 64:127 1000 = DMA write 00:63 1001 = DMA write 64:127 1010 = CI load 00:63 1011 = CI load 64:127
7	RW	PE_CQ_PAR_INJECT_ENABLE: Enable parity inject on CQ arrays.
8:10	RW	PE_CQ_REGISTER_ARRAY: Determines which CQ SRAM array to force the ECC error into: 000 = PBCQ array 001 = TTAG 010 = RTAG 011 = Outbound SMB 100 = CQPB DMAR 101 = CQPB DMAW 110 - 111 = Reserved
11	RW	PE_CONSTANT_EINJ: 1=constant error inject, 0=one hot error inject
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Clock Trace Control Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.NESTTRC_REG
Address	0000000004010C03 (SCOM)
Description	PCI nest clock trace control register.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	Reserved field.
4:7	RW	Reserved field.
8:11	RW	Reserved field.
12:15	RW	Reserved field.
16	RW	Reserved field.
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	PBCQ Performance Monitor Control Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.PMONCTL_REG
Address	0000000004010C04 (SCOM)
Description	PBCQ performance monitor control register.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	PE_PERFMON_EN: Enable performance monitor outputs per bit.
32:33	RW	PE_PERFMON_READ_TYPE: 00: DMA read events count TCE or DMA read requests: 01 = DMA read events count only TCE requests 10 = DMA read events count only DMA read requests 11 = Reserved, behavior unpredictable
34:35	RW	Reserved field.
36:39	RW	PE_PMON_MUX_BYTE0: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110 = Group 6 0111-1111 = Reserved, behavior unpredictable
40:43	RW	PE_PMON_MUX_BYTE1: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110 = Group 6 0111-1111 = Reserved, behavior unpredictable
44:47	RW	PE_PMON_MUX_BYTE2: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110 = Group 6 0111-1111 = Reserved, behavior unpredictable

Bits	SCOM	Field Mnemonic: Description
48:51	RW	PE_PMON_MUX_BYTE3: 0000: Group 0; 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110 = Group 6 0111-1111 = Reserved, behavior unpredictable
52:63	RO	constant = 0b000000000000

Register Name	PBCQ Tunnel BAR Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.TUNNEL_BAR_REG
Address	0000000004010C05 (SCOM)
Description	Tunnel bar for the return address of a tunneled packet.

Bits	SCOM	Field Mnemonic: Description
0:42	RW	PE_TUNNEL_BAR: Tunnel bar for the return address of a tunneled packet.
43:59	RO	constant = 0b00000000000000000

Register Name	PBCQ Predictive Vector Timeout Mask Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.PREDV_REG
Address	0000000004010C06 (SCOM)
Description	Predictive vector timeout mask register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PE_RD_PREDV_TIMEOUT_MASK: Predictive target timeout for reads.
8:15	RW	PE_WR_PREDV_TIMEOUT_MASK: Predictive target timeout for writes.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PE CAPP Control Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.PECAPP_CNTL_REG
Address	0000000004010C07 (SCOM)
Description	PE CAPP control register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_CAPP_EN: Enable CAPP mode of operation.
1	RW	PE_CAPP_P8_MODE: Enable CAPP mode of operation.
2:11	RW	Reserved.
12:15	RW	PE_CAPP_NUM_MSG_ENG: Number of store queue assigned to CAPP for messages. Assigned 15->2 or 7->2 depending on configuration.
16:63	RW	PE_CAPP_APC_ENG: 48 bit vector to assign read queues to CAPP APC engines.

Register Name	PCI Nest FIR Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIR_REG
Address	0000000004010C40 (SCOM) 0000000004010C41 (SCOM1) 0000000004010C42 (SCOM2)
Description	PCI nest FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RWX	WOX_AND	WOX_OR	NFIRNFIR: PCI nest FIR NFIR.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIRMASK_REG
Address	0000000004010C43 (SCOM) 0000000004010C44 (SCOM1) 0000000004010C45 (SCOM2)
Description	PCI nest FIR mask register: 0 = No Mask 1 = Mask Error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RW	WO_AND	WO_OR	NFIRMASK: PCI nest FIR mask.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIRACTION0_REG
Address	0000000004010C46 (SCOM)
Description	PCI nest FIR action0 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION0: Action0 select for corresponding bit in FIR. (Action0,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No Action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action1 Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIRACTION1_REG
Address	0000000004010C47 (SCOM)
Description	PCI nest FIR action1 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION1: Action1 select for corresponding bit in FIR. (Action1,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR WOF Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.NFIRWOF_REG
Address	0000000004010C48 (SCOM)
Description	PCI nest FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX_WCLRREG	Reserved.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CERR Report Hold Register 0
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.CERR_RPT0_REG
Address	0000000004010C4A (SCOM)
Description	CERR report hold register 0.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	CERR Report Hold Register 1
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.CERR_RPT1_REG
Address	0000000004010C4B (SCOM)
Description	CERR report hold register 1.

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	Reserved.
17:47	RO	constant = 0b00000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.CQSTAT_REG
Address	0000000004010C4C (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	PE_INBOUND_ACTIVE: Inbound (PCIE->PB) state machines are active.
1	ROX	PE_OUTBOUND_ACTIVE: Outbound (PB->PCIE) state machines are active.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.PBCQMODE_REG
Address	0000000004010C4D (SCOM)
Description	PBCQ general status register

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_PEER2PEER_MODDE: Enable peer to peer operations.
1	RW	PE_ENHANCED_PEER2PEER_MODDE: Enable enhanced peer to peer operations.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR0_REG
Address	0000000004010C4E (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR0: PE bus I/O base address register 0. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR0_MASK_REG
Address	0000000004010C4F (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK0: PE bus I/O base address register mask 0. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR1_REG
Address	0000000004010C50 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR1: PE bus I/O Base Address Register 1. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR1_MASK_REG
Address	0000000004010C51 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK1: PE bus I/O base address register mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus PHB Base Address Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.PHBBAR_REG
Address	0000000004010C52 (SCOM)
Description	PE bus PHB base address register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	PE_PHB_BAR: PE bus PHB base address register. Bits 8 to 49 of the base address range are specified with this LDial. Bits 8 to 49 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is not a mask.
42:63	RO	constant = 0b00000000000000000000

Register Name	PE Bus Initial Base Address Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.INTBAR_REG
Address	0000000004010C53 (SCOM)
Description	PE Bus initial base address register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_INT_BAR: PE bus initial base address register. Bits 8 to 35 of the base address range are specified with this LDial. Bits 8 to 35 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for int space which is fixed at 256M, so there is not a mask.
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PE BAR Enables Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.BARE_REG
Address	0000000004010C54 (SCOM)
Description	PE BAR enables register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_MMIO_BAR0_EN: PE MMIO base address register 0 enable. Each BAR/Mask set has one enable bit.
1	RW	PE_MMIO_BAR1_EN: PE MMIO base address register 1 enable. Each BAR/Mask set has one enable bit.
2	RW	PE_PHB_BAR_EN: PE PHB base address register enable. Each BAR/Mask set has one enable bit.
3	RW	PE_INT_BAR_EN: PE initial base address register enable. Each BAR/Mask set has one enable bit.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Data Freeze Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#0.REGS.PE_DFREEZE_REG
Address	0000000004010C55 (SCOM)
Description	PCI nest data freeze register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_DFREEZE: Dfreeze select for corresponding bit in FIR: (dfreeze,Mask) = Action Select (1) = data freeze if action0:1=b11 (0) = data freeze if action0:1=b11 and freeze occurs before data is received
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.NFIR_REG
Address	0000000004010C80 (SCOM) 0000000004010C81 (SCOM1) 0000000004010C82 (SCOM2)
Description	PCI nest FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RWX	WOX_AND	WOX_OR	NFIRNFIR: PCI nest FIR NFIR.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.NFIRMASK_REG
Address	0000000004010C83 (SCOM) 0000000004010C84 (SCOM1) 0000000004010C85 (SCOM2)
Description	PCI nest FIR mask register 0 = No mask 1 = Mask error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RW	WO_AND	WO_OR	NFIRMASK: PCI nest FIR mask.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.NFIRACTION0_REG
Address	0000000004010C86 (SCOM)
Description	PCI nest FIR action0 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION0: Action0 select for corresponding bit in FIR. (Action0,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No Action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action1 Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.NFIRACTION1_REG
Address	0000000004010C87 (SCOM)
Description	PCI nest FIR action1 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION1: Action1 select for corresponding bit in FIR. (Action1,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No Action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR WOF Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.NFIRWOF_REG
Address	0000000004010C88 (SCOM)
Description	PCI nest FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX_WCLRREG	Reserved.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CERR Report Hold Register 0
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.CERR_RPT0_REG
Address	0000000004010C8A (SCOM)
Description	CERR report hold register 0.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	CERR Report Hold Register 1
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.CERR_RPT1_REG
Address	0000000004010C8B (SCOM)
Description	CERR report hold register 1.

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	Reserved.
17:47	RO	constant = 0b00000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.CQSTAT_REG
Address	0000000004010C8C (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	PE_INBOUND_ACTIVE: Inbound (PCIE->PB) state machines are active.
1	ROX	PE_OUTBOUND_ACTIVE: Outbound (PB->PCIE) state machines are active.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.PBCQMODE_REG
Address	0000000004010C8D (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_PEER2PEER_MODDE: Enable peer to peer operations.
1	RW	PE_ENHANCED_PEER2PEER_MODDE: Enable enhanced peer to peer operations.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR0_REG
Address	0000000004010C8E (SCOM)
Description	PE bus MMIO base address register 0

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR0: PE bus I/O base address register 0. Bits 8 to 47 of the base address range are specified with this Ldial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR0_MASK_REG
Address	0000000004010C8F (SCOM)
Description	PE bus MMIO base address register 0

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK0: PE bus I/O base address register mask 0. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range. sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR1_REG
Address	0000000004010C90 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR1: PE bus I/O base address register 1. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR1_MASK_REG
Address	0000000004010C91 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK1: PE bus I/O base address register mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus PHB Base Address Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.PHBBAR_REG
Address	0000000004010C92 (SCOM)
Description	PE bus PHB base address register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	PE_PHB_BAR: PE bus PHB base address register. Bits 8 to 49 of the base address range are specified with this LDial. Bits 8 to 49 of a snoop address are compared with this Base Address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is not a mask.
42:63	RO	constant = 0b00000000000000000000

Register Name	PE Bus Initial Base Address Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.INTBAR_REG
Address	0000000004010C93 (SCOM)
Description	PE bus initial base address register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_INT_BAR: PE bus initial base address register. Bits 8 to 35 of the base address range are specified with this Ldial. Bits 8 to 35 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for initial space which is fixed at 256M, so there is not a mask.
28:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	PE BAR Enables Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.BARE_REG
Address	0000000004010C94 (SCOM)
Description	PE BAR enables register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_MMIO_BAR0_EN: PE MMIO base address register 0 enable. Each BAR/Mask set has one enable bit.
1	RW	PE_MMIO_BAR1_EN: PE MMIO base address register 1 enable. Each BAR/Mask set has one enable bit.
2	RW	PE_PHB_BAR_EN: PE PHB base address register enable. Each BAR/Mask set has one enable bit.
3	RW	PE_INT_BAR_EN: PE initial base address register enable. Each BAR/Mask set has one enable bit.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Data Freeze Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#1.REGS.PE_DFREEZE_REG
Address	0000000004010C95 (SCOM)
Description	PCI nest data freeze register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_DFREEZE: Dfreeze select for corresponding bit in FIR. (dfreeze,Mask) = Action Select (1) = Data freeze if action0:1=b11 (0) = Data freeze if action0:1=b11 and freeze occurs before data is received
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.NFIR_REG
Address	0000000004010CC0 (SCOM) 0000000004010CC1 (SCOM1) 0000000004010CC2 (SCOM2)
Description	PCI nest FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RWX	WOX_AND	WOX_OR	NFIRNFIR: PCI nest FIR NFIR.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.NFIRMASK_REG
Address	0000000004010CC3 (SCOM) 0000000004010CC4 (SCOM1) 0000000004010CC5 (SCOM2)
Description	PCI nest FIR mask register: 0 = No mask 1 = Mask error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RW	WO_AND	WO_OR	NFIRMASK: PCI nest FIR Mask.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION0_REG
Address	0000000004010CC6 (SCOM)
Description	PCI nest FIR Action0 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION0: Action0 select for corresponding bit in FIR. (Action0,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b000000000000000000000000000000000000

Register Name	PCI Nest FIR Action1 Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION1_REG
Address	0000000004010CC7 (SCOM)
Description	PCI nest FIR action1 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION1: Action1 select for corresponding bit in FIR. (Action1,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b000000000000000000000000000000000000

Register Name	PCI Nest FIR WOR Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.NFIRWOF_REG
Address	0000000004010CC8 (SCOM)
Description	PCI nest FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX_WCLRREG	Reserved.
30:63	RO	constant = 0b000000000000000000000000000000000000

Register Name	CERR Report Hold Register 0
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.CERR_RPT0_REG
Address	0000000004010CCA (SCOM)
Description	CERR report hold register 0.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	CERR Report Hold Register 1
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.CERR_RPT1_REG
Address	0000000004010CCB (SCOM)
Description	CERR report hold register1.

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	Reserved.
17:47	RO	constant = 0b00000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.CQSTAT_REG
Address	0000000004010CCC (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	PE_INBOUND_ACTIVE: Inbound (PCIE->PB) state machines are active.
1	ROX	PE_OUTBOUND_ACTIVE: Outbound (PB->PCIE) state machines are active.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.PBCQMODE_REG
Address	0000000004010CCD (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_PEER2PEER_MODDE: Enable peer to peer operations.
1	RW	PE_ENHANCED_PEER2PEER_MODDE: Enable enhanced peer-to-peer operations.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_REG
Address	0000000004010CCE (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR0: PE bus I/O base address register 0. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_MASK_REG
Address	0000000004010CCF (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK0: PE bus I/O base address register mask 0. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_REG
Address	0000000004010CD0 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR1: PE bus I/O base address register 1. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this Base Address after ANDing bits 8 to 47 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_MASK_REG
Address	0000000004010CD1 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK1: PE bus I/O base address register mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus PHB Base Address Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.PHBBAR_REG
Address	0000000004010CD2 (SCOM)
Description	PE bus PHB base address register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	PE_PHB_BAR: PE bus PHB base address register. Bits 8 to 49 of the base address range are specified with this LDial. Bits 8 to 49 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is not a mask.

Bits	SCOM	Field Mnemonic: Description
42:63	RO	constant = 0b00000000000000000000

Register Name	PE Bus Initial Base Address Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.INTBAR_REG
Address	0000000004010CD3 (SCOM)
Description	PE Bus initial base address register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_INT_BAR: PE bus initial base address register. Bits 8 to 35 of the base address range are specified with this LDial. Bits 8 to 35 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for initial space which is fixed at 256M, so there is not a mask.
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PE BAR Enables Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.BARE_REG
Address	0000000004010CD4 (SCOM)
Description	PE BAR enables register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_MMIO_BAR0_EN: PE MMIO base address register 0 enable. Each BAR/Mask set has one enable bit.
1	RW	PE_MMIO_BAR1_EN: PE MMIO base address register 1 enable. Each BAR/Mask set has one enable bit.
2	RW	PE_PHB_BAR_EN: PE PHB base address register enable. Each BAR/Mask set has one enable bit.
3	RW	PE_INT_BAR_EN: PE initial base address register enable. Each BAR/Mask set has one enable bit.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Data Freeze Register
Mnemonic	PE0.PB0.PBCQ.PEPBREGS.STACK#2.REGS.PE_DFREEZE_REG
Address	0000000004010CD5 (SCOM)
Description	PCI nest data freeze register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_DFREEZE: Dfreeze select for corresponding bit in FIR. (dfreeze,Mask) = Action Select (1) = Data freeze if action0:1=b11 (0) = Data freeze if action0:1=b11 and freeze occurs before data is received
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI PBCQ Hardware Configuration Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.PBCQHWCFG_REG
Address	0000000004011000 (SCOM)
Description	PCI PBCQ hardware configuration register.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	HANG_POLL_SCALE: How many hang polls that need to be detected to indicate a hang poll to the logic.
4:7	RW	HANG_DATA_SCALE: How many data polls that need to be detected to indicate a data poll to the logic.
8:11	RW	HANG_PE_SCALE: How many data polls that need to be detected to indicate a PE poll to the logic. A PE poll is created by the PCI unit to detect hangs of SMs while waiting on exchanges with the PCI logic.
12	RW	PE_BLOCK_CQPB_PB_INIT: When set, PCI to PB data movement ignores the PB initial signal. When not set, PCI to PB data movement will stop on cache line boundaries.
13	RW	DISABLE_RCMD_CLKGATE: Chicken switch to turn off the clock gating which occurs on rcmd when the command is not for PE.
14	RW	PE_HANG_SM_ON_ARE: Controls processor bus master state machines when an ARE is received.
15	RW	PE_DISABLE_PCI_CLK_CHECK: Disables the logic that checks valid PCI clocks (FIR bit 15).
16	RW	LFSR_ARB_MODE: 1 = Use LFSR in outbound arbitration.
17	RW	PE_ENABLE_DMAR_IOPACING: Allow I/O pacing scheme for DMA read operations.
18	RW	PE_ENABLE_DMAW_IOPACING: Allow I/O pacing scheme for DMA write operations.
19	RW	PE_ADR_BAR_MODE: Address mode register for PE unit.
20	RW	PE_STQ_ALLOCATION: Queue allocation between stores and p2p: 0 = stq_1_Reserved for each type, the rest floating 1 = stq_1_only. Only 1 queue is used for all traffic. The remaining 7 are unused.
21	RW	DISABLE_LPC_CMDS: Disable LPC acknowledgment for commands that the PE does not service.
22	RW	PE_DISABLE_OOO_MODE: PE order OOO type CI stores like a normal CI store command.
23:26	RW	PE_OSMB_EARLY_START: Determines how much overlap of reading/writing the OSMB allows: 0b0000 = Most conservative, full packet written in before signaling PCI side 0b0001 = Most conservative, full packet written in before signaling PCI side 0b0010 = Start 2 writes from the end of the packet 0b0011 = Start 3 writes from the end of the packet 0b0100 = Start 4 writes from the end of the packet 0b0101 = Start 5 writes from the end of the packet 0b0110 = Start 6 writes from the end of the packet 0b0111 = Start 7 writes from the end of the packet 0b1000 = Most aggressive, start 8 writes from the end of the packet, before any data written 0b1111 = Extra aggressive, start before any data written (that is, when command is written)
27:28	RW	PE_QFIFO_HOLD_MODE: Determines how much overlap of reading/writing the OSMB allows: 0b00 = Stop sending outbound commands when QFIFO is full(default) 0b01 = Stop sending outbound commands when QFIFO has 1 entry empty 0b10 = Stop sending outbound commands when QFIFO has 3 entry empty 0b11 = Ignore QFIFO count when sending outbound packets
29:31	RW	Reserved field.
32	RW	PE_WR_STRICT_ORDER_MODE: Strictly order inbound write commands, Independent of node ID.
33	RW	PE_CHANNEL_STREAMING_EN: Enable processor bus channel streaming operations.

Bits	SCOM	Field Mnemonic: Description
34:35	RW	PE_WR_CACHE_INJECT_MODE: Mode bits for controlling processor bus cache inject: DisableCacheInj(00) = Disable all cache injections (debug only) LegacyCacheInj(01) = Cache inject after a addr_hpc_ack combined response TLPHintCacheInj(10) = Start with cache inject if TLP hints indicate cache inject (TLP hints non-zero) P9ModetCacheInj(11) = Start with cache inject unconditionally
36	RW	PE_ENABLE_NEW_FLOW_CACHE_INJECT: Start new flows on PE to send cache inject commands.
37	RW	PE_DISABLE_INJ_ON_RESEND: Controls cache inject on resends when other cache inject modes are disabled.
38	RW	PE_FORCE_DISABLED_CTAG_TO_FOLLOW_FLOW: When CTAGs are disable, forces DMA writes to still use flows for non-ordering reasons.
39	RW	PE_ENABLE_ENH_FLOW: Controls cache inject on resends when other cache inject modes are disabled.
40	RW	Reserved field.
41	RW	PE_DISABLE_WR_VG: Force all DMA write requests to system scope when they progress to VG scope.
42	RW	PE_DISABLE_WR_SCOPE_GROUP: Disable group scope on DMA write requests.
43	RW	PE_DISABLE_INTWR_VG: Force all initial write requests to system scope when they progress to VG scope.
44	RW	PE_DISABLE_INTWR_SCOPE_GROUP: Disable group scope on initial write requests.
45	RW	PE_DISABLE_INTWR_SCOPE_NODE: Disable node scope on initial write requests.
46:47	RW	Reserved field.
48:49	RW	PE_RD_WRITE_ORDERING: Ordering modes for reads versus writes: NodeMatch(110) = All non-write commands wait behind all writes that match its node AnyNode(111) = All non-write commands wait behind all writes All others are reserved.
50	RW	PE_DISABLE_RD_SCOPE_NODAL: Disable nodal scope on non-TCE DMA read requests.
51	RW	PE_DISABLE_RD_SCOPE_GROUP: Disable group scope on non-TCE DMA read requests.
52	RW	PE_DISABLE_RD_SCOPE_RNNN: Disable RN and Nn scopes on non-TCE DMA read requests.
53	RW	PE_ENABLE_RD_SKIP_GROUP: Skip group scope on non-TCE DMA read requests.
54	RW	PE_DISABLE_RD_VG: Use VG(sys) when at VG scope.
55	RW	PE_DISABLE_TCE_SCOPE_NODAL: Disable nodal scope on non-TCE DMA read requests.
56	RW	PE_DISABLE_TCE_SCOPE_GROUP: Disable Group scope on non-TCE DMA read requests.
57	RW	PE_DISABLE_TCE_SCOPE_RNNN: Disable RnNn scopes on non-TCE DMA read requests.
58	RW	PE_ENABLE_TCE_SKIP_GROUP: Skip group scope on TCE DMA read requests.
59	RW	PE_DISABLE_TCE_VG: Use VG(sys) when at VG scope.
60	RW	PE_DISABLE_TCE_ARBITRATION: Disable preferential TCE read request arbitration.
61	RW	PE_DISABLE_CQ_TCE_ARBITRATION: Disable preferential TCE read response arbitration.
62	RW	PE_DISABLE_MC_PREFETCH: Disable setting PADE bits in cl_rd_nc requests.
63	RW	PE_IGNORE_SFSTAT: Controls DMA read state machine behavior when receiving SFSTAT.

Register Name	**Drop Priority Control Register**
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.DRPPRICTL_REG
Address	0000000004011001 (SCOM)
Description	Drop priority control register.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	PE_DROPPRIORITYMASK: Mask value to determine when a rty_drp will cause the priority to increment on the next request (enable_IO_cmd_pacing = 0) or the DropPaceCounter will be incremented base on dep(enable_IO_cmd_pacing = 1). When LSFR bits match mask drop priority, one of these two actions is taken (DMA write commands only).
6	RW	PE_ENABLE_CTAG_DROP_PRIORITY: Allow commands in a CTAG stream to take the priority of previous rty_drp commands in the stream. If not set, each commands priority is sent independently.
7	RW	PE_ENABLE_IO_CMD_PACING: When a rty_drop CRESP is received, keep drop priority constant and lower command rate until the pacing count is reached. Pacing counter is incremented instead. When not set, drop priority is raised when DropPriorityMask = LSFR value.
8:16	RW	PE_DROPPACECOUNT: Value to use when determining if drop priority should be increase when I/O command pacing is enabled. When the drop priority counter reaches this value, the drop priority is increased (enable_IO_cmd_pacing = 1). Not used when enable_IO_cmd_pacing = 0.
17:22	RW	PE_DROPPACEINC: Value to use when determining how much drop pace count should increase when a retry drop CRESP occurs. Not used when enable_IO_cmd_pacing = 0.
23:25	RW	PE_RTYDROPDIVIDER: Value used to divide down rty_drp combined responses before invoking drop priority: 000/001 = 1st retry drop combined response will invoke drop priority mechanism 010 = 2nd retry drop combined response will invoke drop priority mechanism 011 = 3rd retry drop combined response will invoke drop priority mechanism 100 = 4th retry drop combined response will invoke drop priority mechanism 101 = 5th retry drop combined response will invoke drop priority mechanism 110 = 6th retry drop combined response will invoke drop priority mechanism 111 = 7th retry drop combined response will invoke drop priority mechanism
26:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PBCQ Error Inject Control Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.PBCQEINJ_REG
Address	0000000004011002 (SCOM)
Description	PBCQ error inject control register.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PE_ECC_INJECT_TYPE: Determines the type of ECC error injected: 01 = Correctable error/Parity error 10 = Uncorrectable error 11 = Special uncorrectable error
2	RW	PE_CQ_ECC_INJECT_ENABLE: Enable ECC inject on CQ arrays.
3:6	RW	PE_CQ_SRAM_ARRAY: Determines which CQ SRAM array to force the ECC error into: 0000 = CI store 00:63 0001 = CI store 64:127 0010 = DMA read 00:63 0011 = DMA read 64:127 1000 = DMA write 00:63 1001 = DMA write 64:127 1010 = CI load 00:63 1011 = CI load 64:127
7	RW	PE_CQ_PAR_INJECT_ENABLE: Enable parity inject on CQ arrays.

Bits	SCOM	Field Mnemonic: Description
8:10	RW	PE_CQ_REGISTER_ARRAY: Determines which CQ SRAM array to force the ECC error into: 000 = PBCQ array. 001 = TTAG 010 = RTAG 011 = Outbound SMB 100 = CQPB DMAR 101 = CQPB DMAW 110 - 111 = Reserved
11	RW	PE_CONSTANT_EINJ: 1=constant error inject, 0=one hot error inject
12:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Clock Trace Control Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.NESTTRC_REG
Address	0000000004011003 (SCOM)
Description	PCI nest clock trace control register.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	Reserved field.
4:7	RW	Reserved field.
8:11	RW	Reserved field.
12:15	RW	Reserved field.
16	RW	Reserved field.
17:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ Performance Monitor Control Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.PMONCTL_REG
Address	0000000004011004 (SCOM)
Description	PBCQ performance monitor control register.

Bits	SCOM	Field Mnemonic: Description
0:31	RW	PE_PERFMON_EN: Enable performance monitor outputs per bit.
32:33	RW	PE_PERFMON_READ_TYPE: Values: 00 = DMA read events count TCE or DMA read requests 01 = DMA read events count only TCE requests 10 = DMA read events count only DMA Read requests 11 = Reserved, behavior unpredictable
34:35	RW	Reserved field.
36:39	RW	PE_PMON_MUX_BYTE0: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110vGroup 6 0111-1111 = Reserved, behavior unpredictable

Bits	SCOM	Field Mnemonic: Description
40:43	RW	PE_PMON_MUX_BYTE1: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110vGroup 6 0111-1111 = Reserved, behavior unpredictable
44:47	RW	PE_PMON_MUX_BYTE2: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110vGroup 6 0111-1111 = Reserved, behavior unpredictable
48:51	RW	PE_PMON_MUX_BYTE3: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110vGroup 6 0111-1111 = Reserved, behavior unpredictable
52:63	RO	constant = 0b000000000000

Register Name	PBCQ Tunnel BAR Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.TUNNEL_BAR_REG
Address	0000000004011005 (SCOM)
Description	Tunnel bar for the return address of a tunneled packet.

Bits	SCOM	Field Mnemonic: Description
0:42	RW	PE_TUNNEL_BAR: Tunnel bar for the return address of a tunneled packet.
43:59	RO	constant = 0b00000000000000000

Register Name	PBCQ Predictive Vector Timeout Mask Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.PREDV_REG
Address	0000000004011006 (SCOM)
Description	Predictive vector timeout mask register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PE_RD_PREDV_TIMEOUT_MASK: Predictive target timeout for reads.
8:15	RW	PE_WR_PREDV_TIMEOUT_MASK: Predictive target timeout for writes.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PE CAPP Control Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.PECAPP_CNTL_REG
Address	0000000004011007 (SCOM)
Description	PE CAPP control register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_CAPP_EN: Enable CAPP mode of operation.
1	RW	PE_CAPP_P8_MODE: Enable CAPP mode of operation.
2:11	RW	Reserved.
12:15	RW	PE_CAPP_NUM_MSG_ENG: Number of store queue assigned to CAPP for messages. Assigned 15->2 or 7->2 depending on configuration.
16:63	RW	PE_CAPP_APC_ENG: 48 bit vector to assign read queues to CAPP APC engines.

Register Name	PCI Nest FIR Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.NFIR_REG
Address	0000000004011040 (SCOM) 0000000004011041 (SCOM1) 0000000004011042 (SCOM2)
Description	PCI nest FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RWX	WOX_AND	WOX_OR	NFIRNFIR: PCI nest FIR NFIR.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.NFIRMASK_REG
Address	0000000004011043 (SCOM) 0000000004011044 (SCOM1) 0000000004011045 (SCOM2)
Description	PCI nest FIR mask register: 0 = No mask 1 = Mask error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RW	WO_AND	WO_OR	NFIRMASK: PCI nest FIR mask.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.NFIRACTION0_REG
Address	0000000004011046 (SCOM)
Description	PCI nest FIR qction0 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION0: Action0 select for corresponding bit in FIR. (Action0,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action1 Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.NFIRACTION1_REG
Address	0000000004011047 (SCOM)
Description	PCI nest FIR action1 register

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION1: Action1 select for corresponding bit in FIR. (Action1,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR WOF Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.NFIRWOF_REG
Address	0000000004011048 (SCOM)
Description	PCI nest FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX_WCLRREG	Reserved.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CERR Report Hold Register 0
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.CERR_RPT0_REG
Address	000000000401104A (SCOM)
Description	CERR report hold register 0.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	CERR Report Hold Register 1
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.CERR_RPT1_REG
Address	000000000401104B (SCOM)
Description	CERR report hold register 1.

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	Reserved.
17:47	RO	constant = 0b00000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.CQSTAT_REG
Address	000000000401104C (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	PE_INBOUND_ACTIVE: Inbound (PCIE->PB) state machines are active.
1	ROX	PE_OUTBOUND_ACTIVE: Outbound (PB->PCIE) state machines are active.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.PBCQMODE_REG
Address	000000000401104D (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_PEER2PEER_MODDE: Enable peer to peer operations.
1	RW	PE_ENHANCED_PEER2PEER_MODDE: Enable enhanced peer to peer operations.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR0_REG
Address	000000000401104E (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR0: PE bus I/O base address register 0. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR0_MASK_REG
Address	000000000401104F (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK0: PE bus I/O base address register mask 0. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR1_REG
Address	0000000004011050 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR1: PE bus I/O base address register 1. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR1_MASK_REG
Address	0000000004011051 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK1: PE bus I/O base address register mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus PHB Base Address Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.PHBBAR_REG
Address	0000000004011052 (SCOM)
Description	PE bus PHB base address register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	PE_PHB_BAR: PE bus PHB base address register. Bits 8 to 49 of the base address range are specified with this Ldial. Bits 8 to 49 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is not a mask.

Bits	SCOM	Field Mnemonic: Description
42:63	RO	constant = 0b00000000000000000000

Register Name	PE Bus Initial Base Address Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.INTBAR_REG
Address	0000000004011053 (SCOM)
Description	PE bus initial base address register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_INT_BAR: PE bus initial base address register. Bits 8 to 35 of the base address range are specified with this LDial. Bits 8 to 35 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for initial space which is fixed at 256M, so there is not a mask.
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PE BAR Enables Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.BARE_REG
Address	0000000004011054 (SCOM)
Description	PE BAR enables register,

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_MMIO_BAR0_EN: PE MMIO base address register 0 enable. Each BAR/Mask set has one enable bit.
1	RW	PE_MMIO_BAR1_EN: PE MMIO base address register 1 enable. Each BAR/Mask set has one enable bit.
2	RW	PE_PHB_BAR_EN: PE PCH base address register enable. Each BAR/Mask set has one enable bit.
3	RW	PE_INT_BAR_EN: PE initial base address register enable. Each BAR/Mask set has one enable bit.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Data Freeze Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#0.REGS.PE_DFREEZE_REG
Address	0000000004011055 (SCOM)
Description	PCI nest data freeze register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_DFREEZE: Dfreeze select for corresponding bit in FIR. (dfreeze,Mask) = Action Select (1) = Data freeze if action0:1=b11 (0) = Data freeze if action0:1=b11 and freeze occurs before data is received
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.NFIR_REG
Address	0000000004011080 (SCOM) 0000000004011081 (SCOM1) 0000000004011082 (SCOM2)
Description	PCI nest FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RWX	WOX_AND	WOX_OR	NFIRNFIR: PCI nest FIR NFIR.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.NFIRMASK_REG
Address	0000000004011083 (SCOM) 0000000004011084 (SCOM1) 0000000004011085 (SCOM2)
Description	PCI nest FIR Mask register: 0 = No mask 1 = Mask error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RW	WO_AND	WO_OR	NFIRMASK: PCI nest FIR mask.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.NFIRACTION0_REG
Address	0000000004011086 (SCOM)
Description	PCI nest FIR action0 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION0: Action0 select for corresponding bit in FIR. (Action0,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action1 Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.NFIRACTION1_REG
Address	0000000004011087 (SCOM)
Description	PCI nest FIR action1 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION1: Action1 select for corresponding bit in FIR. (Action1,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b000000000000000000000000000000000000

Register Name	PCI Nest FIR WOF Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.NFIRWOF_REG
Address	0000000004011088 (SCOM)
Description	PCI nest FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX_WCLRREG	Reserved.
30:63	RO	constant = 0b000000000000000000000000000000000000

Register Name	CERR Report Hold Register 0
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.CERR_RPT0_REG
Address	000000000401108A (SCOM)
Description	CERR report hold register 0.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	CERR Report Hold Register 1
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.CERR_RPT1_REG
Address	000000000401108B (SCOM)
Description	CERR report hold register 1.

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	Reserved.
17:47	RO	constant = 0b000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.CQSTAT_REG
Address	000000000401108C (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	PE_INBOUND_ACTIVE: Inbound (PCIE->PB) state machines are active.
1	ROX	PE_OUTBOUND_ACTIVE: Outbound (PB->PCIE) state machines are active.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.PBCQMODE_REG
Address	000000000401108D (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_PEER2PEER_MODDE: Enable peer to peer operations.
1	RW	PE_ENHANCED_PEER2PEER_MODDE: Enable enhanced peer to peer operations.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR0_REG
Address	000000000401108E (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR0: PE bus I/O base address register 0. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR0_MASK_REG
Address	000000000401108F (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK0: PE bus I/O base address register mask 0. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR1_REG
Address	0000000004011090 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR1: PE bus I/O base address register 1. Bits 8 to 47 of the base address range are specified with this Ldial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR1_MASK_REG
Address	0000000004011091 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK1: PE bus I/O base address register mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus PHB Base Address Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.PHBBAR_REG
Address	0000000004011092 (SCOM)
Description	PE bus PHB base address register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	PE_PHB_BAR: PE bus PHB base address register. Bits 8 to 49 of the base address range are specified with this LDial. Bits 8 to 49 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is not a mask.
42:63	RO	constant = 0b00000000000000000000

Register Name	PE Bus Initial Base Address Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.INTBAR_REG
Address	0000000004011093 (SCOM)
Description	PE bus initial base address register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_INT_BAR: PE bus initial base address register. Bits 8 to 35 of the base address range are specified with this LDial. Bits 8 to 35 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for int space which is fixed at 256M, so there is not a mask.
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PE BAR Enables Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.BARE_REG
Address	0000000004011094 (SCOM)
Description	PE BAR enables register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_MMIO_BAR0_EN: PE MMIO base address register 0 enable. Each BAR/Mask set has one enable bit.
1	RW	PE_MMIO_BAR1_EN: PE MMIO base address register 1 enable. Each BAR/Mask set has one enable bit.
2	RW	PE_PHB_BAR_EN: PE PHB base address register enable. Each BAR/Mask set has one enable bit.
3	RW	PE_INT_BAR_EN: PE initial base address register enable. Each BAR/Mask set has one enable bit.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Data Freeze Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#1.REGS.PE_DFREEZE_REG
Address	0000000004011095 (SCOM)
Description	PCI nest data freeze register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_DFREEZE: Dfreeze select for corresponding bit in FIR. (dfreeze,Mask) = Action Select (1) = Data freeze if action0:1=b11 (0) = data freeze if action0:1=b11 and freeze occurs before data is received
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.NFIR_REG
Address	00000000040110C0 (SCOM) 00000000040110C1 (SCOM1) 00000000040110C2 (SCOM2)
Description	PCI nest FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RWX	WOX_AND	WOX_OR	NFIRNFIR: PCI nest FIR NFIR.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.NFIRMASK_REG
Address	00000000040110C3 (SCOM) 00000000040110C4 (SCOM1) 00000000040110C5 (SCOM2)
Description	PCI nest FIR mask register: 0 = No mask 1 = Mask error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RW	WO_AND	WO_OR	NFIRMASK: PCI nest FIR mask.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION0_REG
Address	00000000040110C6 (SCOM)
Description	PCI nest FIR action0 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION0: Action0 select for corresponding bit in FIR. (Action0,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action1 Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION1_REG
Address	00000000040110C7 (SCOM)
Description	PCI nest FIR action1 register,

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION1: Action1 select for corresponding bit in FIR. (Action1,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR WOF Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.NFIRWOF_REG
Address	00000000040110C8 (SCOM)
Description	PCI nest FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX_WCLRREG	Reserved.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CERR Report Hold Register 0
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.CERR_RPT0_REG
Address	00000000040110CA (SCOM)
Description	CERR report hold register 0.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	CERR Report Hold Register 1
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.CERR_RPT1_REG
Address	00000000040110CB (SCOM)
Description	CERR report hold register 1.

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	Reserved.
17:47	RO	constant = 0b00000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.CQSTAT_REG
Address	00000000040110CC (SCOM)
Description	PBCQ general status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	PE_INBOUND_ACTIVE: Inbound (PCIE->PB) state machines are active.
1	ROX	PE_OUTBOUND_ACTIVE: Outbound (PB->PCIE) state machines are active.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.PBCQMODE_REG
Address	00000000040110CD (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_PEER2PEER_MODDE: Enable peer to peer operations.
1	RW	PE_ENHANCED_PEER2PEER_MODDE: Enable enhanced peer to peer operations.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_REG
Address	00000000040110CE (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR0: PE bus I/O base address register 0. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_MASK_REG
Address	00000000040110CF (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK0: PE bus I/O base address register mask 0. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_REG
Address	00000000040110D0 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR1: PE bus I/O base address register 1. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_MASK_REG
Address	00000000040110D1 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK1: PE bus I/O base address register mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus PHB Base Address Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.PHBBAR_REG
Address	00000000040110D2 (SCOM)
Description	PE bus PHB base address register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	PE_PHB_BAR: PE bus PHB base address register. Bits 8 to 49 of the base address range are specified with this Ldial. Bits 8 to 49 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is not a mask.
42:63	RO	constant = 0b00000000000000000000

Register Name	PE Bus Initial Base Address Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.INTBAR_REG
Address	00000000040110D3 (SCOM)
Description	PE bus initial base address register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_INT_BAR: PE bus initial base address register. Bits 8 to 35 of the base address range are specified with this LDial. Bits 8 to 35 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for int space which is fixed at 256M, so there is not a mask.
28:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	PE BAR Enables Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.BARE_REG
Address	00000000040110D4 (SCOM)
Description	PE BAR enables register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_MMIO_BAR0_EN: PE MMIO base address register 0 enable. Each BAR/Mask set has one enable bit.
1	RW	PE_MMIO_BAR1_EN: PE MMIO base address register 1enable. Each BAR/Mask set has one enable bit.
2	RW	PE_PHB_BAR_EN: PE PHB base address register enable. Each BAR/Mask set has one enable bit.
3	RW	PE_INT_BAR_EN: PE initial base address register enable. Each BAR/Mask set has one enable bit.
4:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Data Freeze Register
Mnemonic	PE1.PB1.PBCQ.PEPBREGS.STACK#2.REGS.PE_DFREEZE_REG
Address	00000000040110D5 (SCOM)
Description	PCI nest data freeze register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_DFREEZE: Dfreeze select for corresponding bit in FIR. (dfreeze,Mask) = Action Select (1) = Data freeze if action0:1=b11 (0) = Data freeze if action0:1=b11 and freeze occurs before data is received
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI PBCQ Hardware Configuration Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.PBCQHWCFG_REG
Address	0000000004011400 (SCOM)
Description	PCI PBCQ hardware configuration register.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	HANG_POLL_SCALE: How many hang polls that need to be detected to indicate a hang poll to the logic.
4:7	RW	HANG_DATA_SCALE: How many data polls that need to be detected to indicate a data poll to the logic.
8:11	RW	HANG_PE_SCALE: How many data polls that need to be detected to indicate a PE poll to the logic. A PE poll is created by the PCI unit to detect hangs of SMs while waiting on exchanges with the PCI logic.
12	RW	PE_BLOCK_CQPB_PB_INIT: When set, PCI to PB data movement ignores the PB initial signal. When not set, PCI to PB data movement will stop on cache line boundaries.
13	RW	DISABLE_RCMD_CLKGATE: Chicken switch to turn off the clock gating which occurs on rcmd when the command is not for PE.
14	RW	PE_HANG_SM_ON_ARE: Controls processor bus master state machines when an ARE is received.
15	RW	PE_DISABLE_PCI_CLK_CHECK: Disables the logic that checks valid PCI clocks (FIR bit 15).
16	RW	LFSR_ARB_MODE: 1 = Use LFSR in outbound arbitration.
17	RW	PE_ENABLE_DMAR_IOPACING: Allow I/O pacing scheme for DMA read operations.
18	RW	PE_ENABLE_DMAW_IOPACING: Allow I/O pacing scheme for DMA write operations.
19	RW	PE_ADR_BAR_MODE: Address mode register for PE unit.
20	RW	PE_STQ_ALLOCATION: Queue allocation between stores and p2p: 0 = stq_1_Reserved for each type, the rest floating 1 = stq_1_only Only queue used for all traffic, the remaining 7 are unused.
21	RW	DISABLE_LPC_CMDS: Disable LPC acknowledgment for commands that the PE does not service.
22	RW	PE_DISABLE_OOO_MODE: PE order OOO type CI stores like a normal CI store command.
23:26	RW	PE_OSMB_EARLY_START: Determines how much overlap of reading/writing the OSMB allows: 0b0000 = Most conservative, full packet written in before signaling PCI side 0b0001 = Most conservative, full packet written in before signaling PCI side 0b0010 = Start 2 writes from the end of the packet 0b0011 = Start 3 writes from the end of the packet 0b0100 = Start 4 writes from the end of the packet 0b0101 = Start 5 writes from the end of the packet 0b0110 = Start 6 writes from the end of the packet 0b0111 = Start 7 writes from the end of the packet 0b1000 = Most aggressive, start 8 writes from the end of the packet, before any data written 0b1111 = Extra aggressive, start before any data written (that is, when the command is written

Bits	SCOM	Field Mnemonic: Description
27:28	RW	PE_QFIFO_HOLD_MODE: Determines how much overlap of reading/writing the OSMB allows: 0b00 = Stop sending outbound commands when QFIFO is full (default). 0b01 = Stop sending outbound commands when QFIFO has 1 entry empty 0b10 = Stop sending outbound commands when QFIFO has 3 entry empty 0b11 = Ignore QFIFO count when sending outbound packets
29:31	RW	Reserved field.
32	RW	PE_WR_STRICT_ORDER_MODE: Strictly order inbound write commands, independent of node ID.
33	RW	PE_CHANNEL_STREAMING_EN: Enable processor bus channel streaming operations.
34:35	RW	PE_WR_CACHE_INJECT_MODE: Mode bits for controlling processor bus cache inject: DisableCacheInj(00) = Disable all cache Injections (debug only) LegacyCacheInj(01) = Cache inject after a addr_hpc_ack combined response TLPHintCacheInj(10) = Start with cache inject if TLP hints indicate cache inject (TLP hints non-zero) P9ModetCacheInj(11) = Start with cache inject unconditionally
36	RW	PE_ENABLE_NEW_FLOW_CACHE_INJECT: Start new flows on PE to send cache inject commands.
37	RW	PE_DISABLE_INJ_ON_RESEND: Controls cache inject on resends when other cache inject modes are disabled.
38	RW	PE_FORCE_DISABLED_CTAG_TO_FOLLOW_FLOW: When CTAGs are disable, forces DMA writes to still use flows for non-ordering reasons.
39	RW	PE_ENABLE_ENH_FLOW: Controls cache inject on resends when other cache inject modes are disabled.
40	RW	Reserved field.
41	RW	PE_DISABLE_WR_VG: Force all DMA write requests to system scope when they progress to VG scope.
42	RW	PE_DISABLE_WR_SCOPE_GROUP: Disable group scope on DMA write requests.
43	RW	PE_DISABLE_INTWR_VG: Force all initial write requests to system scope when they progress to VG scope.
44	RW	PE_DISABLE_INTWR_SCOPE_GROUP: Disable group scope on initial write requests.
45	RW	PE_DISABLE_INTWR_SCOPE_NODE: Disable node scope on initial write requests.
46:47	RW	Reserved field.
48:49	RW	PE_RD_WRITE_ORDERING: Ordering modes for reads verses writes: NodeMatch(110) = All non-write commands wait behind all writes that match its node AnyNode(111) = All non-write commands wait behind all writes All others are reserved.
50	RW	PE_DISABLE_RD_SCOPE_NODAL: Disable nodal scope on non-TCE DMA read requests.
51	RW	PE_DISABLE_RD_SCOPE_GROUP: Disable group scope on non-TCE DMA read requests.
52	RW	PE_DISABLE_RD_SCOPE_RNNN: Disable RN and Nn scopes on non-TCE DMA read requests.
53	RW	PE_ENABLE_RD_SKIP_GROUP: Skip group scope on non-TCE DMA read requests.
54	RW	PE_DISABLE_RD_VG: Use VG(sys) when at VG scope.
55	RW	PE_DISABLE_TCE_SCOPE_NODAL: Disable nodal scope on non-TCE DMA read requests.
56	RW	PE_DISABLE_TCE_SCOPE_GROUP: Disable Group scope on non-TCE DMA read requests.
57	RW	PE_DISABLE_TCE_SCOPE_RNNN: Disable RnNn scopes on non-TCE DMA read requests.
58	RW	PE_ENABLE_TCE_SKIP_GROUP: Skip group scope on TCE DMA read requests.
59	RW	PE_DISABLE_TCE_VG: Use VG(sys) when at VG scope.
60	RW	PE_DISABLE_TCE_ARBITRATION: Disable preferential TCE read request arbitration.
61	RW	PE_DISABLE_CQ_TCE_ARBITRATION: Disable preferential TCE read response arbitration.
62	RW	PE_DISABLE_MC_PREFETCH: Disable setting PADE bits in cl_rd_nc requests.

Bits	SCOM	Field Mnemonic: Description
63	RW	PE_IGNORE_SFSTAT: Controls DMA read state machine behavior when receiving SFSTAT.

Register Name	Drop Priority Control Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.DRPPRICTL_REG
Address	0000000004011401 (SCOM)
Description	Drop priority control register.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	PE_DROPPRIORITYMASK: Mask value to determine when a rty_drp will cause the priority to increment on the next request (enable_IO_cmd_pacing = 0) or the DropPaceCounter will be incremented based on dep(enable_IO_cmd_pacing = 1). When LSFR bits match mask drop priority, one of these two actions will be taken (DMA write commands only).
6	RW	PE_ENABLE_CTAG_DROP_PRIORITY: Allow commands in a CTAG stream to take the priority of previous rty_drp commands in the stream. If not set, each commands priority is sent independently.
7	RW	PE_ENABLE_IO_CMD_PACING: When a rty_drop CRESP is received, keep drop priority constant and lower command rate until the pacing count is reached. Pacing counter is incremented instead. When not set, drop priority is raised when DropPriorityMask = LSFR value.
8:16	RW	PE_DROPPACECOUNT: Value to use when determining if drop priority should be increase when I/O command pacing is enabled. When the drop priority counter reaches this value, the drop priority is increased (enable_IO_cmd_pacing = 1). It is not used when enable_IO_cmd_pacing = 0.
17:22	RW	PE_DROPPACEINC: Value to use when determining how much drop pace count should increase when a retry drop CRESP occurs. Not used when enable_IO_cmd_pacing = 0.
23:25	RW	PE_RTYDROPDIVIDER: Value used to divide down rty_drp combined responses before invoking drop priority: 000/001 = 1st retry drop combined response will invoke drop priority mechanism 010 = 2nd retry drop combined response will invoke drop priority mechanism 011 = 3rd retry drop combined response will invoke drop priority mechanism 100 = 4th retry drop combined response will invoke drop priority mechanism 101 = 5th retry drop combined response will invoke drop priority mechanism 110 = 6th retry drop combined response will invoke drop priority mechanism 111 = 7th retry drop combined response will invoke drop priority mechanism
26:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PBCQ Error Inject Control Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.PBCQEINJ_REG
Address	0000000004011402 (SCOM)
Description	PBCQ error inject control register.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PE_ECC_INJECT_TYPE: Determines the type of ECC error injected: 01 = Correctable error/Parity error 10 = Uncorrectable error 11 = Special uncorrectable error
2	RW	PE_CQ_ECC_INJECT_ENABLE: Enable ECC inject on CQ arrays.

Bits	SCOM	Field Mnemonic: Description
3:6	RW	PE_CQ_SRAM_ARRAY: Determines which CQ SRAM array to force the ECC error into: 0000 = CI store 00:63 0001 = CI store 64:127 0010 = DMA read 00:63 0011 = DMA read 64:127 1000 = DMA write 00:63 1001 = DMA write 64:127 1010 = CI load 00:63 1011 = CI load 64:127
7	RW	PE_CQ_PAR_INJECT_ENABLE: Enable parity inject on CQ arrays.
8:10	RW	PE_CQ_REGISTER_ARRAY: Determines which CQ SRAM array to force the ECC error into: 000 = PBCQ array 001 = CQ SRAM TTAG 010 = RTAG 011 = Outbound SMB 100 = CQPB DMAR 101 = CQPB DMAW 110 - 111 = Reserved
11	RW	PE_CONSTANT_EINJ: 1 = Constant error inject, 0 = One hot error inject
12:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Clock Trace Control Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.NESTTRC_REG
Address	0000000004011403 (SCOM)
Description	PCI nest clock trace control register.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	Reserved field.
4:7	RW	Reserved field.
8:11	RW	Reserved field.
12:15	RW	Reserved field.
16	RW	Reserved field.
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PBCQ Performance Monitor Control Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.PMONCTL_REG
Address	0000000004011404 (SCOM)
Description	PBCQ performance monitor control register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	PE_PERFMON_EN: Enable performance monitor outputs per bit.
32:33	RW	PE_PERFMON_READ_TYPE: 00: DMA read events count TCE or DMA read requests: 01 = DMA Read events count only TCE requests 10 = DMA Read events count only DMA read requests 11 = Reserved, behavior unpredictable
34:35	RW	Reserved field.

Bits	SCOM	Field Mnemonic: Description
36:39	RW	PE_PMON_MUX_BYTE0: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110 = Group 6 0111-1111 = Reserved, behavior unpredictable
40:43	RW	PE_PMON_MUX_BYTE1: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110 = Group 6 0111-1111 = Reserved, behavior unpredictable
44:47	RW	PE_PMON_MUX_BYTE2: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110 = Group 6 0111-1111 = Reserved, behavior unpredictable
48:51	RW	PE_PMON_MUX_BYTE3: 0000: Group 0: 0001 = Group 1 0010 = Group 2 0011 = Group 3 0100 = Group 4 0101 = Group 5 0110 = Group 6 0111-1111 = Reserved, behavior unpredictable
52:63	RO	constant = 0b000000000000

Register Name	**PBCQ Tunnel BAR Register**
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.TUNNEL_BAR_REG
Address	0000000004011405 (SCOM)
Description	Tunnel bar for the return address of a tunneled packet.

Bits	SCOM	Field Mnemonic: Description
0:42	RW	PE_TUNNEL_BAR: Tunnel bar for the return address of a tunneled packet.
43:59	RO	constant = 0b00000000000000000

Register Name	**PBCQ Predictive Vector Timeout Mask Register**
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.PREDV_REG
Address	0000000004011406 (SCOM)
Description	Predictive vector timeout mask register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PE_RD_PREDV_TIMEOUT_MASK: Predictive target timeout for reads.
8:15	RW	PE_WR_PREDV_TIMEOUT_MASK: Predictive target timeout for writes.
16:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	PE CAPP Control Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.PECAPP_CNTL_REG
Address	0000000004011407 (SCOM)
Description	PE CAPP control register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_CAPP_EN: Enable CAPP mode of operation.
1	RW	PE_CAPP_P8_MODE: Enable CAPP mode of operation.
2:11	RW	Reserved.
12:15	RW	PE_CAPP_NUM_MSG_ENG: Number of store queue assigned to CAPP for messages. Assigned 15->2 or 7->2 depending on configuration.
16:63	RW	PE_CAPP_APC_ENG: 48 bit vector to assign read queues to CAPP APC engines.

Register Name	PCI Nest FIR Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.NFIR_REG
Address	0000000004011440 (SCOM) 0000000004011441 (SCOM1) 0000000004011442 (SCOM2)
Description	PCI nest FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RWX	WOX_AND	WOX_OR	NFIRNFIR: PCI nest FIR NFIR.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.NFIRMASK_REG
Address	0000000004011443 (SCOM) 0000000004011444 (SCOM1) 0000000004011445 (SCOM2)
Description	PCI Nest FIR mask register: 0 = No mask 1 = Mask error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RW	WO_AND	WO_OR	NFIRMASK: PCI nest FIR mask.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.NFIRACTION0_REG
Address	0000000004011446 (SCOM)
Description	PCI nest FIR action0 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION0: Action0 select for corresponding bit in FIR. (Action0,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action1 Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.NFIRACTION1_REG
Address	0000000004011447 (SCOM)
Description	PCI nest FIR Action1 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION1: Action1 select for corresponding bit in FIR. (Action1,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR WOF Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.NFIRWOF_REG
Address	0000000004011448 (SCOM)
Description	PCI nest FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX_WCLRREG	Reserved.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CERR Report Hold Register 0
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.CERR_RPT0_REG
Address	000000000401144A (SCOM)
Description	CERR report hold register 0.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	CERR Report Hold Register 1
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.CERR_RPT1_REG
Address	000000000401144B (SCOM)
Description	CERR report hold register 1.

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	Reserved.
17:47	RO	constant = 0b00000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.CQSTAT_REG
Address	000000000401144C (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	PE_INBOUND_ACTIVE: Inbound (PCIE->PB) state machines are active.
1	ROX	PE_OUTBOUND_ACTIVE: Outbound (PB->PCIE) state machines are active.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.PBCQMODE_REG
Address	000000000401144D (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_PEER2PEER_MODDE: Enable peer to peer operations.
1	RW	PE_ENHANCED_PEER2PEER_MODDE: Enable enhanced peer to peer operations.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR0_REG
Address	000000000401144E (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR0: PE bus I/O Base Address Register 0. Bits 8 to 47 of the Base Address range are specified with this IDial. Bits 8 to 47 of a snoop address are compared with this Base Address. after ANDing bits 8 to 47 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the address range. specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR0_MASK_REG
Address	0000000004011 44F (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK0: PE bus I/O Base Address Register Mask 0. This LDial specifies the size of the address range which is specified by. this BAR/Mask pair. The range size must be a power of two. Valid range. sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR1_REG
Address	0000000004011450 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR1: PE bus I/O base address register 1. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.MMIOBAR1_MASK_REG
Address	0000000004011451 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK1: PE bus I/O base address register mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range. sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus PHB Base Address Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.PHBBAR_REG
Address	0000000004011452 (SCOM)
Description	PE bus PHB base address register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	PE_PHB_BAR: PE bus PHB base address register. Bits 8 to 49 of the base address range are specified with this LDial. Bits 8 to 49 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is not a mask.
42:63	RO	constant = 0b00000000000000000000

Register Name	PE Bus Initial Base Address Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.INTBAR_REG
Address	0000000004011453 (SCOM)
Description	PE bus initial base address register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_INT_BAR: PE bus initial base address register. Bits 8 to 35 of the base address range are specified with this Ldial. Bits 8 to 35 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for initial space which is fixed at 256M, so there is not a mask.
28:63	RO	constant = 0b000000000000000000000000000000000000

Register Name	PE BAR Enables Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.BARE_REG
Address	0000000004011454 (SCOM)
Description	PE BAR enables register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_MMIO_BAR0_EN: PE MMIO base address register 0 enable. Each BAR/Mask set has one enable bit.
1	RW	PE_MMIO_BAR1_EN: PE MMIO base address register 1 enable. Each BAR/Mask set has one enable bit.
2	RW	PE_PHB_BAR_EN: PE PHB base address register enable. Each BAR/Mask set has one enable bit.
3	RW	PE_INT_BAR_EN: PE int Base Address Register Enable. Each BAR/Mask set has one enable bit.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Data Freeze Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#0.REGS.PE_DFREEZE_REG
Address	0000000004011455 (SCOM)
Description	PCI nest data freeze register

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_DFREEZE: Dfreeze select for corresponding bit in FIR. (dfreeze,Mask) = Action Select (1) = Data freeze if action0:1=b11 (0) = Data freeze if action0:1=b11 and freeze occurs before data is received
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.NFIR_REG
Address	0000000004011480 (SCOM) 0000000004011481 (SCOM1) 0000000004011482 (SCOM2)
Description	PCI nest FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RWX	WOX_AND	WOX_OR	NFIRNFIR: PCI nest FIR NFIR.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.NFIRMASK_REG
Address	0000000004011483 (SCOM) 0000000004011484 (SCOM1) 0000000004011485 (SCOM2)
Description	PCI nest FIR mask register: 0 = No mask 1 = Mask error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RW	WO_AND	WO_OR	NFIRMASK: PCI nest FIR mask.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.NFIRACTION0_REG
Address	0000000004011486 (SCOM)
Description	PCI nest FIR action0 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION0: Action0 select for corresponding bit in FIR. (Action0,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Action1 Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.NFIRACTION1_REG
Address	0000000004011487 (SCOM)
Description	PCI nest FIR action1 register

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION1: Action1 select for corresponding bit in FIR. (Action1,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR WOF Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.NFIRWOF_REG
Address	0000000004011488 (SCOM)
Description	PCI nest FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX_WCLRREG	Reserved.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CERR Report Hold Register 0
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.CERR_RPT0_REG
Address	000000004011488A (SCOM)
Description	CERR report hold register 0.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	CERR Report Hold Register 1
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.CERR_RPT1_REG
Address	000000004011488B (SCOM)
Description	CERR report hold register 1.

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	Reserved.
17:47	RO	constant = 0b00000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.CQSTAT_REG
Address	000000000401148C (SCOM)
Description	PBCQ general status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	PE_INBOUND_ACTIVE: Inbound (PCIE->PB) state machines are active.
1	ROX	PE_OUTBOUND_ACTIVE: Outbound (PB->PCIE) state machines are active.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.PBCQMODE_REG
Address	000000000401148D (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_PEER2PEER_MODDE: Enable peer to peer operations.
1	RW	PE_ENHANCED_PEER2PEER_MODDE: Enable enhanced peer to peer operations.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR0_REG
Address	000000000401148E (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR0: PE bus I/O base address register 0. Bits 8 to 47 of the base address range are specified with this Ldial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR0_MASK_REG
Address	000000000401148F (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK0: PE bus I/O base address register mask 0. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR1_REG
Address	0000000004011490 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR1: PE bus I/O base address register 1. Bits 8 to 47 of the base address range are specified with this Ldial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.MMIOBAR1_MASK_REG
Address	0000000004011491 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK1: PE bus I/O base address register mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus PHB Base Address Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.PHBBAR_REG
Address	0000000004011492 (SCOM)
Description	PE bus PHB base address register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	PE_PHB_BAR: PE bus PHB base address register. Bits 8 to 49 of the base address range are specified with this LDial. Bits 8 to 49 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is not a mask.
42:63	RO	constant = 0b00000000000000000000

Register Name	PE Bus Initial Base Address Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.INTBAR_REG
Address	0000000004011493 (SCOM)
Description	PE bus initial base address register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_INT_BAR: PE bus initial base address register. Bits 8 to 35 of the base address range are specified with this LDial. Bits 8 to 35 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for initial space which is fixed at 256M, so there is not a mask.
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PE BAR Enables Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.BARE_REG
Address	0000000004011494 (SCOM)
Description	PE BAR enables register,

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_MMIO_BAR0_EN: PE MMIO base address register 0 enable. Each BAR/Mask set has one enable bit.
1	RW	PE_MMIO_BAR1_EN: PE MMIO base address register 1 enable. Each BAR/Mask set has one enable bit.
2	RW	PE_PHB_BAR_EN: PE PHB base address register enable. Each BAR/Mask set has one enable bit.
3	RW	PE_INT_BAR_EN: PE initial base address register enable. Each BAR/Mask set has one enable bit.
4:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Data Freeze Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#1.REGS.PE_DFREEZE_REG
Address	0000000004011495 (SCOM)
Description	PCI nest data freeze register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_DFREEZE: Dfreeze select for corresponding bit in FIR. (Dfreeze,Mask) = Action Select (1) = Data freeze if action0:1=b11 (0) = Data freeze if action0:1=b11 and freeze occurs before data is received
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIR_REG
Address	00000000040114C0 (SCOM) 00000000040114C1 (SCOM1) 00000000040114C2 (SCOM2)
Description	PCI nest FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RWX	WOX_AND	WOX_OR	NFIRNFIR: PCI nest FIR NFIR.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIRMASK_REG
Address	00000000040114C3 (SCOM) 00000000040114C4 (SCOM1) 00000000040114C5 (SCOM2)
Description	PCI nest FIR mask register: 0 = No mask 1 = Mask error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:29	RW	WO_AND	WO_OR	NFIRMASK: PCI nest FIR Mask.
30:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION0_REG
Address	00000000040114C6 (SCOM)
Description	PCI nest FIR action0 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION0: Action0 select for corresponding bit in FIR. (Action0,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action1 Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIRACTION1_REG
Address	00000000040114C7 (SCOM)
Description	PCI nest FIR action1 register.

Bits	SCOM	Field Mnemonic: Description
0:29	RW	NFIRACTION1: Action1 select for corresponding bit in FIR. (Action1,Mask) = Action Select (0,0) = Checkstop error (0,1) = Recoverable error (1,0) = No action (1,1) = Freeze
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR WOF Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.NFIRWOF_REG
Address	00000000040114C8 (SCOM)
Description	PCI nest FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX_WCLRREG	Reserved.
30:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CERR Report Hold Register 0
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.CERR_RPT0_REG
Address	00000000040114CA (SCOM)
Description	CERR report hold register 0.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	CERR Report Hold Register 1
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.CERR_RPT1_REG
Address	00000000040114CB (SCOM)
Description	CERR report hold register 1.

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	Reserved.
17:47	RO	constant = 0b00000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.CQSTAT_REG
Address	00000000040114CC (SCOM)
Description	PBCQ general status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	PE_INBOUND_ACTIVE: Inbound (PCIE →PB) state machines are active.
1	ROX	PE_OUTBOUND_ACTIVE: Outbound (PB →PCIE) state machines are active.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PBCQ General Status Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.PBCQMODE_REG
Address	00000000040114CD (SCOM)
Description	PBCQ general status register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_PEER2PEER_MODDE: Enable peer to peer operations.
1	RW	PE_ENHANCED_PEER2PEER_MODDE: Enable enhanced peer to peer operations.

Bits	SCOM	Field Mnemonic: Description
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_REG
Address	00000000040114CE (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR0: PE bus I/O base address register 0. Bits 8 to 47 of the base address range are specified with this Ldial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 0
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR0_MASK_REG
Address	00000000040114CF (SCOM)
Description	PE bus MMIO base address register 0.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK0: PE bus I/O base address register mask 0. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_REG
Address	00000000040114D0 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_BAR1: PE bus I/O base address register 1. Bits 8 to 47 of the base address range are specified with this LDial. Bits 8 to 47 of a snoop address are compared with this base address after ANDing bits 8 to 47 of the corresponding mask register with each If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
40:63	RO	constant = 0b0000000000000000000000000

Register Name	PE Bus MMIO Base Address Register 1
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.MMIOBAR1_MASK_REG
Address	00000000040114D1 (SCOM)
Description	PE bus MMIO base address register 1.

Bits	SCOM	Field Mnemonic: Description
0:39	RW	PE_MMIO_MASK1: PE bus I/O base address register mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 32PB.
40:63	RO	constant = 0b0000000000000000000000

Register Name	PE Bus PHB Base Address Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.PHBBAR_REG
Address	00000000040114D2 (SCOM)
Description	PE bus PHB base address register

Bits	SCOM	Field Mnemonic: Description
0:41	RW	PE_PHB_BAR: PE bus PHB base address register. Bits 8 to 49 of the base address range are specified with this LDial. Bits 8 to 49 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is not a mask.
42:63	RO	constant = 0b00000000000000000000

Register Name	PE Bus Initial Base Address Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.INTBAR_REG
Address	00000000040114D3 (SCOM)
Description	PE bus initial base address register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_INT_BAR: PE bus initial base address register. Bits 8 to 35 of the base address range are specified with this LDial. Bits 8 to 35 of a snoop address are compared with this base address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for int space which is fixed at 256M, so there is not a mask.
28:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	PE BAR Enables Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.BARE_REG
Address	00000000040114D4 (SCOM)
Description	PE BAR enables register

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_MMIO_BAR0_EN: PE MMIO base address register 0 enable. Each BAR/Mask set has one enable bit.
1	RW	PE_MMIO_BAR1_EN: PE MMIO base address register 1 enable. Each BAR/Mask set has one enable bit.
2	RW	PE_PHB_BAR_EN: PE PHB base address register enable. Each BAR/Mask set has one enable bit.
3	RW	PE_INT_BAR_EN: PE initial base address register enable. Each BAR/Mask set has one enable bit.
4:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PCI Nest Data Freeze Register
Mnemonic	PE2.PB2.PBCQ.PEPBREGS.STACK#2.REGS.PE_DFREEZE_REG
Address	00000000040114D5 (SCOM)
Description	PCI nest data freeze register.

Bits	SCOM	Field Mnemonic: Description
0:27	RW	PE_DFREEZE: Dfreeze select for corresponding bit in FIR. (dfreeze,Mask) = Action Select (1) = Data freeze if action0:1=b11 (0) = Data freeze if action0:1=b11 and freeze occurs before data is received
28:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	PSI FIR Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.FIR_REG
Address	0000000004011800 (SCOM) 0000000004011801 (SCOM1) 0000000004011802 (SCOM2)
Description	Local FIR register for the PSI logic.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved0: Reserved PSI FIR bit 0.
1	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved1: Reserved PSI FIR bit 1.
2	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved2: Reserved PSI FIR bit 2.
3	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved3: Reserved PSI FIR bit 3.
4	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved4: Reserved PSI FIR bit 4.
5	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR: Internal SCOM error mask.
6	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_CLONE: Internal SCOM error mask clone.
7:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	PSI FIR Mask Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.FIR_MASK_REG
Address	0000000004011803 (SCOM) 0000000004011804 (SCOM1) 0000000004011805 (SCOM2)
Description	Error mask register (Action0,Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved0_MASK: Reserved PSI FIR bit 0 mask.
1	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved1_MASK: Reserved PSI FIR bit 1 mask.
2	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved2_MASK: Reserved PSI FIR bit 2 mask.
3	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved3_MASK: Reserved PSI FIR bit 3 mask.
4	RWX	WOX_AND	WOX_OR	PSI_FIR_Reserved4_MASK: Reserved PSI FIR bit 4 mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK: Internal SCOM error mask.
6	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK_CLONE: Internal SCOM error mask clone.
7:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Fault Isolation Action0 Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.FIR_ACTION0_REG
Address	0000000004011806 (SCOM)
Description	Fault isolation action0 register.

Bits	SCOM	Field Mnemonic: Description
0:6	RW	FIR_ACTION0: Action 0 for FIR(0:6).
7:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Fault Isolation Action1 Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.FIR_ACTION1_REG
Address	0000000004011807 (SCOM)
Description	Fault isolation action1 register.

Bits	SCOM	Field Mnemonic: Description
0:6	RW	FIR_ACTION1: Action 1 for FIR(0:6).
7:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	FIR WOF Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.FIR_WOF_REG
Address	0000000004011808 (SCOM)
Description	FIR WOF register.

Bits	SCOM	Field Mnemonic: Description
0:6	RWX_WCLRREG	Reserved field.
7:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	RX Control Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.RX_PSI_CNTL
Address	0000000004011820 (SCOM)
Description	RX Control register.

Bits	SCOM	Field Mnemonic: Description
0	NCX	Reserved field.
1	RWX	RX_PSI_PATTERN_CHECK_EN: Enables the drive pattern to be tested: DMB. 0b0 = No pattern checking 0b1 = Check for drive pattern
2:3	RWX	RX_PSI_PATTERN_SEL: RX pattern select: DMB. 0b00 = ei4 busy pattern a 0b01 = ei4 busy pattern b 0b10 = 16 bit legacy 0b11 = IE3 busy IAP pattern
4	RWX	RX_PSI_CLK_INVERT: Used to invert the polarity of the clock: DMB. 0b0 = Normal clock polarity (default) 0b1 = Clock inverted
5	RWX	RX_PSI_LANE_INVERT: Used to invert the polarity of the data lane: DMB. 0b0 = Normal data lane polarity (default) 0b1 = Data lane inverted
6	RWX	RX_PSI_PDWN: Used to power down the PSI RX clock and data path: MBS. 0b0 = Operational (default) 0b1 = Clock and data path are powered off
7:13	RWX	RX_PSI_CLK_DLY: Clock delay setting. Default value is 300ps at the fast corner. DMB.
14:20	RWX	RX_PSI_DATA_DLY: Data delay setting. Default value is 300ps at the fast corner. DMB.
21:25	RWX	RX_PSI_DEGLITCH_CLK_DLY: Clock deglitcher delay setting. Default value is 300ps at the fast corner. DMB.
26:30	RWX	RX_PSI_DEGLITCH_DATA_DLY: Data deglitcher match delay setting. To match clock line, default value is 300ps at the fast corner. DMB.
31	RO	constant = 0b0

Register Name	RX Mode Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.RX_PSI_MODE
Address	0000000004011821 (SCOM)
Description	RX mode register.

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	RX_PSI_VREF: VREF SETTING (0-7). Step size is about Vio*5/1100. DMB.
8:11	RO	constant = 0b0000
12	RWX	RX_PSI_TERM_TEST_MODE: Termination segment test mode: MBS. 0b0 = Mission mode enable 0b1 = Termination segment test mode
13:14	RO	constant = 0b00
15:19	RWX	RX_PSI_TERM_MODE_ENC: Slice enable for pfet. fet pairs for termination mode. Bits 0:3 determine how many 1pt2kohm pairs to enable, out of 14. Bit 4 enables a half-strength 2.4kohm pfet. fet pair, and also controls whether that pair is enabled in test mode. MBS.
20:23	RO	constant = 0b0000
24:31	RWX	RX_PSI_MODE_SPARE: Spares. TBD. DMB.

Register Name	RX Status Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.RX_PSI_STATUS
Address	0000000004011822 (SCOM)
Description	RX status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	RO	constant = 0b0
4:7	RWX	RX_PSI_LD_UNLD_DLY: Current PSI load to unload delay. TBD. DMB.
8	RWX	RX_PSI_OVER_OR_UNDERRUN_ERR: FIFO Overrun or under-run error. TBD. DMB.
9	RWX	RX_PSI_STATUS_CLEAR: Clears pattern check status. DMB.
10:15	RWX	RX_PSI_STATUS_SPARE: Spares. TBD. DMB.
16:31	RO	constant = 0b0000000000000000

Register Name	TX Control Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.TX_PSI_CNTL
Address	0000000004011830 (SCOM)
Description	TX control register.

Bits	SCOM	Field Mnemonic: Description
0	NCX	Reserved field.
1	RWX	TX_PSI_DRV_PATTERN_EN: Enables the drive pattern to be driven: DMB. 0b0 = No pattern driven 0b1 = Drive pattern
2:3	RWX	TX_PSI_PATTERN_SEL: TX pattern select: DMB. 0b00 = ei4 busy pattern a 0b01 = ei4 busy pattern b 0b10 = 16 bit legacy 0b11 = IE3 busy IAP pattern
4:5	RWX	TX_PSI_CLK_QUIESCE_P: Used to force the output of the CLK P lane to a particular value: DMB. 0b00 = Functional clock (default) 0b01 = Quiesce clock to a static 0 value 0b10 = Quiesce clock to a static 1 value 0b11 = Tri-state clock output
6:7	RWX	TX_PSI_CLK_QUIESCE_N: Used to force the output of the CLK N lane to a particular value: DMB. 0b00 = Functional clock (default) 0b01 = Quiesce clock to a static 0 value 0b10 = Quiesce clock to a static 1 value 0b11 = Tri-state clock output
8:9	RWX	TX_PSI_LANE_QUIESCE: Used to force the output of the data lane to a particular value: DMB. 0b00 = Functional data (default) 0b01 = Quiesce lane to a static 0 value 0b10 = Quiesce lane to a static 1 value 0b11 = Tri-State lane output

Bits	SCOM	Field Mnemonic: Description
10	RWX	TX_PSI_CLK_INVERT: Used to invert the polarity of the clock: DMB. 0b0 = Normal clock polarity (default) 0b1 = Clock inverted
11	RWX	TX_PSI_LANE_INVERT: Used to invert the polarity of the data lane: DMB. 0b0 = Normal data lane polarity (default). 0b1 = Data lane inverted.
12	RWX	TX_PSI_PDWN: Used to power down the PSI TX clock and data path: MBS. 0b0 = Operational (default) 0b1 = Clock and data path are powered off
13	RWX	TX_PSI_BIST_EN: Used to run TX BIST: JGR. 0b0 = TX BIST disabled 0b1 = TX BIST enabled
14:23	RO	constant = 0b0000000000
24:31	RWX	TX_PSI_CNTL_SPARE: Spares. TBD. DMB.

Register Name	TX Mode Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.TX_PSI_MODE
Address	0000000004011831 (SCOM)
Description	TX mode register

Bits	SCOM	Field Mnemonic: Description
0	RWX	TX_PSI_PC_TEST_MODE: Driver segment test mode: MBS. 0b0 = Mission mode enable. 0b1 = Driver output test mode.
1:3	RO	constant = 0b000
4:7	RWX	TX_PSI_MAIN_SLICE_EN_ENC: 240ohm main slice enable (binary code 0000 is zero slices and 0110 is maximum slices). MBS.
8:11	RO	constant = 0b0000
12:15	RWX	TX_PSI_PC_SLICE_EN_ENC: 240ohm precompensation slice enable (binary code 0000 is zero slices and 1110 is maximum slices). MBS.
16:19	RWX	TX_PSI_SLEWCTL: Driver slew control. Bits 2 and 3 are reserved. MBS. 0b0000 = 80ps nominal rate 0b0100 = 110ps nominal rate 0b1000 = 140ps nominal rate 0b1100 = 170ps nominal rate
20:23	RO	constant = 0b0000
24:25	RWX	TX_PSI_PVTNL_ENC: PVT NFET enables for all driver slices: MBS. 0b00 = No PVT NFET enabled 0b01 = Minimum PVT NFET enabled in parallel 0b10 = Maximum PVT NFET enabled in parallel 0b11 = Both PVT NFETs enabled in parallel
26:27	RO	constant = 0b00
28:29	RWX	TX_PSI_PVTPL_ENC: PVT PFET enables for all driver slices: MBS. 0b00 = No PVT PFET enable 0b01 = Minimum PVT PFET enabled in parallel 0b10 = Maximum PVT PFET enabled in parallel 0b11 = Both PVT PFETs enabled in parallel
30:31	RO	constant = 0b00

Register Name	TX Status Register
Mnemonic	PSI.PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.TX_PSI_STATUS
Address	0000000004011832 (SCOM)
Description	TX status register.

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	TX_PSI_STATUS_SPARE: TX status spared. TBD. DMB.
4:6	RWX	TX_PSI_BIST_ERROR: Indicates a TXBIST clock side error occurred: JGR. 0b000 = No errors 0b001 = An error has been found on clkn side 0b010 = An error has been found on clkp side 0b011 = Errors have been found on both clkp and clkn 0b100 = An error has been found in data path 0b101 = Errors have been found in data and clkn paths 0b110 = Errors have been found in data and clkp paths 0b111 = Errors have been found in data, clkp, and clkn paths
7:9	ROX	Reserved field.
10:31	RO	constant = 0b00000000000000000000

Register Name	Configuration of CC Counters Register
Mnemonic	TP.TCN2.N2.SYNC_CONFIG
Address	0000000004030000 (SCOM)
Description	Configuration of CC counters register.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay incoming synchronous pulse. Default are 8 latches including asynchronous. The following values delay the reset of the phase counter: 0000=8 0001=2 0010=3 0011=4 0100=5 0101=6 0110=7 0111=8 1000=9 1001=10 1010=11 1011=12 1100=13 1101=14 1110=15 1111=16
4	RW	LISTEN_TO_SYNC_PULSE_DIS: Disable phase counter synchronization by sync_pulse signal (default is enabled) ATTENTION: When ENABLE listen_to_sync, chiplet gets corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: Default is 0, when set to 1, the alternative input of the sync_pulse will be used ATTENTION: When toggle the input selected, chiplet gets corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: If set, use OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the chiplet_is_aligned bit. See cplt_stat register.

Bits	SCOM	Field Mnemonic: Description
8	RW	UNIT_REGION_CLKCMD_ENABLE: Enable the unit interface to start/stop one dedicate region. Used for POWER9 cache/core.
9	RW	DISABLE_PCB_ITR: Disable interrupt generation within CC. Interrupt sent on each hold event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enable the vital align check to compare alignment of incoming synchronous pulse with 2:1 vital LCB.
11	RW	SYNC_PULSE_OUT_DIS: Disable sync_pulse output when set to 1, master chiplet will not sending synchronous pulses to slave chiplets anymore.
12:19	RW	Unused1219: Unused.

Register Name	OPCG Align Register
Mnemonic	TP.TCN2.N2.OPCG_ALIGN
Address	0000000004030001 (SCOM)
Description	OPCG align register.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
4:7	RW	SNOP_ALIGN: SNOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
8:11	RW	ENOP_ALIGN: ENOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
12:19	RW	INOP_WAIT: INOP cycle delay (0 - 255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0 - 4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0 - 255).
40	RW	INOP_FORCE_SG: INOP: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: SNOP: Set SG high during SNOP.
42	RW	ENOP_FORCE_SG: ENOP: Set SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: 0: A clock change request will first wait the OPCG_WAIT cycles. 1 = A clock change request will not wait, when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: Values: 0 = Use INOPA setting from opcg_reg0 1 = Use rising edge of synchronous pulse 2 = Use unit0_sync_lvl to align (for AVP, refresh0) 3 = Use unit1_sync_lvl to align (for AVP, refresh1)
46	RW	Unused46: Unused.
47:51	RW	SCAN_RATIO: Scan ratio (n=0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1) - Default 4:1=00011.
52:63	RW	OPCG_WAIT_CYCLES: Old PAD value, delay at the begin and end of the OPCG run to allow DC signals to be there at the right time (0 4095). Needs to be higher than plat depth. Default = 0x020.

Register Name	OPCG Control Register 0
Mnemonic	TP.TCN2.N2.OPCG_REG0
Address	0000000004030002 (SCOM)
Description	OPCG control register 0.

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: Values: 0 = BIST (mode used for LBIST) 1 = RUNN (mode used for ABIST/IOBIST)
1	RWX	OPCG_GO: OPCG go (start OPCG). Bit is cleared when OPCG is done. Poll for opcg_done in cplt_start reg.
2	RWX	RUN_SCAN0: Run scan0 (overrides all BIST mode settings but the scan_ratio). Starts a scan0 run, bit gets cleared when OPCG is done . Poll for opcg_done in cplt_start reg.
3	RW	SCAN0_MODE: Set PRPGs in scan0_mode, but do not run automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, OPCG waits for master chiplet to get started. When Keep_MS_Mode is 0, SLAVE_MODE is cleared after incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, OPCG sends out trigger to all slave chiplets. When Keep_MS_MODE is 0, MASTER_MODE gets cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, OPCG in M/S mode bits will not be cleared after one incoming OPCG trigger. Default is clear M/S mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types, clears all the chiplets.
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run scan0 on all regions and types, clears the all chiplets, excluding PLL region, PLL can keep running.
11	RW	RUN_OPCG_ON_UPDATE_DR: Start OPCG engine when scan updated (update_dr) received (set pulse). Cronus requires this bit be set to 1 for a setpulse WRITE.
12	RW	RUN_OPCG_ON_CAPTURE_DR: Start OPCG engine when scan updated (capture_dr) received (set pulse). Cronus requires this bit be set to 1 for a setpulse READ.
13	RW	STOP_RUNN_ON_XSTOP: RUNN mode. Stop run-n on checkstop.
14	RW	OPCG_STARTS_BIST: RUNN mode. OPCG engine controls start_bist for ABIST or IOBIST. See BIST register.
15:20	RW	Unused1520: Unused.
21:63	RWX	LOOP_COUNT: Loop counter for LBIST and RUNN. Write = target value. Read = current counter value. Counts from 0 to target value.

Register Name	OPCG Control Register 1
Mnemonic	TP.TCN2.N2.OPCG_REG1
Address	0000000004030003 (SCOM)
Description	OPCG control register 1.

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0 – 4095). RUNN mode: start_bist match value(0:11).
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture. RUNN mode: start_bist match value(12:23).
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture. RUNN mode: start_bist match value(24:35).

Bits	SCOM	Field Mnemonic: Description
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture. MISRs get active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG only creates even and not odd clocks. Used for RUNN to create only one clock in fast domain. Default is 0.
49	RW	SCAN_CLK_USE_EVEN: Generate scan clock in even cycle instead of odd. Default is 0 = odd for scan.
50:51	RW	Unused2: Unused.
52	RW	RTIM_THOLD_FORCE: Force rtim_thold low when not in test_dc mode (must be 0 at all time).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0: prevent fire of ARY HLD during NSL-fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0: Hold SG high during NSL-fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode: 00 = Enable skitter during lbist_ip 01 = Enable skitter when misr_active (see misr_init_wait) 10 = Skitter OPCG_GO mode: Falling edge = start, Rising edge = stop 11 = Unused
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0 = a-1 to b-1, 1 = start to a and b to end).
58	RW	INFINITE_MODE: Infinite mode. RUNN and LBIST will run forever and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31).

Register Name	**OPCG Control Register 2**
Mnemonic	TP.TCN2.N2.OPCG_REG2
Address	0000000004030004 (SCOM)
Description	OPCG control register 2.

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: OPCG go for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16.
4:15	RWX	PRPG_VALUE: Set to 0 for PRPG always on, else seed.
16:27	RW	PRPG_A_VAL: a value for PRPG aperture.
28:39	RW	PRPG_B_VAL: b value for PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode (0 = a-1 to b-1, 1 = start to a and b to end).
41:63	RW	Unused41_63: Unused.

Register Name	**Scan Region and Type Register**
Mnemonic	TP.TCN2.N2.SCAN_REGION_TYPE
Address	0000000004030005 (SCOM)
Description	Scan region and type register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: Default is 0. When set to 1, the MASK bits in the CMSK chain decide which part is scanned or scan0. MASK=1=scan0, MASK=0 (part of scan chain).
1:2	RO	constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region vitl (vital = clock).

Bits	SCOM	Field Mnemonic: Description
4	RWX	SCAN_REGION_PERV: Scan clock region perv (Pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region CXA1 - CAPP.
6	RWX	SCAN_REGION_UNIT2: Scan clock region PCIS0 - PCI.
7	RWX	SCAN_REGION_UNIT3: Scan clock region PCIS1 - PCI .
8	RWX	SCAN_REGION_UNIT4: Scan clock region PCIS2 - PCI .
9	RWX	SCAN_REGION_UNIT5: Scan clock region IOPSI- IOPSI.
10	RWX	SCAN_REGION_UNIT6: Scan clock region unused.
11	RWX	SCAN_REGION_UNIT7: Scan clock region unused.
12	RWX	SCAN_REGION_UNIT8: Scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: Scan clock region unused.
14	RWX	SCAN_REGION_UNIT10: Scan clock region reserved.
15:47	RO	constant = 0b00000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain func (functional).
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configuration and debug configuration).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain CCFG / GPTR (Pervasive = CC configuration, Others = GPTR).
51	RW	SCAN_TYPE_REGF: Scan chain REGF (register files).
52	RW	SCAN_TYPE_LBIST: Scan chain LBST.
53	RW	SCAN_TYPE_ABIST: Scan chain ABST.
54	RW	SCAN_TYPE_REPR: Scan chain REPR (array repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (array timing).
56	RW	SCAN_TYPE_BNDY: Scan chain BNDY (boundary I/Os).
57	RW	SCAN_TYPE_FARR: Scan chain FARRr (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain CMSK (LBIST channel mask).
59	RW	SCAN_TYPE_INEX: Scan chain IDEX (c14 ASIC).
60:63	RO	constant = 0b0000

Register Name	Start/Stop of Clocks Register
Mnemonic	TP.TCN2.N2.CLK_REGION
Address	0000000004030006 (SCOM)
Description	Start/stop of clocks register.

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00 = NOP 01 = Start 10 = Stop 11 = Pulse (one pulse)
2	RWX	SLAVE_MODE: When selected, clock command waits for master chiplet to get started. Bit gets cleared after incoming slave trigger and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: When selected, clock command sends out trigger to all slave chiplets. Bit gets cleared after sending out one master trigger and Keep_MS_Mode_after_trigger is set to 0.

Bits	SCOM	Field Mnemonic: Description
4	RWX	CLOCK_REGION_PERV: for clock region perv (Pervasive).
5	RWX	CLOCK_REGION_UNIT1: for clock region CXA1 - CAPP.
6	RWX	CLOCK_REGION_UNIT2: for clock region PCIS0 - PCI .
7	RWX	CLOCK_REGION_UNIT3: for clock region PCIS1 - PCI .
8	RWX	CLOCK_REGION_UNIT4: for clock region PCIS2 - PCI .
9	RWX	CLOCK_REGION_UNIT5: for clock region IOPSI- IOPSI .
10	RWX	CLOCK_REGION_UNIT6: for clock region unused.
11	RWX	CLOCK_REGION_UNIT7: for clock region unused.
12	RWX	CLOCK_REGION_UNIT8: for clock region unused.
13	RWX	CLOCK_REGION_UNIT9: for clock region unused.
14	RWX	CLOCK_REGION_UNIT10: for clock region reserved.
15:47	RO	constant = 0b00000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Select SL thresholds.
49	RWX	SEL_THOLD_NSL: Select NSL thresholds.
50	RWX	SEL_THOLD_ARY: Select array threshold.
51	RO	constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support, default for pulse is ODD phase. When this bit is set, pulse is by applied on even phase.
53:63	RO	constant = 0b00000000000

Register Name	Clocks Running SL Register
Mnemonic	TP.TCN2.N2.CLOCK_STAT_SL
Address	0000000004030008 (SCOM)
Description	Clocks running SL register.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: Status of PERV SL hold: 0=run, 1=stop.
5	ROX	CLOCK_STATUS_UNIT1_SL: Status of CXA1 - CAPP SL hold: 0=run, 1=stop.
6	ROX	CLOCK_STATUS_UNIT2_SL:Status of PCIS0 - PCI SL hold: 0=run, 1=stop.
7	ROX	CLOCK_STATUS_UNIT3_SL: Status of PCIS1 - PCI SL hold: 0=run, 1=stop.
8	ROX	CLOCK_STATUS_UNIT4_SL: Status of PCIS2 - PCI i SL hold: 0=run, 1=stop.
9	ROX	CLOCK_STATUS_UNIT5_SL: Status of IOPSI- IOPSI SL hold: 0=run, 1=stop.
10	ROX	CLOCK_STATUS_UNIT6_SL: Status of unused SL hold: 0=run, 1=stop.
11	ROX	CLOCK_STATUS_UNIT7_SL: Status of unused SL hold: 0=run, 1=stop.
12	ROX	CLOCK_STATUS_UNIT8_SL: Status of unused SL hold: 0=run, 1=stop.
13	ROX	CLOCK_STATUS_UNIT9_SL: Status of unused SL hold: 0=run, 1=stop.
14	ROX	CLOCK_STATUS_UNIT10_SL: Status of reserved SL hold: 0=run, 1=stop.
15:63	RO	constant = 0b111111111111111111111111111111111111111111111111111

Register Name	Clocks Running NSL Register
Mnemonic	TP.TCN2.N2.CLOCK_STAT_NSL
Address	0000000004030009 (SCOM)
Description	Clocks running NSL register.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: Status of PERV NSL hold: 0=run, 1=stop.
5	ROX	CLOCK_STATUS_UNIT1_NSL: Status of CXA1 - CAPP NSL hold: 0=run, 1=stop.
6	ROX	CLOCK_STATUS_UNIT2_NSL: Status of PCIS0 - PCI NSL hold: 0=run, 1=stop.
7	ROX	CLOCK_STATUS_UNIT3_NSL: Status of PCIS1 - PCI NSL hold: 0=run, 1=stop.
8	ROX	CLOCK_STATUS_UNIT4_NSL: Status of PCIS0 - PCI NSL hold: 0=run, 1=stop.
9	ROX	CLOCK_STATUS_UNIT5_NSL: Status of IOPSI- IOPSI NSL hold: 0=run, 1=stop.
10	ROX	CLOCK_STATUS_UNIT6_NSL: Status of unused NSL hold: 0=run, 1=stop.
11	ROX	CLOCK_STATUS_UNIT7_NSL: Status of unused NSL hold: 0=run, 1=stop.
12	ROX	CLOCK_STATUS_UNIT8_NSL: Status of unused NSL hold: 0=run, 1=stop.
13	ROX	CLOCK_STATUS_UNIT9_NSL: Status of unused NSL hold: 0=run, 1=stop.
14	ROX	CLOCK_STATUS_UNIT10_NSL: Status of reserved NSL hold: 0=run, 1=stop.
15:63	RO	constant = 0b11111111111111111111111111111111111111111111111111111

Register Name	Clocks Running ARY Register
Mnemonic	TP.TCN2.N2.CLOCK_STAT_ARY
Address	000000000403000A (SCOM)
Description	Clocks running ARY register.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: Status of PERV ARY hold: 0=run, 1=stop.
5	ROX	CLOCK_STATUS_UNIT1_ARY: Status of CXA1 - CAPP ARY hold: 0=run, 1=stop.
6	ROX	CLOCK_STATUS_UNIT2_ARY: Status of PCIS0 - PCI ARY hold: 0=run, 1=stop.
7	ROX	CLOCK_STATUS_UNIT3_ARY: Status of PCIS1 - PCI ARY hold: 0=run, 1=stop.
8	ROX	CLOCK_STATUS_UNIT4_ARY: Status of PCIS0 - PCI ARY hold: 0=run, 1=stop.
9	ROX	CLOCK_STATUS_UNIT5_ARY: Status of IOPSI- IOPSI ARY hold: 0=run, 1=stop.
10	ROX	CLOCK_STATUS_UNIT6_ARY: Status of unused ARY hold: 0=run, 1=stop.
11	ROX	CLOCK_STATUS_UNIT7_ARY: Status of unused ARY hold: 0=run, 1=stop.
12	ROX	CLOCK_STATUS_UNIT8_ARY: Status of unused ARY hold: 0=run, 1=stop.
13	ROX	CLOCK_STATUS_UNIT9_ARY: Status of unused ARY hold: 0=run, 1=stop.
14	ROX	CLOCK_STATUS_UNIT10_ARY: Status of reserved ARY hold: 0=run, 1=stop.
15:63	RO	constant = 0b11111111111111111111111111111111111111111111111111111

Register Name	ABIST and IOBIST Per Region Register
Mnemonic	TP.TCN2.N2.BIST
Address	000000000403000B (SCOM)
Description	ABIST and IOBIST per region register.

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this 0 during ABIST/IOBIST. It could be used to bypass the RUNN start. When this bit is set, the BIST_START_TEST will go high immediately without waiting for RUNN. BIST will start with the first held clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: Select the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: Select the ABIST engines for eDRAMs.
3	RW	TC_IOBIST_MODE_DC: Select the IOBIST engines.
4	RW	BIST_PERV: Region PERV: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
5	RW	BIST_UNIT1: Region CXA1 - CAPP: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
6	RW	BIST_UNIT2: Region PCIS0 - PCI: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
7	RW	BIST_UNIT3:Region PCIS1 - PCI: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
8	RW	BIST_UNIT4: Region PCIS2 - PCI: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
9	RW	BIST_UNIT5: Region IOPSI- IOPSI: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
10	RW	BIST_UNIT6: Region unused: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
11	RW	BIST_UNIT7: Region unused: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
12	RW	BIST_UNIT8: Region unused: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
13	RW	BIST_UNIT9: region unused: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
14	RW	BIST_UNIT10: Region reserved: 1 = BIST_START_TEST for this region will be triggered 0 = The region will take not part of the ABIST/IOBIST run
15:47	RO	constant = 0b00000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: Enable strobe window only in TE=1 mode. OPCGGO tester pin is enabling ABIST compare, once ABIST has been started. Special setup in ABIST engine is required. Default is 0. System mode can not enable this feature.
49:63	RO	constant = 0b0000000000000000

Register Name	Checkstop Per Region Register
Mnemonic	TP.TCN2.N2.XSTOP1
Address	000000000403000C (SCOM)
Description	Checkstop per region register.

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: Mask for checkstop to clockstop of select regions (see xstop_perv,xstop_unit0..n): 0 = Ignore checkstop 1 = Stop on checkstop
1	RW	XSTOP1_Unused: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP1: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, checkstop will wait independent from flush. Default is no wait, when flush is not set.
4	RW	XSTOP1_PERV: Region PERV: 1 = Region will be stopped 0 = Region will keep running on checkstop
5	RW	XSTOP1_UNIT1: Region CXA1 - CAPP: 1 = Region will be stopped 0 = Region will keep running on checkstop
6	RW	XSTOP1_UNIT2: Region PCIS0 - PCI : 1 = Region will be stopped 0 = Region will keep running on checkstop
7	RW	XSTOP1_UNIT3: Region PCIS1- PCI: 1 = Region will be stopped 0 = Region will keep running on checkstop
8	RW	XSTOP1_UNIT4: Region PCIS2- PCI: 1 = Region will be stopped 0 = Region will keep running on checkstop
9	RW	XSTOP1_UNIT5: Region IOPSI - IOPSI: 1 = Region will be stopped 0 = Region will keep running on checkstop
10	RW	XSTOP1_UNIT6: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
11	RW	XSTOP1_UNIT7: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
12	RW	XSTOP1_UNIT8: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
13	RW	XSTOP1_UNIT9: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
14	RW	XSTOP1_UNIT10: Region reserved: 1 = Region will be stopped 0 = Region will keep running on checkstop
15:47	RO	constant = 0b00000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:59	RW	XSTOP1_WAIT_CYCLES: Defines how many cycles XSRTOP will wait after dropping flush, before thresholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	constant = 0b0000

Register Name	Checkstop Per Region Register
Mnemonic	TP.TCN2.N2.XSTOP2
Address	000000000403000D (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: Mask for checkstop to clockstop of select regions (see xstop_perv,xstop_unit0..n): 0 = Ignore checkstop 1 = Stop on checkstop
1	RW	XSTOP2_Unused: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: When set to 1, checkstop will wait independent from flush. Default is no wait, when flush is not set.
4	RW	XSTOP2_PERV: Region PERV: 1 = Region will be stopped 0 = Region will keep running on checkstop
5	RW	XSTOP2_UNIT1: Region CXA1 - CAPP: 1 = Region will be stopped 0 = Region will keep running on checkstop
6	RW	XSTOP2_UNIT2: Region PCIS0 - PCI: 1 = Region will be stopped 0 = Region will keep running on checkstop
7	RW	XSTOP2_UNIT3: Region PCIS1 - PCI: 1 = Region will be stopped 0 = Region will keep running on checkstop
8	RW	XSTOP2_UNIT4: Region PCIS2 - PCI: 1 = Region will be stopped 0 = Region will keep running on checkstop
9	RW	XSTOP2_UNIT5: Region IOPSI - IOPSI: 1 = Region will be stopped 0 = Region will keep running on checkstop
10	RW	XSTOP2_UNIT6: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
11	RW	XSTOP2_UNIT7: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
12	RW	XSTOP2_UNIT8: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
13	RW	XSTOP2_UNIT9: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop

Bits	SCOM	Field Mnemonic: Description
14	RW	XSTOP2_UNIT10: Region reserved: 1 = Region will be stopped 0 = Region will keep running on checkstop
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Defines how many cycles checkstop waits after dropping flush, before thresholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	constant = 0b0000

Register Name	Checkstop Per Region Register
Mnemonic	TP.TCN2.N2.XSTOP3
Address	000000000403000E (SCOM)
Description	Checkstop per region register.

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: Mask for checkstop to clockstop of select regions (see xstop_perv,xstop_unit0..n): 0 = Ignore checkstop 1 = Stop on checkstop
1	RW	XSTOP3_Unused: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP3: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, checkstop will wait independent from flush. Default is no wait, when flush is not set.
4	RW	XSTOP3_PERV: Region PERV: 1 = Region will be stopped 0 = Region will keep running on checkstop
5	RW	XSTOP3_UNIT1: Region CXA1 - CAPP: 1 = Region will be stopped 0 = Region will keep running on checkstop
6	RW	XSTOP3_UNIT2: Region PCIS0 - PCI: 1 = Region will be stopped 0 = Region will keep running on checkstop
7	RW	XSTOP3_UNIT3: Region PCIS1 - PCI: 1 = Region will be stopped 0 = Region will keep running on checkstop
8	RW	XSTOP3_UNIT4: Region PCIS2 - PCI: 1 = Region will be stopped 0 = Region will keep running on checkstop
9	RW	XSTOP3_UNIT5: Region IOPSI - IOPSI: 1 = Region will be stopped 0 = Region will keep running on checkstop
10	RW	XSTOP3_UNIT6: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
11	RW	XSTOP3_UNIT7: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
12	RW	XSTOP3_UNIT8: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop

Bits	SCOM	Field Mnemonic: Description
13	RW	XSTOP3_UNIT9: Region unused: 1 = Region will be stopped 0 = Region will keep running on checkstop
14	RW	XSTOP3_UNIT10: Region reserved: 1 = Region will be stopped 0 = Region will keep running on checkstop
15:47	RO	constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Defines how many cycles checkstop will wait after dropping flush before thresholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	constant = 0b0000

Register Name	Error Status of CC Register
Mnemonic	TP.TCN2.N2.ERROR_STATUS
Address	000000000403000F (SCOM)
Description	Error status of CC register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: Write on read only register.
1	RWX	PCB_READ_NOT_ALLOWED_ERR: Read not allowed, maybe write only register.
2	RWX	PCB_PARITY_ON_CMD_ERR: Parity error on command.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: Invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on address.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: Protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on SPCIF.
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: PCB write while OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: Scan read when OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: Clock command in progress.
11	RWX	SCAN_COLLISION_ERR: Scan region selected of running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set scan region which is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG gets triggered while OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: Phase counters inside chiplet out of sync.
15	RWX	CLOCK_CMD_PREVENTED_ERR: Security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on OPCG state machine.
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on scan/clock region/type or clock status register.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG registers.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on synchronous configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on checkstop register.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0, 4, 5, and 6 registers.
22	RWX	CLKCMD_REQUEST_ERR: Region clock command has one request pending but gets a second one.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error, REQ/ACK sequence wrong.

Bits	SCOM	Field Mnemonic: Description
24	RWX	VITL_ALIGN_ERR: VITL alignment is out of sync to sync pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 sync level pulses are not in sync, AVP broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on self boot command state.
27	RWX	Unused_ERROR27: Unused.
28	RWX	Unused_ERROR28: Unused.
29	RWX	Unused_ERROR29: Unused.
30	RWX	Unused_ERROR30: Unused.
31	RWX	Unused_ERROR31: Unused.

Register Name	OPCG Control Register Capture 1 Register
Mnemonic	TP.TCN2.N2.OPCG_CAPT1
Address	0000000004030010 (SCOM)
Description	OPCG control register capture 1 register.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000=12 cycle 0001 - 1100= cycle 1-12 1101-1111=24 normal, no fast.
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (SL, NSL, ARY, SE, and FCE).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (SL, NSL, ARY, SE, and FCE).
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (SL, NSL, ARY, SE, and FCE).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (SL, NSL, ARY, SE, and FCE).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (SL, NSL, ARY, SE, and FCE).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (SL, NSL, ARY, SE, and FCE).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (SL, NSL, ARY, SE, and FCE).
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (SL, NSL, ARY, SE, and FCE).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (SL, NSL, ARY, SE, and FCE).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (SL, NSL, ARY, SE, and FCE).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (SL, NSL, ARY, SE, and FCE).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (SL, NSL, ARY, SE, and FCE).

Register Name	OPCG Control Register Capture 2 Register
Mnemonic	TP.TCN2.N2.OPCG_CAPT2
Address	0000000004030011 (SCOM)
Description	OPCG control register capture 2.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	Unused_CAPT2: Unused.
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1 even for fast region or cycle 13 for normal region (SL, NSL, ARY, SE, and FCE).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1 odd for fast region or cycle 14 for normal region (SL, NSL, ARY, SE, and FCE).

Bits	SCOM	Field Mnemonic: Description
14:18	RW	(SL, NSL, ARY, SE, and FCE).(SL, NSL, ARY, SE, and FCE).
19:23	RW	SEQ_16_02ODD: Sequence cycle 2 odd for fast region or cycle 16 for normal region (SL, NSL, ARY, SE, and FCE).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3 even for fast region or cycle 17 for normal region (SL, NSL, ARY, SE, and FCE).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3 odd for fast region or cycle 18 for normal region (SL, NSL, ARY, SE, and FCE).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4 even for fast region or cycle 19 for normal region (SL, NSL, ARY, SE, and FCE).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4 odd for fast region or cycle 20 for normal region (SL, NSL, ARY, SE, and FCE).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5 eve- for fast region or cycle 21 for normal region (SL, NSL, ARY, SE, and FCE).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5 odd for fast region or cycle 22 for normal region (SL, NSL, ARY, SE, and FCE).
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6 even for fast region or cycle 23 for normal region (SL, NSL, ARY, SE, and FCE).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6 odd for fast region or cycle 24 for normal region (SL, NSL, ARY, SE, and FCE).

Register Name	**OPCG Control Register Capture 3 Register**
Mnemonic	TP.TCN2.N2.OPCG_CAPT3
Address	0000000004030012 (SCOM)
Description	OPCG control register capture 3.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	Unused_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7 even for fast region (SL, NSL, ARY, SE, and FCE).
9:13	RW	SEQ_07ODD: Sequence cycle 7 odd for fast region (SL, NSL, ARY, SE, and FCE).
14:18	RW	SEQ_08EVEN: Sequence cycle 8 even for fast region (SL, NSL, ARY, SE, and FCE).
19:23	RW	SEQ_08ODD: Sequence cycle 8 odd for fast region (SL, NSL, ARY, SE, and FCE).
24:28	RW	SEQ_09EVEN: Sequence cycle 9 eve- for fast region (SL, NSL, ARY, SE, and FCE).
29:33	RW	SEQ_09ODD: Sequence cycle 9 odd for fast region (SL, NSL, ARY, SE, and FCE).
34:38	RW	SEQ_10EVEN: Sequence cycle 10 even for fast region (SL, NSL, ARY, SE, and FCE).
39:43	RW	SEQ_10ODD: Sequence cycle 10 odd for fast region (SL, NSL, ARY, SE, and FCE).
44:48	RW	SEQ_11EVEN: Sequence cycle 11 even for fast region (SL, NSL, ARY, SE, and FCE).
49:53	RW	SEQ_11ODD: Sequence cycle 11 odd for fast region (SL, NSL, ARY, SE, and FCE).
54:58	RW	SEQ_12EVEN: Sequence cycle 12 even for fast region (SL, NSL, ARY, SE, and FCE).
59:63	RW	SEQ_12ODD: Sequence cycle 12 odd for fast region (SL, NSL, ARY, SE, and FCE).

Register Name	Debug CBS CC Register
Mnemonic	TP.TCN2.N2.DBG_CBS_CC
Address	0000000004030013 (SCOM)
Description	Debug CBS CC register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset endpoint. Is the CC and CTRL in reset state.
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped, when enabled, need plat-depth cycles to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test enable.
4	ROX	DBG_CBS_REQ: CBS Interface - Request (Latched).
5:7	ROX	DBG_CBS_CMD: CBS Interface - Command (Latched).
8:12	ROX	DBG_CBS_STATE: CBS command state machine 00000=Idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS protocol error. REQ raised, although state machine is not in idle. Need reset_ep to clear this bit. No impact on IPL.
15	ROX	DBG_PCB_IDLE: PCB interface in idle state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: Current/latest OPCG mode: 0 = NOP 1 = LBIST 2 = ABIST 3 = RUNN 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN with CaptureDR 9 = Clock change request 10 – 15 = Unused
20:23	ROX	DBG_LAST_OPCG_MODE: previous OPCG MODE.
24	ROX	DBG_PCB_ERROR: PCB interface error. Read CC error register or set CBS_CMD = 001 to switch FSI CBS debug information to CC error register.
25	ROX	DBG_PARITY_ERROR: Any parity error, non PCB parity. Read CC error register or set CBS_CMD = 001 to switch FSI CBS debug information to CC error register.
26	ROX	DBG_CC_ERROR: Any other CC error. Read CC error register or set CBS_CMD = 001 to switch FSI CBS debug information to CC error register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: Is 1 when the a valid align pulse was send out.
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: Reset will clear that bit, the first PCB request will set it.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: Rising or falling edge on test enable after reset. Need reset_ep to clear, no impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on vitl_clkoff after reset. Need reset_ep to clear, no impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: Only representation of CC acknowledgment signal going to FSI.

Register Name	CC Protect Mode Register
Mnemonic	TP.TCN2.N2.CC_PROTECT_MODE_REG
Address	00000000040303FE (SCOM)
Description	CC protect mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCN2.N2.CC_ATOMIC_LOCK_REG
Address	00000000040303FF (SCOM)
Description	Atomic lock register.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	CC_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	Global Checkstop FIR Register
Mnemonic	TP.TCN2.N2.XFIR
Address	0000000004040000 (SCOM)
Description	Global checkstop FIR register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any checkstop).
1	RWX	XFIR_IN1: Checkstop broadcast via OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from pervasive unit.
4	RWX	XFIR_IN4: Checkstop from CXA1.
5	RWX	XFIR_IN5: Checkstop from PCIS0 FIR.
6	RWX	XFIR_IN6: Checkstop from PCIS1 FIR.
7	RWX	XFIR_IN7: Checkstop from PCIS2 FIR.
8	RWX	XFIR_IN8: Checkstop from IOPSI FIR.
9	RWX	XFIR_IN9: Checkstop from PCIS2 FIR_1.
10	RWX	XFIR_IN10: Checkstop from PCIS2 FIR_2.
11	RWX	XFIR_IN11: Checkstop from IOPSI FIR unstaged.
12:25	RWX	XFIR_IN12: Unused.
26	RWX	XFIR_IN26: Checkstop on debug trigger.

Register Name	Global Recoverable FIR Register
Mnemonic	TP.TCN2.N2.RFIR
Address	0000000004040001 (SCOM)
Description	Global recoverable FIR register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop from CXA1.
1	ROX	LFIR_RECOV_ERR: Recoverable error from pervasive unit.
2	ROX	RFIR_IN4: Recover from CXA1.
3	ROX	RFIR_IN5: Recover from PCIS0.
4	ROX	RFIR_IN6: Recover from PCIS1 FIR.
5	ROX	RFIR_IN7: Recover from PCIS2 FIR.
6	ROX	RFIR_IN8: Recover from IOPSI FIR.
7	ROX	RFIR_IN9: Recover from PCIS2 FIR_1.
8	ROX	RFIR_IN10: Recover from PCIS2 FIR_2.
9	ROX	RFIR_IN11: Recover from IOPSI FIR unstaged.
10:23	ROX	RFIR_IN12: Unused.

Register Name	FIR Mask Register
Mnemonic	TP.TCN2.N2.FIR_MASK
Address	0000000004040002 (SCOM)
Description	FIR mask register

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR/RFIR summary bit.
1	RW	FIR_MASK_IN1: Mask for XFIR bit received via OOB broadcast.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: Mask for XFIR from pervasive unit.
4	RW	FIR_MASK_IN4: Mask for CXA1 XFIR and RFIR.
5	RW	FIR_MASK_IN5: Mask for PCIS0 XFIR and RFIR.
6	RW	FIR_MASK_IN6: Mask for PCIS1 XFIR and RFIR.
7	RW	FIR_MASK_IN7: Mask for PCIS2 XFIR and RFIR.
8	RW	FIR_MASK_IN8: Mask for IOPSI XFIR and RFIR.
9	RW	FIR_MASK_IN9: Mask for IOPSI XFIR and RFIR.
10	RW	FIR_MASK_IN10: Mask for IOPSI XFIR and RFIR.
11	RW	FIR_MASK_IN11: Mask for IOPSI XFIR and RFIR.
12:25	RW	FIR_MASK_IN12: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local checkstop to recoverable error.

Register Name	Special Attention Register
Mnemonic	TP.TCN2.N2.SPATTN
Address	0000000004040004 (SCOM) 0000000004040005 (SCOM1) 0000000004040006 (SCOM2)
Description	Special attention register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:9	ROX	NCX	NCX	SPATTN_IN: Unused special attentions.

Register Name	Special Attention Mask Register
Mnemonic	TP.TCN2.N2.SPA_MASK
Address	0000000004040007 (SCOM)
Description	Special attention mask register.

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	Mode Register
Mnemonic	TP.TCN2.N2.EPS.FIR.MODE_REG
Address	0000000004040008 (SCOM)
Description	Mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop chip TOD on checkstop (Unused in POWER9).
5	RW	MODE_IN5: Stop chip TOD on recoverable (Unused in POWER9).
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enable checkstop on special attention.
9	RW	MODE_IN9: Mask direct/local error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention Register
Mnemonic	TP.TCN2.N2.HOSTATTN
Address	0000000004040009 (SCOM)
Description	Host attention register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host attention summary bit.
1	ROX	HOSTATTN_IN1: Unused.
2	ROX	HOSTATTN_IN2: Unused.
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	Local FIR Register
Mnemonic	TP.TCN2.N2.LOCAL_FIR
Address	000000000404000A (SCOM) 000000000404000B (SCOM1) 000000000404000C (SCOM2)
Description	Local FIR register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Local errors from GPIO (PCB error).
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, ...).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from Thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from Thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from Thermal (trip error critical).
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from Thermal (trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Thermal volt trip error.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from debug (error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from trace array0 (SCOM error).
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Local errors from trace array0.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Unused.
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Unused.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Unused.
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Unused.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Unused.
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Unused.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Unused.
21	RWX	WOX_AND	WOX_OR	FIR_IN21: Unused.
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Unused.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Unused.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Errors from Bsense I/O.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Unused.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Unused.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Unused.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Unused.
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Unused.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Unused.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Unused.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Unused.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Unused.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Unused.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction alert broadcast via OOB.

Register Name	Local FIR Mask Register
Mnemonic	TP.TCN2.N2.EPS.FIR.LOCAL_FIR_MASK
Address	000000000404000D (SCOM) 000000000404000E (SCOM1) 000000000404000F (SCOM2)
Description	Local FIR mask register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for LEM error collection vector.

Register Name	Local FIR Action0 Register
Mnemonic	TP.TCN2.N2.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000004040010 (SCOM)
Description	Local FIR action0 register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: Action0 mask.

Register Name	Local FIR Action1 Register
Mnemonic	TP.TCN2.N2.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000004040011 (SCOM)
Description	Local FIR action1 register.

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: Action1 mask.

Register Name	Group Checkstop Mask Register
Mnemonic	TP.TCN2.N2.EPS.FIR.GXSTOP_TRIG_REG
Address	0000000004040013 (SCOM)
Description	Group checkstop mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for group checkstop input (0).

Bits	SCOM	Field Mnemonic: Description
8	RW	GXSTP_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group0 Checkstop Mask Register
Mnemonic	TP.TCN2.N2.EPS.FIR.GXSTOP0_MASK_REG
Address	0000000004040014 (SCOM)
Description	Group0 checkstop mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP0_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group1 Checkstop Mask Register
Mnemonic	TP.TCN2.N2.EPS.FIR.GXSTOP1_MASK_REG
Address	0000000004040015 (SCOM)
Description	Group1 checkstop mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for group checkstop input (1).

Bits	SCOM	Field Mnemonic: Description
9	RW	GXSTP1_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group2 Checkstop Mask Register
Mnemonic	TP.TCN2.N2.EPS.FIR.GXSTOP2_MASK_REG
Address	0000000004040016 (SCOM)
Description	Group2 checkstop mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for OOB sys_checkstop input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for OOB sys_checkstop input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	Summary Mask Register
Mnemonic	TP.TCN2.N2.EPS.FIR.SUM_MASK_REG
Address	0000000004040017 (SCOM)
Description	Summary mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type4 (host attention) summary bit.

Register Name	Local Checkstop Register
Mnemonic	TP.TCN2.N2.LOCAL_XSTOP_ERR
Address	0000000004040018 (SCOM)
Description	Local checkstop register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop from CXA1, bit 0.
1	ROX	LOCAL_XSTOP_IN1: Local checkstop from CXA1, bit 0.
2	ROX	LOCAL_XSTOP_IN2: Unused.
3	ROX	LOCAL_XSTOP_IN3: Unused.
4	ROX	LOCAL_XSTOP_IN4: Unused.
5	ROX	LOCAL_XSTOP_IN5: Unused.
6	ROX	LOCAL_XSTOP_IN6: Unused.
7	ROX	LOCAL_XSTOP_IN7: Unused.
8	ROX	LOCAL_XSTOP_IN8: Unused.
9	ROX	LOCAL_XSTOP_IN9: Unused.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask Register
Mnemonic	TP.TCN2.N2.LOCAL_XSTOP_MASK
Address	0000000004040019 (SCOM)
Description	Local checkstop mask register.

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask Register
Mnemonic	TP.TCN2.N2.HOSTATTN_MASK
Address	000000000404001A (SCOM)
Description	Host attention mask register.

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Thermal Sensor loop1 Results Register
Mnemonic	TP.TCN2.N2.EPS.THERM.DTS_RESULT0
Address	0000000004050000 (SCOM)
Description	DTS thermal sensor loop1 results.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results Register
Mnemonic	TP.TCN2.N2.EPS.THERM.DTS_TRC_RESULT
Address	0000000004050003 (SCOM)
Description	DTS trace results register.

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.

Register Name	CPM and DTS Enables and Controls Register
Mnemonic	TP.TCN2.N2.EPS.THERM.THERM_MODE_REG
Address	000000000405000F (SCOM)
Description	CPM and DTS enables and controls register.

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: Force tpc_therm_thres_mac clock gating off and activates clocks.
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables: 1xx = trip0 - warning x1x =trip1 - critical xx1 =trip2 - fatal

Bits	SCOM	Field Mnemonic: Description
5	RW	THERM_DTS_SAMPLE_ENA: 0: No DTS sampling, 1 = DTS sampling is enabled and below counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is feed into an 18 bit counter. With the therm_sample_pulse_cnt it is possible to select a high order bit of the counter to enable a resolutions of sampling DTSs between 2.5 us and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a DTS sample. 0000 = 16 ms 0001 = 8 ms 0010 = 4 ms 0011 = 2 ms 0100 = 1 ms 0101 = 0.5 ms 0110 = 250 us 0111 = 125 us 1000 = 62 .5us 1001 = 31.3 us 1010 = 15.6 us 1011 = 7.8 us 1100 = 3.9 us 1101 = 2 us 1110 = 1 us 1111 = 0.5 us
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in threshold unit: 00 = Off 11 = Illegal 10 = Maximum mode 01 = Minimum mode
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: Values: 0 = therm_overflow_err will be enabled 1 = therm_overflow_err will be disabled
15	RW	THERM_MODE_Unused: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result will be provided with PCB read addr_v(4): 0000 = DTS 0 0001 = DTS 1 0010 = DTS 2 0100 = DTS 4 1111 = Worst case sensor
20:21	RW	THERM_DTS_ENABLE_L1: Loop1 DTS enables: 1x = DTS 0 available x1 = DTS 1 available
22:34	RO	constant = 0b0000000000000
35:36	RW	Reserved field.

Register Name	Skitter Control Register
Mnemonic	TP.TCN2.N2.EPS.THERM.SKITTER_MODE_REG
Address	0000000004050010 (SCOM)
Description	Skitter control register.

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold current sample.
1	RW	DISABLE_SKITTER_STICKINESS: If '0' accumulation mode, '1' samples new value each cycle and resets sticky value.
2:3	RW	SKITTER_MODE_Unused1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0 = hold_on_trigger0, bit1 = _on_trigger1.
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0 = reset_sticky_on_trigger0, bit1 = reset_sticky_on_trigger1.
8:9	RW	SKITTER_SAMPLE_GUTS: Selects guts to measure: 00 = guts1 01 = guts2 10 = guts3 11 = guts4
10:43	RO	constant = 0b00000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold current sample on DBG trigger, this has highest priority.
45	ROX	SKITTER_DATA_V_LT: If '1' the data requested by a skitter force read register has finished and data is present in skitter data register in the collector macro. The data can be read by any combination of V25/V26/V27 PCB reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TCN2.N2.EPS.THERM.INJECT_REG
Address	0000000004050011 (SCOM)
Description	Error injection control register.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: Values: 00 = No injection 01 = Warning trip level injection 10 = Critical trip level injection 11 = Fatal trip level injection
2:3	RW	THERM_INJECT_MODE: Values: 00 = No injection 01 = Injection on the next DTS sample 10 = Solid injection for the next DTS samples until bit setting changes 11 = Not used

Register Name	Control/Force Reset Register
Mnemonic	TP.TCN2.N2.EPS.THERM.CONTROL_REG
Address	0000000004050012 (SCOM)
Description	Control/force reset register.

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved field.
1	WO_1P	Reserved field.
2	WO_1P	Reserved field.
3	WO_1P	Reserved field.

Bits	SCOM	Field Mnemonic: Description
4	WO_1P	Reserved field.
5	WO_1P	Reserved field.
6	WO_1P	Reserved field.
7	WO_1P	Reserved field.
8	WO_1P	Reserved field.
9	WO_1P	Reserved field.
10	WO_1P	Reserved field.
11	WO_1P	Reserved field.
12	WO_1P	Reserved field.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCN2.N2.EPS.THERM.ERR_STATUS_REG
Address	0000000004050013 (SCOM)
Description	Thermal error status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Thermal mode register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter mode register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter force register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan initial version register parity error mask.
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt mode register parity error mask.
22	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: Threshold state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Force skitter read one hot error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	constant = 0b00000000
40:43	ROX	Reserved field.
44:46	ROX	Reserved field.
47	ROX	Reserved field.
48	ROX	Reserved field.
49:50	ROX	Reserved field.
51:54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCN2.N2.EPS.THERM.SKITTER_FORCE_REG
Address	0000000004050014 (SCOM)
Description	Skitter force read register.

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter.

Register Name	Skitter Clock Source Control Register
Mnemonic	TP.TCN2.N2.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000004050016 (SCOM)
Description	Skitter clock source control register.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects clock to measure: 000 = Local mesh clock 001 = External pin skitter_c1_1_in 010 = Local d1clk only if d_mode = 1 011 = External pin skitter_c1_2_in 100 = Local lclk only if d_mode = 1 101 = External pin skitter_c1_3_in 110 = Unused 111 = External pin skitter_c1_4_in
3:35	RO	constant = 0b00000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: To select delay to be added between clock source MUX inverter chain (base line delay is 12.2 psec) of skitter 0: 00 = No delay 01 = 0.6psec 10 = 1.8 psec 11 = 5 psec

Register Name	Skitter Data Register Read Bit 0:63
Mnemonic	TP.TCN2.N2.EPS.THERM.SKITTER_DATA0
Address	0000000004050019 (SCOM)
Description	Skitter data register read bit 0:63.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bit 32:95
Mnemonic	TP.TCN2.N2.EPS.THERM.SKITTER_DATA1
Address	000000000405001A (SCOM)
Description	Skitter data register read bit 32:95.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bit 64:127
Mnemonic	TP.TCN2.N2.EPS.THERM.SKITTER_DATA2
Address	000000000405001B (SCOM)
Description	Skitter data register read bit 64:127.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Timestamp Counter Read
Mnemonic	TP.TCN2.N2.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000405001C (SCOM)
Description	Timestamp counter read.

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.

8. PB Chiplet (Nest Chiplet 3)

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
BRIDGE.HCA.EHHCA_FIR_ACTION0_REG	0x0000000005012986	1980
BRIDGE.HCA.EHHCA_FIR_ACTION1_REG	0x0000000005012987	1981
BRIDGE.HCA.EHHCA_FIR_MASK_REG	0x0000000005012983	1979
BRIDGE.HCA.EHHCA_FIR_REG	0x0000000005012980	1978
BRIDGE.HCA.HCA_BAR	0x000000000501298A	1983
BRIDGE.HCA.HCA_COUNT_BAR	0x000000000501298B	1983
BRIDGE.HCA.HCA_DROP	0x0000000005012991	1985
BRIDGE.HCA.HCA_FLUSH	0x0000000005012990	1984
BRIDGE.HCA.HCA_MIRROR_BAR	0x0000000005012993	1985
BRIDGE.HCA.HCA_MODES	0x000000000501298F	1984
BRIDGE.HCA.HCA_REF_BAR	0x000000000501298E	1983
BRIDGE.HCA.HCA_RESET	0x0000000005012992	1985
BRIDGE.LPC.SYNC_FIR_ACTION0_REG	0x00000000050129C6	1987
BRIDGE.LPC.SYNC_FIR_ACTION1_REG	0x00000000050129C7	1988
BRIDGE.LPC.SYNC_FIR_MASK_REG	0x00000000050129C3	1986
BRIDGE.LPC.SYNC_FIR_REG	0x00000000050129C0	1985
BRIDGE.NHTM.NHTM0.SC.HTM_CFG	0x0000000005012888	1961
BRIDGE.NHTM.NHTM0.SC.HTM_CTRL	0x0000000005012885	1959
BRIDGE.NHTM.NHTM0.SC.HTM_FILT	0x0000000005012886	1959
BRIDGE.NHTM.NHTM0.SC.HTM_FLEX	0x0000000005012889	1961
BRIDGE.NHTM.NHTM0.SC.HTM_LAST	0x0000000005012883	1958
BRIDGE.NHTM.NHTM0.SC.HTM_MEM	0x0000000005012881	1957
BRIDGE.NHTM.NHTM0.SC.HTM_MODE	0x0000000005012880	1955
BRIDGE.NHTM.NHTM0.SC.HTM_STAT	0x0000000005012882	1957
BRIDGE.NHTM.NHTM0.SC.HTM_TRIG	0x0000000005012884	1958
BRIDGE.NHTM.NHTM0.SC.HTM_TTYPEFILT	0x0000000005012887	1960
BRIDGE.NHTM.NHTM1.SC.HTM_CFG	0x00000000050128C8	1967
BRIDGE.NHTM.NHTM1.SC.HTM_CTRL	0x00000000050128C5	1965
BRIDGE.NHTM.NHTM1.SC.HTM_FILT	0x00000000050128C6	1966
BRIDGE.NHTM.NHTM1.SC.HTM_FLEX	0x00000000050128C9	1967
BRIDGE.NHTM.NHTM1.SC.HTM_LAST	0x00000000050128C3	1964
BRIDGE.NHTM.NHTM1.SC.HTM_MEM	0x00000000050128C1	1963
BRIDGE.NHTM.NHTM1.SC.HTM_MODE	0x00000000050128C0	1962
BRIDGE.NHTM.NHTM1.SC.HTM_STAT	0x00000000050128C2	1964
BRIDGE.NHTM.NHTM1.SC.HTM_TRIG	0x00000000050128C4	1965
BRIDGE.NHTM.NHTM1.SC.HTM_TTYPEFILT	0x00000000050128C7	1966
BRIDGE.PBA.PBACFG	0x000000000501284B	1946
BRIDGE.PBA.PBAERRRPT0	0x000000000501284C	1948
BRIDGE.PBA.PBAERRRPT1	0x000000000501284D	1949
BRIDGE.PBA.PBAERRRPT2	0x000000000501284E	1949
BRIDGE.PBA.PBAFIR	0x0000000005012840	1941
BRIDGE.PBA.PBAFIRACT0	0x0000000005012846	1945

Mnemonic	Address	Page
BRIDGE.PBA.PBAFIRACT1	0x0000000005012847	1946
BRIDGE.PBA.PBAFIRMASK	0x0000000005012843	1944
BRIDGE.PBA.PBAOCCACT	0x000000000501284A	1946
BRIDGE.PBA.PBARBUFVAL0	0x0000000005012850	1950
BRIDGE.PBA.PBARBUFVAL1	0x0000000005012851	1951
BRIDGE.PBA.PBARBUFVAL2	0x0000000005012852	1951
BRIDGE.PBA.PBARBUFVAL3	0x0000000005012853	1952
BRIDGE.PBA.PBARBUFVAL4	0x0000000005012854	1953
BRIDGE.PBA.PBARBUFVAL5	0x0000000005012855	1953
BRIDGE.PBA.PBAWBUFVAL0	0x0000000005012858	1954
BRIDGE.PBA.PBAWBUFVAL1	0x0000000005012859	1955
BRIDGE.PBA.SCOMTRUST.PBABAR0	0x0000000005012B00	1988
BRIDGE.PBA.SCOMTRUST.PBABAR1	0x0000000005012B01	1989
BRIDGE.PBA.SCOMTRUST.PBABAR2	0x0000000005012B02	1989
BRIDGE.PBA.SCOMTRUST.PBABAR3	0x0000000005012B03	1990
BRIDGE.PBA.SCOMTRUST.PBABARMSK0	0x0000000005012B04	1990
BRIDGE.PBA.SCOMTRUST.PBABARMSK1	0x0000000005012B05	1991
BRIDGE.PBA.SCOMTRUST.PBABARMSK2	0x0000000005012B06	1991
BRIDGE.PBA.SCOMTRUST.PBABARMSK3	0x0000000005012B07	1991
BRIDGE.PSI.PSI_WRAP.EECNT_REG	0x0000000005012809	1936
BRIDGE.PSI.PSI_WRAP.RX_CH_FSM_REG	0x000000000501280D	1938
BRIDGE.PSI.PSI_WRAP.RX_CH_INTADDR_REG	0x0000000005012818	1940
BRIDGE.PSI.PSI_WRAP.RX_CH_MISC_REG	0x000000000501281B	1941
BRIDGE.PSI.PSI_WRAP.RX_CTRL_STAT_REG	0x0000000005012808	1935
BRIDGE.PSI.PSI_WRAP.RX_DBFF_REG0	0x0000000005012819	1940
BRIDGE.PSI.PSI_WRAP.RX_DBFF_REG1	0x000000000501281A	1940
BRIDGE.PSI.PSI_WRAP.RX_DF_FSM_REG	0x000000000501280E	1938
BRIDGE.PSI.PSI_WRAP.RX_ERROR_REG	0x000000000501280A	1936
BRIDGE.PSI.PSI_WRAP.RX_ERR_MODE	0x000000000501280F	1938
BRIDGE.PSI.PSI_WRAP.RX_MASK_REG	0x000000000501280B	1937
BRIDGE.PSI.PSI_WRAP.TX_CH_FSM_REG	0x0000000005012805	1934
BRIDGE.PSI.PSI_WRAP.TX_CH_INTADDR_REG	0x0000000005012810	1939
BRIDGE.PSI.PSI_WRAP.TX_CH_MISC_REG	0x0000000005012813	1939
BRIDGE.PSI.PSI_WRAP.TX_CTRL_STAT_REG	0x0000000005012800	1931
BRIDGE.PSI.PSI_WRAP.TX_DBFF_REG0	0x0000000005012811	1939
BRIDGE.PSI.PSI_WRAP.TX_DBFF_REG1	0x0000000005012812	1939
BRIDGE.PSI.PSI_WRAP.TX_DF_FSM_REG	0x0000000005012806	1935
BRIDGE.PSI.PSI_WRAP.TX_ERROR_REG	0x0000000005012802	1932
BRIDGE.PSI.PSI_WRAP.TX_ERR_MODE	0x0000000005012807	1935
BRIDGE.PSI.PSI_WRAP.TX_MASK_REG	0x0000000005012803	1933
BRIDGE.PSI.PSI_WRAP.TX_TO_RT_REG	0x0000000005012801	1932
BRIDGE.PSIHB.DMA_UP_ADDR	0x0000000005012914	1976
BRIDGE.PSIHB.ESB_CI_BASE	0x0000000005012916	1976
BRIDGE.PSIHB.ESB_NOTIFY	0x0000000005012917	1976
BRIDGE.PSIHB.IVT_OFFSET	0x0000000005012918	1977
BRIDGE.PSIHB.NOTRUST_BAR0	0x0000000005012B40	1992
BRIDGE.PSIHB.NOTRUST_BAR0MASK	0x0000000005012B42	1992
BRIDGE.PSIHB.NOTRUST_BAR1	0x0000000005012B41	1992

Mnemonic	Address	Page
BRIDGE.PSIHB.NOTRUST_BAR1MASK	0x0000000005012B43	1992
BRIDGE.PSIHB.PSIHB_DEBUG_REG	0x0000000005012911	1975
BRIDGE.PSIHB.PSIHB_ERROR_MASK_REG	0x000000000501290F	1975
BRIDGE.PSIHB.PSIHB_FIR_ACTION0_REG	0x0000000005012906	1970
BRIDGE.PSIHB.PSIHB_FIR_ACTION1_REG	0x0000000005012907	1971
BRIDGE.PSIHB.PSIHB_FIR_MASK_REG	0x0000000005012903	1969
BRIDGE.PSIHB.PSIHB_FIR_REG	0x0000000005012900	1968
BRIDGE.PSIHB.PSIHB_INTERRUPT_CONTROL	0x0000000005012915	1976
BRIDGE.PSIHB.PSIHB_INTERRUPT_LEVEL	0x0000000005012919	1977
BRIDGE.PSIHB.PSIHB_INTERRUPT_STATUS	0x000000000501291A	1978
BRIDGE.PSIHB.PSIHB_STATUS_CTL_REG	0x000000000501290E	1973
BRIDGE.PSIHB.PSI_BRIDGE_BAR_REG	0x000000000501290A	1972
BRIDGE.PSIHB.PSI_BRIDGE_FSP_BAR_REG	0x000000000501290B	1973
BRIDGE.PSIHB.PSI_FSP_MMR_REG	0x000000000501290C	1973
BRIDGE.PSIHB.PSI_TCE_ADDR_REG	0x0000000005012B44	1993
BRIDGE.PSIHB.TRUST_CONTROL	0x0000000005012B45	1993
INT.INT_CQ.INT_CQ_ACTION0	0x0000000005013036	2030
INT.INT_CQ.INT_CQ_ACTION1	0x0000000005013037	2030
INT.INT_CQ.INT_CQ_AIB_CTL	0x0000000005013022	2019
INT.INT_CQ.INT_CQ_CFG_LDQ	0x0000000005013026	2022
INT.INT_CQ.INT_CQ_CFG_PB_GEN	0x000000000501300A	2012
INT.INT_CQ.INT_CQ_CFG_STQ1	0x0000000005013024	2021
INT.INT_CQ.INT_CQ_CFG_STQ2	0x0000000005013025	2021
INT.INT_CQ.INT_CQ_CNPM_SEL	0x000000000501300F	2013
INT.INT_CQ.INT_CQ_ERR_INFO0	0x000000000501303A	2031
INT.INT_CQ.INT_CQ_ERR_INFO1	0x000000000501303B	2032
INT.INT_CQ.INT_CQ_ERR_INFO2	0x000000000501303C	2032
INT.INT_CQ.INT_CQ_ERR_INFO3	0x000000000501303D	2033
INT.INT_CQ.INT_CQ_ERR_RPT_HOLD	0x0000000005013039	2030
INT.INT_CQ.INT_CQ_FIR	0x0000000005013030	2025
INT.INT_CQ.INT_CQ_FIRMASK	0x0000000005013033	2029
INT.INT_CQ.INT_CQ_IC_BAR	0x0000000005013010	2013
INT.INT_CQ.INT_CQ_MSGSND	0x000000000501300B	2012
INT.INT_CQ.INT_CQ_PBI_CTL	0x0000000005013020	2016
INT.INT_CQ.INT_CQ_PBO_CTL	0x0000000005013021	2017
INT.INT_CQ.INT_CQ_PC_BAR	0x0000000005013016	2014
INT.INT_CQ.INT_CQ_PC_BARM	0x0000000005013017	2015
INT.INT_CQ.INT_CQ_PMC_0	0x0000000005013028	2023
INT.INT_CQ.INT_CQ_PMC_1	0x0000000005013029	2023
INT.INT_CQ.INT_CQ_PMC_2	0x000000000501302A	2023
INT.INT_CQ.INT_CQ_PMC_3	0x000000000501302B	2024
INT.INT_CQ.INT_CQ_PMC_4	0x000000000501302C	2024
INT.INT_CQ.INT_CQ_PMC_5	0x000000000501302D	2024
INT.INT_CQ.INT_CQ_PMC_6	0x000000000501302E	2025
INT.INT_CQ.INT_CQ_PMC_7	0x000000000501302F	2025
INT.INT_CQ.INT_CQ_PM_CTL	0x0000000005013027	2022
INT.INT_CQ.INT_CQ_RST_CTL	0x0000000005013023	2020
INT.INT_CQ.INT_CQ_SWI_RSP	0x0000000005013009	2011

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INT.INT_CQ.INT_CQ_TAR	0x000000000501301E	2016
INT.INT_CQ.INT_CQ_TM1_BAR	0x0000000005013012	2014
INT.INT_CQ.INT_CQ_TM2_BAR	0x0000000005013014	2014
INT.INT_CQ.INT_CQ_VC_BAR	0x0000000005013018	2015
INT.INT_CQ.INT_CQ_VC_BARM	0x0000000005013019	2015
INT.INT_PC.INT_PC_AIB_RX_CRD_CMD	0x0000000005013121	2045
INT.INT_PC.INT_PC_AIB_RX_CRD_DAT	0x0000000005013122	2046
INT.INT_PC.INT_PC_AIB_RX_CRD_INIT	0x0000000005013120	2045
INT.INT_PC.INT_PC_AIB_TX_CRD	0x0000000005013124	2046
INT.INT_PC.INT_PC_AIB_TX_ORDER	0x0000000005013126	2047
INT.INT_PC.INT_PC_AIB_TX_PRIO	0x0000000005013125	2047
INT.INT_PC.INT_PC_AT_KILL	0x0000000005013116	2038
INT.INT_PC.INT_PC_AT_KILL_MASK	0x0000000005013117	2039
INT.INT_PC.INT_PC_DBG_ECC	0x0000000005013131	2048
INT.INT_PC.INT_PC_DBG_PMC	0x0000000005013134	2049
INT.INT_PC.INT_PC_DBG_PMC_ATX0	0x0000000005013135	2050
INT.INT_PC.INT_PC_DBG_PMC_ATX1	0x0000000005013136	2050
INT.INT_PC.INT_PC_DBG_PMC_ATX2	0x0000000005013137	2051
INT.INT_PC.INT_PC_DBG_TMOT	0x0000000005013130	2048
INT.INT_PC.INT_PC_DBG_TRACE	0x0000000005013133	2049
INT.INT_PC.INT_PC_EQD_BLOCK_MODE	0x0000000005013114	2038
INT.INT_PC.INT_PC_ERR0_CFG0	0x0000000005013140	2051
INT.INT_PC.INT_PC_ERR0_CFG1	0x0000000005013141	2052
INT.INT_PC.INT_PC_ERR0_FATAL	0x0000000005013144	2052
INT.INT_PC.INT_PC_ERR0_INFO	0x0000000005013146	2053
INT.INT_PC.INT_PC_ERR0_RECOV	0x0000000005013145	2052
INT.INT_PC.INT_PC_ERR0_WOF	0x0000000005013142	2052
INT.INT_PC.INT_PC_ERR0_WOF_DETAIL	0x0000000005013143	2052
INT.INT_PC.INT_PC_ERR1_CFG0	0x0000000005013148	2053
INT.INT_PC.INT_PC_ERR1_CFG1	0x0000000005013149	2053
INT.INT_PC.INT_PC_ERR1_FATAL	0x000000000501314C	2054
INT.INT_PC.INT_PC_ERR1_INFO	0x000000000501314E	2054
INT.INT_PC.INT_PC_ERR1_RECOV	0x000000000501314D	2054
INT.INT_PC.INT_PC_ERR1_WOF	0x000000000501314A	2053
INT.INT_PC.INT_PC_ERR1_WOF_DETAIL	0x000000000501314B	2054
INT.INT_PC.INT_PC_GLOBAL_CFG	0x0000000005013110	2036
INT.INT_PC.INT_PC_IVE_BLOCK_MODE	0x0000000005013113	2037
INT.INT_PC.INT_PC_MMIO_ARB	0x000000000501311A	2040
INT.INT_PC.INT_PC_PCMD_ARB	0x0000000005013118	2039
INT.INT_PC.INT_PC_VPD_BLOCK_MODE	0x0000000005013115	2038
INT.INT_PC.INT_PC_VRQ_CFG	0x000000000501311C	2041
INT.INT_PC.INT_PC_VRQ_PEND_ARB	0x000000000501311D	2042
INT.INT_PC.INT_PC_VRQ_VPC_ARB	0x000000000501311F	2044
INT.INT_PC.INT_PC_VRQ_VPC_CRD	0x000000000501311E	2043
INT.INT_PC.INT_PC_VSD_TABLE_ADDR	0x0000000005013111	2037
INT.INT_PC.INT_TCTXT_CFG	0x0000000005013100	2033
INT.INT_PC.INT_TCTXT_EN0	0x0000000005013108	2036
INT.INT_PC.INT_TCTXT_EN1	0x000000000501310C	2036

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INT.INT_PC.INT_TCTXT_INDIR0	0x0000000005013104	2035
INT.INT_PC.INT_TCTXT_INDIR1	0x0000000005013105	2035
INT.INT_PC.INT_TCTXT_INDIR2	0x0000000005013106	2035
INT.INT_PC.INT_TCTXT_INDIR3	0x0000000005013107	2035
INT.INT_PC.INT_TCTXT_TRACK	0x0000000005013101	2034
INT.INT_PC.LBS2.INT_PC_VPC_ADDITIONAL_PERF_1	0x0000000005013174	2062
INT.INT_PC.LBS2.INT_PC_VPC_ADDITIONAL_PERF_2	0x0000000005013175	2063
INT.INT_PC.LBS2.INT_PC_VPC_CACHE_EN	0x0000000005013161	2055
INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA0	0x0000000005013168	2057
INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA2	0x000000000501316A	2058
INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA3	0x000000000501316B	2058
INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA4	0x000000000501316C	2058
INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA6	0x000000000501316E	2059
INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA7	0x000000000501316F	2059
INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_SPEC	0x0000000005013167	2057
INT.INT_PC.LBS2.INT_PC_VPC_CONFIG	0x0000000005013164	2056
INT.INT_PC.LBS2.INT_PC_VPC_DEBUG	0x0000000005013170	2059
INT.INT_PC.LBS2.INT_PC_VPC_ERR_CFG0	0x0000000005013178	2063
INT.INT_PC.LBS2.INT_PC_VPC_ERR_CFG1	0x0000000005013179	2063
INT.INT_PC.LBS2.INT_PC_VPC_FATAL_ERR	0x000000000501317C	2064
INT.INT_PC.LBS2.INT_PC_VPC_INFO_ERR	0x000000000501317E	2064
INT.INT_PC.LBS2.INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD	0x0000000005013160	2054
INT.INT_PC.LBS2.INT_PC_VPC_PERF_EVENT_SEL_1	0x0000000005013171	2060
INT.INT_PC.LBS2.INT_PC_VPC_PERF_EVENT_SEL_2	0x0000000005013172	2061
INT.INT_PC.LBS2.INT_PC_VPC_PERF_EVENT_SEL_3	0x0000000005013173	2062
INT.INT_PC.LBS2.INT_PC_VPC_RECOV_ERR	0x000000000501317D	2064
INT.INT_PC.LBS2.INT_PC_VPC_SCRUB_MASK	0x0000000005013163	2056
INT.INT_PC.LBS2.INT_PC_VPC_SCRUB_TRIG	0x0000000005013162	2055
INT.INT_PC.LBS2.INT_PC_VPC_WOF_ERR	0x000000000501317A	2063
INT.INT_PC.LBS2.INT_PC_VPC_WOF_ERR_DETAIL	0x000000000501317B	2064
INT.INT_VC.INT_VC_AIB_TIMEOUT	0x000000000501322B	2084
INT.INT_VC.INT_VC_AIB_TX_CMD_PRIORITY	0x000000000501323D	2090
INT.INT_VC.INT_VC_AIB_TX_ORDERING_TAG_1	0x000000000501322C	2084
INT.INT_VC.INT_VC_AIB_TX_ORDERING_TAG_2	0x000000000501322D	2084
INT.INT_VC.INT_VC_ATX_INIT_CREDIT_COUNT	0x000000000501323C	2089
INT.INT_VC.INT_VC_ATX_PERF_EVENT_SEL_1	0x0000000005013240	2091
INT.INT_VC.INT_VC_ATX_PERF_EVENT_SEL_2	0x0000000005013241	2092
INT.INT_VC.INT_VC_ATX_PERF_EVENT_SEL_3	0x0000000005013242	2092
INT.INT_VC.INT_VC_AT_MACRO_KILL	0x000000000501323E	2090
INT.INT_VC.INT_VC_AT_MACRO_KILL_MASK	0x000000000501323F	2091
INT.INT_VC.INT_VC_EQC_ADDITIONAL_PERF_1	0x0000000005013253	2095
INT.INT_VC.INT_VC_EQC_ADDITIONAL_PERF_2	0x0000000005013254	2095
INT.INT_VC.INT_VC_EQC_CACHE_EN	0x0000000005013211	2074
INT.INT_VC.INT_VC_EQC_CACHE_WATCH_DATA0	0x0000000005013216	2076
INT.INT_VC.INT_VC_EQC_CACHE_WATCH_DATA1	0x0000000005013217	2076
INT.INT_VC.INT_VC_EQC_CACHE_WATCH_DATA2	0x0000000005013218	2077
INT.INT_VC.INT_VC_EQC_CACHE_WATCH_DATA3	0x0000000005013219	2077
INT.INT_VC.INT_VC_EQC_CACHE_WATCH_SPEC	0x0000000005013215	2075

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INT.INT_VC.INT_VC_EQC_CONFIG	0x0000000005013214	2075
INT.INT_VC.INT_VC_EQC_DEBUG	0x000000000501321A	2078
INT.INT_VC.INT_VC_EQC_PERF_EVENT_SEL_1	0x0000000005013250	2093
INT.INT_VC.INT_VC_EQC_PERF_EVENT_SEL_2	0x0000000005013251	2094
INT.INT_VC.INT_VC_EQC_PERF_EVENT_SEL_3	0x0000000005013252	2094
INT.INT_VC.INT_VC_EQC_SCRUB_MASK	0x0000000005013213	2074
INT.INT_VC.INT_VC_EQC_SCRUB_TRIG	0x0000000005013212	2074
INT.INT_VC.INT_VC_EQD_BLOCK_MODE	0x0000000005013204	2066
INT.INT_VC.INT_VC_ERR_CFG_G0R0	0x0000000005013270	2102
INT.INT_VC.INT_VC_ERR_CFG_G0R1	0x0000000005013271	2102
INT.INT_VC.INT_VC_ERR_CFG_G1R0	0x0000000005013272	2102
INT.INT_VC.INT_VC_ERR_CFG_G1R1	0x0000000005013273	2103
INT.INT_VC.INT_VC_FATAL_ERR_G0	0x0000000005013278	2108
INT.INT_VC.INT_VC_FATAL_ERR_G1	0x000000000501327B	2109
INT.INT_VC.INT_VC_GLOBAL_CONFIG	0x0000000005013200	2065
INT.INT_VC.INT_VC_INFO_ERR_G0	0x000000000501327A	2108
INT.INT_VC.INT_VC_INFO_ERR_G1	0x000000000501327D	2109
INT.INT_VC.INT_VC_IRQ_CONFIG_0	0x0000000005013208	2067
INT.INT_VC.INT_VC_IRQ_CONFIG_1	0x0000000005013209	2068
INT.INT_VC.INT_VC_IRQ_CONFIG_2	0x000000000501320A	2069
INT.INT_VC.INT_VC_IRQ_CONFIG_3	0x000000000501320B	2070
INT.INT_VC.INT_VC_IRQ_CONFIG_4	0x000000000501320C	2071
INT.INT_VC.INT_VC_IRQ_CONFIG_5	0x000000000501320D	2072
INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_0	0x0000000005013268	2099
INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_1	0x0000000005013269	2100
INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_2	0x000000000501326A	2100
INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_3	0x000000000501326B	2101
INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_4	0x000000000501326C	2101
INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_5	0x000000000501326D	2101
INT.INT_VC.INT_VC_IRQ_TO_EQC_CREDITS	0x000000000501320E	2072
INT.INT_VC.INT_VC_IVC_ADDITIONAL_PERF	0x000000000501325B	2097
INT.INT_VC.INT_VC_IVC_CACHE_EN	0x0000000005013221	2080
INT.INT_VC.INT_VC_IVC_CACHE_WATCH_ADDR	0x0000000005013225	2081
INT.INT_VC.INT_VC_IVC_CACHE_WATCH_DATA	0x0000000005013226	2081
INT.INT_VC.INT_VC_IVC_DEBUG	0x000000000501322A	2083
INT.INT_VC.INT_VC_IVC_HASH_1	0x0000000005013227	2081
INT.INT_VC.INT_VC_IVC_HASH_2	0x0000000005013228	2082
INT.INT_VC.INT_VC_IVC_HASH_3	0x0000000005013229	2082
INT.INT_VC.INT_VC_IVC_PERF_EVENT_SEL_1	0x0000000005013258	2096
INT.INT_VC.INT_VC_IVC_PERF_EVENT_SEL_2	0x0000000005013259	2096
INT.INT_VC.INT_VC_IVC_PERF_EVENT_SEL_3	0x000000000501325A	2097
INT.INT_VC.INT_VC_IVC_SCRUB_MASK	0x0000000005013223	2080
INT.INT_VC.INT_VC_IVC_SCRUB_TRIG	0x0000000005013222	2080
INT.INT_VC.INT_VC_IVE_ISB_BLOCK_MODE	0x0000000005013203	2065
INT.INT_VC.INT_VC_LBS6_DEBUG	0x0000000005013206	2066
INT.INT_VC.INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD	0x0000000005013210	2073
INT.INT_VC.INT_VC_MAX_OUTSTANDING_IRQ_DMA	0x000000000501323B	2089
INT.INT_VC.INT_VC_MAX_OUTSTANDING_IVC_CMD	0x0000000005013220	2079

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INT.INT_VC.INT_VC_MAX_OUTSTANDING_SBC_CMD	0x0000000005013230	2085
INT.INT_VC.INT_VC_RECOV_ERR_G0	0x0000000005013279	2108
INT.INT_VC.INT_VC_RECOV_ERR_G1	0x000000000501327C	2109
INT.INT_VC.INT_VC_SBC_ADDITIONAL_PERF	0x0000000005013263	2099
INT.INT_VC.INT_VC_SBC_CACHE_EN	0x0000000005013231	2085
INT.INT_VC.INT_VC_SBC_CACHE_WATCH_ADDR	0x0000000005013235	2086
INT.INT_VC.INT_VC_SBC_CACHE_WATCH_DATA	0x0000000005013236	2087
INT.INT_VC.INT_VC_SBC_CONFIG	0x0000000005013234	2086
INT.INT_VC.INT_VC_SBC_DEBUG	0x000000000501323A	2088
INT.INT_VC.INT_VC_SBC_PERF_EVENT_SEL_1	0x0000000005013260	2098
INT.INT_VC.INT_VC_SBC_PERF_EVENT_SEL_2	0x0000000005013261	2098
INT.INT_VC.INT_VC_SBC_PERF_EVENT_SEL_3	0x0000000005013262	2099
INT.INT_VC.INT_VC_SBC_SCRUB_MASK	0x0000000005013233	2086
INT.INT_VC.INT_VC_SBC_SCRUB_TRIG	0x0000000005013232	2085
INT.INT_VC.INT_VC_SBC_SOFTWR_ADDR	0x0000000005013237	2087
INT.INT_VC.INT_VC_SBC_SOFTWR_DATA	0x0000000005013239	2088
INT.INT_VC.INT_VC_SBC_SOFTWR_MASK	0x0000000005013238	2087
INT.INT_VC.INT_VC_VPS_BLOCK_MODE	0x0000000005013205	2066
INT.INT_VC.INT_VC_VSD_TABLE_ADDR	0x0000000005013201	2065
INT.INT_VC.INT_VC_WOF_ERR_G0	0x0000000005013274	2103
INT.INT_VC.INT_VC_WOF_ERR_G0_DETAIL	0x0000000005013275	2105
INT.INT_VC.INT_VC_WOF_ERR_G1	0x0000000005013276	2106
INT.INT_VC.INT_VC_WOF_ERR_G1_DETAIL	0x0000000005013277	2108
NMMU.MM_CFG_NMMU_CTL_MISC	0x0000000005012C53	2006
NMMU.MM_CFG_NMMU_CTL_SLB	0x0000000005012C54	2007
NMMU.MM_CFG_NMMU_CTL_SM	0x0000000005012C52	2004
NMMU.MM_CFG_NMMU_CTL_TLB	0x0000000005012C55	2008
NMMU.MM_CFG_NMMU_XLAT_CTL_REG0	0x0000000005012C4A	2003
NMMU.MM_CFG_NMMU_XLAT_CTL_REG1	0x0000000005012C4B	2003
NMMU.MM_CFG_NMMU_XLAT_CTL_REG2	0x0000000005012C4C	2004
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.MMCQ_PB_MODE_REG	0x0000000005012C15	1996
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.MM_EPSILON_COUNTER_VALUE	0x0000000005012C1D	1998
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_ACTION0_REG	0x0000000005012C06	1995
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_ACTION1_REG	0x0000000005012C07	1995
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_MASK_REG	0x0000000005012C03	1994
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_REG	0x0000000005012C00	1993
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_WOF_REG	0x0000000005012C08	1995
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_MISC_CONTROL_REG	0x0000000005012C28	2000
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PB_DEBUG_REG	0x0000000005012C10	1995
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PB_ECC_REG	0x0000000005012C11	1996
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PB_ERR_RPT_0	0x0000000005012C22	1998
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PMU_CONTROL_REG	0x0000000005012C26	1999
NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PMU_COUNTER_REG	0x0000000005012C27	2000
NMMU.MM_FBC.CQ_WRAP.NX_DEBUG_SNAPSHOT_0	0x0000000005012C24	1998
NMMU.MM_FBC.CQ_WRAP.NX_DEBUG_SNAPSHOT_1	0x0000000005012C25	1998
NMMU.MM_FIR1_ACTION0_REG	0x0000000005012C46	2002
NMMU.MM_FIR1_ACTION1_REG	0x0000000005012C47	2003
NMMU.MM_FIR1_MASK_REG	0x0000000005012C43	2002

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NMMU.MM_FIR1_REG	0x0000000005012C40	2000
NMMU.MM_FIR1_WOF_REG	0x0000000005012C48	2003
NMMU.MM_NMMU_DBG_MODE	0x0000000005012C59	2010
NMMU.MM_NMMU_ERR_INJ	0x0000000005012C58	2010
NMMU.MM_NMMU_ERR_LOG	0x0000000005012C57	2009
NPU.ATS.REG.ATS_CKSW	0x0000000005011304	1810
NPU.ATS.REG.ATS_CTRL	0x0000000005011320	1812
NPU.ATS.REG.ATS_HOLD	0x0000000005011305	1810
NPU.ATS.REG.ATS_MASK	0x0000000005011306	1812
NPU.ATS.REG.ATS_TCR	0x0000000005011326	1815
NPU.ATS.REG.DMA_SYNC	0x0000000005011323	1814
NPU.ATS.REG.IODA_ADDR	0x0000000005011321	1812
NPU.ATS.REG.IODA_DAT0	0x0000000005011322	1813
NPU.ATS.REG.NPU_ATS_DEBUG	0x0000000005011303	1810
NPU.ATS.REG.NPU_AT_ECC	0x0000000005011302	1809
NPU.ATS.REG.NPU_AT_ESMR	0x0000000005011328	1816
NPU.ATS.REG.NPU_AT_ESR	0x0000000005011327	1816
NPU.ATS.REG.NPU_AT_FESMR	0x000000000501132A	1817
NPU.ATS.REG.NPU_AT_FESR	0x0000000005011329	1816
NPU.ATS.REG.NPU_AT_PMU_CNT	0x0000000005011301	1809
NPU.ATS.REG.NPU_AT_PMU_CTRL	0x0000000005011300	1808
NPU.ATS.REG.NPU_Q_DMA_R	0x0000000005011325	1815
NPU.ATS.REG.TCE_KILL	0x0000000005011324	1814
NPU.MISC.FIR_ACTION0_REG_0	0x0000000005011406	1860
NPU.MISC.FIR_ACTION0_REG_1	0x0000000005011446	1863
NPU.MISC.FIR_ACTION1_REG_0	0x0000000005011407	1860
NPU.MISC.FIR_ACTION1_REG_1	0x0000000005011447	1864
NPU.MISC.FIR_MASK_REG_0	0x0000000005011403	1860
NPU.MISC.FIR_MASK_REG_1	0x0000000005011443	1863
NPU.MISC.FIR_REG_0	0x0000000005011400	1858
NPU.MISC.FIR_REG_1	0x0000000005011440	1861
NPU.MISC.FIR_WOF_REG_0	0x0000000005011408	1861
NPU.MISC.FIR_WOF_REG_1	0x0000000005011448	1864
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NPU.XTS.ATSD.XTS_ATSD_HYP6	0x0000000005011366	1825
NPU.XTS.ATSD.XTS_ATSD_HYP7	0x0000000005011367	1826
NPU.XTS.REG.DEBUG0_CONFIG	0x0000000005011346	1821
NPU.XTS.REG.DEBUG1_CONFIG	0x0000000005011347	1821
NPU.XTS.REG.ERR_FIRST	0x0000000005011343	1819
NPU.XTS.REG.ERR_HOLD	0x0000000005011340	1817
NPU.XTS.REG.ERR_MASK	0x0000000005011342	1819
NPU.XTS.REG.TEST_CERR	0x0000000005011341	1818
NPU.XTS.REG.XTS_ATRMISS	0x000000000501134A	1822
NPU.XTS.REG.XTS_ATRMISS2	0x000000000501134C	1824
NPU.XTS.REG.XTS_ATRMISSCLR	0x000000000501134B	1822
NPU.XTS.REG.XTS_CONFIG	0x0000000005011344	1819
NPU.XTS.REG.XTS_CONFIG2	0x0000000005011345	1820
NPU.XTS.REG.XTS_PMU_CNT	0x0000000005011348	1822
PB.COM.EXTFIR_ACTION0_REG	0x0000000005011C34	1907
PB.COM.EXTFIR_ACTION1_REG	0x0000000005011C35	1908
PB.COM.EXTFIR_MASK_REG	0x0000000005011C31	1907
PB.COM.EXTFIR_REG	0x0000000005011C2E	1907
PB.COM.PB_CENT_CNPME	0x0000000005011C13	1888
PB.COM.PB_CENT_CNPMW	0x0000000005011C14	1891
PB.COM.PB_CENT_CR_ERROR	0x0000000005011C2C	1906
PB.COM.PB_CENT_EVENT_COMPA	0x0000000005011C17	1898
PB.COM.PB_CENT_EVENT_COMPB	0x0000000005011C18	1898
PB.COM.PB_CENT_EVENT_COMPX	0x0000000005011C19	1899
PB.COM.PB_CENT_EVENT_SEL	0x0000000005011C16	1897
PB.COM.PB_CENT_EXTDAT_COUNTER	0x0000000005011C25	1903
PB.COM.PB_CENT_FIR_ACTION0_REG	0x0000000005011C06	1877

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PB.COM.PB_CENT_FIR_MASK_REG	0x0000000005011C03	1876
PB.COM.PB_CENT_FIR_REG	0x0000000005011C00	1876
PB.COM.PB_CENT_GP_CMD_RATE_DP0	0x0000000005011C26	1903
PB.COM.PB_CENT_GP_CMD_RATE_DP1	0x0000000005011C27	1903
PB.COM.PB_CENT_HPA_MODE_CURR	0x0000000005011C0E	1883
PB.COM.PB_CENT_HPA_MODE_NEXT	0x0000000005011C0D	1882
PB.COM.PB_CENT_HPX_MODE_CURR	0x0000000005011C10	1885
PB.COM.PB_CENT_HPX_MODE_NEXT	0x0000000005011C0F	1884
PB.COM.PB_CENT_HP_MODE_CURR	0x0000000005011C0C	1880
PB.COM.PB_CENT_HP_MODE_NEXT	0x0000000005011C0B	1879
PB.COM.PB_CENT_LMPM_COUNTER	0x0000000005011C23	1902
PB.COM.PB_CENT_MODE	0x0000000005011C0A	1878
PB.COM.PB_CENT_NMPM_COUNTER	0x0000000005011C22	1901
PB.COM.PB_CENT_PMU0_CNPME_COUNTER	0x0000000005011C1A	1899
PB.COM.PB_CENT_PMU0_CNPMW_COUNTER	0x0000000005011C1E	1900
PB.COM.PB_CENT_PMU1_CNPME_COUNTER	0x0000000005011C1B	1899
PB.COM.PB_CENT_PMU1_CNPMW_COUNTER	0x0000000005011C1F	1901
PB.COM.PB_CENT_PMU2_CNPME_COUNTER	0x0000000005011C1C	1900
PB.COM.PB_CENT_PMU2_CNPMW_COUNTER	0x0000000005011C20	1901
PB.COM.PB_CENT_PMU3_CNPME_COUNTER	0x0000000005011C1D	1900
PB.COM.PB_CENT_PMU3_CNPMW_COUNTER	0x0000000005011C21	1901
PB.COM.PB_CENT_PMU_PRESCALER	0x0000000005011C15	1894
PB.COM.PB_CENT_RCMD_INTDAT_COUNTER	0x0000000005011C24	1902
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PB.COM.PB_CENT_RGP_CMD_RATE_DP1	0x0000000005011C29	1904
PB.COM.PB_CENT_SCONFIG_LOAD	0x0000000005011C11	1886
PB.COM.PB_CENT_SP_CMD_RATE_DP0	0x0000000005011C2A	1905
PB.COM.PB_CENT_SP_CMD_RATE_DP1	0x0000000005011C2B	1906
PB.COM.PB_CENT_TRACE	0x0000000005011C12	1886
PB.COM.PB_EAST_FIR_ACTION0_REG	0x0000000005012006	1911
PB.COM.PB_EAST_FIR_ACTION1_REG	0x0000000005012007	1911
PB.COM.PB_EAST_FIR_MASK_REG	0x0000000005012003	1909
PB.COM.PB_EAST_FIR_REG	0x0000000005012000	1908
PB.COM.PB_EAST_FW_SCRATCH0	0x0000000005012013	1923
PB.COM.PB_EAST_FW_SCRATCH1	0x0000000005012016	1923
PB.COM.PB_EAST_HPA_MODE_CURR	0x000000000501200E	1918
PB.COM.PB_EAST_HPA_MODE_NEXT	0x000000000501200D	1917
PB.COM.PB_EAST_HPX_MODE_CURR	0x0000000005012010	1921
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PB.COM.PB_WEST_FIR_ACTION0_REG	0x0000000005011806	1867
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PB.COM.PB_WEST_SCONFIG_LOAD	0x0000000005011811	1875
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PB.IOE.SCOM.PB_ELINK_DATA_01_CFG_REG	0x0000000005013410	2117
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TP.TCN3.N3.OPCG_CAPT2	0x0000000005030011	2177
TP.TCN3.N3.OPCG_CAPT3	0x0000000005030012	2177
TP.TCN3.N3.OPCG_REG0	0x0000000005030002	2166
TP.TCN3.N3.OPCG_REG1	0x0000000005030003	2167
TP.TCN3.N3.OPCG_REG2	0x0000000005030004	2168
TP.TCN3.N3.RFIR	0x0000000005040001	2180
TP.TCN3.N3.SCAN_REGION_TYPE	0x0000000005030005	2168
TP.TCN3.N3.SPATTN	0x0000000005040004	2181
TP.TCN3.N3.SPA_MASK	0x0000000005040007	2182
TP.TCN3.N3.SYNC_CONFIG	0x0000000005030000	2165
TP.TCN3.N3.TRA0.TR0.TRACE_HI_DATA_REG	0x0000000005010400	1065
TP.TCN3.N3.TRA0.TR0.TRACE_LO_DATA_REG	0x0000000005010401	1065
TP.TCN3.N3.TRA0.TR0.TRACE_TRCTRL_CONFIG	0x0000000005010402	1065
TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x0000000005010403	1066
TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x0000000005010404	1066
TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_2	0x0000000005010405	1066
TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x0000000005010406	1066
TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x0000000005010407	1067
TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x0000000005010408	1067
TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x0000000005010409	1067
TP.TCN3.N3.TRA0.TR1.TRACE_HI_DATA_REG	0x0000000005010440	1068
TP.TCN3.N3.TRA0.TR1.TRACE_LO_DATA_REG	0x0000000005010441	1069
TP.TCN3.N3.TRA0.TR1.TRACE_TRCTRL_CONFIG	0x0000000005010442	1069
TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_0	0x0000000005010443	1069
TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_1	0x0000000005010444	1070
TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_2	0x0000000005010445	1070
TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_3	0x0000000005010446	1070
TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_4	0x0000000005010447	1070
TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_5	0x0000000005010448	1071
TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_9	0x0000000005010449	1071
TP.TCN3.N3.TRA1.TR0.TRACE_HI_DATA_REG	0x0000000005010480	1072
TP.TCN3.N3.TRA1.TR0.TRACE_LO_DATA_REG	0x0000000005010481	1072
TP.TCN3.N3.TRA1.TR0.TRACE_TRCTRL_CONFIG	0x0000000005010482	1073
TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_0	0x0000000005010483	1073
TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_1	0x0000000005010484	1073
TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_2	0x0000000005010485	1074
TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_3	0x0000000005010486	1074
TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_4	0x0000000005010487	1074
TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_5	0x0000000005010488	1074
TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_9	0x0000000005010489	1074
TP.TCN3.N3.TRA1.TR1.TRACE_HI_DATA_REG	0x00000000050104C0	1076
TP.TCN3.N3.TRA1.TR1.TRACE_LO_DATA_REG	0x00000000050104C1	1076
TP.TCN3.N3.TRA1.TR1.TRACE_TRCTRL_CONFIG	0x00000000050104C2	1076
TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_0	0x00000000050104C3	1077
TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_1	0x00000000050104C4	1077
TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_2	0x00000000050104C5	1077
TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_3	0x00000000050104C6	1077

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TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_4	0x00000000050104C7	1078
TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_5	0x00000000050104C8	1078
TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_9	0x00000000050104C9	1078
TP.TCN3.N3.TRA2.TR0.TRACE_HI_DATA_REG	0x0000000005010500	1079
TP.TCN3.N3.TRA2.TR0.TRACE_LO_DATA_REG	0x0000000005010501	1080
TP.TCN3.N3.TRA2.TR0.TRACE_TRCTRL_CONFIG	0x0000000005010502	1080
TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_0	0x0000000005010503	1080
TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_1	0x0000000005010504	1081
TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_2	0x0000000005010505	1081
TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_3	0x0000000005010506	1081
TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_4	0x0000000005010507	1081
TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_5	0x0000000005010508	1081
TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_9	0x0000000005010509	1082
TP.TCN3.N3.TRA2.TR1.TRACE_HI_DATA_REG	0x0000000005010540	1083
TP.TCN3.N3.TRA2.TR1.TRACE_LO_DATA_REG	0x0000000005010541	1083
TP.TCN3.N3.TRA2.TR1.TRACE_TRCTRL_CONFIG	0x0000000005010542	1084
TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_0	0x0000000005010543	1084
TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_1	0x0000000005010544	1084
TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_2	0x0000000005010545	1084
TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_3	0x0000000005010546	1085
TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_4	0x0000000005010547	1085
TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_5	0x0000000005010548	1085
TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_9	0x0000000005010549	1085
TP.TCN3.N3.TRA3.TR0.TRACE_HI_DATA_REG	0x0000000005010580	1087
TP.TCN3.N3.TRA3.TR0.TRACE_LO_DATA_REG	0x0000000005010581	1087
TP.TCN3.N3.TRA3.TR0.TRACE_TRCTRL_CONFIG	0x0000000005010582	1087
TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_0	0x0000000005010583	1088
TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_1	0x0000000005010584	1088
TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_2	0x0000000005010585	1088
TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_3	0x0000000005010586	1088
TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_4	0x0000000005010587	1089
TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_5	0x0000000005010588	1089
TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_9	0x0000000005010589	1089
TP.TCN3.N3.TRA3.TR1.TRACE_HI_DATA_REG	0x00000000050105C0	1090
TP.TCN3.N3.TRA3.TR1.TRACE_LO_DATA_REG	0x00000000050105C1	1091
TP.TCN3.N3.TRA3.TR1.TRACE_TRCTRL_CONFIG	0x00000000050105C2	1091
TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_0	0x00000000050105C3	1091
TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_1	0x00000000050105C4	1092
TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_2	0x00000000050105C5	1092
TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_3	0x00000000050105C6	1092
TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_4	0x00000000050105C7	1092
TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_5	0x00000000050105C8	1092
TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_9	0x00000000050105C9	1093
TP.TCN3.N3.TRA4.TR0.TRACE_HI_DATA_REG	0x0000000005010600	1094
TP.TCN3.N3.TRA4.TR0.TRACE_LO_DATA_REG	0x0000000005010601	1094
TP.TCN3.N3.TRA4.TR0.TRACE_TRCTRL_CONFIG	0x0000000005010602	1095
TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_0	0x0000000005010603	1095
TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_1	0x0000000005010604	1095

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TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_2	0x0000000005010605	1095
TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_3	0x0000000005010606	1096
TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_4	0x0000000005010607	1096
TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_5	0x0000000005010608	1096
TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_9	0x0000000005010609	1096
TP.TCN3.N3.TRA5.TR0.TRACE_HI_DATA_REG	0x0000000005010680	1098
TP.TCN3.N3.TRA5.TR0.TRACE_LO_DATA_REG	0x0000000005010681	1098
TP.TCN3.N3.TRA5.TR0.TRACE_TRCTRL_CONFIG	0x0000000005010682	1098
TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_0	0x0000000005010683	1099
TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_1	0x0000000005010684	1099
TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_2	0x0000000005010685	1099
TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_3	0x0000000005010686	1099
TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_4	0x0000000005010687	1100
TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_5	0x0000000005010688	1100
TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_9	0x0000000005010689	1100
TP.TCN3.N3.TRA5.TR1.TRACE_HI_DATA_REG	0x00000000050106C0	1101
TP.TCN3.N3.TRA5.TR1.TRACE_LO_DATA_REG	0x00000000050106C1	1102
TP.TCN3.N3.TRA5.TR1.TRACE_TRCTRL_CONFIG	0x00000000050106C2	1102
TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_0	0x00000000050106C3	1102
TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_1	0x00000000050106C4	1103
TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_2	0x00000000050106C5	1103
TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_3	0x00000000050106C6	1103
TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_4	0x00000000050106C7	1103
TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_5	0x00000000050106C8	1103
TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_9	0x00000000050106C9	1104
TP.TCN3.N3.XFIR	0x0000000005040000	2179
TP.TCN3.N3.XSTOP1	0x000000000503000C	2172
TP.TCN3.N3.XSTOP2	0x000000000503000D	2173
TP.TCN3.N3.XSTOP3	0x000000000503000E	2174

The POWER9 processor registers are listed in the following tables.

Register Name	**Chiplet Control Register 0**
Mnemonic	TP.TCN3.N3.CPLT_CTRL0
Address	0000000005000000 (SCOM) 0000000005000010 (SCOM1) 0000000005000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select the ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks are used from a chiplet with ABIST.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the synchronous clock for asynchronous latches. (The initial value is 1.)
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode. (The initial value is 1.)
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force an alignment signal to be sent. (The initial value is 1. Drop before dropping flushmode_inh.)
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set the array into write-through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: Switches from refresh pulse to phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC: Unused.
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC: Skitter used functional during BIST. The scan chain is bypassed and scan enable (SE) is degated if 1.
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode. For example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of N1L latches. Prevents lock when switching SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC: Enable test only logic and latches to increase test coverage.
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO selected.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INT mode for BSC.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Allows you to delay the alignment by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into a flush state. For DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select: 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM program mode.
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only. Sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. The LBIST is controlled by the pin, not by the OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	Chiplet Control Register 1
Mnemonic	TP.TCN3.N3.CPLT_CTRL1
Address	0000000005000001 (SCOM) 0000000005000011 (SCOM1) 0000000005000021 (SCOM2)
Description	This register contains the second set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL fence. Protect the VITL region logic from pollution by other regions during LBIST, or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for the PERV region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for region PB.
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for region BR (TP).
7	RW	WO_OR	WO_CLEAR	TC_REGION3_FENCE: Fence for region NP (NPU).
8	RW	WO_OR	WO_CLEAR	TC_REGION4_FENCE: Fence for region MM (NMMU).
9	RW	WO_OR	WO_CLEAR	TC_REGION5_FENCE: Fence for region INT.
10	RW	WO_OR	WO_CLEAR	TC_REGION6_FENCE: Fence for region unused.
11	RW	WO_OR	WO_CLEAR	UNUSED_11B: Unused.
12	RW	WO_OR	WO_CLEAR	UNUSED_12B: Unused.
13	RW	WO_OR	WO_CLEAR	UNUSED_13B: Unused.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.
15	RW	WO_OR	WO_CLEAR	RESERVED: Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE: Fence logic that is indeterminate at any frequency.
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	UNUSED_20B: Unused.
21	RW	WO_OR	WO_CLEAR	UNUSED_21B: Unused.
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	**Chiplet Configuration Register 0**
Mnemonic	TP.TCN3.N3.CPLT_CONF0
Address	0000000005000008 (SCOM) 0000000005000018 (SCOM1) 0000000005000028 (SCOM2)
Description	This register contains the first set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 selected.
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 selected.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 selected.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3 selected.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: Enables ABIST overflow or failure indication.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection and the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from CC or chiplet control.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in CC which are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: System ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	**Chiplet Configuration Register 1**
Mnemonic	TP.TCN3.N3.CPLT_CONF1
Address	0000000005000009 (SCOM) 0000000005000019 (SCOM1) 0000000005000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0D: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1D: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2D: Unused.
3	RW	WO_OR	WO_CLEAR	UNUSED_3D: Unused.
4	RW	WO_OR	WO_CLEAR	IOVALID_4D: Unused.
5	RW	WO_OR	WO_CLEAR	IOVALID_5D: Unused.
6	RW	WO_OR	WO_CLEAR	IOVALID_6D: Unused.
7	RW	WO_OR	WO_CLEAR	IOVALID_7D: Unused.
8	RW	WO_OR	WO_CLEAR	IOVALID_8D: Unused.
9	RW	WO_OR	WO_CLEAR	IOVALID_9D: Unused.
10	RW	WO_OR	WO_CLEAR	IOVALID_10D: Unused.
11	RW	WO_OR	WO_CLEAR	IOVALID_11D: Unused.
12	RW	WO_OR	WO_CLEAR	TC_LP_RESET:
13	RW	WO_OR	WO_CLEAR	FREE_USAGE_13D: Free usage.
14	RW	WO_OR	WO_CLEAR	FREE_USAGE_14D: Free usage.
15	RW	WO_OR	WO_CLEAR	FREE_USAGE_15D: Free usage.
16	RW	WO_OR	WO_CLEAR	FREE_USAGE_16D: Free usage.
17	RW	WO_OR	WO_CLEAR	FREE_USAGE_17D: Free usage.
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	Chiplet Status Register
Mnemonic	TP.TCN3.N3.CPLT_STAT0
Address	0000000005000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask register. A mask only masks the interrupt, not the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM and eDRAM ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic output port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic output port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: Used for LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that the chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	MCS23_TC_0_FIR_HOST_ATTN: Chiplet specific.
13	ROX	MCS23_TC_1_FIR_HOST_ATTN: Chiplet specific.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.
16	ROX	FREE_USAGE_16E: Free usage.
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	Chiplet Mask Register
Mnemonic	TP.TCN3.N3.CPLT_MASK0
Address	0000000005000101 (SCOM)
Description	This register masks an interrupt when a bit changes in the Chiplet Status register. It does not mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: Bitwise masking of the Chiplet Status register.

Register Name	Control Protect Mode Register
Mnemonic	TP.TCN3.N3.CTRL_PROTECT_MODE_REG
Address	00000000050003FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCN3.N3.CTRL_ATOMIC_LOCK_REG
Address	00000000050003FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: Atomic ID.
5:7	RO	Constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCN3.N3.EPS.PSC.PSC.PSCOM_MODE_REG
Address	0000000005010000 (SCOM)
Description	This is the parallel to serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on PCB write data parity error.
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: Unused.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on DL, return write data parity error.
4	RW	WATCHDOG_ENABLE: Enable watchdog.
5:6	RW	SCOM_HANG_LIMIT: 11 = 256 10 = 512 01 = 768 00 = 1023
7	RW	FORCE_ALL_RINGS: Set to a logical 1 if all rings should be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on STATEVEC parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCN3.N3.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000005010001 (SCOM)
Description	This is the parallel to serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on the interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on the parallel to serial machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on the parallel to serial machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.

Bits	SCOM	Field Mnemonic: Description
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	PSCOMLE Error Mask Register
Mnemonic	TP.TCN3.N3.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	0000000005010002 (SCOM)
Description	This is the parallel to serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on the interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on the parallel to serial machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting for ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCN3.N3.EPS.PSC.PSC.ADDR_TRAP_REG
Address	0000000005010003 (SCOM)
Description	This is the parallel to serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write, of the last transaction with an error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: Reserved.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial to parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit. This bit is set to 1 if no parity error (parity of the satellite response, excluding read data) is detected.
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: Set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: Set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: Set if an invalid register address is detected by the satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TCN3.N3.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	0000000005010005 (SCOM)
Description	This register enables the ring lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking on a write to a specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	Write Protect Rings Register
Mnemonic	TP.TCN3.N3.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	0000000005010006 (SCOM)
Description	This register writes ring protect bit maps.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Write a protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TCN3.N3.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	0000000005010007 (SCOM)
Description	This register provides a bit mask for atomic locking.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: A bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TCN3.N3.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	0000000005010008 (SCOM)
Description	This register provides a bit mask for ring fencing.

Bits	SCOM	Field Mnemonic: Description
0	RO	Constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: A bit mask for ring fencing on a ring-by-ring basis.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000005010400 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000005010401 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000005010402 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.

Bits	SCOM	Field Mnemonic: Description
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000005010403 (SCOM)
Description	This register contains a trace data compare mask for bits 0 - 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000005010404 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000005010405 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000005010406 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000005010407 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000005010408 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000005010409 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.

Bits	SCOM	Field Mnemonic: Description
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR . 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND . 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	**Trace Array High Data Register**
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_HI_DATA_REG
Address	0000000005010440 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_LO_DATA_REG
Address	0000000005010441 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_TRCTRL_CONFIG
Address	0000000005010442 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000005010443 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000005010444 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000005010445 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000005010446 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000005010447 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000005010448 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA0.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000005010449 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.

Bits	SCOM	Field Mnemonic: Description
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_HI_DATA_REG
Address	0000000005010480 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_LO_DATA_REG
Address	0000000005010481 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.

Bits	SCOM	Field Mnemonic: Description
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_TRCTRL_CONFIG
Address	0000000005010482 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000005010483 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000005010484 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000005010485 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000005010486 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000005010487 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000005010488 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA1.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000005010489 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.

Bits	SCOM	Field Mnemonic: Description
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_HI_DATA_REG
Address	00000000050104C0 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_LO_DATA_REG
Address	00000000050104C1 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_TRCTRL_CONFIG
Address	00000000050104C2 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.

Bits	SCOM	Field Mnemonic: Description
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_0
Address	00000000050104C3 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_1
Address	00000000050104C4 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_2
Address	00000000050104C5 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_3
Address	00000000050104C6 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_4
Address	00000000050104C7 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_5
Address	00000000050104C8 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA1.TR1.TRACE_TRDATA_CONFIG_9
Address	00000000050104C9 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_HI_DATA_REG
Address	0000000005010500 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_LO_DATA_REG
Address	0000000005010501 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_TRCTRL_CONFIG
Address	0000000005010502 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000005010503 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000005010504 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000005010505 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000005010506 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000005010507 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000005010508 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA2.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000005010509 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.

Bits	SCOM	Field Mnemonic: Description
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_HI_DATA_REG
Address	0000000005010540 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_LO_DATA_REG
Address	0000000005010541 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_TRCTRL_CONFIG
Address	0000000005010542 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000005010543 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000005010544 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000005010545 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.

Bits	SCOM	Field Mnemonic: Description
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000005010546 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000005010547 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000005010548 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA2.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000005010549 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).

Bits	SCOM	Field Mnemonic: Description
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.

Bits	SCOM	Field Mnemonic: Description
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_HI_DATA_REG
Address	0000000005010580 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_LO_DATA_REG
Address	0000000005010581 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_TRCTRL_CONFIG
Address	0000000005010582 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).

Bits	SCOM	Field Mnemonic: Description
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000005010583 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000005010584 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000005010585 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000005010586 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000005010587 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000005010588 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA3.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000005010589 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_HI_DATA_REG
Address	00000000050105C0 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_LO_DATA_REG
Address	00000000050105C1 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_TRCTRL_CONFIG
Address	00000000050105C2 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_0
Address	00000000050105C3 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_1
Address	00000000050105C4 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_2
Address	00000000050105C5 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_3
Address	00000000050105C6 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_4
Address	00000000050105C7 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_5
Address	00000000050105C8 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA3.TR1.TRACE_TRDATA_CONFIG_9
Address	00000000050105C9 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.

Bits	SCOM	Field Mnemonic: Description
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_HI_DATA_REG
Address	0000000005010600 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_LO_DATA_REG
Address	0000000005010601 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_TRCTRL_CONFIG
Address	0000000005010602 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000005010603 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000005010604 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000005010605 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.

Bits	SCOM	Field Mnemonic: Description
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000005010606 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000005010607 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000005010608 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA4.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000005010609 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).

Bits	SCOM	Field Mnemonic: Description
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.

Bits	SCOM	Field Mnemonic: Description
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_HI_DATA_REG
Address	0000000005010680 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_LO_DATA_REG
Address	0000000005010681 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_TRCTRL_CONFIG
Address	0000000005010682 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).

Bits	SCOM	Field Mnemonic: Description
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000005010683 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000005010684 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000005010685 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000005010686 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000005010687 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000005010688 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA5.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000005010689 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_HI_DATA_REG
Address	00000000050106C0 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_LO_DATA_REG
Address	00000000050106C1 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_TRCTRL_CONFIG
Address	00000000050106C2 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace is run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, the internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_0
Address	00000000050106C3 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_1
Address	00000000050106C4 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_2
Address	00000000050106C5 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 - 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_3
Address	00000000050106C6 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_4
Address	00000000050106C7 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_5
Address	00000000050106C8 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCN3.N3.TRA5.TR1.TRACE_TRDATA_CONFIG_9
Address	00000000050106C9 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23). 01 = Debug bus bits(24:47). 10 = Debug bus bits(48:71). 11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.

Bits	SCOM	Field Mnemonic: Description
22:25	RW	TRIG1_AND_MASK: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	Debug Mode Register
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_MODE_REG
Address	00000000050107C0 (SCOM)
Description	This is the debug macro configuration register 0 for the configuration component.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: global_broadcast_mode (0 to 2): 100 = dbg_trace_run and dbg_trace_freeze. 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze. 110 = dbg_triggers_out(0 to 1). 111 = pc_tcdbg_triggers(0 to 1) (from core).
3:5	RW	TRACE_SEL_MODE: Select source for trace_run and bank. 001 = Core trace run and bank. 010 = TP broadcast run and 0. 011 = tc_dbg_inter_brcst latched. 100 = tc_dbg_dbg_sync_brcst_rcv. else = dbg_trace_run and dbg_trace_bank.
6:7	RW	TRIG_SEL_MODE: Select source for tcdbg_trigger(0). 10 = Global broadcast. 11 = pc_tcdbg_trigger (from core). else = dbg_triggers_out(0:1).
8	RW	STOP_ON_XSTOP_SELECTION: Enable trace stop on checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: Enable trace stop on recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: Enable trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select freeze source: 0 = Local debug freeze. 1 = Via broadcast: tp_tcdbg_glb_brcst(1).
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode. Currently unused (obsolete, see trace_sel_mode).
14	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
15	RO	Constant = 0b0
16:31	ROX	dbg_status: Debug status.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000050107C1 (SCOM)
Description	This is debug macro configuration register 1 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 selects constant 0 . 001 selects constant 1. -- CONDITION FEEDBACK -- 002 selects inst1_dbg_cond1. 003 selects inst1_dbg_cond2. 004 selects inst1_dbg_cond3. 005 selects inst1_dbg_cond2timeout. 006 selects inst2_dbg_cond1. 007 selects inst2_dbg_cond2. 008 selects inst2_dbg_cond3. 009 selects inst2_dbg_cond2timeout. 010 selects inst3_dbg_cond1 - Unused, tied down. 011 selects inst3_dbg_cond2 - Unused, tied down. 012 selects inst3_dbg_cond3 - Unused, tied down. 013 selects inst3_dbg_cond2timeout - Unused, tied down. 014 selects inst4_dbg_cond1 - Unused, tied down. 015 selects inst4_dbg_cond2 - Unused, tied down. 016 selects inst4_dbg_cond3 - Unused, tied down. 017 selects inst4_dbg_cond2timeout - Unused, tied down. 018 selects inst1_dbg_trig_sp. 019 selects inst2_dbg_trig_sp. 020 selects inst3_dbg_trig_sp - Unused, tied down. 021 selects inst4_dbg_trig_sp - Unused, tied down. 022 selects tctrc_tcdbg_trigger_a(0). 023 selects tctrc_tcdbg_trigger_b(0). 024 selects tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 selects tctrc_tcdbg_trigger_a(1). 026 selects tctrc_tcdbg_trigger_b(1). 027 selects tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 selects tctrc_tcdbg_trigger_a(2). 029 selects tctrc_tcdbg_trigger_b(2). 030 selects tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 selects tctrc_tcdbg_trigger_a(3). 032 selects tctrc_tcdbg_trigger_b(3). 033 selects tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 selects tctrc_tcdbg_trigger_a(4). 035 selects tctrc_tcdbg_trigger_b(4). 036 selects tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 037 selects tctrc_tcdbg_trigger_a(5). 038 selects tctrc_tcdbg_trigger_b(5). 039 selects tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 040 selects tctrc_tcdbg_trigger_a(6). 041 selects tctrc_tcdbg_trigger_b(6). 042 selects tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6).

Bits	SCOM	Field Mnemonic: Description
		043 selects tctrc_tcdbg_trigger_a(7). 044 selects tctrc_tcdbg_trigger_b(7). 045 selects tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 046 selects tctrc_tcdbg_trigger_a(8). 047 selects tctrc_tcdbg_trigger_b(8). 048 selects tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 049 selects tctrc_tcdbg_trigger_a(9). 050 selects tctrc_tcdbg_trigger_b(9). 051 selects tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 052 selects tctrc_tcdbg_trigger_a(10). 053 selects tctrc_tcdbg_trigger_b(10). 054 selects tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10). 055 selects tctrc_tcdbg_trigger_a(11). 056 selects tctrc_tcdbg_trigger_b(11). 057 selects tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11). 058 selects tctrc_tcdbg_trigger_a(12). 059 selects tctrc_tcdbg_trigger_b(12). 060 selects tctrc_tcdbg_trigger_a(12) and tctrc_tcdbg_trigger_b(12). 061 selects tctrc_tcdbg_trigger_a(13). 062 selects tctrc_tcdbg_trigger_b(13). 063 selects tctrc_tcdbg_trigger_a(13) and ctr_tcdbg_trigger_b(13). 064 selects tctrc_tcdbg_trigger_a(14). 065 selects tctrc_tcdbg_trigger_b(14). 066 selects tctrc_tcdbg_trigger_a(14) and tctrc_tcdbg_trigger_b(14). 067 selects tctrc_tcdbg_trigger_a(15). 068 selects tctrc_tcdbg_trigger_b(15). 069 selects tctrc_tcdbg_trigger_a(15) and tctrc_tcdbg_trigger_b(15). 070 selects tctrc_tcdbg_trigger_a(16). 071 selects tctrc_tcdbg_trigger_b(16). 072 selects tctrc_tcdbg_trigger_a(16) and tctrc_tcdbg_trigger_b(16). 073 selects tctrc_tcdbg_trigger_a(17). 074 selects tctrc_tcdbg_trigger_b(17). 075 selects tctrc_tcdbg_trigger_a(17) and tctrc_tcdbg_trigger_b(17). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 076 selects logic_trigger_in(0). 077 selects logic_trigger_in(1). 078 selects logic_trigger_in(2). 079 selects logic_trigger_in(3). 080 selects logic_trigger_in(4). 081 selects logic_trigger_in(5). 082 selects logic_trigger_in(6). 083 selects logic_trigger_in(7). 084 selects logic_trigger_in(8). 085 selects logic_trigger_in(9). 086 selects logic_trigger_in(10). 087 selects logic_trigger_in(11). 088 selects logic_trigger_in(12). 089 selects logic_trigger_in(13). 090 selects logic_trigger_in(14). 091 selects logic_trigger_in(15). 092 selects pc_tcdbg_trigger(0). 093 selects pc_tcdbg_trigger(1). 094 selects tctrc_tcdbg_glb_brcst(0). 095 selects tctrc_tcdbg_glb_brcst(1). 096 selects xstop_err. 097 selects recov_err. 098 selects spattn. 099 selects fir_dbg_local_xstop_err. 100 selects tc_dbg_inter_brcst(0).

Bits	SCOM	Field Mnemonic: Description
		101 selects tc_dbg_inter_brcst(1). -- CORE TRIGGERS (EP chip only) -- **Note:** Set core_slave_mode to honor ec[0:5]_tc_trace_run. 102 selects core trigger 0: Any rising edge of ec[0:5]_tc_trace_run(0). 103 selects core trigger 1: Any rising edge of ec[0:5]_tc_trace_run(1). 104 selects core trigger 2: Any falling edge of ec[0:5]_tc_trace_run(0). 105 selects core trigger 3: Any falling edge of ec[0:5]_tc_trace_run(1). 106 selects glb_trig_or_trace_in(0). 107 selects glb_trig_or_trace_in(1). 108 selects core_local_brcst_trc(0). 109 selects core_local_brcst_trc(1). 110 selects glb_freeze_brcst_rec(0). 111 selects trig_2_extern_in(0). 112 selects trig_2_extern_in(1). 113 selects dbg_triggers_out(2). 114 selects dbg_triggers_out(3). 115 selects dbg_triggers_out(4). 116 selects dbg_triggers_out(5). 117 selects dbg_triggers_out(6). 118 selects tcdbg_trigger_in(0). 119 selects tcdbg_trigger_in(1).
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Front-end instance 1 counter 1 in-a-row mode.
33	RW	INST1_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST1_UNUSED_1: Unused.
39	RW	INST1_C2_INAROW_MODE: Front-end instance 1 counter 2 in-a-row mode.
40	RW	INST1_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode 2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front-end instance 1edge trigger.
43:45	RWX	INST1_UNUSED_2: Unused.
46	RW	INST1_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST1_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST1_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST1_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: Instance 1 condition 1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: Instance 1 condition 2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front-end instance 1, reset condition 3 for reset_c3_on_c0: 100 = dbg_cross_couple_triggers(4). 101 = dbg_cross_couple_triggers(12). 110 = dbg_cross_couple_triggers(20). 111 = dbg_cross_couple_triggers(28).

Register Name	Debug Instance 1 Condition 2 Register
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_INST1_COND_REG_2
Address	00000000050107C2 (SCOM)
Description	This is the debug macro configuration register 2 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 selects inst1_cond1_trig_a. 00001 selects inst1_cond1_trig_b. 00010 selects inst1_cond2_trig_a. 00011 selects inst1_cond2_trig_b. 00100 selects inst1_condition1. 00101 selects inst1_condition2. 00110 selects inst1_condition3. 00111 selects inst1_cond2_timeout. 01000 selects inst2_cond1_trig_a. 01001 selects inst2_cond1_trig_b. 01010 selects inst2_cond2_trig_a. 01011 selects inst2_cond2_trig_b. 01100 selects inst2_condition1. 01101 selects inst2_condition2. 01110 selects inst2_condition3. 01111 selects inst2_cond2_timeout. 10000 selects inst3_cond1_trig_a. 10001 selects inst3_cond1_trig_b. 10010 selects inst3_cond2_trig_a. 10011 selects inst3_cond2_trig_b. 10100 selects inst3_condition1. 10101 selects inst3_condition2. 10110 selects inst3_condition3. 10111 selects inst3_cond2_timeout. 11000 selects inst4_cond1_trig_a. 11001 selects inst4_cond1_trig_b. 11010 selects inst4_cond2_trig_a. 11011 selects inst4_cond2_trig_b. 11100 selects inst4_condition1. 11101 selects inst4_condition2. 11110 selects inst4_condition3. 11111 selects inst4_cond2_timeout.
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: Instance 1 cross couple select 1b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: Instance 1 cross couple select 2a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: Instance 1 cross couple select 2b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate to compare without actual compare.

Register Name	Debug Instance 1 Condition 3 Register
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_INST1_COND_REG_3
Address	00000000050107C3 (SCOM)
Description	This is the debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	**Debug Instance 2 Condition 1 Register**
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000050107C4 (SCOM)
Description	This is the debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 selects constant 0. 001 selects constant 1. -- CONDITION FEEDBACK -- 002 selects inst2_dbg_cond1. 003 selects inst2_dbg_cond2. 004 selects inst2_dbg_cond3. 005 selects inst2_dbg_cond2timeout. 006 selects inst2_dbg_cond1. 007 selects inst2_dbg_cond2. 008 selects inst2_dbg_cond3. 009 selects inst2_dbg_cond2timeout. 010 selects inst3_dbg_cond1 - Unused, tied down. 011 selects inst3_dbg_cond2 - Unused, tied down. 012 selects inst3_dbg_cond3 - Unused, tied down. 013 selects inst3_dbg_cond2timeout - Unused, tied down. 014 selects inst4_dbg_cond1 - Unused, tied down. 015 selects inst4_dbg_cond2 - Unused, tied down. 016 selects inst4_dbg_cond3 - Unused, tied down. 017 selects inst4_dbg_cond2timeout - Unused, tied down. 018 selects inst2_dbg_trig_sp. 019 selects inst2_dbg_trig_sp. 020 selects inst3_dbg_trig_sp - Unused, tied down. 021 selects inst4_dbg_trig_sp - Unused, tied down. 022 selects tctrc_tcdbg_trigger_a(0). 023 selects tctrc_tcdbg_trigger_b(0). 024 selects tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 selects tctrc_tcdbg_trigger_a(1). 026 selects tctrc_tcdbg_trigger_b(1). 027 selects tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 selects tctrc_tcdbg_trigger_a(2). 029 selects tctrc_tcdbg_trigger_b(2). 030 selects tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 selects tctrc_tcdbg_trigger_a(3). 032 selects tctrc_tcdbg_trigger_b(3). 033 selects tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 selects tctrc_tcdbg_trigger_a(4). 035 selects tctrc_tcdbg_trigger_b(4). 026 selects tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 027 selects tctrc_tcdbg_trigger_a(5). 028 selects tctrc_tcdbg_trigger_b(5). 029 selects tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 030 selects tctrc_tcdbg_trigger_a(6). 031 selects tctrc_tcdbg_trigger_b(6). 032 selects tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 033 selects tctrc_tcdbg_trigger_a(7). 034 selects tctrc_tcdbg_trigger_b(7). 035 selects tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 036 selects tctrc_tcdbg_trigger_a(8). 037 selects tctrc_tcdbg_trigger_b(8). 038 selects tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8).

Bits	SCOM	Field Mnemonic: Description
		039 selects tctrc_tcdbg_trigger_a(9). 040 selects tctrc_tcdbg_trigger_b(9). 041 selects tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 042 selects xstop_err. 043 selects recov_err. 044 selects spattn. 045 selects fir_dbg_local_xstop_err. 046 selects tc_dbg_inter_brcst(0). 047 selects tc_dbg_inter_brcst(1). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 102 selects logic_trigger_in(0). 103 selects logic_trigger_in(1). 104 selects logic_trigger_in(2). 105 selects logic_trigger_in(3). 106 selects logic_trigger_in(4). 107 selects logic_trigger_in(5). 108 selects logic_trigger_in(6). 109 selects logic_trigger_in(7). 110 selects logic_trigger_in(8). 111 selects logic_trigger_in(9). 112 selects logic_trigger_in(10). 113 selects logic_trigger_in(11). 114 selects logic_trigger_in(12). 115 selects logic_trigger_in(13). 116 selects logic_trigger_in(14). 117 selects logic_trigger_in(15). -- CORE TRIGGERS (EP chip only) -- **Note:** Set core_slave_mode to honor ec[0:5]_tc_trace_run. 118 selects core trigger 0: Any rising edge of ec[0:5]_tc_trace_run(0). 119 selects core trigger 1: Any rising edge of ec[0:5]_tc_trace_run(1). 120 selects core trigger 2: Any falling edge of ec[0:5]_tc_trace_run(0). 121 selects core trigger 3: Any falling edge of ec[0:5]_tc_trace_run(1). -- BROADCAST / ERRORS -- 122 selects glb_trc_bdcst_recv (received global broadcast). 123 selects edge detected fir_dbg_xstop_err. 124 selects edge detected fir_dbg_recov_err. 125 selects edge detected fir_dbg_spatn. 126 ... 127 selects constant 0 (unused).
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Front-end instance 1 counter 1 in-a-row mode.
33	RW	INST2_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST2_UNUSED_1: Unused.
39	RW	INST2_C2_INAROW_MODE: Front-end instance 1 counter 2 in-a-row mode.
40	RW	INST2_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode 2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST2_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST2_UNUSED_2: Unused.

Bits	SCOM	Field Mnemonic: Description
46	RW	INST2_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST2_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST2_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST2_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: Instance 2 condition 1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: Instance 2 condition 2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front-end instance 1, reset condition 3 for reset_c3_on_c0: 100 = dbg_cross_couple_triggers(4). 101 = dbg_cross_couple_triggers(12). 110 = dbg_cross_couple_triggers(20). 111 = dbg_cross_couple_triggers(28).

Register Name	**Debug Instance 2 Condition 2 Register**
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000050107C5 (SCOM)
Description	This is the debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 selects inst2_cond1_trig_a. 00001 selects inst2_cond1_trig_b. 00010 selects inst2_cond2_trig_a. 00011 selects inst2_cond2_trig_b. 00100 selects inst2_condition1. 00101 selects inst2_condition2. 00110 selects inst2_condition3. 00111 selects inst2_cond2_timeout. 01000 selects inst2_cond1_trig_a. 01001 selects inst2_cond1_trig_b. 01010 selects inst2_cond2_trig_a. 01011 selects inst2_cond2_trig_b. 01100 selects inst2_condition1. 01101 selects inst2_condition2. 01110 selects inst2_condition3. 01111 selects inst2_cond2_timeout. 10000 selects inst3_cond1_trig_a. 10001 selects inst3_cond1_trig_b. 10010 selects inst3_cond2_trig_a. 10011 selects inst3_cond2_trig_b. 10100 selects inst3_condition1. 10101 selects inst3_condition2. 10110 selects inst3_condition3. 10111 selects inst3_cond2_timeout. 11000 selects inst4_cond1_trig_a. 11001 selects inst4_cond1_trig_b. 11010 selects inst4_cond2_trig_a. 11011 selects inst4_cond2_trig_b. 11100 selects inst4_condition1. 11101 selects inst4_condition2. 11110 selects inst4_condition3. 11111 selects inst4_cond2_timeout.

Bits	SCOM	Field Mnemonic: Description
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: Instance 2 cross couple select 1b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: Instance 2 cross couple select 2a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: Instance 2 cross couple select 2b.
20:43	RW	INST2_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Force test mode to indicate to compare without actual compare.

Register Name	Debug Instance 2 Condition 3 Register
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_INST2_COND_REG_3
Address	00000000050107C6 (SCOM)
Description	This is the debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_TRACE_REG_0
Address	00000000050107CD (SCOM)
Description	This is the debug macro configuration register 0 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: Enable of instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: Enable of instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: Enable slow LFSR mode of front-end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: Enable slow LFSR mode of front-end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: Select instance 1 condition1 for output (external) triggers: 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
10:11	RW	INST1_CONDITION2_TRIG_SEL: Select instance 1 condition 2 for output (external) triggers: 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: Select instance 1 condition 2 timeout counter for output (external) triggers: 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).

Bits	SCOM	Field Mnemonic: Description
14:15	RW	INST2_CONDITION1_TRIG_SEL: Select instance 2 condition1 for output (external) triggers: 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
16:17	RW	INST2_CONDITION2_TRIG_SEL: Select instance 2 condition 2 trigger for output (external) triggers: 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: Select instance 2 condition 2 timeout counter for output (external) triggers: 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
20:31	RO	Constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: Enable trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: Enable trigger on freeze.
34:38	RW	CORE_RAS0_TRIG_SEL:
39:43	RW	CORE_RAS1_TRIG_SEL:
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(0). **Note:** Some are N/A (instance 3 and instance 4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).

Bits	SCOM	Field Mnemonic: Description
54:57	RW	TRIG1_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(1). **Note:** Some are N/A (instance 3 and instance 4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
58:63	RO	Constant = 0b000000

Register Name	Debug Trace 1 Register
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_TRACE_REG_1
Address	00000000050107CE (SCOM)
Description	This is the debug macro configuration register 1 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Instance 1 action selection, condition 1: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
2:3	RW	INST1_CONDITION2_ACTION_DO: Instance 1 action selection, condition 2: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Instance 1 action selection, c2_timeout: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
6:7	RW	INST2_CONDITION1_ACTION_DO: Instance 2 action selection, condition 1: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
8:9	RW	INST2_CONDITION2_ACTION_DO: Instance 2 action selection, condition 2: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.

Bits	SCOM	Field Mnemonic: Description
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Instance 2 action selection, c2_timeout: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
12:23	RO	Constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For wait-N.
25	RW	INST1_CONDITION2_ACTION_WAITN: For wait-N.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For wait-N.
27	RW	INST2_CONDITION1_ACTION_WAITN: For wait-N.
28	RW	INST2_CONDITION2_ACTION_WAITN: For wait-N.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For wait-N.
30:35	RO	Constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (instance 1, condition 1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (instance 1, condition 2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (instance 2, condition 1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (instance 2, condition 2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 2, c2_timeout).
42:47	RO	Constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt. 001 = inst1_condition2_lt. 010 = inst1_condition3_lt. 011 = inst1_cond2_timeout_lt. 1XX = Disable checkstop mode.
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: Enable_fir_trig_xstop. Enable checkstop on debug trigger: 0 = Disable checkstop on debug trigger. 1 = Enable checkstop on debug trigger.
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt. 001 = inst2_condition2_lt. 010 = inst2_condition3_lt. 011 = inst2_cond2_timeout_lt. 1XX = Disable checkstop_mode.
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: Enable_fir_error_xstop. Enable checkstop on FIR error: 0 = Disable checkstop on FIR error. 1 = Enable checkstop on FIR error.
56:63	RO	Constant = 0b00000000

Register Name	**Debug Trace Mode 2 Register**
Mnemonic	TP.TCN3.N3.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000050107CF (SCOM)
Description	This is the debug macro configuration register 2 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the RUNN counter used in trace modes RUNN and wait-N.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on RUNN match.
19	RW	FORCE_TEST_MODE: Force RUNN condition to be true.
20	RW	ACCUM_HIST_MODE: Accumulate history mode, do not clear history mode when trace run is active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.CONFIG0
Address	0000000005011000 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: When set to 1, use Read.RWC/Upgrade.DN for DCLAIM/DCBZ to GPU memory.
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: When set to 1, use Read.RWC/Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: When set to 1, use DMA/Read-Push for Write.NC to processor memory.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable VG less than system. 1 = Force all VG to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc. 1 = Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending DMA. 1 = Change to _inj.

Bits	SCOM	Field Mnemonic: Description
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = Change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp: 0 = 100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7 = 1.5% chance to increase priority.
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: Reserved for future option.
18	RW	CONFIG_MA_RSNOOP_OPT_C: Reserved for future option.
19	RW	CONFIG_MA_SCRESP_OPT_A: Reserved for future option.
20	RW	CONFIG_MA_SCRESP_OPT_B: Reserved for future option.
21	RW	CONFIG_MA_SCRESP_OPT_C: Reserved for future option.
22	RW	CONFIG_RESERVED4: Reserved.
23	RW	CONFIG_MACH_CORRENAB: Disable/enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: Disable/enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: Disable/enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: Disable/enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: Disable/enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: Disable/enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: Disable/enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: Disable/enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: Disable/enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack + rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack + rty_lpc + start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 1 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: Disable/enable NPU processor bus RCMD, PRESP, and CRESP interfaces.

Bits	SCOM	Field Mnemonic: Description
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.
40	RW	CONFIG_ENABLE_SNARF_CPM: Disable/enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: When set to 1, preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: When set to 1, preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: When set to 1, preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: When set to 1, preallocate two state machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: When set to 1, preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to 0: config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode report local masters as near. 1 = In basic mode report local masters as local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOs greater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU to PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.CONFIG1
Address	0000000005011001 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = 1 / ($2^{(n+1)}$) cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = 1 / ($2^{(n+1)}$) cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non-REQIN events going down the arbiter pipe. After n + 1 REQIN events go through the arbiter while a non-CRR event is waiting, REQIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll: 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data: 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	Power Bus Epsilon Configuration Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.EPSILON_CONFIG
Address	0000000005011002 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Decrement Epsilon count at 1:16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/VG scope CP write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope reads.

Register Name	Timer Configuration Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.XTIMER_CONFIG
Address	0000000005011003 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate – 1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate – 1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for the pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for the pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward progress timer (2^n cycles).
20:25	RW	CONFIG_CTL_TICK: Rate for the CTL timer tick (default 63 = off). **Note:** This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for the SM inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for the SM inhibit timer tick1 (default 63 = off). **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for the NV response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.GPU_BAR
Address	0000000005011004 (SCOM)
Description	Memory BARs. BAR register defining GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: Disable/enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: The base address (1 GB address) of the BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512 byte boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024 byte boundary (hashbits(0:7) = addr(46:53)).

Bits	SCOM	Field Mnemonic: Description
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of the base address match for the BAR for brick 0: 0 = 1 GB 1 = 2 GB 2 = 4 GB ... 9 = 512 GB 10 = 1 TB 11 = 2 TB 12 = 4 TB > 12 = Reserved.
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: Disable/enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. **Note:** It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: The base address (1GB address) of the BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = Hash on 512 byte boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024 byte boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of the base address match for the BAR for brick 1: 0 = 1 GB 1 = 2 GB 2 = 4 GB ... 9 = 512 GB 10 = 1 TB 11 = 2 TB 12 = 4 TB > 12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.PHY_BAR
Address	0000000005011006 (SCOM)
Description	BAR register defining the PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2MB range mapped to PHY 0 registers. Stack 1 PHY_BAR defines a 2MB range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16MB range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: Disable/enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2MB aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2MB aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2MB aligned address of this PHY_BAR's 2MB range. **Note:** In stack two, the low three address bits are reserved (16 MB range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.GENID_BAR
Address	0000000005011007 (SCOM)
Description	ID registers MMIO BAR. BAR register defining Generation ID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: Disable/enable this BAR.
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of the 128KB aligned address of this GENID_BAR.

Bits	SCOM	Field Mnemonic: Description
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of the 128KB aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128KB aligned address of this BAR's 128KB range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Low Water Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.LOW_WATER
Address	0000000005011008 (SCOM)
Description	Water marks. State machine allocation for low water marks. Each low water mark should be greater than or equal to 1 and the sum of the low water marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. This can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus RD/DCLAIM/atomic requests (among others). Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be ≥ 8 and ≤ 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. This can only be changed from 0 to 1 and must stay at 1 once it is set.
52:63	RO	Constant = 0b000000000000

Register Name	High Water Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.HIGH_WATER
Address	0000000005011009 (SCOM)
Description	Water marks. State machine allocation for high water marks. Each high water mark should be greater than or equal to τηε corresponding config_low_water and config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.

Bits	SCOM	Field Mnemonic: Description
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus RD/DCLAIM/atomic requests (among others).
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	Relaxed Configuration 0 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CONFIG_RELAXED0
Address	000000000501100A (SCOM)
Description	Ordering configuration 0 register used to configure relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: Disable/enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: Disable/enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: Relaxed source 0 tag mask value: 0 = Bit is masked off, and the corresponding match bit must be 0. 1 = Bit must equal the corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: Disable/enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: Disable/enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CONFIG_RELAXED1
Address	000000000501100B (SCOM)
Description	Ordering configuration 1 register used to configure relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.

Bits	SCOM	Field Mnemonic: Description
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: Disable/enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: Disable/enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 2 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	**Relaxed Configuration 2 Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.CONFIG_RELAXED2
Address	0000000005011000C (SCOM)
Description	Ordering configuration 2 register used to configure relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F=0).

Bits	SCOM	Field Mnemonic: Description
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: Disable/enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: Disable/enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 0 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.NDT0_BAR
Address	000000000501100D (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: Disable/enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128KB aligned address of BAR for brick 0's 128KB range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**NTL1/NDL1 MMIO BAR Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.NDT1_BAR
Address	000000000501100E (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: Disable/enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128KB aligned address of BAR for brick 1's 128KB range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.PERF_CONFIG
Address	000000000501100F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 selected.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 selected.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 selected.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 selected.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.INHIBIT_CONFIG
Address	0000000005011010 (SCOM)
Description	This register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0...11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre-frequency 0: 0 = Inhibit timer tick0. 1 = Inverted inhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: Disable blocky mode / enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 1: 0...12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$

Bits	SCOM	Field Mnemonic: Description
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 1: 0 = Inhibit timer tick1. 1 = Inverted inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: Disable blocky mode / enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_MESSAGE0
Address	0000000005011011 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_MESSAGE1
Address	0000000005011012 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_MESSAGE2
Address	0000000005011013 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_MESSAGE3
Address	0000000005011014 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_MESSAGE4
Address	0000000005011015 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.SM_STATUS
Address	0000000005011016 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: This field is set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: This field is set to 1 when brick 0 probe allocation is at its idle level.
2	ROX	SM_STATUS_CREQ1: This field is set to 1 when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: This field is set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: This field is set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: This field is set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: This field is set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: This field is set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: This field is set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: This field is set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: This field is set to 1 when the outbound Rn/VG scope processor bus request queue is empty.

Bits	SCOM	Field Mnemonic: Description
27	ROX	SM_STATUS_N0REQ: This field is set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: This field is set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: This field is set to 1 when the outbound brick 1 CREQ request queue is empty.
30	ROX	SM_STATUS_N1DGD: This field is set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: This field is set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: This field is set to 1 when the outbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: This field is set to 1 when the outbound processor bus data response/merge operation queue is empty.
34	ROX	SM_STATUS_N0RSP: This field is set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: This field is set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: This field is set to 1 when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: This field is set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: This field is set to 1 when the free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b00000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_FIRST0
Address	0000000005011017 (SCOM)
Description	First c_err_rpt register. read-write-1 clears the register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3. NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3. NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3. NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3. NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3. NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3. NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3. NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3. NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3. NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3. NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3. NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3. NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3. NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3. NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3. NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3. UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3. NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3. NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3. NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3. Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3. Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3. UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30. NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF. An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).

Bits	SCOM	Field Mnemonic: Description
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF4 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NCF6. NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NCF7. NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0. SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1. SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2. SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3. PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3. PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4. Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR6 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3. Address/length/alignment error on MMIO/GENID access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved)..
56:63	RO	Constant = 0b00000000

Register Name	CERR First 1 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_FIRST1
Address	0000000005011018 (SCOM)
Description	First 1 c_err_rpt register Read-write-1 clears the register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0. RCMD pre-snoop table look-up missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX0. RCMD final-snoop table look-up missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX0. Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX0. RCMD pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX0. RCMD final-snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3. Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3. rpt_hang.data waiting for data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: AUE0. UE ECC error detected from state machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: AUE1. UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: AUE2. UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: PBP0. Parity error detected on RCMD TTAG field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: PBP1. Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: PBP2. Parity error detected on CRESP TTAG.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: PBP3. Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3. M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3. PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3. PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3. PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3. M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3. PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3. SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).

Bits	SCOM	Field Mnemonic: Description
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3. PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3. PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: PBC4. RCMD TTAG received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: PBC5. RCMD TTAG received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: PBC6. CRESP TTAG received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: PBC7. CRESP TTAG received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11(Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR First 2 Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_FIRST2
Address	0000000005011019 (SCOM)
Description	First 2 c_err_rpt register read-write-1 clears the register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.

Bits	SCOM	Field Mnemonic: Description
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: Master CRESP received. but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.

Bits	SCOM	Field Mnemonic: Description
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_MASK0
Address	0000000005011010A (SCOM)
Description	c_err_rpt mask 0 register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30. NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31. NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0. An NVLink probe did not match its GPU bar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
a41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_MASK1
Address	000000000501101B (SCOM)
Description	c_err_rpt mask 1 register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.

Bits	SCOM	Field Mnemonic: Description
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: AUE0 UE ECC error detected from state machine array.
21	RW	IDIAL_SM_MASK_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: Reserved.
24	RW	IDIAL_SM_MASK_PBP_0: PBP0 Parity error detected on RCMD TTAG field.
25	RW	IDIAL_SM_MASK_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: PBP2 Parity error detected on CRESP TTAG.
27	RW	IDIAL_SM_MASK_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: PBC4 RCMD TTAG received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: PBC5 RCMD TTAG received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: PBC6 CRESP TTAG received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: PBC7 CRESP TTAG received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC2 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC2 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC2 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC2 (Reserved).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	CERR Mask 2 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_MASK2
Address	000000000501101C (SCOM)
Description	c_err_rpt mask 2 register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.

Bits	SCOM	Field Mnemonic: Description
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown state.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53(Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved)..
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).

Bits	SCOM	Field Mnemonic: Description
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	**CERR Hold 0 Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_HOLD0
Address	000000000501101D (SCOM)
Description	Hold 0 c_err_rpt register Read-write clears the register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.

Bits	SCOM	Field Mnemonic: Description
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF 22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF 23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF 24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF 25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF 26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF 27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF 28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF 29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from state machine array.

Bits	SCOM	Field Mnemonic: Description
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (reserved0.
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Hold 1 Register**
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_HOLD1
Address	000000000501101E (SCOM)
Description	Hold 1 c_err_rpt register Read-write clears the register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS response.

Bits	SCOM	Field Mnemonic: Description
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: AUE0 UE ECC error detected from state machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: PBP0 Parity error detected on RCMD TTAG field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: PBP2 Parity error detected on CRESP TTAG.

Bits	SCOM	Field Mnemonic: Description
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: PBC4 RCMD TTAG received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: PBC5 RCMD TTAG received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: CRESP TTAG received with illegal group ID.

Bits	SCOM	Field Mnemonic: Description
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 RCMD
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 RCMD
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 RCMD
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 RCMD
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK0.CS.SM0.MISC.CERR_HOLD2
Address	000000000501101F (SCOM)
Description	Hold 2 c_err_rpt register Read-write clears the register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.

Bits	SCOM	Field Mnemonic: Description
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.CONFIG0
Address	0000000005011020 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0 = Use Read.RWC for DCLAIM/DCBZ to GPU memory. 1 = Use Upgrade.DN for DCLAIM/DCBZ to GPU memory.
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0 = Use Read.RWC for DCBF/DCBFC to GPU memory. 1 = Use Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0 = Use DMA for Write.NC to processor memory. 1 = Use Read-Push for Write.NC to processor memory.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable Vg less than system. 1 = Force all Vg to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.

Bits	SCOM	Field Mnemonic: Description
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc. 1 = Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending DMA. 1 = Change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = Change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp: 0 =100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7 = 1.5% chance to increase priority.
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD, future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD, future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD, future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD, future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD, future option bit.
22	RW	CONFIG_RESERVED4: Reserved.
23	RW	CONFIG_MACH_CORRENAB: 0 = Disable state machine array ECC correction. 1 = Enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0 = Disable state machine array ECC error inject bit 1. 1 = Enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0 = Disable state machine array ECC error inject bit 2. 1 = Enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0 = Disable ReqRspOut array ECC correction. 1 = Enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.

Bits	SCOM	Field Mnemonic: Description
29	RW	CONFIG_RSI_CORRENAB: 0 = Disable PB-Rsp-In array ECC correction. 1 = Enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 1 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0 = Disable NPU processor bus RCMD, PRESP, and CRESP interfaces. 1 = Enable NPU processor bus RCMD, PRESP, and CRESP interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.
40	RW	CONFIG_ENABLE_SNARF_CPM: 0 = Disable Probe.I.MO snarfing a cp_m. 1 = Enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = Preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = Preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = Preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = Preallocate two state machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = Preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to 0: config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.

Bits	SCOM	Field Mnemonic: Description
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode report local masters as near. 1 = In basic mode report local masters as local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOs greater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU to PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.CONFIG1
Address	0000000005011021 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non-REGIN events going down the arbiter pipe. After n+1 REGIN events go through the arbiter while a non-CRR event is waiting, REGIIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.

Bits	SCOM	Field Mnemonic: Description
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll: 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data: 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	**Power Bus Epsilon Configuration Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.EPSILON_CONFIG
Address	0000000005011022 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/Vg scope CP write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope reads.

Register Name	**Timer Configuration Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.XTIMER_CONFIG
Address	0000000005011023 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e -10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward progress timer (2^n cycles).

Bits	SCOM	Field Mnemonic: Description
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). **Note**: This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for SM inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for SM inhibit timer tick1 (default 63 = off). **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The Short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.GPU_BAR
Address	0000000005011024 (SCOM)
Description	Memory BARs. BAR register defining GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: Base address (1G address) of BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).

Bits	SCOM	Field Mnemonic: Description
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of the base address match for the BAR for brick 0: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. **Note:** It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: Base address (1G address) of BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of base address match for the BAR for brick 1: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 =0 . 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.PHY_BAR
Address	0000000005011026 (SCOM)
Description	BAR register defining PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2M range mapped to PHY 0 registers. Stack 1 PHY_BAR defines a 2M range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16M range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0 = Disable PHY_BAR. 1 = Enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2M aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2M aligned address of this PHY_BAR's 2M range. **Note:** In stack two, the low three address bits are reserved (16M range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.GENID_BAR
Address	0000000005011027 (SCOM)
Description	ID registers MMIO BAR. BAR register defining Generation ID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0 = Disable this BAR. 1 = Enable this BAR.

Bits	SCOM	Field Mnemonic: Description
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of the 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of the 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128K aligned address of this BAR's 128K range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Low Water Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.LOW_WATER
Address	0000000005011028 (SCOM)
Description	Water marks. State machine allocation for low water marks. Each low water mark should be greater than or equal to 1 and the sum of the low water marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be >= 8 and <= 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. Can only be changed from 0 to 1 and must stay at 1 once it is set.
52:63	RO	Constant = 0b000000000000

Register Name	High Water Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.HIGH_WATER
Address	0000000005011029 (SCOM)
Description	Water marks. State machine allocation for high water marks. Each high water mark should be greater than or equal to the corresponding config_low_water and config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Relaxed Configuration 0 Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.CONFIG_RELAXED0
Address	000000000501102A (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0 = Disable relaxed source 0 for write operations. 1 = Enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0 = Disable relaxed source 0 for read operations. 1 = Enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: Relaxed source 0 tag mask value: 0 = Bit is masked off, corresponding match bit must be 0. 1 = Bit must equal corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0 = Disable relaxed source 1 for write operations. 1 = Enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0 = Disable relaxed source 1 for read operations. 1 = Enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CONFIG_RELAXED1
Address	000000000501102B (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0 = Disable relaxed source 2 for write operations. 1 = Enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0 = Disable relaxed source 2 for read operations. 1 = Enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 0 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CONFIG_RELAXED2
Address	000000000501102C (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.

Bits	SCOM	Field Mnemonic: Description
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F=0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0 = Disable relaxed source 3 for write operations. 1 = Enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0 = Disable relaxed source 3 for read operations. 1 = Enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 0 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.NDT0_BAR
Address	000000000501102D (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	NTL1/NDL1 MMIO BAR Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.NDT1_BAR
Address	000000000501102E (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128K aligned address of BAR for brick 1's 128K range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.PERF_CONFIG
Address	000000000501102F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.INHIBIT_CONFIG
Address	0000000005011030 (SCOM)
Description	This register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0 -11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre-frequency 0: 0 = Inhibit timer tick0. 1 = Inverted Inhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = Inhibit timer tick1. 1 = Inverted Inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	**CERR Message 0 Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_MESSAGE0
Address	0000000005011031 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_MESSAGE1
Address	0000000005011032 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_MESSAGE2
Address	0000000005011033 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_MESSAGE3
Address	0000000005011034 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_MESSAGE4
Address	0000000005011035 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.SM_STATUS
Address	0000000005011036 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: Set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: Set to 1 when brick 0 probe allocation is at its idle level.

Bits	SCOM	Field Mnemonic: Description
2	ROX	SM_STATUS_CREQ1: Set to 1 when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: Set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: Set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: Set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: Set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: Set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: Set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: Set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: Set to 1 when the outbound Rn/Vg scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: Set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: Set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: Set to 1 when the outbound brick 1 CREQ request queue is empty.
30	ROX	SM_STATUS_N1DGD: Set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: Set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: Set to 1 when the outbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: Set to 1 when the outbound processor bus data response/merge operation queue is empty.
34	ROX	SM_STATUS_N0RSP: Set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: Set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: Set to 1 when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: Set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: Set to 1 when the free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_FIRST0
Address	0000000005011037 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF 22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF 23 (Reserved).

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF 24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF 25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF 26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF 27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF 28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF 29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF 30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF 31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved)..
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 1 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_FIRST1
Address	0000000005011038 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: AUE0 UE ECC error detected from state machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: PBP0 Parity error detected on RCMD TTAG field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: PBP2 Parity error detected on CRESP TTAG.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: PBC4 RCMD TTAG received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: PBC5 RCMD TTAG received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: PBC6 CRESP TTAG received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: PBC7 CRESP TTAG received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11(Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_FIRST2
Address	0000000005011039 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.

Bits	SCOM	Field Mnemonic: Description
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP .
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP .
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55(Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_MASK0
Address	0000000005011030A (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).

Bits	SCOM	Field Mnemonic: Description
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NVF32 An NVLink probe did not match its GPU bar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: Reserved.
54	RW	IDIAL_SM_MASK_REG_2: Reserved.
55	RW	IDIAL_SM_MASK_REG_3: Reserved.
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_MASK1
Address	0000000005011038 (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS response.

Bits	SCOM	Field Mnemonic: Description
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: AUE0 UE ECC error detected from state machine array.
21	RW	IDIAL_SM_MASK_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: PBP0 Parity error detected on RCMD TTAG field.
25	RW	IDIAL_SM_MASK_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: PBP2 Parity error detected on CRESP TTAG.
27	RW	IDIAL_SM_MASK_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved)..
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).

Bits	SCOM	Field Mnemonic: Description
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: PBC4 RCMD TTAG received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: PBC5 RCMD TTAG received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: PBC6 CRESP TTAG received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: PBC7 CRESP TTAG received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 2 Register**
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_MASK2
Address	0000000005011030 (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).

Bits	SCOM	Field Mnemonic: Description
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown state.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP .
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP .
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.

Bits	SCOM	Field Mnemonic: Description
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved)..
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_HOLD0
Address	000000000501103D (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from the state machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_HOLD1
Address	000000000501103E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: AUE0 UE ECC error detected from state machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: PBP0 Parity error detected on RCMD TTAG field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: PBP2 Parity error detected on CRESP TTAG.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: PBC4 RCMD TTAG received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: PBC5 RCMD TTAG received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: PBC6 CRESP TTAG received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: PBC7 RESP TTAG received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK0.CS.SM1.MISC.CERR_HOLD2
Address	000000000501103F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate,' but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT translate response even,t but not in wait translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.

Bits	SCOM	Field Mnemonic: Description
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.CONFIG0
Address	0000000005011040 (SCOM)
Description	Miscellaneous configuration 0 register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0 = Use Read.RWC for DCLAIM/DCBZ to GPU memory. 1 = Use Upgrade.DN for DCLAIM/DCBZ to GPU memory.

Bits	SCOM	Field Mnemonic: Description
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0 = Use Read.RWC for DCBF/DCBFC to GPU memory. 1 = Use Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0 = Use DMA for Write.NC to processor memory. 1 = Use Read-Push for Write.NC to processor memory.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable Vg less than system. 1 = Force all Vg to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc. 1 = Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending dma. 1 = Change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = Change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp: 0 = 100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7 = 1.5% chance to increase priority.
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD, future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD, future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD, future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD, future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD, future option bit.
22	RW	CONFIG_RESERVED4: Reserved.

Bits	SCOM	Field Mnemonic: Description
23	RW	CONFIG_MACH_CORRENAB: 0 = Disable state machine array ECC correction. 1 = Enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0 = Disable state machine array ECC error inject bit 1. 1 = Enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0 = Disable state machine array ECC error inject bit 2. 1 = Enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0 = Disable ReqRspOut array ECC correction. 1 = Enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0 = Disable PB-Rsp-In array ECC correction. 1 = Enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 1 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0 = Disable NPU processor bus RCMD, PRESP, and CRESP interfaces. 1 = Enable NPU processor bus RCMD, PRESP, and CRESP interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.

Bits	SCOM	Field Mnemonic: Description
40	RW	CONFIG_ENABLE_SNARF_CPM: 0 = Disable Probe.I.MO snarfing a cp_m. 1 = Enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = Preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = Preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = Preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = Preallocate two state machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = Preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode report local masters as near. 1 = In basic mode report local masters as local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOs greater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU to PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.CONFIG1
Address	0000000005011041 (SCOM)
Description	Miscellaneous configuration 1 register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non-REGIN events going down the arbiter pipe. After n+1 REGIN events go through the arbiter while a non-CRR event is waiting, REGIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.

Bits	SCOM	Field Mnemonic: Description
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll: 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data: 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	**Power Bus Epsilon Configuration Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.EPSILON_CONFIG
Address	0000000005011042 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/Vg scope CP write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope reads.

Register Name	**Timer Configuration Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.XTIMER_CONFIG
Address	0000000005011043 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward progress timer (2^n cycles).

Bits	SCOM	Field Mnemonic: Description
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). **Note:** This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for SM inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for SM inhibit timer tick1 (default 63 = off). **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV-Response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63. f(0b10) = 511. f(0b11) = 4095.
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV-Response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 51 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.GPU_BAR
Address	0000000005011044 (SCOM)
Description	Memory BARs. BAR register defining GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: Base address (1G address) of BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).

Bits	SCOM	Field Mnemonic: Description
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of the base address match for the BAR for brick 0: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. **Note:** It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: Base address (1G address) of BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of the base address match for the BAR for brick 1: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3=1 . 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.PHY_BAR
Address	0000000005011046 (SCOM)
Description	BAR register defining PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2M range mapped to PHY 0 registers. Stack 1 PHY_BAR defines a 2M range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16M range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0 = Disable PHY_BAR. 1 = Enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2M aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2M aligned address of this PHY_BAR's 2M range. **Note:** In stack two, the low three address bits are reserved (16M range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.GENID_BAR
Address	0000000005011047 (SCOM)
Description	ID registers MMIO BAR. BAR register defining Generation ID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0 = Disable this BAR. 1 = Enable this BAR.

Bits	SCOM	Field Mnemonic: Description
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of the 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of the 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128K aligned address of this BAR's 128K range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**Low Water Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.LOW_WATER
Address	0000000005011048 (SCOM)
Description	Water marks. State machine allocation for low water marks. Each low water mark should be greater than or equal to1 and the sum of the low water marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be >= 8 and <= 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. Can only be changed from 0 to1 and must stay at 1 once it is set.
52:63	RO	Constant = 0b000000000000

Register Name	**High Water Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.HIGH_WATER
Address	0000000005011049 (SCOM)
Description	Water marks. State machine allocation for high water marks. Each high water mark should be greater than or equal to the corresponding config_low_water and config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Relaxed Configuration 0 Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.CONFIG_RELAXED0
Address	000000000501104A (SCOM)
Description	Ordering configuration 0 register used to configure relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0 = Disable relaxed source 0 for write operations. 1 = Enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0 = Disable relaxed source 0 for read operations. 1 = Enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: relaxed source 0 tag mask value. 0 = Bit is masked off, corresponding match bit must be 0. 1 = Bit must equal corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0 = Disable relaxed source 1 for write operations. 1 = Enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0 = Disable relaxed source 1 for read operations. 1 = Enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CONFIG_RELAXED1
Address	000000000501104B (SCOM)
Description	Ordering configuration 1 register used to configure relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0 = Disable relaxed source 2 for write operations. 1 = Enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0 = Disable relaxed source 2 for read operations. 1 = Enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 2 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CONFIG_RELAXED2
Address	000000000501104C (SCOM)
Description	Ordering configuration 2 register used to configure relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.

Bits	SCOM	Field Mnemonic: Description
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F=0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0 = Disable relaxed source 3 for write operations. 1 = Enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0 = Disable relaxed source 3 for read operations. 1 = Enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 0 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.NDT0_BAR
Address	0000000005011040 (SCOM)
Description	BAR register defining NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	NTL1/NDL1 MMIO BAR Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.NDT1_BAR
Address	000000000501104E (SCOM)
Description	BAR register defining NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128K aligned address of BAR for brick 1's 128K range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.PERF_CONFIG
Address	000000000501104F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.INHIBIT_CONFIG
Address	0000000005011050 (SCOM)
Description	This register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre frequency 0: 0 = Inhibit timer tick0. 1 = Inverted inhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = Inhibit timer tick1. 1 = Inverted inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_MESSAGE0
Address	0000000005011051 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_MESSAGE1
Address	0000000005011052 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_MESSAGE2
Address	0000000005011053 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_MESSAGE3
Address	0000000005011054 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_MESSAGE4
Address	0000000005011055 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.SM_STATUS
Address	0000000005011056 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: Set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: Set to 1 when brick 0 probe allocation is at its idle level.

Bits	SCOM	Field Mnemonic: Description
2	ROX	SM_STATUS_CREQ1: Set to 1 when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: Set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: Set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: Set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: Set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: Set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: Set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: Set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: Set to 1 when the outbound Rn/Vg scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: Set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: Set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: Set to 1 when the outbound brick 1 CREQ request queue is empty.
30	ROX	SM_STATUS_N1DGD: Set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: Set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: Set to 1 when the outbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: Set to 1 when the outbound processor bus data response/merge operation queue is empty.
34	ROX	SM_STATUS_N0RSP: Set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: Set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: Set to 1 when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: Set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: Set to 1 when the free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b0000000000000000000000

Register Name	**CERR First 0 Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_FIRST0
Address	0000000005011057 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR First 1 Register**
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_FIRST1
Address	0000000005011058 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or A=TAG) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_FIRST2
Address	0000000005011059 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket hit event ,but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.

Bits	SCOM	Field Mnemonic: Description
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown sate.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	CERR Mask 0 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_MASK0
Address	000000000501105A (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).

Bits	SCOM	Field Mnemonic: Description
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Mask 1 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_MASK1
Address	0000000005011058 (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS response.

Bits	SCOM	Field Mnemonic: Description
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: UE ECC error detected from state machine array.
21	RW	IDIAL_SM_MASK_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: Parity error detected on RCMD TTAG field.
25	RW	IDIAL_SM_MASK_PBP_1: Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: Parity error detected on CRESP TTAG.
27	RW	IDIAL_SM_MASK_PBP_3: Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).

Bits	SCOM	Field Mnemonic: Description
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: RCMD TTAG received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: RCMD TTAG received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: CRESP TTAG received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: CRESP TTAG received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Mask 2 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_MASK2
Address	000000000501105C (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD event received but state machine is not idle.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).

Bits	SCOM	Field Mnemonic: Description
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT translate response event ,but not in wait translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown state.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.

Bits	SCOM	Field Mnemonic: Description
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_HOLD0
Address	000000000501105D (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_HOLD1
Address	000000000501105E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: Parity error detected on r RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK0.CS.SM2.MISC.CERR_HOLD2
Address	000000000501105F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD event received but state machine is not idle.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.

Bits	SCOM	Field Mnemonic: Description
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK0.CS.SM3.MISC.CONFIG0
Address	0000000005011060 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0 = Use Read.RWC for DCLAIM/DCBZ to GPU memory. 1 = Use Upgrade.DN for DCLAIM/DCBZ to GPU memory.

Bits	SCOM	Field Mnemonic: Description
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0 = Use Read.RWC for DCBF/DCBFC to GPU memory. 1 = Use Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0 = Use DMA for Write.NC to processor memory. 1 = Use Read-Push for Write.NC to processor memory.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable Vg less than system. 1 = Force all Vg to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc . 1 = Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending dma. 1 = Change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = Change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp: 0 = 100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7: 1.5% chance to increase priority.
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD, future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD, future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD, future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD, future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD, future option bit.
22	RW	CONFIG_RESERVED4: Reserved.

Bits	SCOM	Field Mnemonic: Description
23	RW	CONFIG_MACH_CORRENAB: 0 = Disable state machine array ECC correction 1 = Enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0 = Disable state machine array ECC error inject bit 1. 1 = Enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0 = Disable state machine array ECC error inject bit 2. 1 = Enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0 = Disable ReqRspOut array ECC correction. 1 = Enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0 = Disable PB-Rsp-In array ECC correction. 1 = Enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 1 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0 = Disable NPU processor bus RCMD, PRESP, and CRESP interfaces. 1 = Enable NPU processor bus RCMD, PRESP, and CRESP interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.

Bits	SCOM	Field Mnemonic: Description
40	RW	CONFIG_ENABLE_SNARF_CPM: 0 = Disable Probe.I.MO snarfing a cp_m. 1 = Enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = Preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = Preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = Preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = Preallocate two state machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = Preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode report local masters as near. 1 = In basic mode report local masters as local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath.. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOsgreater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU tp PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK0.CS.SM3.MISC.CONFIG1
Address	0000000005011061 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non-REQIN events going down the arbiter pipe. After n+1 REQIN events go through the arbiter while a non-CRR event is waiting, REQIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.

Bits	SCOM	Field Mnemonic: Description
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll: 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data: 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	**Power Bus Epsilon Configuration Register**
Mnemonic	NPU.STCK0.CS.SM3.MISC.EPSILON_CONFIG
Address	0000000005011062 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/Vg scope CP write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope Reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope Reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope Reads.

Register Name	**Timer Configuration Register**
Mnemonic	NPU.STCK0.CS.SM3.MISC.XTIMER_CONFIG
Address	0000000005011063 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward-progress timer (2^n cycles).

Bits	SCOM	Field Mnemonic: Description
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). **Note:** This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for SM-Inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for SM-Inhibit timer tick1 (default 63 = off). **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV-Response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7. f(0b01) = 63. f(0b10) = 511. f(0b11) = 4095.
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV-Response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The Short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.GPU_BAR
Address	0000000005011064 (SCOM)
Description	Memory BARs. BAR register defining GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: Base address (1G address) of BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).

Bits	SCOM	Field Mnemonic: Description
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of the base address match for the BAR for brick 0: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. **Note:** It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: Base address (1G address) of BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of the base address match for the BAR for brick 1: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved

Bits	SCOM	Field Mnemonic: Description
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.PHY_BAR
Address	0000000005011066 (SCOM)
Description	BAR register defining PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2M range mapped to PHY 0 registers. Stack 1 PHY_BAR defines a 2M range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16M range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0 = Disable PHY_BAR. 1 = Enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2M aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2M aligned address of this PHY_BAR's 2M range. **Note:** In stack two, the low three address bits are reserved (16M range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.GENID_BAR
Address	0000000005011067 (SCOM)
Description	ID registers MMIO BAR. BAR register defining Generation ID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0 = Disable this BAR. 1 = Enable this BAR.

Bits	SCOM	Field Mnemonic: Description
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of the 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of the 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128K aligned address of this BAR's 128K range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Low Water Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.LOW_WATER
Address	0000000005011068 (SCOM)
Description	Water marks. State machine allocation for low water marks. Each low water mark should be greater than or equal to 1 and the sum of the low water marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be >= 8 and <= 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. Can only be changed from 0 to 1 and must stay at 1 once set.
52:63	RO	Constant = 0b000000000000

Register Name	High Water Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.HIGH_WATER
Address	0000000005011069 (SCOM)
Description	Water marks. State machine allocation for high water marks. Each high water mark should be greater than or equal to the corresponding config_low_water and less than config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Relaxed Configuration 0 Register**
Mnemonic	NPU.STCK0.CS.SM3.MISC.CONFIG_RELAXED0
Address	000000000501106A (SCOM)
Description	Ordering configuration 0 register used to configure relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0 = Disable relaxed source 0 for write operations. 1 = Enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0 = Disable relaxed source 0 for read operations. 1 = Enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: Relaxed source 0 tag mask value: 0 = Bit is masked off, corresponding match bit must be 0. 1 = Bit must equal corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0 = Disable relaxed source 1 for write operations. 1 = Enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0 = Disable relaxed source 1 for read operations. 1 = Enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CONFIG_RELAXED1
Address	000000000501106B (SCOM)
Description	Ordering configuration 1 register used to configure relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0 = Disable relaxed source 2 for write operations. 1 = Enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0 = Disable relaxed source 2 for read operations. 1 = Enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 2 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CONFIG_RELAXED2
Address	000000000501106C (SCOM)
Description	Ordering configuration 2 register used to configure relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.

Bits	SCOM	Field Mnemonic: Description
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F=0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0 = Disable relaxed source 3 for write operations. 1 = Enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0 = Disable relaxed source 3 for read operations. 1 = Enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 0 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK0.CS.SM3.MISC.NDT0_BAR
Address	0000000005011060 (SCOM)
Description	BAR register defining NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	NTL1/NDL1 MMIO BAR Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.NDT1_BAR
Address	000000000501106E (SCOM)
Description	BAR register defining NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128K aligned address of BAR for brick 1's 128K range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.PERF_CONFIG
Address	000000000501106F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.INHIBIT_CONFIG
Address	0000000005011070 (SCOM)
Description	This register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre-frequency 0: 0 = Inhibit timer tick0. 1 = Inverted nhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode . 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = Inhibit timer tick1. 1 = Inverted inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode . 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_MESSAGE0
Address	0000000005011071 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_MESSAGE1
Address	0000000005011072 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_MESSAGE2
Address	0000000005011073 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_MESSAGE3
Address	0000000005011074 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_MESSAGE4
Address	0000000005011075 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.SM_STATUS
Address	0000000005011076 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: Set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: Set to 1 when brick 0 probe allocation is at its idle level.

Bits	SCOM	Field Mnemonic: Description
2	ROX	SM_STATUS_CREQ1: Set to 1 when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: Set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: Set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: Set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: Set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: Set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: Set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: Set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: Set to 1 when the outbound Rn/Vg scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: Set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: Set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: Set to 1 when the outbound brick 1 CREQrequest queue is empty.
30	ROX	SM_STATUS_N1DGD: Set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: Set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: Set to 1 when the outbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: Set to 1 when the outbound processor bus dataresponse/merge operation queue is empty.
34	ROX	SM_STATUS_N0RSP: Set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: Set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: 1Set to when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: Set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: Set to 1 when the free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_FIRST0
Address	0000000005011077 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 1 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_FIRST1
Address	0000000005011078 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_FIRST2
Address	0000000005011079 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: Sart Epsilon, but Epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: Snoop CRESP received. but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.

Bits	SCOM	Field Mnemonic: Description
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_MASK0
Address	000000000501107A (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).

Bits	SCOM	Field Mnemonic: Description
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Mask 1 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_MASK1
Address	000000000501107B (SCOM)
Description	c_err_rpt mask reg **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: RCMD pre-snoop table look-up missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS response.

Bits	SCOM	Field Mnemonic: Description
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting fo data timeout.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: UE ECC error detected from state machine array.
21	RW	IDIAL_SM_MASK_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: Parity error detected on RCMD TTAG field.
25	RW	IDIAL_SM_MASK_PBP_1: Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: Parity error detected on CRESP TTAG.
27	RW	IDIAL_SM_MASK_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).

Bits	SCOM	Field Mnemonic: Description
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: RCMD TTAG received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: RCMD TTAG received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: CRESP TTAG received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: CRESP TTAG received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 2 Register**
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_MASK2
Address	0000000005011070 (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).

Bits	SCOM	Field Mnemonic: Description
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RSPL event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown state.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.

Bits	SCOM	Field Mnemonic: Description
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_HOLD0
Address	000000000501107D (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_HOLD1
Address	000000000501107E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK0.CS.SM3.MISC.CERR_HOLD2
Address	000000000501107F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket hit event but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did o't match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.

Bits	SCOM	Field Mnemonic: Description
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry ,but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	CQ_CTL Miscellaneous Configuration 0 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CONFIG0
Address	0000000005011080 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED0: Reserved. **Note:** This was 1dot0 mode.
1:3	RW	CONFIG1_RESERVED1: Reserved.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.

Bits	SCOM	Field Mnemonic: Description
5:9	RW	CONFIG_GEN_HEAD_DELAY: Number of cycles to wait for generation done when reading a generation head register. **Note:** Setting this field to 0 hangs the NPU.
10	RW	CONFIG_MRBGP_DIV2_COUNT_AT_EXP: 0 = Reset the master retry back-off retry count to zero when the sample period expires for group-pump. 1 = Divide the master retry back-off retry count by two when the sample period expires for group-pump.
11	RW	CONFIG_MRBSP_DIV2_COUNT_AT_EXP: 0 = Reset the master retry back-off retry count to zero when the sample period expires for system-pump. 1 = Divide the master retry back-off retry count by two when the sample period expires for system-pump.
12	RW	CONFIG_MRBGP_DIS_DYN_ADJ: 0 = Enable dynamically adjusting the master retry back-off sample period based on level for group-pump. 1 = Disable dynamically adjusting the master retry back-off sample period based on level for group-pump.
13	RW	CONFIG_MRBSP_DIS_DYN_ADJ: 0 = Enable dynamically adjusting the master retry back-off sample period based on level for system-pump. 1 = Disable dynamically adjusting the master retry back-off sample period based on level for system-pump.
14	RW	CONFIG_MRBGP_DIS_DYN_LVL_ADJ: 0 = Enable dynamically adjusting the master retry back-off thresholds based on level for group-pump. 1 = Disable dynamically adjusting the master retry back-off thresholds based on level for group-pump.
15	RW	CONFIG_MRBSP_DIS_DYN_LVL_ADJ: 0 = Enable dynamically adjusting the master retry back-off thresholds based on level for system-pump 1 = Disable dynamically adjusting the master retry back-off thresholds based on level for system-pump.
16:21	RW	CONFIG_MRBGP_THRESH1: Master retry back-off retry-count threshold at which to reduce the level for group-pump.
22:27	RW	CONFIG_MRBGP_THRESH2: Master retry back-off retry count threshold at which to increase the level for group-pump. **Note:** Make sure that thresh2 is greater than thresh1or the back-off level will only increase.
28:33	RW	CONFIG_MRBSP_THRESH1: Master retry back-off retry-count threshold at which to reduce the level for system-pump.
34:39	RW	CONFIG_MRBSP_THRESH2: Master retry back-off retry count threshold at which to increase the level for system-pump. **Note:** Make sure that thresh2 is greater than thresh1 or the back-off level will only increase.
40:43	RW	CONFIG_MRBGP_MAX_LEVEL: Master retry back-off maximum level for group-pump.
44:47	RW	CONFIG_MRBSP_MAX_LEVEL: Master retry back-off maximum level for system-pump.
48	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.
49	RW	CONFIG_DISABLE_PBM_ECC_COR: 0 = Enable ECC correction of MMIO store data. 1 = Disable ECC correction.
50	RW	CONFIG_LAB_RANDOMIZE_PE_01: 0 = Do not randomize PE(0:1). 1 = Randomize PE(0:1).
51	RW	CONFIG_LAB_RANDOMIZE_PE_23: 0 = Do not randomize PE(2:3). 1 = Randomize PE(2:3).
52:63	RW	CONFIG1_RESERVED2: Reserved.

Register Name	Future Configuration 1 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CONFIG1
Address	0000000005011081 (SCOM)
Description	Currently a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_CONFIG1: Future configuration register.

Register Name	Future Configuration 2 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CONFIG2
Address	0000000005011082 (SCOM)
Description	Currently a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_CONFIG2: Future configuration register.

Register Name	Future Configuration 3 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CONFIG3
Address	0000000005011083 (SCOM)
Description	Currently reserved a register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_CONFIG3: Future configuration register.

Register Name	Performance Match Configuration Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.PERF_MATCH_CONFIG
Address	0000000005011084 (SCOM)
Description	Performance event field match register.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	PERF_MATCH_NMCMD: NVLink command.
6:10	RW	PERF_MATCH_NMEXCMD: NVLink ExtReqCmd.
11	RW	PERF_MATCH_BE: NVLink byte enables.
12:17	RW	PERF_MATCH_CS: NVLink CS(0:5).
18:33	RW	PERF_MATCH_AECS: NVLink AECS(0:15).
34:37	RW	PERF_MATCH_PE: PE.
38:39	RW	PERF_MATCH_RESERVED1: Reserved.
40:63	RO	Constant = 0b00000000000000000000000

Register Name	Performance Mask Configuration Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.PERF_MASK_CONFIG
Address	0000000005011085 (SCOM)
Description	Performance event field mask register.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	PERF_MASK_NMCMD: NVLink command.
6:10	RW	PERF_MASK_NMEXCMD: NVLink ExtReqCmd.
11	RW	PERF_MASK_BE: NVLink byte enables.
12:17	RW	PERF_MASK_CS: NVLink CS(0:5).
18:33	RW	PERF_MASK_AECS: NVLink AECS(0:15).
34:37	RW	PERF_MASK_PE: PE.
38:39	RW	PERF_MASK_RESERVED1: Reserved.
40:63	RO	Constant = 0b0000000000000000000000000

Register Name	CQ_CTL Performance Count Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.PERF_COUNT
Address	0000000005011086 (SCOM)
Description	PMULet count values register.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	IDIAL_PERF_COUNT0: Performance counter 0.
16:31	RWX_WCLRREG	IDIAL_PERF_COUNT1: Performance counter 1.
32:47	RWX_WCLRREG	IDIAL_PERF_COUNT2: Performance counter 2.
48:63	RWX_WCLRREG	IDIAL_PERF_COUNT3: Performance counter 3.

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.PERF_CONFIG
Address	0000000005011087 (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: PMULet Enable (clocks enable).
1	RW	PERF_CONFIG_RESETMODE: 0 = Reset on read. 1 = Reset on write.
2	RW	PERF_CONFIG_FREEZEMODE: 0 = Free run mode. 1 = Freeze on any maximum.
3	RW	PERF_CONFIG_DISABLE_PMISC: 0 = Enable PMISC control of counters. 1 = Disable PMISC control of counters.

Bits	SCOM	Field Mnemonic: Description
4	RW	PERF_CONFIG_PMISC_MODE: 0 = Global PMU PMISC no reset. 1 = Global PMU PMISC reset on enable.
5:7	RW	PERF_CONFIG_CASCADE: PMULet cascade configuration.
8:9	RW	PERF_CONFIG_PRESCALE_C0: Prescale configuration for counter 0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: Prescale configuration for counter 1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: Prescale configuration for counter 2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: Prescale configuration for counter 3.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:52	RW	PERF_CONFIG_LATSTART: Latency count start event.
53:57	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
58:62	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
63	RW	PERF_CONFIG_RESERVED: Reserved.

Register Name	**Debug0 Configuration Register**
Mnemonic	NPU.STCK0.CS.CTL.MISC.DEBUG0_CONFIG
Address	0000000005011088 (SCOM)
Description	Configuration register for trace 0 chain.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of trace 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of trace 0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of trace 0.
55:62	RW	DEBUG0_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	Debug1 Configuration Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.DEBUG1_CONFIG
Address	0000000005011089 (SCOM)
Description	Configuration register for trace 1 chain.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of trace 1.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of trace 1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of trace 1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of trace 1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of trace 1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of trace 1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of trace 1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of trace 1.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of trace 1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of trace 1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of trace 1.
55:62	RW	DEBUG1_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	Brick 0 BDF-to-PE Configuration 0 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.BDF2PE_00_CONFIG
Address	000000000501108A (SCOM)
Description	Configured BDF-to-PE mapping #0 for brick 0 register. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_00_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1	RW	CONFIG_BDF2PE_00_WILDCARD: 0 = This BDF-to-PE mapping matches only this BDF. 1 = This BDF-to-PE mapping matches all BDFs.
2:3	RW	CONFIG_BDF2PE_00_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_00_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_00_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 0 BDF-to-PE Configuration 1 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.BDF2PE_01_CONFIG
Address	000000000501108B (SCOM)
Description	Configured BDF-to-PE mapping #1 for brick 0 register. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_01_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_01_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_01_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_01_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 0 BDF-to-PE Configuration 2 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.BDF2PE_02_CONFIG
Address	000000000501108C (SCOM)
Description	Configured BDF-to-PE mapping #2 for brick 0 register. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_02_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_02_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_02_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_02_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 1 BDF-to-PE Configuration 0 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.BDF2PE_10_CONFIG
Address	000000000501108D (SCOM)
Description	Configured BDF-to-PE mapping #0 for brick 1 register. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_10_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1	RW	CONFIG_BDF2PE_10_WILDCARD: 0 = This BDF-to-PE mapping matches only this BDF. 1 = This BDF-to-PE mapping matches all BDFs.
2:3	RW	CONFIG_BDF2PE_10_RESERVED: Reserved.

Bits	SCOM	Field Mnemonic: Description
4:7	RW	CONFIG_BDF2PE_10_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_10_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	**Brick 1 BDF-to-PE Configuration 1 Register**
Mnemonic	NPU.STCK0.CS.CTL.MISC.BDF2PE_11_CONFIG
Address	000000000501108E (SCOM)
Description	Configured BDF-to-PE mapping #1 for brick 1 register. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_11_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_11_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_11_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_11_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	**Brick 1 BDF-to-PE Configuration 2 Register**
Mnemonic	NPU.STCK0.CS.CTL.MISC.BDF2PE_12_CONFIG
Address	000000000501108F (SCOM)
Description	Configured BDF-to-PE mapping #2 for brick 1 register. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_12_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_12_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_12_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_12_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	**LPC Threshold Configuration Register**
Mnemonic	NPU.STCK0.CS.CTL.MISC.LPCTH_CONFIG
Address	0000000005011090 (SCOM)
Description	Threshold configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_LPCTH_BUSY_ENABLE: 0 = Disable thresholding. 1 = Enable thresholding.
1:3	RW	CONFIG_LPCTH_WINDOW_SELECT: 001 = 256 cycle window. 010 = 512 cycle window. 100 = 1024 cycle window.
4:13	RW	CONFIG_LPCTH_THRESH_0: Busy counter threshold 0. When this threshold is exceeded, the LPC_th field in the partial response ATAG is set to '01'.
14:23	RW	CONFIG_LPCTH_THRESH_1: Busy counter threshold 1. When this threshold is exceeded, the LPC_th field in the partial response ATAG is set to '10'.
24:33	RW	CONFIG_LPCTH_THRESH_2: Busy counter threshold 2. When this threshold is exceeded, the LPC_th field in the partial response ATAG is set to '11'.
34:35	RW	CONFIG_LPCTH_RESERVED1: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.INHIBIT_CONFIG
Address	0000000005011091 (SCOM)
Description	This register configures inhibits for CQ_CTL.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre-frequency 0: 0 = SM0 timer tick. 1 = Inverted SM0 timer tick. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$

Bits	SCOM	Field Mnemonic: Description
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = SM1 timer tick. 1 = Inverted SM1 timer tick. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CQ_CTL Status Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CTL_STATUS
Address	0000000005011092 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	CTL_STATUS_SM_MMIO0: Set to 1 when SM slice 0 has an MMIO pending.
1	ROX	CTL_STATUS_SM_MMIO1: Set to 1 when SM slice 1 has an MMIO pending.
2	ROX	CTL_STATUS_SM_MMIO2: Set to 1 when SM slice 2 has an MMIO pending.
3	ROX	CTL_STATUS_SM_MMIO3: Set to 1 when SM slice 3 has an MMIO pending.
4:7	ROX	CTL_STATUS_MRBGP: Master retry back-off level for group-pump commands.
8:11	ROX	CTL_STATUS_MRBSP: Master retry back-off level for system-pump commands.
12:15	ROX	CTL_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 1001 = Fenced state, fence sequencing complete. 1100 = Half-fenced state, NTL is not fenced. others = In transition between fenced and not fenced.
16:19	ROX	CTL_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 1001 = Fenced state, fence sequencing complete. 1100 = Half-fenced state, NTL is not fenced. others = In transition between fenced and not fenced.
20:21	ROX	CTL_STATUS_LPCTH: LPC threshold value driven in partial responses.
22:26	ROX	CTL_STATUS_PBM_STATE: PB-MMIO/GenId state (0b00000 = Idle).
27	ROX	CTL_STATUS_BRK0_RLX: Set to 1 when brick 0 Gen-Id/relaxed ordering is idle.
28	ROX	CTL_STATUS_BRK1_RLX: Set to1 when brick 1 Gen-Id/relaxed ordering is idle.
29	ROX	CTL_STATUS_BRK0_NVL: Set to 1 when brick 0 NVLink flush is idle.
30	ROX	CTL_STATUS_BRK1_NVL: Set to 1 when brick 1 NVLink flush is idle.
31	ROX	CTL_STATUS_ATS_SYNC: Set to 1 when ATS sync is idle.
32	ROX	CTL_STATUS_NMMU: Set to 1 when the NMMU outbound message is idle.
33	ROX	CTL_STATUS_PBLN: Set to 1 when the outbound processor bus Ln scope queue is empty.

Bits	SCOM	Field Mnemonic: Description
34	ROX	CTL_STATUS_PBNNG: Set to 1 when the outbound processor bus Nn/G scope queue is empty.
35	ROX	CTL_STATUS_PBRNVG: Set to 1 when the outbound processor bus Rn/Vg scope queue is empty.
36	ROX	CTL_STATUS_NVREQ0: Set to 1 when the outbound brick 0 request queue is empty.
37	ROX	CTL_STATUS_NVDGD0: Set to 1 when the outbound brick 0 downgrade queue is empty.
38	ROX	CTL_STATUS_NVREQ1: Set to 1 when the outbound brick 1 request queue is empty.
39	ROX	CTL_STATUS_NVDGD1: Set to 1 when the outbound brick 1 downgrade queue is empty.
40	ROX	CTL_STATUS_ATSREQ: Set to 1 when the outbound ATS TCE translate request queue is empty.
41	ROX	CTL_STATUS_MMIO: Set to 1 when the MMIO/GenId state machine is idle.
42	ROX	CTL_STATUS_PBRS: Set to 1 when the outbound PB response/merge queue is empty.
43	ROX	CTL_STATUS_NVRS0: Set to 1 when the outbound brick 0 response queue is empty.
44	ROX	CTL_STATUS_NVRS1: Set to 1 when the outbound brick 0 response queue is empty.
45	ROX	CTL_STATUS_XARS: Set to 1 when the outbound ATS/MISC response queue is empty.
46	ROX	CTL_STATUS_ATRR: Set to 1 when the outbound ATR response logic is idle.
47	ROX	CTL_STATUS_RESERVED1: Reserved.
48:63	RO	Constant = 0b0000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CERR_MESSAGE0
Address	0000000005011098 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CERR_MESSAGE1
Address	0000000005011099 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CERR_FIRST0
Address	000000000501109A (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_0: NCF0 SM0 NCF error.

Bits	SCOM	Field Mnemonic: Description
1	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_1: NCF1 SM1 NCF error.
2	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_2: NCF2 SM2 NCF error.
3	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_3: NCF3 SM3 NCF error.
4	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_4: NCF4 (Reserved).
5	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_5: NCF5 (Reserved).
6	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_6: NCF6 (Reserved).
7	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_7: NCF7 (Reserved).
8	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_0: NVF0 SM0 NVF error.
9	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_1: NVF1 SM1 NVF error.
10	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_2: NVF2 SM2 NVF error.
11	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_3: NVF3 SM3 NVF error.
12	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_4: NVF4 Illegal Probe.MO: Probe.MO received with illegal probe state.
13	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_5: NVF5 Illegal Probe.N: Probe.N received with illegal probe state.
14	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_6: NVF6 Illegal Atomic: Illegal atomic command for Atomic.NR with red = 1.
15	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_7: NVF7 Illegal Atomic: Atomic.NR with red = 0.
16	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_8: NVF8 Illegal Atomic: Atomic.NR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
17	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_9: NVF9 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 0.
18	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_10: NVF10 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 1.
19	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_11: NVF11 Illegal Atomic: Atomic.RR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
20	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_12: NVF12 Illegal ExCmd for Cmd = ExCmd-CREQ.
21	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_13: NVF13 Illegal ExCmd for Cmd = ExCmd-ATR.
22	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_14: NVF14 Illegal command or RMW with illegal length.
23	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_15: NVF15 BDF-to-PE look-up failed.
24	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_16: NVF16 Received a 256B FO = 1 write.
25	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_17: NVF17 Received an invalid AddrType field, neither 00 or 11.
26	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_18: NVF18 Received an invalid transaction ID in a NVLink response.
27	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_19: NVF19 Received a rsp_status of target error in an ATSD response.
28	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_20: NVF20 Received a rsp_status of unsupported request in an ATSD response.
29	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_21: NVF21 Received a rsp_status of '11', reserved value, in an ATSD response.
30	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_22: NVF22 Brick 0 NVF error occurred.
31	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_23: NVF23 Brick 1 NVF error occurred.
32	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_0: RSV10 (Reserved).
33	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_1: RSV11 (Reserved).
34	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_2: RSV12 (Reserved).
35	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_3: RSV13 (Reserved).
36	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_0: ASBE0 SM0 ASBE error.
37	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_1: ASBE1 SM1ASBE error.

Bits	SCOM	Field Mnemonic: Description
38	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_2: ASBE2 SM2 ASBE error.
39	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_3: ASBE3 SM3 ASBE error.
40	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_4: ASBE4 Processor bus MMIO Data Ecc CE Error.
41	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_5: ASBE5 (Reserved).
42	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_6: ASBE6 (Reserved).
43	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_7: ASBE7 (Reserved).
44	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_0: PBR0 SM0 PBR error.
45	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_1: PBR1 SM1 PBR error.
46	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_2: PBR2 SM2 PBR error.
47	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_3: PBR3 SM3 PBR error.
48	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_4: PBR4 (Reserved).
49	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_0: REG0 SM0 REG error.
53	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_1: REG1 SM1 REG error.
54	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_2: REG2 SM2 REG error.
55	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_3: REG3 SM3 REG error.
56	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_0: DUE0 Processor bus MMIO data ECC UE error.
57	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_1: DUE1 Processor bus MMIO data ECC SUE error.
58	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_2: DUE2 (Reserved).
59	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_3: DUE3 (Reserved).
60	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_0: PEF0 Brick 0 received a request to a frozen BDF/PE.
61	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_1: PEF1 Brick 1 received a request to a frozen BDF/PE.
62	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_2: PEF2 (Reserved).
63	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_3: PEF3 (Reserved).

Register Name	CERR First 1 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CERR_FIRST1
Address	000000000501109B (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_0: NLG0 SM0 NLG error.
1	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_1: NLG1 SM1 NLG error.
2	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_2: NLG2 SM2 NLG error.
3	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_3: NLG3 SM3 NLG error.
4	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_4: NLG4 Processor bus MMIO state machine invalid state.
5	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_5: NLG5 Buffer used for PB response before NTL finished writing data.

Bits	SCOM	Field Mnemonic: Description
6	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_6: NLG6 Buffer read before NTL finished writing data.
7	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_7: NLG7 Invalid state in data read state machine.
8	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_8: NLG8 Attempt to send NV request with unknown NMCMD_ command type.
9	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_9: NLG9 Attempt to send NV response with unknown NRTYPE_ response type.
10	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_10: NLG10 Invalid state in XA response state machine.
11	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_11: NLG11 (Reserved).
12	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_12: NLG12 (Reserved).
13	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_13: NLG13 (Reserved).
14	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_14: NLG14 (Reserved).
15	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_15: NLG15 (Reserved).
16	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_0: FWD0 SM0 FWD error.
17	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_1: FWD1 SM1 FWD error.
18	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_2: FWD2 SM2 FWD error.
19	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_3: FWD3 SM3 FWD error.
20	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_4: FWD4 (Reserved).
21	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_5: FWD5 (Reserved).
22	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_6: FWD6 (Reserved).
23	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_7: FWD7 (Reserved).
24	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_0: AUE0 SM0 AUE error.
25	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_1: AUE1 SM1 AUE error.
26	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_2: AUE2 SM2 AUE error.
27	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_3: AUE3 SM3 AUE error.
28	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_4: AUE4 (Reserved).
29	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_5: AUE5 (Reserved).
30	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_6: AUE6 (Reserved).
31	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_7: AUE7 (Reserved).
32	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_0: PBP0 SM0 PBP error.
33	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_1: PBP1 SM1 PBP error.
34	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_2: PBP2 SM2 PBP error.
35	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_3: PBP3 SM3 PBP error.
36	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_4: PBP4 (Reserved).
37	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_5: PBP5 (Reserved).
38	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_6: PBP6 (Reserved).
39	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_7: PBP7 (Reserved).
40	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_0: PBF0 SM0 PBF error.
41	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_1: PBF1 SM1 PBF error.
42	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_2: PBF2 SM2 PBF error.
43	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_3: PBF3 SM3 PBF error.

Bits	SCOM	Field Mnemonic: Description
44	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_4: PBR4 (Reserved).
45	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_5: PBR5 (Reserved).
46	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_6: PBR6 (Reserved).
47	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_7: PBR7 (Reserved).
48	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_0: PBC0 SM0 PBC error.
49	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_1: PBC1 SM1 PBC error.
50	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_2: PBC2 SM2 PBC error.
51	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_3: PBC3 SM3 PBC error.
52	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_4: PBC4 (Reserved).
53	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_5: PBC5 (Reserved).
54	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_6: PBC6 (Reserved).
55	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_7: PBC7 (Reserved).
56	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_0: RSV20 SM0 RSV2 error.
57	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_1: RSV21 SM1 RSV2 error.
58	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_2: RSV22 SM2 RSV2 error.
59	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_3: RSV23 SM3 RSV2 error.
60	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_0: RSV30 (Reserved).
61	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_1: RSV31 (Reserved).
62	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_2: RSV32 (Reserved).
63	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_3: RSV33 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK0.CS.CTL.MISC.CERR_MASK0
Address	000000000501109C (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_CTL_MASK_NCF_0: NCF0 SM0 NCF error.
1	RW	IDIAL_CTL_MASK_NCF_1: NCF1 SM1 NCF error.
2	RW	IDIAL_CTL_MASK_NCF_2: NCF2 SM2 NCF error.
3	RW	IDIAL_CTL_MASK_NCF_3: NCF3 SM3 NCF error.
4	RW	IDIAL_CTL_MASK_NCF_4: NCF4 (Reserved).
5	RW	IDIAL_CTL_MASK_NCF_5: NCF5 (Reserved).
6	RW	IDIAL_CTL_MASK_NCF_6: NCF6 (Reserved).
7	RW	IDIAL_CTL_MASK_NCF_7: NCF7 (Reserved).
8	RW	IDIAL_CTL_MASK_NVF_0: NVF0 SM0 NVF error.
9	RW	IDIAL_CTL_MASK_NVF_1: NVF1 SM1 NVF error.
10	RW	IDIAL_CTL_MASK_NVF_2: NVF2 SM2 NVFerror.
11	RW	IDIAL_CTL_MASK_NVF_3: NVF3 SM3 NVF error.

Bits	SCOM	Field Mnemonic: Description
12	RW	IDIAL_CTL_MASK_NVF_4: NVF4 Illegal Probe.MO: Probe.MO received with illegal probe state.
13	RW	IDIAL_CTL_MASK_NVF_5: NVF5 Illegal Probe.N: Probe.N received with illegal probe state.
14	RW	IDIAL_CTL_MASK_NVF_6: NVF6 Illegal Atomic: Illegal atomic command for Atomic.NR with red = 1.
15	RW	IDIAL_CTL_MASK_NVF_7: NVF7 Illegal Atomic: Atomic.NR with red = 0.
16	RW	IDIAL_CTL_MASK_NVF_8: NVF8 Illegal Atomic: Atomic.NR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
17	RW	IDIAL_CTL_MASK_NVF_9: NVF9 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 0.
18	RW	IDIAL_CTL_MASK_NVF_10: NVF10 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 1.
19	RW	IDIAL_CTL_MASK_NVF_11: NVF11 Illegal Atomic: Atomic.RR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
20	RW	IDIAL_CTL_MASK_NVF_12: NVF12 Illegal ExCmd for Cmd = ExCmd-CREQ.
21	RW	IDIAL_CTL_MASK_NVF_13: NVF13 Illegal ExCmd for Cmd = ExCmd-ATR.
22	RW	IDIAL_CTL_MASK_NVF_14: NVF14 Illegal command or RMW with illegal length.
23	RW	IDIAL_CTL_MASK_NVF_15: NVF15 BDF-to-PE look-up failed.
24	RW	IDIAL_CTL_MASK_NVF_16: NVF16 Received a 256B FO = 1 write.
25	RW	IDIAL_CTL_MASK_NVF_17: NVF17 Received an invalid AddrType field, neither 00 or 11.
26	RW	IDIAL_CTL_MASK_NVF_18: NVF18 Received an invalid transaction ID in a NVLink response.
27	RW	IDIAL_CTL_MASK_NVF_19: NVF19 Received a rsp_status of target error in an ATSD response.
28	RW	IDIAL_CTL_MASK_NVF_20: NVF20 Received a rsp_status of unsupported request in an ATSD response.
29	RW	IDIAL_CTL_MASK_NVF_21: NVF21 Received a rsp_status of '11', reserved value. in an ATSD response.
30	RW	IDIAL_CTL_MASK_NVF_22: NVF22 Brick 0 NVF error occurred.
31	RW	IDIAL_CTL_MASK_NVF_23: NVF23 Brick 1 NVF error occurred.
32	RW	IDIAL_CTL_MASK_RSV1_0: RSV10 (Reserved).
33	RW	IDIAL_CTL_MASK_RSV1_1: RSV11 (Reserved).
34	RW	IDIAL_CTL_MASK_RSV1_2: RSV12 (Reserved).
35	RW	IDIAL_CTL_MASK_RSV1_3: RSV13 (Reserved).
36	RW	IDIAL_CTL_MASK_ASBE_0: ASBE0 SM0 ASBE error.
37	RW	IDIAL_CTL_MASK_ASBE_1: ASBE1 SM1 ASBE error.
38	RW	IDIAL_CTL_MASK_ASBE_2: ASBE2 SM2 ASBE error.
39	RW	IDIAL_CTL_MASK_ASBE_3: ASBE3 SM3 ASBE error.
40	RW	IDIAL_CTL_MASK_ASBE_4: ASBE4 Processor bus MMIO Data ECC CE Error.
41	RW	IDIAL_CTL_MASK_ASBE_5: ASBE5 (Reserved).
42	RW	IDIAL_CTL_MASK_ASBE_6: ASBE6 (Reserved).
43	RW	IDIAL_CTL_MASK_ASBE_7: ASBE7 (Reserved).
44	RW	IDIAL_CTL_MASK_PBR_0: PBR0 SM0 PBR error.
45	RW	IDIAL_CTL_MASK_PBR_1: PBR1 SM1 PBR error.
46	RW	IDIAL_CTL_MASK_PBR_2: PBR2 SM2 PBR error.
47	RW	IDIAL_CTL_MASK_PBR_3: PBR3 SM3 PBR error.
48	RW	IDIAL_CTL_MASK_PBR_4: PBR4 (Reserved).
49	RW	IDIAL_CTL_MASK_PBR_5: PBR5 (Reserved).

Bits	SCOM	Field Mnemonic: Description
50	RW	IDIAL_CTL_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_CTL_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_CTL_MASK_REG_0: REG0 SM0 REG error.
53	RW	IDIAL_CTL_MASK_REG_1: REG1 SM1 REG error.
54	RW	IDIAL_CTL_MASK_REG_2: REG2 SM2 REG error.
55	RW	IDIAL_CTL_MASK_REG_3: REG3 SM3 REG error.
56	RW	IDIAL_CTL_MASK_DUE_0: DUE0 Processor bus MMIO data ECC UE error.
57	RW	IDIAL_CTL_MASK_DUE_1: DUE1 processor bus MMIO data ECC SUE error.
58	RW	IDIAL_CTL_MASK_DUE_2: DUE2 (Reserved).
59	RW	IDIAL_CTL_MASK_DUE_3: DUE3 (Reserved).
60	RW	IDIAL_CTL_MASK_PEF_0: PEF0 Brick 0 received a request to a frozen BDF/PE.
61	RW	IDIAL_CTL_MASK_PEF_1: PEF1 Brick 1 received a request to a frozen BDF/PE.
62	RW	IDIAL_CTL_MASK_PEF_2: PEF2 (Reserved).
63	RW	IDIAL_CTL_MASK_PEF_3: PEF3 (Reserved).

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK0.CS.CTL.MISC.CERR_MASK1
Address	000000000501109D (SCOM)
Description	c_err_rpt mask register **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_CTL_MASK_NLG_0: NLG0 SM0 NLG error.
1	RW	IDIAL_CTL_MASK_NLG_1: NLG1 SM1 NLG error.
2	RW	IDIAL_CTL_MASK_NLG_2: NLG2 SM2 NLG error.
3	RW	IDIAL_CTL_MASK_NLG_3: NLG3 SM3 NLG error.
4	RW	IDIAL_CTL_MASK_NLG_4: NLG4 Processor bus MMIO state machine invalid state.
5	RW	IDIAL_CTL_MASK_NLG_5: NLG5 Buffer used for PB response before NTL finished writing data.
6	RW	IDIAL_CTL_MASK_NLG_6: NLG6 Buffer read before NTL finished writing data.
7	RW	IDIAL_CTL_MASK_NLG_7: NLG7 Invalid state in data read state machine.
8	RW	IDIAL_CTL_MASK_NLG_8: NLG8 Attempt to send NV request with unknown NMCMD_ command type.
9	RW	IDIAL_CTL_MASK_NLG_9: NLG9 Attempt to send NV response with unknown NRTYPE_ response type.
10	RW	IDIAL_CTL_MASK_NLG_10: NLG10 Invalid state in XA response state machine.
11	RW	IDIAL_CTL_MASK_NLG_11: NLG11 (Reserved).
12	RW	IDIAL_CTL_MASK_NLG_12: NLG12 (Reserved).
13	RW	IDIAL_CTL_MASK_NLG_13: NLG13 (Reserved).
14	RW	IDIAL_CTL_MASK_NLG_14: NLG14 (Reserved).
15	RW	IDIAL_CTL_MASK_NLG_15: NLG15 (Reserved).
16	RW	IDIAL_CTL_MASK_FWD_0: FWD0 SM0 FWD error.
17	RW	IDIAL_CTL_MASK_FWD_1: FWD1 SM1 FWD error.

Bits	SCOM	Field Mnemonic: Description
18	RW	IDIAL_CTL_MASK_FWD_2: FWD2 SM2 FWD error.
19	RW	IDIAL_CTL_MASK_FWD_3: FWD3 SM3 FWD error.
20	RW	IDIAL_CTL_MASK_FWD_4: FWD4 (Reserved).
21	RW	IDIAL_CTL_MASK_FWD_5: FWD5 (Reserved).
22	RW	IDIAL_CTL_MASK_FWD_6: FWD6 (Reserved).
23	RW	IDIAL_CTL_MASK_FWD_7: FWD7 (Reserved).
24	RW	IDIAL_CTL_MASK_AUE_0: AUE0 SM0 AUE error.
25	RW	IDIAL_CTL_MASK_AUE_1: AUE1 SM1 AUE error.
26	RW	IDIAL_CTL_MASK_AUE_2: AUE2 SM2 AUE error.
27	RW	IDIAL_CTL_MASK_AUE_3: AUE3 SM3 AUE error.
28	RW	IDIAL_CTL_MASK_AUE_4: AUE4 (Reserved).
29	RW	IDIAL_CTL_MASK_AUE_5: AUE5 (Reserved).
30	RW	IDIAL_CTL_MASK_AUE_6: AUE6 (Reserved).
31	RW	IDIAL_CTL_MASK_AUE_7: AUE7 (Reserved).
32	RW	IDIAL_CTL_MASK_PBP_0: PBP0 SM0 PBP error.
33	RW	IDIAL_CTL_MASK_PBP_1: PBP1 SM1 PBP error.
34	RW	IDIAL_CTL_MASK_PBP_2: PBP2 SM2 PBP error.
35	RW	IDIAL_CTL_MASK_PBP_3: PBP3 SM3 PBP error.
36	RW	IDIAL_CTL_MASK_PBP_4: PBP4 (Reserved).
37	RW	IDIAL_CTL_MASK_PBP_5: PBP5 (Reserved).
38	RW	IDIAL_CTL_MASK_PBP_6: PBP6 (Reserved).
39	RW	IDIAL_CTL_MASK_PBP_7: PBP7 (Reserved).
40	RW	IDIAL_CTL_MASK_PBF_0: PBF0 SM0 PBF error.
41	RW	IDIAL_CTL_MASK_PBF_1: PBF1 SM1 PBF error.
42	RW	IDIAL_CTL_MASK_PBF_2: PBF2 SM2 PBF error.
43	RW	IDIAL_CTL_MASK_PBF_3: PBF3 SM3 PBF error.
44	RW	IDIAL_CTL_MASK_PBF_4: PBR4 (Reserved).
45	RW	IDIAL_CTL_MASK_PBF_5: PBR5 (Reserved).
46	RW	IDIAL_CTL_MASK_PBF_6: PBR6 (Reserved).
47	RW	IDIAL_CTL_MASK_PBF_7: PBR7 (Reserved).
48	RW	IDIAL_CTL_MASK_PBC_0: PBC0 SM0 PBC error.
49	RW	IDIAL_CTL_MASK_PBC_1: PBC1 SM1 PBC error.
50	RW	IDIAL_CTL_MASK_PBC_2: PBC2 SM2 PBC error.
51	RW	IDIAL_CTL_MASK_PBC_3: PBC3 SM3 PBC error.
52	RW	IDIAL_CTL_MASK_PBC_4: PBC4 (Reserved).
53	RW	IDIAL_CTL_MASK_PBC_5: PBC5 (Reserved).
54	RW	IDIAL_CTL_MASK_PBC_6: PBC6 (Reserved).
55	RW	IDIAL_CTL_MASK_PBC_7: PBC7 (Reserved).
56	RW	IDIAL_CTL_MASK_RSV2_0: RSV20 SM0 RSV2 error.

Bits	SCOM	Field Mnemonic: Description
57	RW	IDIAL_CTL_MASK_RSV2_1: RSV21 SM1 RSV2 error.
58	RW	IDIAL_CTL_MASK_RSV2_2: RSV22 SM2 RSV2 error.
59	RW	IDIAL_CTL_MASK_RSV2_3: RSV23 SM3 RSV2 error.
60	RW	IDIAL_CTL_MASK_RSV3_0: RSV30 (Reserved).
61	RW	IDIAL_CTL_MASK_RSV3_1: RSV31 (Reserved).
62	RW	IDIAL_CTL_MASK_RSV3_2: RSV32 (Reserved).
63	RW	IDIAL_CTL_MASK_RSV3_3: RSV33 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CERR_HOLD0
Address	000000000501109E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_0: NCF0 SM0 NCF error.
1	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_1: NCF1 SM1 NCF error.
2	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_2: NCF2 SM2 NCF error.
3	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_3: NCF3 SM3 NCF error.
4	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_4: NCF4 (Reserved).
5	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_5: NCF5 (Reserved).
6	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_6: NCF6 (Reserved).
7	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_7: NCF7 (Reserved).
8	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_0: NVF0 SM0 NVF error.
9	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_1: NVF1 SM1 NVF error.
10	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_2: NVF2 SM2 NVF error.
11	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_3: NVF3 SM3 NVF error.
12	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_4: NVF4 Illegal Probe.MO: Probe.MO received with illegal probe state.
13	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_5: NVF5 Illegal Probe.N: Probe.N received with illegal probe state.
14	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_6: NVF6 Illegal Atomic: Illegal atomic command for Atomic.NR with red = 1.
15	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_7: NVF7 Illegal Atomic: Atomic.NR with red = 0.
16	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_8: NVF8 Illegal Atomic: Atomic.NR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
17	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_9: NVF9 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 0.
18	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_10: NVF10 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 1.
19	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_11: NVF11 Illegal Atomic: Atomic.RR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
20	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_12: NVF12 Illegal ExCmd for Cmd = ExCmd-CREQ.
21	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_13: NVF13 Illegal ExCmd for Cmd = ExCmd-ATR.
22	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_14: NVF14 Illegal command or RMW with illegal length.
23	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_15: NVF15 BDF-to-PE look-up failed.

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_16: NVF16 Received a 256B FO = 1 write.
25	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_17: NVF17 Received an invalid AddrType field, neither 00 or 11.
26	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_18: NVF18 Received an invalid transaction ID in a NVLink response.
27	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_19: NVF19 Received a rsp_status of target error in an ATSD response.
28	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_20: NVF20 Received a rsp_status of unsupported request in an ATSD response.
29	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_21: NVF21 Received a rsp_status of '11', reserved value, in an ATSD response.
30	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_22: NVF22 Brick 0 NVF error occurred.
31	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_23: NVF23 Brick 1 NVF error occurred.
32	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_0: RSV10 (Reserved).
33	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_1: RSV11 (Reserved).
34	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_2: RSV12 (Reserved).
35	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_3: RSV13 (Reserved).
36	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_0: ASBE0 SM0 ASBE error.
37	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_1: ASBE1 SM1 ASBE error.
38	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_2: ASBE2 SM2 ASBE error.
39	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_3: ASBE3 SM3 ASBE error.
40	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_4: ASBE4 Processor bus MMIO Data ECC CE Error.
41	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_5: ASBE5 (Reserved).
42	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_6: ASBE6 (Reserved).
43	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_7: ASBE7 (Reserved).
44	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_0: PBR0 SM0 PBR error.
45	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_1: PBR1 SM1 PBR error.
46	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_2: PBR2 SM2 PBR error.
47	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_3: PBR3 SM3 PBR error.
48	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_4: PBR4 (Reserved).
49	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_0: REG0 SM0 REG error.
53	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_1: REG1 SM1 REG error.
54	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_2: REG2 SM2 REG error.
55	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_3: REG3 SM3 REG error.
56	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_0: DUE0 Processor bus MMIO data ECC UE error.
57	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_1: DUE1 Processor bus MMIO data ECC SUE error.
58	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_2: DUE2 (Reserved).
59	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_3: DUE3 (Reserved).
60	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_0: PEF0 Brick 0 received a request to a frozen BDF/PE.
61	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_1: PEF1 Brick 1 received a request to a frozen BDF/PE.

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_2: PEF2 (Reserved).
63	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_3: PEF3 (Reserved).

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK0.CS.CTL.MISC.CERR_HOLD1
Address	000000000501109F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_0: NLG0 SM0 NLG error.
1	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_1: NLG1 SM1 NLG error.
2	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_2: NLG2 SM2 NLG error.
3	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_3: NLG3 SM3 NLG error.
4	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_4: NLG4 Processor bus MMIO state machine invalid state.
5	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_5: NLG5 Buffer used for PB response before NTL finished writing data.
6	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_6: NLG6 Buffer read before NTL finished writing data.
7	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_7: NLG7 Invalid state in data read state machine.
8	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_8: NLG8 Attempt to send NV request with unknown NMCMD_ command type.
9	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_9: NLG9 Attempt to send NV response with unknown NRTYPE_ response type.
10	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_10: NLG10 Invalid state in XA response state machine.
11	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_11: NLG11 (Reserved).
12	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_12: NLG12 (Reserved).
13	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_13: NLG13 (Reserved).
14	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_14: NLG14 (Reserved).
15	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_15: NLG15 (Reserved).
16	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_0: FWD0 SM0 FWD error.
17	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_1: FWD1 SM1 FWD error.
18	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_2: FWD2 SM2 FWD error.
19	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_3: FWD3 SM3 FWD error.
20	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_4: FWD4 (Reserved).
21	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_5: FWD5 (Reserved).
22	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_6: FWD6 (Reserved).
23	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_7: FWD7 (Reserved).
24	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_0: AUE0 SM0 AUE error.
25	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_1: AUE1 SM1 AUE error.
26	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_2: AUE2 SM2 AUE error.
27	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_3: AUE3 SM3 AUE error.
28	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_4: AUE4 (Reserved).

Bits	SCOM	Field Mnemonic: Description
29	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_5: AUE5 (Reserved).
30	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_6: AUE6 (Reserved).
31	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_7: AUE7 (Reserved).
32	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_0: PBP0 SM0 PBP error.
33	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_1: PBP1 SM1 PBP error.
34	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_2: PBP2 SM2 PBP error.
35	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_3: PBP3 SM3 PBP error.
36	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_4: PBP4 (Reserved).
37	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_5: PBP5 (Reserved).
38	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_6: PBP6 (Reserved).
39	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_7: PBP7 (Reserved).
40	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_0: PBF0 SM0 PBF error.
41	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_1: PBF1 SM1 PBF error.
42	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_2: PBF2 SM2 PBF error.
43	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_3: PBF3 SM3 PBF error.
44	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_4: PBR4 (Reserved).
45	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_5: PBR5 (Reserved).
46	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_6: PBR6 (Reserved).
47	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_7: PBR7 (Reserved).
48	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_0: PBC0 SM0 PBC error.
49	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_1: PBC1 SM1 PBC error.
50	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_2: PBC2 SM2 PBC error.
51	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_3: PBC3 SM3 PBC error.
52	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_4: PBC4 (Reserved).
53	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_5: PBC5 (Reserved).
54	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_6: PBC6 (Reserved).
55	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_7: PBC7 (Reserved).
56	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_0: RSV20 SM0 RSV2 error.
57	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_1: RSV21 SM1 RSV2 error.
58	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_2: RSV22 SM2 RSV2 error.
59	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_3: RSV23 SM3 RSV2 error.
60	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_0: RSV30 (Reserved).
61	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_1: RSV31 (Reserved).
62	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_2: RSV32 (Reserved).
63	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_3: RSV33 (Reserved).

Register Name	CQ_DAT Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK0.DAT.MISC.CONFIG1
Address	00000000050110A1 (SCOM)
Description	CQ_DAT miscellaneous configuration 1 register.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG1_MGR_CREDIT: CTL to DAT merge request interface number of credits.
2:4	RW	CONFIG1_MRG_PBTX_NBUF: CTL to DAT merge request Power bus TX interface logic request buffer size.
5:8	RW	CONFIG1_MRG_RDBF_NBUF: CTL to DAT merge request Power bus TX array read logic request buffer size.
9:12	RW	CONFIG1_MRG_IBWR_NBUF: CTL to DAT merge request BE merge/OI loopback/AMO inbound buffer write logic request buffer size.
13:15	RW	CONFIG1_MRG_IBRD_NBUF: CTL to DAT merge request BE merge/IO loopback/AMO inbound buffer read logic request buffer size.
16:18	RW	CONFIG1_MRG_BBRD_NBUF: CTL to DAT merge request BE merge BE buffer read logic request buffer size.
19:21	RW	CONFIG1_MRG_OBRD_NBUF: CTL to DAT merge request BE merge/OI loopback/AMO outbound buffer read logic request buffer size.
22	RW	CONFIG1_MRG_CR_DIS: Writing a 1 disables CQ_DAT to send credits to CTL for merge operations.
23	RW	CONFIG1_MRG_CTLW_CR_DIS: Writing a 1 disables CQ_DAT to send credits to CTL for inbound buffer write operations.
24:25	RW	CONFIG1_NTLR_PAUSE_THRESH: Specifies the number of outbound buffer NTL port occupation cycles before raising NTL pause request: 00 = 32 cycles. 01 = 16 cycles. 10 = 8 cycles. 11 = Never.
26:27	RW	CONFIG1_CTLR_HP_THRESH: Specifies the number of outbound buffer CTL read wait cycles before giving high priority: 00 = 16 cycles. 01 = 8 cycles. 10 = 4 cycles. 11 = Never.
28:29	RW	CONFIG1_NTLW_PAUSE_THRESH: Specifies the number of inbound buffer NTL port occupation cycles before raising NTL pause request: 00 = 16 cycles. 01 = 8 cycles. 10 = 4 cycles. 11 = Never.
30:31	RW	CONFIG1_CTLW_HP_THRESH: Specifies the number of inbound buffer CTL write wait cycles before giving high priority: 00b = 16 cycles. 01 = 8 cycles. 10 = 4 cycles. 11 = Never.
32	RW	CONFIG1_PBTX_REDUCE_RTAG: Writing a 1 has the CQ_DAT limit number of outstanding RTAGs to 1 on PB transmit interface (default is 2).
33	RW	CONFIG1_PBTX_DELAY_BDONE: Writing a 1 has the CQ_DAT PB transmit logic wait until all the OWs are presented on the PB before raising buffdone to CTL.
34	RW	CONFIG1_PBTX_FLIP_IMIN_BIG: Writing a 1 has the CQ_DAT PB transmit logic flip the endian of the integer minimum value on failed inc/dec when e = 0 is specified.

Bits	SCOM	Field Mnemonic: Description
35	RW	CONFIG1_PBTX_FLIP_IMIN_LITTLE: Writing a 1 has the CQ_DAT PB transmit logic flip the endian of the integer minimum value on failed inc/dec when e = 1 is specified.
36	RW	CONFIG1_ALU_SAFE_LATENCY: Writing a 1 has the CQ_DAT wait for one more cycle for ALU output in case x2 phase detection logic goes wrong.
37	RW	CONFIG1_ALU_FLIP_ENDIAN_BIG: Writing a 1 has the CQ_DAT flip the ALU endian when e = 0 is specified.
38	RW	CONFIG1_ALU_FLIP_ENDIAN_LITTLE: Writing a 1 has the CQ_DAT flip the ALU endian when e = 1 is specified.
39	RW	CONFIG1_PBTX_EARLY_AFTAG: Writing a 1 has the CQ_DAT raise buffdone to CTL earlier for armwf_* operations. CQ_DAT does not wait for fetch data to be presented on the PB. However CQ_DAT does wait for fetch data to leave the inbound buffer that is, the buffer entry can still be safely reused. This bit can be randomized in verification.
40:63	RW	CONFIG1_RESERVED1: Reserved.

Register Name	CQ_DAT ECC Configuration Register
Mnemonic	NPU.STCK0.DAT.MISC.ECC_CONFIG
Address	00000000050110A2 (SCOM)
Description	CQ_DAT ECC configuration register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ECC_CONFIG_PBTX_AMO_IGNORE_XUE: For armwf_inc/dec ttypes, replace PB transmit data with negative maximum value when comparison fails, even if the data has UE or SUE. The negative maximum value will be marked with SUE as long as suedis_pt = 0.
1	RW	ECC_CONFIG_SUE_DIS_BR_PERR: Writing a 1 disables marking merge result data with SUE when BE-buf read data latch has parity error.
2	RW	ECC_CONFIG_SUE_DIS_IR_PERR: Writing a 1 disables marking merge result data with SUE when inbound buffer read data latch has parity error.
3	RW	ECC_CONFIG_SUE_DIS_OR_PERR: Writing a 1 disables marking merge result data with SUE when the outbound buffer read data latch has parity error.
4	RW	ECC_CONFIG_CORR_DIS_PT: Writing a 1 disables ECC correction in Power bus TX.
5	RW	ECC_CONFIG_CORR_DIS_PR: Writing a 1 disables ECC correction in Power bus RX.
6	RW	ECC_CONFIG_CORR_DIS_BR: Writing a 1 disables ECC correction in byte enable buffer read.
7	RW	ECC_CONFIG_CORR_DIS_IR: Writing a 1 disables ECC correction in merge operation inbound buffer read.
8	RW	ECC_CONFIG_CORR_DIS_OR: Writing a 1 disables ECC correction in merge operation outbound buffer read.
9	RW	ECC_CONFIG_SUE_DIS_PT: Writing a 1 disables converting ECC UE to SUE in Power bus TX.
10	RW	ECC_CONFIG_SUE_DIS_PR: Writing a 1 disables converting ECC UE to SUE in Power bus RX.
11	RW	ECC_CONFIG_SUE_DIS_BR: Writing a 1 disables converting ECC UE to SUE in byte enable buffer read.
12	RW	ECC_CONFIG_SUE_DIS_IR: Writing a 1 disables converting ECC UE to SUE in merge operation inbound buffer read.
13	RW	ECC_CONFIG_SUE_DIS_OR: Writing a 1 disables converting ECC UE to SUE in merge operation outbound buffer read.
14:31	RW	ECC_CONFIG_RESERVED: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CQ_DAT Scratch 0 Register
Mnemonic	NPU.STCK0.DAT.MISC.SCRATCH0
Address	00000000050110A3 (SCOM)
Description	CQ_DAT scratch register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	SCRATCH0_IDIAL: Scratch register.

Register Name	CQ_DAT CERR ECC Hold Register
Mnemonic	NPU.STCK0.DAT.MISC.CERR_ECC_HOLD
Address	00000000050110A4 (SCOM)
Description	CQ_DAT ECC error c_err_rpt status and clear register.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:13	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PT_UE: ECC UE on Power Bus TX data path (4 ECC words).
14:17	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PR_UE: ECC UE on Power Bus RX data path (4 ECC words).
18:19	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_BR_UE: ECC UE on byte enable buffer read data path (2 ECC words).
20:23	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_IR_UE: ECC UE on merge operation inbound buffer read data path (4 ECC words).
24:27	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_OR_UE: ECC UE on merge operation outbound buffer read data path (4 ECC words).
28:31	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PT_SUE: ECC SUE on Power Bus TX data path (4 ECC words).
32:35	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PR_SUE: ECC SUE on Power Bus RX data path (4 ECC words).
36:37	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_BR_SUE: ECC SUE on byte enable buffer read data path (2 ECC words).
38:41	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_IR_SUE: ECC SUE on merge operation inbound buffer read data path (4 ECC words).
42:45	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_OR_SUE: ECC SUE on merge operation outbound buffer read data path (4 ECC words).
46:49	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PT_CE: ECC CE on Power Bus TX data path (4 ECC words).
50:53	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PR_CE: ECC CE on Power Bus RX data path (4 ECC words).
54:55	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_BR_CE: ECC CE on byte enable buffer read data path (2 ECC words).
56:59	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_IR_CE: ECC CE on merge operation inbound buffer read data path (4 ECC words).
60:63	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_OR_CE: ECC CE on merge operation outbound buffer read data path (4 ECC words).

Register Name	CQ_DAT CERR ECC Mask Register
Mnemonic	NPU.STCK0.DAT.MISC.CERR_ECC_MASK
Address	00000000050110A5 (SCOM)
Description	CQ_DAT ECC error c_err_rpt mask register.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:63	RW	CERR_ECC_MASK_BITS: CQ_DAT ECC error c_err_rpt mask bits.

Register Name	CQ_DAT CERR ECC First Register
Mnemonic	NPU.STCK0.DAT.MISC.CERR_ECC_FIRST
Address	00000000050110A6 (SCOM)
Description	CQ_DAT ECC error c_err_rpt first register.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:63	RWX_WCLEAR	CERR_ECC_FIRST_BITS: CQ_DAT ECC error c_err_rpt first error bits.

Register Name	CQ_DAT CERR Parity Hold Register
Mnemonic	NPU.STCK0.DAT.MISC.CERR_PTY_HOLD
Address	00000000050110A7 (SCOM)
Description	CQ_DAT parity error c_err_rpt status and clear register.

Bits	SCOM	Field Mnemonic: Description
0:36	RO	Constant = 0b000000000000000000000000000000000000
37	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_INHIBIT_CONFIG: Parity error on inhibit configuration register.
38	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_MISC_STATE: Parity error on critical state latches in the miscellaneous subunit.
39	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_MRG_STATE: Parity error on critical state latches in the merge subunit.
40	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_OBUF_STATE: Parity error on critical state latches in the outbound buffer subunit.
41	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_PBTX_STATE: Parity error on critical state latches in the PB transmit subunit.
42	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_RQIN_STATE: Parity error on critical state latches in the merge request buffer subunit.
43	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_IBUF_STATE: Parity error on critical state latches in the inbound buffer subunit.
44	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_ERRINJ: Parity error on ecc_errinj register.
45:48	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_PBTX_AMO: Parity error in PB transmit AMO inc/dec data path (4 words).
49:52	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_IBRD: Parity error in merge operation inbound buffer read data path (4 words).
53:56	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_OBRD: Parity error in merge operation outbound buffer read data path (4 words).
57:58	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_BBRD: Parity error in byte enable buffer read data path (2 words).
59	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_PBRX_RTAG: Parity error on received RTAG on the PB receive interface.
60	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_ECC_CONFIG: Parity error on ecc_config register.
61	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_CONFIG1: Parity error on configuration 1 register.
62	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_DEBUG0_CONFIG: Parity error on debug 0 configuration register.

Bits	SCOM	Field Mnemonic: Description
63	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_DEBUG1_CONFIG: Parity error on debug1_config register.

Register Name	CQ_DAT CERR Parity Mask Register
Mnemonic	NPU.STCK0.DAT.MISC.CERR_PTY_MASK
Address	00000000050110A8 (SCOM)
Description	CQ_DAT parity error c_err_rpt mask register.

Bits	SCOM	Field Mnemonic: Description
0:36	RO	Constant = 0b000000000000000000000000000000000000
37:63	RW	CERR_PTY_MASK_BITS: CQ_DAT parity error c_err_rpt mask bits.

Register Name	CQ_DAT CERR Parity First Register
Mnemonic	NPU.STCK0.DAT.MISC.CERR_PTY_FIRST
Address	00000000050110A9 (SCOM)
Description	CQ_DAT parity error c_err_rpt first register.

Bits	SCOM	Field Mnemonic: Description
0:36	RO	Constant = 0b000000000000000000000000000000000000
37:63	RWX_WCLEAR	CERR_PTY_FIRST_BITS: CQ_DAT parity error c_err_rpt first error bits.

Register Name	CQ_DAT CERR Logic Hold Register
Mnemonic	NPU.STCK0.DAT.MISC.CERR_LOG_HOLD
Address	00000000050110AA (SCOM)
Description	CQ_DAT logic error c_err_rpt status and clear register.

Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b00000000000000000000000000000000000000000000000
47	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_BBUF_RDWR: Logic error: Read/write conflict on BE buffer, the same buffer entry was read and written in the same cycle.
48	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_RDWR: Logic error: Read/write conflict on inbound buffer, the same buffer entry was read and written in the same cycle.
49	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_OBUF_RDWR: Logic error: Read-write conflict on outbound buffer, the same buffer entry was read and written in the same cycle.
50:55	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_RQIN_OVF: Logic error: Merge request buffer overflow in a merge pipeline: bit 0 = Error in PB transmit request pipeline. bit 1 = Error in PB transmit array read pipeline. bit 2 = Error in merge inbound buffer write pipeline. bit 3 = Error in merge inbound buffer read pipeline. bit 4 = Error in merge BE buffer read pipeline. bit 5 = Error in merge outbound buffer read pipeline.
56	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_CTL_PIPE: Logic error: Inbound buffer CTL write request/data lost due to excessive incoming request.
57	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_PBTX_PIPE: Logic error: Pipeline overflow in PB transmit logic.

Bits	SCOM	Field Mnemonic: Description
58	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_MRG_IR_PIPE: Logic error: Pipeline overflow in merge inbound buffer read logic.
59	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_MRG_OR_PIPE: Logic error: Pipeline overflow in merge outbound buffer read logic.
60	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_AMO_ADDR: Logic error: Invalid address position within OW for armw_cas_t, armwf_inc_b, armwf_inc_e, and armwf_dec_b ttypes.
61	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_PBRX_RTAG: Logic error: Invalid RTAG observed on the PB receive interface.
62	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_WRITE: Logic error: NTL/ CTL wrote inbound buffer entry 0 - 3 cycles after the same entry was read for PB TX.
63	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_WARB: Logic error: More than one write requests granted on inbound buffer write port.

Register Name	**CQ_DAT CERR Logic Mask Register**
Mnemonic	NPU.STCK0.DAT.MISC.CERR_LOG_MASK
Address	00000000050110AB (SCOM)
Description	CQ_DAT logic error c_err_rpt mask register.

Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b00000000000000000000000000000000000000000000000
47:63	RW	CERR_LOG_MASK_BITS: CQ_DAT logic error c_err_rpt mask bits.

Register Name	**CQ_DAT CERR Logic First Register**
Mnemonic	NPU.STCK0.DAT.MISC.CERR_LOG_FIRST
Address	00000000050110AC (SCOM)
Description	CQ_DAT logic error c_err_rpt first register

Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b00000000000000000000000000000000000000000000000
47:63	RWX_WCLEAR	CERR_LOG_FIRST_BITS: CQ_DAT logic error c_err_rpt first error bits.

Register Name	**CQ_DAT RAS Error Message 0 Register**
Mnemonic	NPU.STCK0.DAT.MISC.REM0
Address	00000000050110AD (SCOM)
Description	CQ_DAT RAS error message register.

Bits	SCOM	Field Mnemonic: Description
0:16	RO	Constant = 0b00000000000000000

Bits	SCOM	Field Mnemonic: Description
17:21	ROX	REM0_IBUF_WSRC: Indicates the inbound buffer write requester that caused the read-write conflict: 0 = NTL0 datin immediate write. 1 = NTL1 datin immediate write. 2 = NTL1 datin delayed write. 3 = CTL write. 4 = Merge logic.
22:23	ROX	REM0_IBUF_RSRC: Indicates the inbound buffer read requester that caused read-write conflict. 0 = PBTX transmit. 1 = Merge logic.
24:31	ROX	REM0_IBUF_AIDX: The inbound buffer entry (0 - 255) on which read/write conflict occurred.
32:33	ROX	REM0_IBUF_ABANK: The inbound buffer array bank (0 - 3) on which read/write conflict occurred.
34:35	ROX	REM0_OBUF_WSRC: Indicates the outbound buffer write requester that caused read/write conflict: 0 = PBTX receive. 1 = Merge logic I-O loopback.
36:41	ROX	REM0_OBUF_RSRC: Indicates the outbound read requester that caused read/write conflict: 0 = NTL0 datout immediate read. 1 = NTL1 datout immediate read. 2 = NTL0 datout regular read. 3 = NTL1 datout regular read. 4 = Merge logic. 5 = CTL read.
42:49	ROX	REM0_OBUF_AIDX: The outbound entry (0 - 255) on which the read/write conflict occurred.
50:51	ROX	REM0_OBUF_ABANK: The outbound array bank (0-3) on which the read/write conflict occurred.
52:53	ROX	REM0_BBUF_WSRC: Indicates the BE buffer write requester that caused read/write conflict: bit 0 : NTL datin. bit 1 : Dispalt logic in MISC.
54:55	ROX	REM0_BBUF_RSRC: Indicates the BE buffer read requester that caused read/write conflict: bit 0 : Merge logic. bit 1 : Dispalt logic in MISC.
56:63	ROX	REM0_BBUF_AIDX: The BE buffer entry (0 - 255) on which the read/write conflict occurred.

Register Name	CQ_DAT RAS Error Message 1 Register
Mnemonic	NPU.STCK0.DAT.MISC.REM1
Address	00000000050110AE (SCOM)
Description	CQ_DAT RAS error message register.

Bits	SCOM	Field Mnemonic: Description
0:33	RO	Constant = 0b00000000000000000000000000000000
34:55	ROX	REM1_PBRX_RTAG: The invalid RTAG observed on the PB receive interface.
56:58	ROX	REM1_ALU_ADR: The invalid ALU address in the OW that caused the address error (in unit of 4B, 0 - 7).
59:62	ROX	REM1_ALU_TYPE: The ALU optype with which an address error was detected.
63	ROX	REM1_ALU_SZ: The ALU operand size (0:4B, 1:8B) when an address error was detected.

Register Name	CQ_DAT Debug0 Configuration Register
Mnemonic	NPU.STCK0.DAT.MISC.DEBUG0_CONFIG
Address	00000000050110B0 (SCOM)
Description	CQ_DAT debug 0 configuration register.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of trace 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of trace 0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of trace 0.
55:62	RW	DEBUG0_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	CQ_DAT Debug1 Configuration Register
Mnemonic	NPU.STCK0.DAT.MISC.DEBUG1_CONFIG
Address	00000000050110B1 (SCOM)
Description	CQ_DAT debug 1 configuration register.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of trace 0.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of trace 0.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of trace 0.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of trace 0.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of trace 0.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of trace 0.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of trace 0.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of trace 0.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of trace 0.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of trace 0.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of trace 0.
55:62	RW	DEBUG1_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	CQ_DAT Scratch 1 Register
Mnemonic	NPU.STCK0.DAT.MISC.SCRATCH1
Address	00000000050110BC (SCOM)
Description	CQ_DAT scratch register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	SCRATCH1_IDIAL: Scratch register.

Register Name	NTL Miscellaneous Configuration 2 Register
Mnemonic	NPU.STCK0.NTL0.REGS.CONFIG2
Address	00000000050110C0 (SCOM)
Description	This register is used to control internal NTL function. It contains mode bits, chicken switches, and thresholds.

Bits	SCOM	Field Mnemonic: Description
0	RW	BRICK_ENABLE: When set to 0b1, this NVLink brick is enabled. This configuration bit is used as a general clock gate for latches in the NTL design.
1	RW	RSP_CTL_CRED_SINGLE_ENA: When set to 0b1, NTL only gives CQ_CTL one RSP credit at a time, instead of the normal 2.
2	RW	CREQ_BE_128: When set to 0b1, NTL always sends 128 bytes of data when it needs to send a byte enable (BE) flit to the GPU for a CREQ packet. When set to 0b0, NTL sends the least number of data flits required.
3	RW	DGD_BE_128: When set to 0b1, NTL always sends 128 bytes of data when it needs to send a byte enable (BE) flit to the GPU for a downgrade packet (BE and data flits are sent in the TransDone packet for the downgrade). When set to 0b0, NTL sends the least number of data flits required.
4	RW	WR_SPLIT_UT0_ENA: When set to 0b1, NTL splits up the write requests with UT = 0 from the GPU that maps to MMIO space into the legal processor bus sizes/alignments. When set to 0b0, NTL passes all write requests with UT = 0 as is to CQ.
5	RW	WR_SPLIT_UT1_ENA: When set to 0b1, NTL splits up the write requests with UT = 1 from the GPU into legal processor bus sizes/alignments. This includes both DMA writes and MMIO writes since there is no way for NTL to distinguish between them. When set to 0b0, NTL passes all write requests with UT = 1 as is to CQ.
6	RW	BRICK_DEBUG_MODE: When set to 0b1, NTL ignores all incoming NVLink packets from the GPU and throws away all NVLink requests/responses from CQ destined for the GPU. This mode is used for debug purposes only when the NPU is not connected over NVLink to a GPU.
7	RW	P9_TO_P9_MODE: When set to 0b1, NTL sets UT = 1 for all incoming read, write, and atomic NVLink packets before sending to CQ. This mode is used for debug purposes only when the NPU is connected to another/same NPU over NVLink.
8:9	RW	CONFIG2_RESERVED1: Reserved.
10:15	RW	CAM256_MAX_CNT: This field specifies the number of entries in the CAM that holds information to send responses for 256 byte operations that require a response (maximum value = 48).
16	RW	NDL_RX_PARITY_ENA: When set to 0b1, NTL checks the parity on the incoming NDL RX signals.
17	RW	NDL_TX_PARITY_ENA: When set to 0b1, NTL checks the parity on the incoming NDL TX (that is, TX credits) signals.
18	RW	NDL_PRI_PARITY_ENA: When set to 0b1, NTL checks the parity on the incoming NDL signals.
19	RW	RCV_CREDIT_OVERFLOW_ENA: When set to 0b1, NTL checks for overflows on any received credits from the GPU, NDL, and NDL wrapper.

Bits	SCOM	Field Mnemonic: Description
20	RW	HDR_ARR_ECC_CORR_ENA: When set to 0b1, NTL corrects ECC SBEs when reading the RX header array.
21	RW	DAT_ARR_ECC_CORR_ENA: When set to 0b1, NTL corrects ECC SBEs when reading the RX data array. NTL only corrects ECC on reads of the RX data array that require NTL to update the data before sending to CQ_DAT (for example, BE flit or data flits for atomic CAS ops).
22	RW	TX_DATA_ECC_CORR_ENA: When set to 0b1, NTL corrects ECC SBEs when reading TX data from CQ_DAT.
23	RW	CONFIG2_RESERVED2: Reserved.
24	RW	PARITY_ERROR_SUE_ENA: When set to 0b1, NTL drives SUE on all data transfers to CQ_DAT for a packet that has a parity error on an incoming data flit.
25	RW	DATA_POISON_SUE_ENA: When set to 0b1, NTL drives SUE on all data transfers to CQ_DAT for a packet that receives LMD = data poison.
26	RW	HDR_ARR_ECC_SUE_ENA: When set to 0b1, NTL drives SUE on all data transfers to CQ_DAT for a packet that has an ECC UE/SUE on the header information read from the RX header array.
27	RW	DAT_ARR_ECC_SUE_ENA: When set to 0b1, NTL drives SUE on all data transfers to CQ_DAT for a packet that has an ECC UE/SUE on data read from the RX data array. NTL only checks ECC on reads of the RX data array that require the NTL to update the data before sending to CQ_DAT (for example, BE flit or data flits for atomic CAS ops).
28	RW	TX_ECC_DATA_POISON_ENA: When set to 0b1, NTL sends LMD = data poison for an outgoing NVLink packet that encounters an ECC UE/SUE on data read from CQ_DAT.
29:31	RW	CONFIG2_RESERVED3: Reserved.
32	RW	PRI_STATE_MACHINE_RESET: Reset PRI state machine to idle state (debug use only).
33:63	RW	CONFIG2_RESERVED4: Reserved.

Register Name	NTL Miscellaneous Configuration 3 Register
Mnemonic	NPU.STCK0.NTL0.REGS.CONFIG3
Address	00000000050110C1 (SCOM)
Description	The NTL miscellaneous configuration 3 register is used for future control of internal NTL functions. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG3_RESERVED1: Reserved.

Register Name	NTL CERR Hold 1 Register
Mnemonic	NPU.STCK0.NTL0.REGS.CERR_HOLD1
Address	00000000050110C2 (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLRREG	NTL_HOLD1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RWX_WCLRREG	NTL_HOLD1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.

Bits	SCOM	Field Mnemonic: Description
3	RWX_WCLRREG	NTL_HOLD1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RWX_WCLRREG	NTL_HOLD1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RWX_WCLRREG	NTL_HOLD1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLRREG	NTL_HOLD1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RWX_WCLRREG	NTL_HOLD1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RWX_WCLRREG	NTL_HOLD1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RWX_WCLRREG	NTL_HOLD1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RWX_WCLRREG	NTL_HOLD1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLRREG	NTL_HOLD1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RWX_WCLRREG	NTL_HOLD1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	RWX_WCLRREG	NTL_HOLD1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RWX_WCLRREG	NTL_HOLD1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RWX_WCLRREG	NTL_HOLD1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RWX_WCLRREG	NTL_HOLD1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RWX_WCLRREG	NTL_HOLD1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLRREG	NTL_HOLD1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLRREG	NTL_HOLD1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLRREG	NTL_HOLD1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLRREG	NTL_HOLD1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLRREG	NTL_HOLD1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLRREG	NTL_HOLD1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLRREG	NTL_HOLD1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RWX_WCLRREG	NTL_HOLD1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RWX_WCLRREG	NTL_HOLD1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RWX_WCLRREG	NTL_HOLD1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RWX_WCLRREG	NTL_HOLD1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RWX_WCLRREG	NTL_HOLD1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RWX_WCLRREG	NTL_HOLD1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RWX_WCLRREG	NTL_HOLD1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RWX_WCLRREG	NTL_HOLD1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RWX_WCLRREG	NTL_HOLD1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.

Bits	SCOM	Field Mnemonic: Description
34	RWX_WCLRREG	NTL_HOLD1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RWX_WCLRREG	NTL_HOLD1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RWX_WCLRREG	NTL_HOLD1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RWX_WCLRREG	NTL_HOLD1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RWX_WCLRREG	NTL_HOLD1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RWX_WCLRREG	NTL_HOLD1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RWX_WCLRREG	NTL_HOLD1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RWX_WCLRREG	NTL_HOLD1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RWX_WCLRREG	NTL_HOLD1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RWX_WCLRREG	NTL_HOLD1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RWX_WCLRREG	NTL_HOLD1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RWX_WCLRREG	NTL_HOLD1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RWX_WCLRREG	NTL_HOLD1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RWX_WCLRREG	NTL_HOLD1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RWX_WCLRREG	NTL_HOLD1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RWX_WCLRREG	NTL_HOLD1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RWX_WCLRREG	NTL_HOLD1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLRREG	NTL_HOLD1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLRREG	NTL_HOLD1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLRREG	NTL_HOLD1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLRREG	NTL_HOLD1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLRREG	NTL_HOLD1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLRREG	NTL_HOLD1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RWX_WCLRREG	NTL_HOLD1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RWX_WCLRREG	NTL_HOLD1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RWX_WCLRREG	NTL_HOLD1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RWX_WCLRREG	NTL_HOLD1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RWX_WCLRREG	NTL_HOLD1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLRREG	NTL_HOLD1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLRREG	NTL_HOLD1_63: ERROR - NTL RX - Reserved.

Register Name	NTL CERR Mask 1 Register
Mnemonic	NPU.STCK0.NTL0.REGS.CERR_MASK1
Address	00000000050110C3 (SCOM)
Description	c_err_rpt mask latches read-only register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	ROX	NTL_MASK1_1: ERROR - NTL RX – AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	ROX	NTL_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	ROX	NTL_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	ROX	NTL_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	ROX	NTL_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	ROX	NTL_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	ROX	NTL_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	ROX	NTL_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	ROX	NTL_MASK1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	ROX	NTL_MASK1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	ROX	NTL_MASK1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	ROX	NTL_MASK1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	ROX	NTL_MASK1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	ROX	NTL_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	ROX	NTL_MASK1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	ROX	NTL_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	ROX	NTL_MASK1_17: ERROR - NTL RX - Reserved.
18	ROX	NTL_MASK1_18: ERROR - NTL RX - Reserved.
19	ROX	NTL_MASK1_19: ERROR - NTL RX - Reserved.
20	ROX	NTL_MASK1_20: ERROR - NTL RX - Reserved.

Bits	SCOM	Field Mnemonic: Description
21	ROX	NTL_MASK1_21: ERROR - NTL RX - Reserved.
22	ROX	NTL_MASK1_22: ERROR - NTL RX - Reserved.
23	ROX	NTL_MASK1_23: ERROR - NTL RX - Reserved.
24	ROX	NTL_MASK1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	ROX	NTL_MASK1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	ROX	NTL_MASK1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	ROX	NTL_MASK1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	ROX	NTL_MASK1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	ROX	NTL_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	ROX	NTL_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	ROX	NTL_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	ROX	NTL_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	ROX	NTL_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	ROX	NTL_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	ROX	NTL_MASK1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	ROX	NTL_MASK1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	ROX	NTL_MASK1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	ROX	NTL_MASK1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	ROX	NTL_MASK1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	ROX	NTL_MASK1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	ROX	NTL_MASK1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	ROX	NTL_MASK1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	ROX	NTL_MASK1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	ROX	NTL_MASK1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	ROX	NTL_MASK1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	ROX	NTL_MASK1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	ROX	NTL_MASK1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	ROX	NTL_MASK1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	ROX	NTL_MASK1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).

Bits	SCOM	Field Mnemonic: Description
50	ROX	NTL_MASK1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	ROX	NTL_MASK1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	ROX	NTL_MASK1_52: ERROR - NTL RX - Reserved.
53	ROX	NTL_MASK1_53: ERROR - NTL RX - Reserved.
54	ROX	NTL_MASK1_54: ERROR - NTL RX - Reserved.
55	ROX	NTL_MASK1_55: ERROR - NTL RX - Reserved.
56	ROX	NTL_MASK1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	ROX	NTL_MASK1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	ROX	NTL_MASK1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	ROX	NTL_MASK1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	ROX	NTL_MASK1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	ROX	NTL_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	ROX	NTL_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	ROX	NTL_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First 1 Register**
Mnemonic	NPU.STCK0.NTL0.REGS.CERR_FIRST1
Address	00000000050110C4 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLEAR	NTL_FIRST1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RWX_WCLEAR	NTL_FIRST1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RWX_WCLEAR	NTL_FIRST1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RWX_WCLEAR	NTL_FIRST1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RWX_WCLEAR	NTL_FIRST1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLEAR	NTL_FIRST1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RWX_WCLEAR	NTL_FIRST1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RWX_WCLEAR	NTL_FIRST1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RWX_WCLEAR	NTL_FIRST1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.

Bits	SCOM	Field Mnemonic: Description
10	RWX_WCLEAR	NTL_FIRST1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLEAR	NTL_FIRST1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RWX_WCLEAR	NTL_FIRST1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	RWX_WCLEAR	NTL_FIRST1_13: ERROR - NTL RX – DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RWX_WCLEAR	NTL_FIRST1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RWX_WCLEAR	NTL_FIRST1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RWX_WCLEAR	NTL_FIRST1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RWX_WCLEAR	NTL_FIRST1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLEAR	NTL_FIRST1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLEAR	NTL_FIRST1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLEAR	NTL_FIRST1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLEAR	NTL_FIRST1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLEAR	NTL_FIRST1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLEAR	NTL_FIRST1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLEAR	NTL_FIRST1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RWX_WCLEAR	NTL_FIRST1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RWX_WCLEAR	NTL_FIRST1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RWX_WCLEAR	NTL_FIRST1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RWX_WCLEAR	NTL_FIRST1_28: ERROR - NTL RX - ECC UE on ata(64:127) read from the data array.
29	RWX_WCLEAR	NTL_FIRST1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RWX_WCLEAR	NTL_FIRST1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RWX_WCLEAR	NTL_FIRST1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RWX_WCLEAR	NTL_FIRST1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RWX_WCLEAR	NTL_FIRST1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RWX_WCLEAR	NTL_FIRST1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RWX_WCLEAR	NTL_FIRST1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RWX_WCLEAR	NTL_FIRST1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RWX_WCLEAR	NTL_FIRST1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RWX_WCLEAR	NTL_FIRST1_38: ERROR - NTL RX - New RSP hader flit from NVLink received when the RSP header array is full.
39	RWX_WCLEAR	NTL_FIRST1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RWX_WCLEAR	NTL_FIRST1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.

Bits	SCOM	Field Mnemonic: Description
41	RWX_WCLEAR	NTL_FIRST1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RWX_WCLEAR	NTL_FIRST1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RWX_WCLEAR	NTL_FIRST1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RWX_WCLEAR	NTL_FIRST1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RWX_WCLEAR	NTL_FIRST1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RWX_WCLEAR	NTL_FIRST1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RWX_WCLEAR	NTL_FIRST1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RWX_WCLEAR	NTL_FIRST1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RWX_WCLEAR	NTL_FIRST1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RWX_WCLEAR	NTL_FIRST1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLEAR	NTL_FIRST1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLEAR	NTL_FIRST1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLEAR	NTL_FIRST1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLEAR	NTL_FIRST1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLEAR	NTL_FIRST1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLEAR	NTL_FIRST1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RWX_WCLEAR	NTL_FIRST1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RWX_WCLEAR	NTL_FIRST1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RWX_WCLEAR	NTL_FIRST1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RWX_WCLEAR	NTL_FIRST1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RWX_WCLEAR	NTL_FIRST1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLEAR	NTL_FIRST1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLEAR	NTL_FIRST1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First Mask 1 Register**
Mnemonic	NPU.STCK0.NTL0.REGS.CERR_FIRST_MASK1
Address	00000000050110C5 (SCOM)
Description	This register mask errors from being captured in the First-1 Error registers and the RAS Error Message registers

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.

Bits	SCOM	Field Mnemonic: Description
1	RW	NTL_FIRST_MASK1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RW	NTL_FIRST_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RW	NTL_FIRST_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RW	NTL_FIRST_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RW	NTL_FIRST_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RW	NTL_FIRST_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RW	NTL_FIRST_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RW	NTL_FIRST_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RW	NTL_FIRST_MASK1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RW	NTL_FIRST_MASK1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RW	NTL_FIRST_MASK1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RW	NTL_FIRST_MASK1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	RW	NTL_FIRST_MASK1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RW	NTL_FIRST_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RW	NTL_FIRST_MASK1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RW	NTL_FIRST_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RW	NTL_FIRST_MASK1_17: ERROR - NTL RX - Reserved.
18	RW	NTL_FIRST_MASK1_18: ERROR - NTL RX - Reserved.
19	RW	NTL_FIRST_MASK1_19: ERROR - NTL RX - Reserved.
20	RW	NTL_FIRST_MASK1_20: ERROR - NTL RX - Reserved.
21	RW	NTL_FIRST_MASK1_21: ERROR - NTL RX - Reserved.
22	RW	NTL_FIRST_MASK1_22: ERROR - NTL RX - Reserved.
23	RW	NTL_FIRST_MASK1_23: ERROR - NTL RX - Reserved.
24	RW	NTL_FIRST_MASK1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RW	NTL_FIRST_MASK1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RW	NTL_FIRST_MASK1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RW	NTL_FIRST_MASK1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RW	NTL_FIRST_MASK1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RW	NTL_FIRST_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.

Bits	SCOM	Field Mnemonic: Description
30	RW	NTL_FIRST_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RW	NTL_FIRST_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RW	NTL_FIRST_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RW	NTL_FIRST_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RW	NTL_FIRST_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RW	NTL_FIRST_MASK1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RW	NTL_FIRST_MASK1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RW	NTL_FIRST_MASK1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RW	NTL_FIRST_MASK1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RW	NTL_FIRST_MASK1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RW	NTL_FIRST_MASK1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RW	NTL_FIRST_MASK1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RW	NTL_FIRST_MASK1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RW	NTL_FIRST_MASK1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RW	NTL_FIRST_MASK1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RW	NTL_FIRST_MASK1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RW	NTL_FIRST_MASK1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RW	NTL_FIRST_MASK1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RW	NTL_FIRST_MASK1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RW	NTL_FIRST_MASK1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RW	NTL_FIRST_MASK1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RW	NTL_FIRST_MASK1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RW	NTL_FIRST_MASK1_52: ERROR - NTL RX - Reserved.
53	RW	NTL_FIRST_MASK1_53: ERROR - NTL RX - Reserved.
54	RW	NTL_FIRST_MASK1_54: ERROR - NTL RX - Reserved.
55	RW	NTL_FIRST_MASK1_55: ERROR - NTL RX - Reserved.
56	RW	NTL_FIRST_MASK1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RW	NTL_FIRST_MASK1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.

Bits	SCOM	Field Mnemonic: Description
58	RW	NTL_FIRST_MASK1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RW	NTL_FIRST_MASK1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RW	NTL_FIRST_MASK1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RW	NTL_FIRST_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RW	NTL_FIRST_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RW	NTL_FIRST_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR Hold 2 Register**
Mnemonic	NPU.STCK0.NTL0.REGS.CERR_HOLD2
Address	00000000050110C6 (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RWX_WCLRREG	NTL_HOLD2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RWX_WCLRREG	NTL_HOLD2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RWX_WCLRREG	NTL_HOLD2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RWX_WCLRREG	NTL_HOLD2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RWX_WCLRREG	NTL_HOLD2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RWX_WCLRREG	NTL_HOLD2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLRREG	NTL_HOLD2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLRREG	NTL_HOLD2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLRREG	NTL_HOLD2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLRREG	NTL_HOLD2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLRREG	NTL_HOLD2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLRREG	NTL_HOLD2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLRREG	NTL_HOLD2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RWX_WCLRREG	NTL_HOLD2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RWX_WCLRREG	NTL_HOLD2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLRREG	NTL_HOLD2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLRREG	NTL_HOLD2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLRREG	NTL_HOLD2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLRREG	NTL_HOLD2_19: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
20	RWX_WCLRREG	NTL_HOLD2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLRREG	NTL_HOLD2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLRREG	NTL_HOLD2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLRREG	NTL_HOLD2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLRREG	NTL_HOLD2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RWX_WCLRREG	NTL_HOLD2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RWX_WCLRREG	NTL_HOLD2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLRREG	NTL_HOLD2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLRREG	NTL_HOLD2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLRREG	NTL_HOLD2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLRREG	NTL_HOLD2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLRREG	NTL_HOLD2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLRREG	NTL_HOLD2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RWX_WCLRREG	NTL_HOLD2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RWX_WCLRREG	NTL_HOLD2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RWX_WCLRREG	NTL_HOLD2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RWX_WCLRREG	NTL_HOLD2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RWX_WCLRREG	NTL_HOLD2_37: ERROR - NTL REGS - RSP Data credits received from the GPU are greater than maximum value.
38	RWX_WCLRREG	NTL_HOLD2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RWX_WCLRREG	NTL_HOLD2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RWX_WCLRREG	NTL_HOLD2_40: ERROR - NTL REGS - Multiple PRI requests active at the same time for different NTLs.
41	RWX_WCLRREG	NTL_HOLD2_41: ERROR - NTL REGS - Multiple PRI requests active at the same time for the same NTL.
42	RWX_WCLRREG	NTL_HOLD2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLRREG	NTL_HOLD2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLRREG	NTL_HOLD2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLRREG	NTL_HOLD2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLRREG	NTL_HOLD2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLRREG	NTL_HOLD2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLRREG	NTL_HOLD2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLRREG	NTL_HOLD2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLRREG	NTL_HOLD2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLRREG	NTL_HOLD2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLRREG	NTL_HOLD2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.

Bits	SCOM	Field Mnemonic: Description
53	RWX_WCLRREG	NTL_HOLD2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RWX_WCLRREG	NTL_HOLD2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RWX_WCLRREG	NTL_HOLD2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RWX_WCLRREG	NTL_HOLD2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RWX_WCLRREG	NTL_HOLD2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RWX_WCLRREG	NTL_HOLD2_58: ERROR - NTL REGS - PRI acknowledgment signal from the NDL wrapper went invalid in the middle of a PRI response.
59	RWX_WCLRREG	NTL_HOLD2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RWX_WCLRREG	NTL_HOLD2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLRREG	NTL_HOLD2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLRREG	NTL_HOLD2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLRREG	NTL_HOLD2_63: ERROR - NTL REGS - Reserved.

Register Name	NTL CERR Mask 2 Register
Mnemonic	NPU.STCK0.NTL0.REGS.CERR_MASK2
Address	00000000050110C7 (SCOM)
Description	c_err_rpt mask latches read-only register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	ROX	NTL_MASK2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	ROX	NTL_MASK2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	ROX	NTL_MASK2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	ROX	NTL_MASK2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	ROX	NTL_MASK2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	ROX	NTL_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	ROX	NTL_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	ROX	NTL_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	ROX	NTL_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	ROX	NTL_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	ROX	NTL_MASK2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	ROX	NTL_MASK2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	ROX	NTL_MASK2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	ROX	NTL_MASK2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	ROX	NTL_MASK2_15: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
16	ROX	NTL_MASK2_16: ERROR - NTL TX - Reserved.
17	ROX	NTL_MASK2_17: ERROR - NTL TX - Reserved.
18	ROX	NTL_MASK2_18: ERROR - NTL TX - Reserved.
19	ROX	NTL_MASK2_19: ERROR - NTL TX - Reserved.
20	ROX	NTL_MASK2_20: ERROR - NTL TX - Reserved.
21	ROX	NTL_MASK2_21: ERROR - NTL TX - Reserved.
22	ROX	NTL_MASK2_22: ERROR - NTL TX - Reserved.
23	ROX	NTL_MASK2_23: ERROR - NTL TX - Reserved.
24	ROX	NTL_MASK2_24: ERROR - NTL TX – ECC CE on data(0:63) read from CQ_DAT.
25	ROX	NTL_MASK2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	ROX	NTL_MASK2_26: ERROR - NTL TX - Reserved.
27	ROX	NTL_MASK2_27: ERROR - NTL TX - Reserved.
28	ROX	NTL_MASK2_28: ERROR - NTL TX - Reserved.
29	ROX	NTL_MASK2_29: ERROR - NTL TX - Reserved.
30	ROX	NTL_MASK2_30: ERROR - NTL TX - Reserved.
31	ROX	NTL_MASK2_31: ERROR - NTL TX - Reserved.
32	ROX	NTL_MASK2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	ROX	NTL_MASK2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	ROX	NTL_MASK2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	ROX	NTL_MASK2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	ROX	NTL_MASK2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	ROX	NTL_MASK2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	ROX	NTL_MASK2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	ROX	NTL_MASK2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	ROX	NTL_MASK2_40: ERROR - NTL REGS - Multiple PRI requests active at the same time for different NTLs.
41	ROX	NTL_MASK2_41: ERROR - NTL REGS - Multiple PRI requests active at the same time for the same NTL.
42	ROX	NTL_MASK2_42: ERROR - NTL REGS - Reserved.
43	ROX	NTL_MASK2_43: ERROR - NTL REGS - Reserved.
44	ROX	NTL_MASK2_44: ERROR - NTL REGS - Reserved.
45	ROX	NTL_MASK2_45: ERROR - NTL REGS - Reserved.
46	ROX	NTL_MASK2_46: ERROR - NTL REGS - Reserved.
47	ROX	NTL_MASK2_47: ERROR - NTL REGS - Reserved.
48	ROX	NTL_MASK2_48: ERROR - NTL REGS - Reserved.
49	ROX	NTL_MASK2_49: ERROR - NTL REGS - Reserved.
50	ROX	NTL_MASK2_50: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
51	ROX	NTL_MASK2_51: ERROR - NTL REGS - Reserved.
52	ROX	NTL_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	ROX	NTL_MASK2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	ROX	NTL_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	ROX	NTL_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	ROX	NTL_MASK2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	ROX	NTL_MASK2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	ROX	NTL_MASK2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	ROX	NTL_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	ROX	NTL_MASK2_60: ERROR - NTL REGS - Reserved.
61	ROX	NTL_MASK2_61: ERROR - NTL REGS - Reserved.
62	ROX	NTL_MASK2_62: ERROR - NTL REGS - Reserved.
63	ROX	NTL_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR First 2 Register**
Mnemonic	NPU.STCK0.NTL0.REGS.CERR_FIRST2
Address	00000000050110C8 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RWX_WCLEAR	NTL_FIRST2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RWX_WCLEAR	NTL_FIRST2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RWX_WCLEAR	NTL_FIRST2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RWX_WCLEAR	NTL_FIRST2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RWX_WCLEAR	NTL_FIRST2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RWX_WCLEAR	NTL_FIRST2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLEAR	NTL_FIRST2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLEAR	NTL_FIRST2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLEAR	NTL_FIRST2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLEAR	NTL_FIRST2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLEAR	NTL_FIRST2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLEAR	NTL_FIRST2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.

Bits	SCOM	Field Mnemonic: Description
13	RWX_WCLEAR	NTL_FIRST2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RWX_WCLEAR	NTL_FIRST2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RWX_WCLEAR	NTL_FIRST2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLEAR	NTL_FIRST2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLEAR	NTL_FIRST2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLEAR	NTL_FIRST2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLEAR	NTL_FIRST2_19: ERROR - NTL TX - Reserved.
20	RWX_WCLEAR	NTL_FIRST2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLEAR	NTL_FIRST2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLEAR	NTL_FIRST2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLEAR	NTL_FIRST2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLEAR	NTL_FIRST2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RWX_WCLEAR	NTL_FIRST2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RWX_WCLEAR	NTL_FIRST2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLEAR	NTL_FIRST2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLEAR	NTL_FIRST2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLEAR	NTL_FIRST2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLEAR	NTL_FIRST2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLEAR	NTL_FIRST2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLEAR	NTL_FIRST2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RWX_WCLEAR	NTL_FIRST2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RWX_WCLEAR	NTL_FIRST2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RWX_WCLEAR	NTL_FIRST2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RWX_WCLEAR	NTL_FIRST2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RWX_WCLEAR	NTL_FIRST2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RWX_WCLEAR	NTL_FIRST2_38: ERROR - NTL REGS - Replay bffer credits received from NDL are greater than 512.
39	RWX_WCLEAR	NTL_FIRST2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RWX_WCLEAR	NTL_FIRST2_40: ERROR - NTL REGS - Multiple PRI requests active at the same time for different NTLs.
41	RWX_WCLEAR	NTL_FIRST2_41: ERROR - NTL REGS - Multiple PRI requests active at the same time for the same NTL.
42	RWX_WCLEAR	NTL_FIRST2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLEAR	NTL_FIRST2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLEAR	NTL_FIRST2_44: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
45	RWX_WCLEAR	NTL_FIRST2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLEAR	NTL_FIRST2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLEAR	NTL_FIRST2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLEAR	NTL_FIRST2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLEAR	NTL_FIRST2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLEAR	NTL_FIRST2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLEAR	NTL_FIRST2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLEAR	NTL_FIRST2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RWX_WCLEAR	NTL_FIRST2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RWX_WCLEAR	NTL_FIRST2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RWX_WCLEAR	NTL_FIRST2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RWX_WCLEAR	NTL_FIRST2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RWX_WCLEAR	NTL_FIRST2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RWX_WCLEAR	NTL_FIRST2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RWX_WCLEAR	NTL_FIRST2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RWX_WCLEAR	NTL_FIRST2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLEAR	NTL_FIRST2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLEAR	NTL_FIRST2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLEAR	NTL_FIRST2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR First Mask 2 Register**
Mnemonic	NPU.STCK0.NTL0.REGS.CERR_FIRST_MASK2
Address	00000000050110C9 (SCOM)
Description	This register mask errors from being captured in the First-2 Error registers and the RAS Error Message registers.

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RW	NTL_FIRST_MASK2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RW	NTL_FIRST_MASK2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RW	NTL_FIRST_MASK2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RW	NTL_FIRST_MASK2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RW	NTL_FIRST_MASK2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RW	NTL_FIRST_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RW	NTL_FIRST_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RW	NTL_FIRST_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).

Bits	SCOM	Field Mnemonic: Description
9	RW	NTL_FIRST_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RW	NTL_FIRST_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RW	NTL_FIRST_MASK2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	RW	NTL_FIRST_MASK2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RW	NTL_FIRST_MASK2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RW	NTL_FIRST_MASK2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RW	NTL_FIRST_MASK2_15: ERROR - NTL TX - Reserved.
16	RW	NTL_FIRST_MASK2_16: ERROR - NTL TX - Reserved.
17	RW	NTL_FIRST_MASK2_17: ERROR - NTL TX - Reserved.
18	RW	NTL_FIRST_MASK2_18: ERROR - NTL TX - Reserved.
19	RW	NTL_FIRST_MASK2_19: ERROR - NTL TX - Reserved.
20	RW	NTL_FIRST_MASK2_20: ERROR - NTL TX - Reserved.
21	RW	NTL_FIRST_MASK2_21: ERROR - NTL TX - Reserved.
22	RW	NTL_FIRST_MASK2_22: ERROR - NTL TX - Reserved.
23	RW	NTL_FIRST_MASK2_23: ERROR - NTL TX - Reserved.
24	RW	NTL_FIRST_MASK2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RW	NTL_FIRST_MASK2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RW	NTL_FIRST_MASK2_26: ERROR - NTL TX - Reserved.
27	RW	NTL_FIRST_MASK2_27: ERROR - NTL TX - Reserved.
28	RW	NTL_FIRST_MASK2_28: ERROR - NTL TX - Reserved.
29	RW	NTL_FIRST_MASK2_29: ERROR - NTL TX - Reserved.
30	RW	NTL_FIRST_MASK2_30: ERROR - NTL TX - Reserved.
31	RW	NTL_FIRST_MASK2_31: ERROR - NTL TX - Reserved.
32	RW	NTL_FIRST_MASK2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RW	NTL_FIRST_MASK2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RW	NTL_FIRST_MASK2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RW	NTL_FIRST_MASK2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RW	NTL_FIRST_MASK2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RW	NTL_FIRST_MASK2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RW	NTL_FIRST_MASK2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.

Bits	SCOM	Field Mnemonic: Description
39	RW	NTL_FIRST_MASK2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RW	NTL_FIRST_MASK2_40: ERROR - NTL REGS - Multiple PRI requests active at the same time for different NTLs.
41	RW	NTL_FIRST_MASK2_41: ERROR - NTL REGS - Multiple PRI requests active at the same time for the same NTL.
42	RW	NTL_FIRST_MASK2_42: ERROR - NTL REGS - Reserved.
43	RW	NTL_FIRST_MASK2_43: ERROR - NTL REGS - Reserved.
44	RW	NTL_FIRST_MASK2_44: ERROR - NTL REGS - Reserved.
45	RW	NTL_FIRST_MASK2_45: ERROR - NTL REGS - Reserved.
46	RW	NTL_FIRST_MASK2_46: ERROR - NTL REGS - Reserved.
47	RW	NTL_FIRST_MASK2_47: ERROR - NTL REGS - Reserved.
48	RW	NTL_FIRST_MASK2_48: ERROR - NTL REGS - Reserved.
49	RW	NTL_FIRST_MASK2_49: ERROR - NTL REGS - Reserved.
50	RW	NTL_FIRST_MASK2_50: ERROR - NTL REGS - Reserved.
51	RW	NTL_FIRST_MASK2_51: ERROR - NTL REGS - Reserved.
52	RW	NTL_FIRST_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RW	NTL_FIRST_MASK2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RW	NTL_FIRST_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RW	NTL_FIRST_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RW	NTL_FIRST_MASK2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RW	NTL_FIRST_MASK2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RW	NTL_FIRST_MASK2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RW	NTL_FIRST_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RW	NTL_FIRST_MASK2_60: ERROR - NTL REGS - Reserved.
61	RW	NTL_FIRST_MASK2_61: ERROR - NTL REGS - Reserved.
62	RW	NTL_FIRST_MASK2_62: ERROR - NTL REGS - Reserved.
63	RW	NTL_FIRST_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	NTL Scratch 2 Register
Mnemonic	NPU.STCK0.NTL0.REGS.SCRATCH2
Address	00000000050110CA (SCOM)
Description	The NTL Scratch 2 register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH2: Scratch register.

Register Name	NTL Scratch 3 Register
Mnemonic	NPU.STCK0.NTL0.REGS.SCRATCH3
Address	00000000050110CB (SCOM)
Description	The NTL Scratch 3 register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH3: Scratch register.

Register Name	NTL Debug0 Configuration Register
Mnemonic	NPU.STCK0.NTL0.REGS.DEBUG0_CONFIG
Address	00000000050110CC (SCOM)
Description	The NTL Debug Trace 0 Configuration register is used to configure what debug information is sent on the debug trace 0 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of debug trace 0: 0x00 = Debug trace 0 byte 0 inputs. 0x01 = Debug trace 0 byte 1 inputs. 0x02 = Debug trace 0 byte 2 inputs. 0x03 = Debug trace 0 byte 3 inputs. 0x04 = Debug trace 0 byte 4 inputs. 0x05 = Debug trace 0 byte 5 inputs. 0x06 = Debug trace 0 byte 6 inputs. 0x07 = Debug trace 0 byte 7 inputs. 0x08 = Debug trace 0 byte 8 inputs. 0x09 = Debug trace 0 byte 9 inputs. 0x0A = Debug trace 0 byte 10 inputs. 0x0B = RX debug group 0. 0x0C = RX debug group 1. 0x0D = RX debug group 2. 0x0E = RX debug group 3. 0x0F = RX debug group 4. 0x10 = RX debug group 5. 0x11 = RX debug group 6. 0x12 = RX debug group 7. 0x13 = RX debug group 8. 0x14 = TX debug group 0. 0x15 = TX debug group 1. 0x16 = TX debug group 2. 0x17 = TX debug group 3. 0x18 = TX debug group 4. 0x19 = TX debug group 5. 0x1A = TX debug group 6. 0x1B = REGS debug group 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of debug trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of debug trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of debug trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of debug trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of debug trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of debug trace 0.

Bits	SCOM	Field Mnemonic: Description
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of debug trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of debug trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of debug trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of debug trace 0.
55:62	RW	DEBUG0_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	**NTL Debug1 Configuration Register**
Mnemonic	NPU.STCK0.NTL0.REGS.DEBUG1_CONFIG
Address	00000000050110CD (SCOM)
Description	The NTL Debug Trace 1 Configuration register is used to configure what debug information is sent on the debug trace 1 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of debug trace 1: 0x00 = Debug trace 1 byte 0 inputs. 0x01 = Debug trace 1 byte 1 inputs. 0x02 = Debug trace 1 byte 2 inputs. 0x03 = Debug trace 1 byte 3 inputs. 0x04 = Debug trace 1 byte 4 inputs. 0x05 = Debug trace 1 byte 5 inputs. 0x06 = Debug trace 1 byte 6 inputs. 0x07 = Debug trace 1 byte 7 inputs. 0x08 = Debug trace 1 byte 8 inputs. 0x09 = Debug trace 1 byte 9 inputs. 0x0A = Debug trace 1 byte 10 inputs. 0x0B = RX debug group 0. 0x0C = RX debug group 1. 0x0D = RX debug group 2. 0x0E = RX debug group 3. 0x0F = RX debug group 4. 0x10 = RX debug group 5. 0x11 = RX debug group 6. 0x12 = RX debug group 7. 0x13 = RX debug group 8. 0x14 = TX debug group 0. 0x15 = TX debug group 1. 0x16 = TX debug group 2. 0x17 = TX debug group 3. 0x18 = TX debug group 4. 0x19 = TX debug group 5. 0x1A = TX debug group 6. 0x1B = REGS debug group 0.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of debug trace 1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of debug trace 1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of debug trace 1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of debug trace 1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of debug trace 1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of debug trace 1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of debug trace 1.

Bits	SCOM	Field Mnemonic: Description
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of debug trace 1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of debug trace 1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of debug trace 1.
55:62	RW	DEBUG1_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	**NTL Performance Configuration Register**
Mnemonic	NPU.STCK0.NTL0.REGS.PERF_CONFIG
Address	00000000050110CE (SCOM)
Description	The NTL Performance Configuration register is used to configure what information is counted by the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: PMULet enable (clocks enable).
1	RW	PERF_CONFIG_RESETMODE: 0 = Reset on read. 1 = Reset on write.
2	RW	PERF_CONFIG_FREEZEMODE: 0 = Free run mode. 1 = Freeze on any maximum.
3	RW	PERF_CONFIG_DISABLE_PMISC: 0 = Enable PMISC control of counters. 1 = Disable PMISC control of counters.
4	RW	PERF_CONFIG_PMISC_MODE: 0 = Global PMU PMISC no reset. 1 = Global PMU PMISC reset on enable.
5:7	RW	PERF_CONFIG_CASCADE: PMULet cascade configuration.
8:9	RW	PERF_CONFIG_PRESCALE_C0: Prescale configuration for counter 0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: Prescale configuration for counter 1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: Prescale configuration for counter 2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: Prescale configuration for counter 3.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select: 0x00 = Disable. 0x01 = Cycles. 0x02 = Latency events. 0x03 = Latency cycles. 0x04 = Latency aborts. 0x20 = REGS - NDL PRI request. 0x21 = REGS - NDL PRI write request. 0x22 = REGS - NDL PRI read request. 0x23 = REGS - PHY PRI request. 0x24 = REGS - PHY PRI write request. 0x25 = REGS - PHY PRI read request. 0x40 = TX - Any flit sent. 0x41 = TX - Header flit sent. 0x42 = TX - AE flit sent.

Bits	SCOM	Field Mnemonic: Description
		0x43 = TX - BE flit sent. 0x44 = TX - Data flit sent. 0x45 = TX - Flow control packet. 0x46 = TX - Write.NC. 0x47 = TX - Write.NC 128B. 0x48 = TX - Write.NC 32B - 96B. 0x49 = TX - Write.NC 1B -16B. 0x4A = TX - Write.NC with BE flit. 0x4B = TX - Read. 0x4C = TX - Upgrade. 0x4D = TX - Atomic. 0x4E = TX - Downgrade. 0x4F = TX - ATSD. 0x50 = TX - Request response no data. 0x51 = TX - Request response with data. 0x52 = TX - Probe response no data. 0x53 = TX - Probe response with data. 0x54 = TX - ATR response. 0x55 = TX - TransDone response no data. 0x56 = TX - TransDone response with data. 0x57 = TX - TransDone response with data 128B. 0x58 = TX - TransDone response with data 32B - 96B. 0x59 = TX - TransDone response with data 1B - 16B. 0x5A = TX - TransDone response with data with BE flit. 0x5B = TX - Not enough CREQ header credits. 0x5C = TX - Not enough DGD header credits. 0x5D = TX - Not enough ATSD header credits. 0x5E = TX - Not enough RSP header credits. 0x5F = TX - Not enough CREQ data credits. 0x60 = TX - Not enough RSP data credits. 0x61 = TX - Not enough replay buffer credits. 0x62 = TX - Not enough asynchronous buffer credits. 0x80 = RX - CREQ header array full. 0x81 = RX - PRB header array full. 0x82 = RX - ATR header array full. 0x83 = RX - RSP header array full. 0x84 = RX - CREQ data array full. 0x85 = RX - RSP data array full. 0x86 = RX - Any flit received. 0x87 = RX - Header flit received. 0x88 = RX - AE flit received. 0x89 = RX - BE flit received. 0x8A = RX - Data flit received. 0x8B = RX - NOP flow control flit received. 0x8C = RX - Write.NC (UT = 0). 0x8D = RX - Write.NC (UT = 1). 0x8E = RX - Write.NC (UT = 0) 128B. 0x8F = RX - Write.NC (UT = 1) 128B. 0x90 = RX - Write.NC (UT = 0) 256B. 0x91 = RX - Write.NC (UT = 1) 256B. 0x92 = RX - Write.NC (UT = 0) 32B - 96B. 0x93 = RX - Write.NC (UT = 1) 32B - 96B. 0x94 = RX - Write.NC (UT = 0) 1B -16B. 0x95 = RX - Write.NC (UT = 1) 1B -16B. 0x96 = RX - Write.NC (UT = 0) with BE flit. 0x97 = RX - Write.NC (UT = 1) with BE flit. 0x98 = RX - Write.NC (UT = 0) to MMIO space. 0x99 = RX - Write.NC (UT = 0) to MMIO space and split into multiple requests. 0x9A = RX - Write.NC (UT = 1) and split into multiple requests. 0x9B = RX - Read.NC (UT = 0).

Bits	SCOM	Field Mnemonic: Description
		0x9C = RX - Read.NC (UT = 1). 0x9D = RX - Read.NC (UT = 0) 128B. 0x9E = RX - Read.NC (UT = 1) 128B. 0x9F = RX - Read.NC (UT = 0) 256B. 0xA0 = RX - Read.NC (UT = 1) 256B. 0xA1 = RX - Read.NC (UT = 0) 32B - 96B. 0xA2 = RX - Read.NC (UT = 1) 32B - 96B. 0xA3 = RX - Read.NC (UT = 0) 1B - 16B. 0xA4 = RX - Read.NC (UT = 1) 1B - 16B. 0xA5 = RX - Flush. 0xA6 = RX - RMW. 0xA7 = RX - Atomic.NR. 0xA8 = RX - Atomic.RR. 0xA9 = RX - Probe.I.MO. 0xAA = RX - Probe.I.N. 0xAB = RX - Probe.X.MO. 0xAC = RX - ATR. 0xAD = RX - ReqRsp.ND. 0xAE = RX - ReqRsp.D. 0xAF = RX - DGDRsp. 0xB0 = RX - ATSDRsp. 0xB1 = RX - TransDone.ND. 0xB2 = RX - TransDone.D. 0xB3 = RX - TransDone.D with BE flit. 0xB4 = RX - CREQ non-flush waiting for CQ credit. 0xB5 = RX - CREQ flush waiting for CQ credit. 0xB6 = RX - CREQ waiting for global credit. 0xB7 = RX - CREQ 256B OP waiting for 256B Ops CAM entry. 0xB8 = RX - PRB waiting for CQ credit. 0xB9 = RX - PRB waiting for global credit. 0xBA = RX - ATR waiting for CQ credit. 0xBB = RX - ATR waiting for global credit.
24:31	RW	PERF_CONFIG_EVENT1: Event 1 select (see Event 0 select for encodes).
32:39	RW	PERF_CONFIG_EVENT2: Event 2 select (see Event 0 select for encodes).
40:47	RW	PERF_CONFIG_EVENT3: Event 3 select (see Event 0 select for encodes).
48:50	RW	PERF_CONFIG_LATENCY: Latency select: 0 = Disable. 1 = Read.NC to response. 2 = Write.RR to response. 3 = Atomic.RR to response. 4 = RMW to response. 5 = Flush to response. 6 = Probe to response. 7 = ATR to response.
51:63	RW	PERF_CONFIG_RESERVED: Reserved.

Register Name	**NTL Performance Count Register**
Mnemonic	NPU.STCK0.NTL0.REGS.PERF_COUNT
Address	00000000050110CF (SCOM)
Description	The NTL Performance Count register holds the performance counts from the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	IDIAL_PERF_COUNT0: Performance counter 0.

Bits	SCOM	Field Mnemonic: Description
16:31	RWX_WCLRREG	IDIAL_PERF_COUNT1: Performance counter 1.
32:47	RWX_WCLRREG	IDIAL_PERF_COUNT2: Performance counter 2.
48:63	RWX_WCLRREG	IDIAL_PERF_COUNT3: Performance counter 3.

Register Name	NTL CREQ Header Array Pointer Register
Mnemonic	NPU.STCK0.NTL0.REGS.CREQ_HA_PTR
Address	00000000050110D0 (SCOM)
Description	The NTL CREQ Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding CREQ header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	CREQ_HA_PTR_RESERVED1: Reserved.
5:11	RW	CREQ_HA_PTR_START: Starting header array location for CREQ headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	CREQ_HA_PTR_RESERVED2: Reserved.
17:23	RW	CREQ_HA_PTR_END: Ending header array location for CREQ headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL PRB Header Array Pointer Register
Mnemonic	NPU.STCK0.NTL0.REGS.PRB_HA_PTR
Address	00000000050110D1 (SCOM)
Description	The NTL PRB Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding PRB header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	PRB_HA_PTR_RESERVED1: Reserved.
5:11	RW	PRB_HA_PTR_START: Starting header array location for PRB headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	PRB_HA_PTR_RESERVED2: Reserved.
17:23	RW	PRB_HA_PTR_END: Ending header array location for PRB headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL ATR Header Array Pointer Register
Mnemonic	NPU.STCK0.NTL0.REGS.ATR_HA_PTR
Address	00000000050110D2 (SCOM)
Description	The NTL ATR Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding ATR header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	ATR_HA_PTR_RESERVED1: Reserved.
5:11	RW	ATR_HA_PTR_START: Starting header array location for ATR headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	ATR_HA_PTR_RESERVED2: Reserved.
17:23	RW	ATR_HA_PTR_END: Ending header array location for ATR headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Header Array Pointer Register
Mnemonic	NPU.STCK0.NTL0.REGS.RSP_HA_PTR
Address	00000000050110D3 (SCOM)
Description	The NTL RSP Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding RSP header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	RSP_HA_PTR_RESERVED1: Reserved.
5:11	RW	RSP_HA_PTR_START: Starting header array location for RSP headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	RSP_HA_PTR_RESERVED2: Reserved.
17:23	RW	RSP_HA_PTR_END: Ending header array location for RSP headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL CREQ Data Array Pointer Register
Mnemonic	NPU.STCK0.NTL0.REGS.CREQ_DA_PTR
Address	00000000050110D4 (SCOM)
Description	The NTL CREQ Data Array Pointer register is used to change the start and/or end entry in the NTL data array for holding CREQ data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	CREQ_DA_PTR_RESERVED1: Reserved.
3:11	RW	CREQ_DA_PTR_START: Starting data array location for CREQ data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	CREQ_DA_PTR_RESERVED2: Reserved.
15:23	RW	CREQ_DA_PTR_END: Ending data array location for CREQ data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Data Array Pointer Register
Mnemonic	NPU.STCK0.NTL0.REGS.RSP_DA_PTR
Address	00000000050110D5 (SCOM)
Description	The NTL RSP Data Array Pointer register is used to change the start and/or end entry in the NTL data array for holding RSP data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	RSP_DA_PTR_RESERVED1: Reserved.
3:11	RW	RSP_DA_PTR_START: Starting data array location for RSP data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	RSP_DA_PTR_RESERVED2: Reserved.
15:23	RW	RSP_DA_PTR_END: Ending data array location for RSP data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL Private Register Interface (PRI) Configuration Register
Mnemonic	NPU.STCK0.NTL0.REGS.PRI_CONFIG
Address	00000000050110D6 (SCOM)
Description	The NTL Private Register Interface (PRI) Configuration register is used to set up the PRI settings for this NTL. **Note:** This register must be configured before any PRI requests are attempted to NDL or PHY registers.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PRI_CONFIG_NDL: NDL indication sent in the PRI read/write access: 00 = NDL 0. 01 = NDL 1. 10 = NDL 2. 11 = Disable (this disables the NTL from decoding the NDL register space).
2:3	RW	PRI_CONFIG_PHY: Indicates if this NTL should decode a PHY register space: 00 = Decode PHY0 register space (only one NTL that is connected to PHY 0 must be set to this value). 01 = Decode PHY1 register space (only one NTL that is connected to PHY 1 must be set to this value). 1X = Do not decode any PHY register space.
4:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	NTL Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK0.NTL0.REGS.CONFIG1
Address	00000000050110D8 (SCOM)
Description	The NVLink transaction layer (NTL) Miscellaneous Configuration 1 register is used to control NVLink packet formatting by the POWER9 processor. It also controls resetting of the POWER9 NTL.

Bits	SCOM	Field Mnemonic: Description
0	RW	COMPRESSED_RSP_ENA: When set to 0b1, NTL attempts to compress responses that it sends to the GPU whenever possible.
1:3	RW	CONFIG1_RESERVED1: Reserved.

Bits	SCOM	Field Mnemonic: Description
4	RW	CREQ_AE_ALWAYS: When set to 0b1, NTL always sends an AE flit when it sends a CREQ packet to the GPU.
5	RW	DGD_AE_ALWAYS: When set to 0b1, NTL always sends an AE flit when it sends a downgrade packet to the GPU.
6	RW	RSP_AE_ALWAYS: When set to 0b1, NTL always sends an AE flit when it sends a response packet to the GPU.
7	RW	CONFIG1_RESERVED2: Reserved.
8:9	RW	NTL_RESET: This field indicates the NTL Reset mode: 00 = Reset disabled. 11 = Reset (fence) both NTL and the processor bus for this brick. 10 = Reset (fence) only the processor bus for this brick, the NTL is operational. 01 = Reserved. **Note:** The only legal sequence is 00 →11 →10 →00. This field should not be changed unless bits 0:1 in the CQ Fence Status register equals the value in this field.
10:63	RW	CONFIG1_RESERVED3: Reserved.

Register Name	NTL Scratch 1 Register
Mnemonic	NPU.STCK0.NTL0.REGS.SCRATCH1
Address	00000000050110DA (SCOM)
Description	The NTL Scratch 1 register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH1: Scratch register.

Register Name	NTL Low Power Configuration Register
Mnemonic	NPU.STCK0.NTL0.REGS.LOW_PWR
Address	00000000050110DC (SCOM)
Description	The NTL Low Power Configuration register is used to enable the NPU to request that the NVLink interconnect be placed into low-power mode. The register also defines the conditions under which the NPU turns its low-power request on or off.

Bits	SCOM	Field Mnemonic: Description
0	RW	LP_MODE_ENABLE: When set to 0b1, this NTL is allowed to activate the low-power requested signal to NDL when the low-power count is less than or equal to the low-power count threshold.
1	RW	LP_ONLY_MODE: When set to 0b1, this NTL activates the low-power requested signal to NDL continuously. This can be used for lab stress or debug.
2:7	RW	LP_TIMER_TICK_CONFIG: Rate for the low-power timer tick (2^n cycles).
8:19	RW	LP_MIN_CRED_THRESH: Whenever the NDL replay buffer credits is less than this threshold, the low-power requested signal to NDL is deactivated. This value must be greater than 0 and less than the maximum credit threshold.
20:31	RW	LP_MAX_CRED_THRESH: Whenever the NDL replay buffer credits is greater than or equal to this threshold and the low-power timer tick is active, then the low-power count is incremented by 1. This value must be greater than the minimum credit threshold.

Bits	SCOM	Field Mnemonic: Description
32:43	RW	LP_CNT_THRESH: Whenever the low-power count is greater than or equal to this threshold, this NTL activates the low-power requested signal to NDL until the NDL replay buffer credits is less than the low-power minimum credit threshold. This value must be greater than 0.
44:63	RO	Constant = 0b00000000000000000000

Register Name	NTL Miscellaneous Configuration 2 Register
Mnemonic	NPU.STCK0.NTL1.REGS.CONFIG2
Address	00000000050110E0 (SCOM)
Description	The NTL Miscellaneous Configuration 2 register is used to control internal NTL function. It contains mode bits, chicken switches, and thresholds.

Bits	SCOM	Field Mnemonic: Description
0	RW	BRICK_ENABLE: When set to 0b1, this NVLink brick is enabled. This configuration bit is used as a general clock gate for latches in the NTL design.
1	RW	RSP_CTL_CRED_SINGLE_ENA: When set to 0b1, NTL only gives CQ_CTL one RSP credit at a time, instead of the normal two.
2	RW	CREQ_BE_128: When set to 0b1, NTL always sends 128 bytes of data when it needs to send a byte enable (BE) flit to the GPU for a CREQ packet. When set to 0b0, NTL sends the least number of data flits required.
3	RW	DGD_BE_128: When set to 0b1, NTL always sends 128 bytes of data when it needs to send a byte enable (BE) flit to the GPU for a downgrade packet (BE and data flits are sent in the TransDone packet for the downgrade). When set to 0b0, NTL sends the least number of data flits required.
4	RW	WR_SPLIT_UT0_ENA: When set to 0b1, NTL splits up write requests with UT = 0 from the GPU that map to MMIO space into legal processor bus sizes/alignments. When set to 0b0, NTL passes all write requests with UT = 0 as is to CQ.
5	RW	WR_SPLIT_UT1_ENA: When set to 0b1, NTL splits up write requests with UT = 1 from the GPU into legal processor bus sizes/alignments. This includes both DMA writes and MMIO writes since there is no way for NTL to distinguish between them. When set to 0b0, NTL passes all write requests with UT = 1 as is to CQ.
6	RW	BRICK_DEBUG_MODE: When set to 0b1, NTL ignores all incoming NVLink packets from the GPU and throws away all NVLink requests/responses from CQ destined for the GPU. This mode is used for debug purposes only when the NPU is not connected over NVLink to a GPU.
7	RW	P9_TO_P9_MODE: When set to 0b1, NTL sets UT = 1 for all incoming read, write, and atomic NVLink packets before sending to CQ. This mode is used for debug purposes only when the NPU is connected to another/same NPU over NVLink.
8:9	RW	CONFIG2_RESERVED1: Reserved.
10:15	RW	CAM256_MAX_CNT: This field specifies the number of entries in the CAM that holds information to send responses for 256 byte operations that require a response (maximum value = 48).
16	RW	NDL_RX_PARITY_ENA: When set to 0b1, NTL checks the parity on the incoming NDL RX signals.
17	RW	NDL_TX_PARITY_ENA: When set to 0b1, NTL check the parity on the incoming NDL TX (that is, TX credits) signals.
18	RW	NDL_PRI_PARITY_ENA: When set to 0b1, NTL checks the parity on the incoming NDL signals.
19	RW	RCV_CREDIT_OVERFLOW_ENA: When set to 0b1, NTL checks for overflows on any received credits from the GPU, NDL, and NDL wrapper.
20	RW	HDR_ARR_ECC_CORR_ENA: When set to 0b1, NTL correctw ECC SBEs when reading the RX header array.
21	RW	DAT_ARR_ECC_CORR_ENA: When set to 0b1, NTL corrects ECC SBEs when reading the RX data array. NTL only corrects ECC on reads of the RX data array that require NTL to update the data before sending to CQ_DAT (for example, BE flit or data flits for atomic CAS ops).

Bits	SCOM	Field Mnemonic: Description
22	RW	TX_DATA_ECC_CORR_ENA: When set to 0b1, NTL corrects ECC SBEs when reading TX data from CQ_DAT.
23	RW	CONFIG2_RESERVED2: Reserved.
24	RW	PARITY_ERROR_SUE_ENA: When set to 0b1, NTL drives SUE on all data transfers to CQ_DAT for a packet that has a parity error on an incoming data flit.
25	RW	DATA_POISON_SUE_ENA: When set to 0b1, NTL drives SUE on all data transfers to CQ_DAT for a packet that receives LMD = data poison.
26	RW	HDR_ARR_ECC_SUE_ENA: When set to 0b1, NTL drives SUE on all data transfers to CQ_DAT for a packet that has an ECC UE/SUE on the header information read from the RX header array.
27	RW	DAT_ARR_ECC_SUE_ENA: When set to 0b1, NTL drives SUE on all data transfers to CQ_DAT for a packet that has an ECC UE/SUE on data read from the RX data array. NTL only checks ECC on reads of the RX data array that requires NTL to update the data before sending to CQ_DAT (for example, BE flit or data flits for atomic CAS ops).
28	RW	TX_ECC_DATA_POISON_ENA: When set to 0b1, NTL sends LMD = data poison for an outgoing NVLink packet that encounters an ECC UE/SUE on data read from CQ_DAT.
29:31	RW	CONFIG2_RESERVED3: Reserved.
32	RW	PRI_STATE_MACHINE_RESET: Reset PRI state machine to idle state (debug use only).
33:63	RW	CONFIG2_RESERVED4: Reserved.

Register Name	NTL Miscellaneous Configuration 3 Register
Mnemonic	NPU.STCK0.NTL1.REGS.CONFIG3
Address	00000000050110E1 (SCOM)
Description	The NTL Miscellaneous Configuration 3 Register is used for future control of internal NTL functions. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG3_RESERVED1: Reserved.

Register Name	NTL CERR Hold 1 Register
Mnemonic	NPU.STCK0.NTL1.REGS.CERR_HOLD1
Address	00000000050110E2 (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLRREG	NTL_HOLD1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RWX_WCLRREG	NTL_HOLD1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RWX_WCLRREG	NTL_HOLD1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RWX_WCLRREG	NTL_HOLD1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.

Bits	SCOM	Field Mnemonic: Description
5	RWX_WCLRREG	NTL_HOLD1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLRREG	NTL_HOLD1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RWX_WCLRREG	NTL_HOLD1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RWX_WCLRREG	NTL_HOLD1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RWX_WCLRREG	NTL_HOLD1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RWX_WCLRREG	NTL_HOLD1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLRREG	NTL_HOLD1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RWX_WCLRREG	NTL_HOLD1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	RWX_WCLRREG	NTL_HOLD1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RWX_WCLRREG	NTL_HOLD1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RWX_WCLRREG	NTL_HOLD1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RWX_WCLRREG	NTL_HOLD1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RWX_WCLRREG	NTL_HOLD1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLRREG	NTL_HOLD1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLRREG	NTL_HOLD1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLRREG	NTL_HOLD1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLRREG	NTL_HOLD1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLRREG	NTL_HOLD1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLRREG	NTL_HOLD1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLRREG	NTL_HOLD1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RWX_WCLRREG	NTL_HOLD1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RWX_WCLRREG	NTL_HOLD1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RWX_WCLRREG	NTL_HOLD1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RWX_WCLRREG	NTL_HOLD1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RWX_WCLRREG	NTL_HOLD1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RWX_WCLRREG	NTL_HOLD1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RWX_WCLRREG	NTL_HOLD1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RWX_WCLRREG	NTL_HOLD1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RWX_WCLRREG	NTL_HOLD1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RWX_WCLRREG	NTL_HOLD1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RWX_WCLRREG	NTL_HOLD1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.

Bits	SCOM	Field Mnemonic: Description
36	RWX_WCLRREG	NTL_HOLD1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RWX_WCLRREG	NTL_HOLD1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RWX_WCLRREG	NTL_HOLD1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RWX_WCLRREG	NTL_HOLD1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RWX_WCLRREG	NTL_HOLD1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RWX_WCLRREG	NTL_HOLD1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RWX_WCLRREG	NTL_HOLD1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RWX_WCLRREG	NTL_HOLD1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RWX_WCLRREG	NTL_HOLD1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RWX_WCLRREG	NTL_HOLD1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RWX_WCLRREG	NTL_HOLD1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RWX_WCLRREG	NTL_HOLD1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RWX_WCLRREG	NTL_HOLD1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RWX_WCLRREG	NTL_HOLD1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RWX_WCLRREG	NTL_HOLD1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLRREG	NTL_HOLD1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLRREG	NTL_HOLD1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLRREG	NTL_HOLD1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLRREG	NTL_HOLD1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLRREG	NTL_HOLD1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLRREG	NTL_HOLD1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RWX_WCLRREG	NTL_HOLD1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RWX_WCLRREG	NTL_HOLD1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RWX_WCLRREG	NTL_HOLD1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RWX_WCLRREG	NTL_HOLD1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RWX_WCLRREG	NTL_HOLD1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLRREG	NTL_HOLD1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLRREG	NTL_HOLD1_63: ERROR - NTL RX - Reserved.

Register Name	NTL CERR Mask 1 Register
Mnemonic	NPU.STCK0.NTL1.REGS.CERR_MASK1
Address	00000000050110E3 (SCOM)
Description	c_err_rpt mask latches read-only register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	ROX	NTL_MASK1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	ROX	NTL_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	ROX	NTL_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	ROX	NTL_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	ROX	NTL_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	ROX	NTL_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	ROX	NTL_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	ROX	NTL_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	ROX	NTL_MASK1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	ROX	NTL_MASK1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	ROX	NTL_MASK1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	ROX	NTL_MASK1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	ROX	NTL_MASK1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	ROX	NTL_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	ROX	NTL_MASK1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	ROX	NTL_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	ROX	NTL_MASK1_17: ERROR - NTL RX - Reserved.
18	ROX	NTL_MASK1_18: ERROR - NTL RX - Reserved.
19	ROX	NTL_MASK1_19: ERROR - NTL RX - Reserved.
20	ROX	NTL_MASK1_20: ERROR - NTL RX - Reserved.
21	ROX	NTL_MASK1_21: ERROR - NTL RX - Reserved.
22	ROX	NTL_MASK1_22: ERROR - NTL RX - Reserved.
23	ROX	NTL_MASK1_23: ERROR - NTL RX - Reserved.
24	ROX	NTL_MASK1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.

Bits	SCOM	Field Mnemonic: Description
25	ROX	NTL_MASK1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	ROX	NTL_MASK1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	ROX	NTL_MASK1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	ROX	NTL_MASK1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	ROX	NTL_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	ROX	NTL_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	ROX	NTL_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	ROX	NTL_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	ROX	NTL_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	ROX	NTL_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	ROX	NTL_MASK1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	ROX	NTL_MASK1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	ROX	NTL_MASK1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	ROX	NTL_MASK1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	ROX	NTL_MASK1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	ROX	NTL_MASK1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	ROX	NTL_MASK1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	ROX	NTL_MASK1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	ROX	NTL_MASK1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	ROX	NTL_MASK1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	ROX	NTL_MASK1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	ROX	NTL_MASK1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	ROX	NTL_MASK1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	ROX	NTL_MASK1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	ROX	NTL_MASK1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	ROX	NTL_MASK1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	ROX	NTL_MASK1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	ROX	NTL_MASK1_52: ERROR - NTL RX - Reserved.

Bits	SCOM	Field Mnemonic: Description
53	ROX	NTL_MASK1_53: ERROR - NTL RX - Reserved.
54	ROX	NTL_MASK1_54: ERROR - NTL RX - Reserved.
55	ROX	NTL_MASK1_55: ERROR - NTL RX - Reserved.
56	ROX	NTL_MASK1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	ROX	NTL_MASK1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	ROX	NTL_MASK1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	ROX	NTL_MASK1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	ROX	NTL_MASK1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	ROX	NTL_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	ROX	NTL_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	ROX	NTL_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First 1 Register**
Mnemonic	NPU.STCK0.NTL1.REGS.CERR_FIRST1
Address	00000000050110E4 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLEAR	NTL_FIRST1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RWX_WCLEAR	NTL_FIRST1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RWX_WCLEAR	NTL_FIRST1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RWX_WCLEAR	NTL_FIRST1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RWX_WCLEAR	NTL_FIRST1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLEAR	NTL_FIRST1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RWX_WCLEAR	NTL_FIRST1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RWX_WCLEAR	NTL_FIRST1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RWX_WCLEAR	NTL_FIRST1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RWX_WCLEAR	NTL_FIRST1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLEAR	NTL_FIRST1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RWX_WCLEAR	NTL_FIRST1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.

Bits	SCOM	Field Mnemonic: Description
13	RWX_WCLEAR	NTL_FIRST1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RWX_WCLEAR	NTL_FIRST1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RWX_WCLEAR	NTL_FIRST1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RWX_WCLEAR	NTL_FIRST1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RWX_WCLEAR	NTL_FIRST1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLEAR	NTL_FIRST1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLEAR	NTL_FIRST1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLEAR	NTL_FIRST1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLEAR	NTL_FIRST1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLEAR	NTL_FIRST1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLEAR	NTL_FIRST1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLEAR	NTL_FIRST1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RWX_WCLEAR	NTL_FIRST1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RWX_WCLEAR	NTL_FIRST1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RWX_WCLEAR	NTL_FIRST1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RWX_WCLEAR	NTL_FIRST1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RWX_WCLEAR	NTL_FIRST1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RWX_WCLEAR	NTL_FIRST1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RWX_WCLEAR	NTL_FIRST1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RWX_WCLEAR	NTL_FIRST1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RWX_WCLEAR	NTL_FIRST1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RWX_WCLEAR	NTL_FIRST1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RWX_WCLEAR	NTL_FIRST1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RWX_WCLEAR	NTL_FIRST1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RWX_WCLEAR	NTL_FIRST1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RWX_WCLEAR	NTL_FIRST1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RWX_WCLEAR	NTL_FIRST1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RWX_WCLEAR	NTL_FIRST1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RWX_WCLEAR	NTL_FIRST1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RWX_WCLEAR	NTL_FIRST1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RWX_WCLEAR	NTL_FIRST1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.

Bits	SCOM	Field Mnemonic: Description
44	RWX_WCLEAR	NTL_FIRST1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RWX_WCLEAR	NTL_FIRST1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RWX_WCLEAR	NTL_FIRST1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RWX_WCLEAR	NTL_FIRST1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RWX_WCLEAR	NTL_FIRST1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RWX_WCLEAR	NTL_FIRST1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RWX_WCLEAR	NTL_FIRST1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLEAR	NTL_FIRST1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLEAR	NTL_FIRST1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLEAR	NTL_FIRST1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLEAR	NTL_FIRST1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLEAR	NTL_FIRST1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLEAR	NTL_FIRST1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RWX_WCLEAR	NTL_FIRST1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RWX_WCLEAR	NTL_FIRST1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RWX_WCLEAR	NTL_FIRST1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RWX_WCLEAR	NTL_FIRST1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RWX_WCLEAR	NTL_FIRST1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLEAR	NTL_FIRST1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLEAR	NTL_FIRST1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First Mask 1 Register**
Mnemonic	NPU.STCK0.NTL1.REGS.CERR_FIRST_MASK1
Address	00000000050110E5 (SCOM)
Description	This register mask errors from being captured in the First-1 Error registers and the RAS Error Message registers.

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RW	NTL_FIRST_MASK1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RW	NTL_FIRST_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RW	NTL_FIRST_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.

Bits	SCOM	Field Mnemonic: Description
4	RW	NTL_FIRST_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RW	NTL_FIRST_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RW	NTL_FIRST_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RW	NTL_FIRST_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RW	NTL_FIRST_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RW	NTL_FIRST_MASK1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RW	NTL_FIRST_MASK1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RW	NTL_FIRST_MASK1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RW	NTL_FIRST_MASK1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	RW	NTL_FIRST_MASK1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RW	NTL_FIRST_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RW	NTL_FIRST_MASK1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RW	NTL_FIRST_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RW	NTL_FIRST_MASK1_17: ERROR - NTL RX - Reserved.
18	RW	NTL_FIRST_MASK1_18: ERROR - NTL RX - Reserved.
19	RW	NTL_FIRST_MASK1_19: ERROR - NTL RX - Reserved.
20	RW	NTL_FIRST_MASK1_20: ERROR - NTL RX - Reserved.
21	RW	NTL_FIRST_MASK1_21: ERROR - NTL RX - Reserved.
22	RW	NTL_FIRST_MASK1_22: ERROR - NTL RX - Reserved.
23	RW	NTL_FIRST_MASK1_23: ERROR - NTL RX - Reserved.
24	RW	NTL_FIRST_MASK1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RW	NTL_FIRST_MASK1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RW	NTL_FIRST_MASK1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RW	NTL_FIRST_MASK1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RW	NTL_FIRST_MASK1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RW	NTL_FIRST_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RW	NTL_FIRST_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RW	NTL_FIRST_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RW	NTL_FIRST_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RW	NTL_FIRST_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RW	NTL_FIRST_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.

Bits	SCOM	Field Mnemonic: Description
35	RW	NTL_FIRST_MASK1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RW	NTL_FIRST_MASK1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RW	NTL_FIRST_MASK1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RW	NTL_FIRST_MASK1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RW	NTL_FIRST_MASK1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RW	NTL_FIRST_MASK1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RW	NTL_FIRST_MASK1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RW	NTL_FIRST_MASK1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RW	NTL_FIRST_MASK1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RW	NTL_FIRST_MASK1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RW	NTL_FIRST_MASK1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RW	NTL_FIRST_MASK1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RW	NTL_FIRST_MASK1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RW	NTL_FIRST_MASK1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RW	NTL_FIRST_MASK1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RW	NTL_FIRST_MASK1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RW	NTL_FIRST_MASK1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RW	NTL_FIRST_MASK1_52: ERROR - NTL RX - Reserved.
53	RW	NTL_FIRST_MASK1_53: ERROR - NTL RX - Reserved.
54	RW	NTL_FIRST_MASK1_54: ERROR - NTL RX - Reserved.
55	RW	NTL_FIRST_MASK1_55: ERROR - NTL RX - Reserved.
56	RW	NTL_FIRST_MASK1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RW	NTL_FIRST_MASK1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RW	NTL_FIRST_MASK1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RW	NTL_FIRST_MASK1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RW	NTL_FIRST_MASK1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RW	NTL_FIRST_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RW	NTL_FIRST_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.

Bits	SCOM	Field Mnemonic: Description
63	RW	NTL_FIRST_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR Hold 2 Register**
Mnemonic	NPU.STCK0.NTL1.REGS.CERR_HOLD2
Address	00000000050110E6 (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RWX_WCLRREG	NTL_HOLD2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RWX_WCLRREG	NTL_HOLD2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RWX_WCLRREG	NTL_HOLD2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RWX_WCLRREG	NTL_HOLD2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RWX_WCLRREG	NTL_HOLD2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RWX_WCLRREG	NTL_HOLD2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLRREG	NTL_HOLD2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLRREG	NTL_HOLD2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLRREG	NTL_HOLD2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLRREG	NTL_HOLD2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLRREG	NTL_HOLD2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLRREG	NTL_HOLD2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLRREG	NTL_HOLD2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RWX_WCLRREG	NTL_HOLD2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RWX_WCLRREG	NTL_HOLD2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLRREG	NTL_HOLD2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLRREG	NTL_HOLD2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLRREG	NTL_HOLD2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLRREG	NTL_HOLD2_19: ERROR - NTL TX - Reserved.
20	RWX_WCLRREG	NTL_HOLD2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLRREG	NTL_HOLD2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLRREG	NTL_HOLD2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLRREG	NTL_HOLD2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLRREG	NTL_HOLD2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.

Bits	SCOM	Field Mnemonic: Description
25	RWX_WCLRREG	NTL_HOLD2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RWX_WCLRREG	NTL_HOLD2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLRREG	NTL_HOLD2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLRREG	NTL_HOLD2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLRREG	NTL_HOLD2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLRREG	NTL_HOLD2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLRREG	NTL_HOLD2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLRREG	NTL_HOLD2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RWX_WCLRREG	NTL_HOLD2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RWX_WCLRREG	NTL_HOLD2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RWX_WCLRREG	NTL_HOLD2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RWX_WCLRREG	NTL_HOLD2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RWX_WCLRREG	NTL_HOLD2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RWX_WCLRREG	NTL_HOLD2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RWX_WCLRREG	NTL_HOLD2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RWX_WCLRREG	NTL_HOLD2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	RWX_WCLRREG	NTL_HOLD2_41: ERROR - NTL REGS - Multiple PRI requests active at the same time for the same NTL.
42	RWX_WCLRREG	NTL_HOLD2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLRREG	NTL_HOLD2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLRREG	NTL_HOLD2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLRREG	NTL_HOLD2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLRREG	NTL_HOLD2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLRREG	NTL_HOLD2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLRREG	NTL_HOLD2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLRREG	NTL_HOLD2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLRREG	NTL_HOLD2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLRREG	NTL_HOLD2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLRREG	NTL_HOLD2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RWX_WCLRREG	NTL_HOLD2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RWX_WCLRREG	NTL_HOLD2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RWX_WCLRREG	NTL_HOLD2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RWX_WCLRREG	NTL_HOLD2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RWX_WCLRREG	NTL_HOLD2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.

Bits	SCOM	Field Mnemonic: Description
58	RWX_WCLRREG	NTL_HOLD2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RWX_WCLRREG	NTL_HOLD2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RWX_WCLRREG	NTL_HOLD2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLRREG	NTL_HOLD2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLRREG	NTL_HOLD2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLRREG	NTL_HOLD2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR Mask 2 Register**
Mnemonic	NPU.STCK0.NTL1.REGS.CERR_MASK2
Address	00000000050110E7 (SCOM)
Description	c_err_rpt mask latches read-only register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	ROX	NTL_MASK2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	ROX	NTL_MASK2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	ROX	NTL_MASK2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	ROX	NTL_MASK2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	ROX	NTL_MASK2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	ROX	NTL_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	ROX	NTL_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	ROX	NTL_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	ROX	NTL_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	ROX	NTL_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	ROX	NTL_MASK2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	ROX	NTL_MASK2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	ROX	NTL_MASK2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	ROX	NTL_MASK2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	ROX	NTL_MASK2_15: ERROR - NTL TX - Reserved.
16	ROX	NTL_MASK2_16: ERROR - NTL TX - Reserved.
17	ROX	NTL_MASK2_17: ERROR - NTL TX - Reserved.
18	ROX	NTL_MASK2_18: ERROR - NTL TX - Reserved.
19	ROX	NTL_MASK2_19: ERROR - NTL TX - Reserved.
20	ROX	NTL_MASK2_20: ERROR - NTL TX - Reserved.
21	ROX	NTL_MASK2_21: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
22	ROX	NTL_MASK2_22: ERROR - NTL TX - Reserved.
23	ROX	NTL_MASK2_23: ERROR - NTL TX - Reserved.
24	ROX	NTL_MASK2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	ROX	NTL_MASK2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	ROX	NTL_MASK2_26: ERROR - NTL TX - Reserved.
27	ROX	NTL_MASK2_27: ERROR - NTL TX - Reserved.
28	ROX	NTL_MASK2_28: ERROR - NTL TX - Reserved.
29	ROX	NTL_MASK2_29: ERROR - NTL TX - Reserved.
30	ROX	NTL_MASK2_30: ERROR - NTL TX - Reserved.
31	ROX	NTL_MASK2_31: ERROR - NTL TX - Reserved.
32	ROX	NTL_MASK2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	ROX	NTL_MASK2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	ROX	NTL_MASK2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	ROX	NTL_MASK2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	ROX	NTL_MASK2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	ROX	NTL_MASK2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	ROX	NTL_MASK2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	ROX	NTL_MASK2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	ROX	NTL_MASK2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	ROX	NTL_MASK2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	ROX	NTL_MASK2_42: ERROR - NTL REGS - Reserved.
43	ROX	NTL_MASK2_43: ERROR - NTL REGS - Reserved.
44	ROX	NTL_MASK2_44: ERROR - NTL REGS - Reserved.
45	ROX	NTL_MASK2_45: ERROR - NTL REGS - Reserved.
46	ROX	NTL_MASK2_46: ERROR - NTL REGS - Reserved.
47	ROX	NTL_MASK2_47: ERROR - NTL REGS - Reserved.
48	ROX	NTL_MASK2_48: ERROR - NTL REGS - Reserved.
49	ROX	NTL_MASK2_49: ERROR - NTL REGS - Reserved.
50	ROX	NTL_MASK2_50: ERROR - NTL REGS - Reserved.
51	ROX	NTL_MASK2_51: ERROR - NTL REGS - Reserved.
52	ROX	NTL_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	ROX	NTL_MASK2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	ROX	NTL_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.

Bits	SCOM	Field Mnemonic: Description
55	ROX	NTL_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	ROX	NTL_MASK2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	ROX	NTL_MASK2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	ROX	NTL_MASK2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	ROX	NTL_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	ROX	NTL_MASK2_60: ERROR - NTL REGS - Reserved.
61	ROX	NTL_MASK2_61: ERROR - NTL REGS - Reserved.
62	ROX	NTL_MASK2_62: ERROR - NTL REGS - Reserved.
63	ROX	NTL_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR First 2 Register**
Mnemonic	NPU.STCK0.NTL1.REGS.CERR_FIRST2
Address	00000000050110E8 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RWX_WCLEAR	NTL_FIRST2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RWX_WCLEAR	NTL_FIRST2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RWX_WCLEAR	NTL_FIRST2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RWX_WCLEAR	NTL_FIRST2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RWX_WCLEAR	NTL_FIRST2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RWX_WCLEAR	NTL_FIRST2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLEAR	NTL_FIRST2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLEAR	NTL_FIRST2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLEAR	NTL_FIRST2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLEAR	NTL_FIRST2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLEAR	NTL_FIRST2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLEAR	NTL_FIRST2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLEAR	NTL_FIRST2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RWX_WCLEAR	NTL_FIRST2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RWX_WCLEAR	NTL_FIRST2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLEAR	NTL_FIRST2_16: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
17	RWX_WCLEAR	NTL_FIRST2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLEAR	NTL_FIRST2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLEAR	NTL_FIRST2_19: ERROR - NTL TX - Reserved.
20	RWX_WCLEAR	NTL_FIRST2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLEAR	NTL_FIRST2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLEAR	NTL_FIRST2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLEAR	NTL_FIRST2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLEAR	NTL_FIRST2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RWX_WCLEAR	NTL_FIRST2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RWX_WCLEAR	NTL_FIRST2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLEAR	NTL_FIRST2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLEAR	NTL_FIRST2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLEAR	NTL_FIRST2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLEAR	NTL_FIRST2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLEAR	NTL_FIRST2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLEAR	NTL_FIRST2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RWX_WCLEAR	NTL_FIRST2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RWX_WCLEAR	NTL_FIRST2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RWX_WCLEAR	NTL_FIRST2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RWX_WCLEAR	NTL_FIRST2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RWX_WCLEAR	NTL_FIRST2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RWX_WCLEAR	NTL_FIRST2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RWX_WCLEAR	NTL_FIRST2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RWX_WCLEAR	NTL_FIRST2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	RWX_WCLEAR	NTL_FIRST2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	RWX_WCLEAR	NTL_FIRST2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLEAR	NTL_FIRST2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLEAR	NTL_FIRST2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLEAR	NTL_FIRST2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLEAR	NTL_FIRST2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLEAR	NTL_FIRST2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLEAR	NTL_FIRST2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLEAR	NTL_FIRST2_49: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
50	RWX_WCLEAR	NTL_FIRST2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLEAR	NTL_FIRST2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLEAR	NTL_FIRST2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RWX_WCLEAR	NTL_FIRST2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RWX_WCLEAR	NTL_FIRST2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RWX_WCLEAR	NTL_FIRST2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RWX_WCLEAR	NTL_FIRST2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RWX_WCLEAR	NTL_FIRST2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RWX_WCLEAR	NTL_FIRST2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RWX_WCLEAR	NTL_FIRST2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RWX_WCLEAR	NTL_FIRST2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLEAR	NTL_FIRST2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLEAR	NTL_FIRST2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLEAR	NTL_FIRST2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR First Mask 2 Register**
Mnemonic	NPU.STCK0.NTL1.REGS.CERR_FIRST_MASK2
Address	00000000050110E9 (SCOM)
Description	This register mask errors from being captured in the First-2 Error registers and the RAS Error Message registers.

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RW	NTL_FIRST_MASK2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RW	NTL_FIRST_MASK2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RW	NTL_FIRST_MASK2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RW	NTL_FIRST_MASK2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RW	NTL_FIRST_MASK2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RW	NTL_FIRST_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RW	NTL_FIRST_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RW	NTL_FIRST_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RW	NTL_FIRST_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RW	NTL_FIRST_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RW	NTL_FIRST_MASK2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.

Bits	SCOM	Field Mnemonic: Description
12	RW	NTL_FIRST_MASK2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RW	NTL_FIRST_MASK2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RW	NTL_FIRST_MASK2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RW	NTL_FIRST_MASK2_15: ERROR - NTL TX - Reserved.
16	RW	NTL_FIRST_MASK2_16: ERROR - NTL TX - Reserved.
17	RW	NTL_FIRST_MASK2_17: ERROR - NTL TX - Reserved.
18	RW	NTL_FIRST_MASK2_18: ERROR - NTL TX - Reserved.
19	RW	NTL_FIRST_MASK2_19: ERROR - NTL TX - Reserved.
20	RW	NTL_FIRST_MASK2_20: ERROR - NTL TX - Reserved.
21	RW	NTL_FIRST_MASK2_21: ERROR - NTL TX - Reserved.
22	RW	NTL_FIRST_MASK2_22: ERROR - NTL TX - Reserved.
23	RW	NTL_FIRST_MASK2_23: ERROR - NTL TX - Reserved.
24	RW	NTL_FIRST_MASK2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RW	NTL_FIRST_MASK2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RW	NTL_FIRST_MASK2_26: ERROR - NTL TX - Reserved.
27	RW	NTL_FIRST_MASK2_27: ERROR - NTL TX - Reserved.
28	RW	NTL_FIRST_MASK2_28: ERROR - NTL TX - Reserved.
29	RW	NTL_FIRST_MASK2_29: ERROR - NTL TX - Reserved.
30	RW	NTL_FIRST_MASK2_30: ERROR - NTL TX - Reserved.
31	RW	NTL_FIRST_MASK2_31: ERROR - NTL TX - Reserved.
32	RW	NTL_FIRST_MASK2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RW	NTL_FIRST_MASK2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RW	NTL_FIRST_MASK2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RW	NTL_FIRST_MASK2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RW	NTL_FIRST_MASK2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RW	NTL_FIRST_MASK2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RW	NTL_FIRST_MASK2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RW	NTL_FIRST_MASK2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RW	NTL_FIRST_MASK2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	RW	NTL_FIRST_MASK2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	RW	NTL_FIRST_MASK2_42: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
43	RW	NTL_FIRST_MASK2_43: ERROR - NTL REGS - Reserved.
44	RW	NTL_FIRST_MASK2_44: ERROR - NTL REGS - Reserved.
45	RW	NTL_FIRST_MASK2_45: ERROR - NTL REGS - Reserved.
46	RW	NTL_FIRST_MASK2_46: ERROR - NTL REGS - Reserved.
47	RW	NTL_FIRST_MASK2_47: ERROR - NTL REGS - Reserved.
48	RW	NTL_FIRST_MASK2_48: ERROR - NTL REGS - Reserved.
49	RW	NTL_FIRST_MASK2_49: ERROR - NTL REGS - Reserved.
50	RW	NTL_FIRST_MASK2_50: ERROR - NTL REGS - Reserved.
51	RW	NTL_FIRST_MASK2_51: ERROR - NTL REGS - Reserved.
52	RW	NTL_FIRST_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RW	NTL_FIRST_MASK2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RW	NTL_FIRST_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RW	NTL_FIRST_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RW	NTL_FIRST_MASK2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RW	NTL_FIRST_MASK2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RW	NTL_FIRST_MASK2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RW	NTL_FIRST_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RW	NTL_FIRST_MASK2_60: ERROR - NTL REGS - Reserved.
61	RW	NTL_FIRST_MASK2_61: ERROR - NTL REGS - Reserved.
62	RW	NTL_FIRST_MASK2_62: ERROR - NTL REGS - Reserved.
63	RW	NTL_FIRST_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	NTL Scratch 2 Register
Mnemonic	NPU.STCK0.NTL1.REGS.SCRATCH2
Address	00000000050110EA (SCOM)
Description	The NTL Scratch 2 register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH2: Scratch register.

Register Name	NTL Scratch 3 Register
Mnemonic	NPU.STCK0.NTL1.REGS.SCRATCH3
Address	00000000050110EB (SCOM)
Description	The NTL Scratch 3 register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH3: Scratch register.

Register Name	NTL Debug0 Configuration Register
Mnemonic	NPU.STCK0.NTL1.REGS.DEBUG0_CONFIG
Address	00000000050110EC (SCOM)
Description	The NTL Debug Trace 0 Configuration register is used to configure what debug information is sent on the debug trace 0 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of debug trace 0: 0x00 = Debug trace 0 byte 0 inputs. 0x01 = Debug trace 0 byte 1 inputs. 0x02 = Debug trace 0 byte 2 inputs. 0x03 = Debug trace 0 byte 3 inputs. 0x04 = Debug trace 0 byte 4 inputs. 0x05 = Debug trace 0 byte 5 inputs. 0x06 = Debug trace 0 byte 6 inputs. 0x07 = Debug trace 0 byte 7 inputs. 0x08 = Debug trace 0 byte 8 inputs. 0x09 = Debug trace 0 byte 9 inputs. 0x0A = Debug trace 0 byte 10 inputs. 0x0B = RX debug group 0. 0x0C = RX debug group 1. 0x0D = RX debug group 2. 0x0E = RX debug group 3. 0x0F = RX debug group 4. 0x10 = RX debug group 5. 0x11 = RX debug group 6. 0x12 = RX debug group 7. 0x13 = RX debug group 8. 0x14 = TX debug group 0. 0x15 = TX debug group 1. 0x16 = TX debug group 2. 0x17 = TX debug group 3. 0x18 = TX debug group 4. 0x19 = TX debug group 5. 0x1A = TX debug group 6. 0x1B = REGS debug group 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of debug trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of debug trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of debug trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of debug trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of debug trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of debug trace 0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of debug trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of debug trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of debug trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of debug trace 0.
55:62	RW	DEBUG0_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	NTL Debug1 Configuration Register
Mnemonic	NPU.STCK0.NTL1.REGS.DEBUG1_CONFIG
Address	00000000050110ED (SCOM)
Description	The NTL Debug Trace 1 Configuration register is used to configure what debug information is sent on the debug trace 1 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of debug trace 1: 0x00 = Debug trace 1 byte 0 inputs. 0x01 = Debug trace 1 byte 1 inputs. 0x02 = Debug trace 1 byte 2 inputs. 0x03 = Debug trace 1 byte 3 inputs. 0x04 = Debug trace 1 byte 4 inputs. 0x05 = Debug trace 1 byte 5 inputs. 0x06 = Debug trace 1 byte 6 inputs. 0x07 = Debug trace 1 byte 7 inputs. 0x08 = Debug trace 1 byte 8 inputs. 0x09 = Debug trace 1 byte 9 inputs. 0x0A = Debug trace 1 byte 10 inputs. 0x0B = RX debug group 0. 0x0C = RX debug group 1. 0x0D = RX debug group 2. 0x0E = RX debug group 3. 0x0F = RX debug group 4. 0x10 = RX debug group 5. 0x11 = RX debug group 6. 0x12 = RX debug group 7. 0x13 = RX debug group 8. 0x14 = TX debug group 0. 0x15 = TX debug group 1. 0x16 = TX debug group 2. 0x17 = TX debug group 3. 0x18 = TX debug group 4. 0x19 = TX debug group 5. 0x1A = TX debug group 6. 0x1B = REGS debug group 0.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of debug trace 1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of debug trace 1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of debug trace 1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of debug trace 1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of debug trace 1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of debug trace 1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of debug trace 1.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of debug trace 1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of debug trace 1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of debug trace 1.
55:62	RW	DEBUG1_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	NTL Performance Configuration Register
Mnemonic	NPU.STCK0.NTL1.REGS.PERF_CONFIG
Address	00000000050110EE (SCOM)
Description	The NTL Performance Configuration register is used to configure what information is counted by the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: PMULet enable (clocks enable).
1	RW	PERF_CONFIG_RESETMODE: 0 = Reset on read. 1 = Reset on write.
2	RW	PERF_CONFIG_FREEZEMODE: 0 = Free run mode. 1 = Freeze on any maximum.
3	RW	PERF_CONFIG_DISABLE_PMISC: 0 = Enable PMISC control of counters. 1 = Disable PMISC control of counters.
4	RW	PERF_CONFIG_PMISC_MODE: 0 = Global PMU PMISC no reset. 1 = Global PMU PMISC reset on enable.
5:7	RW	PERF_CONFIG_CASCADE: PMULet cascade configuration.
8:9	RW	PERF_CONFIG_PRESCALE_C0: Pre-scale configuration for counter 0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: Pre-scale configuration for counter 1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: Pre-scale configuration for counter 2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: Pre-scale configuration for counter 3.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select: 0x00 = Disable. 0x01 = Cycles. 0x02 = Latency events. 0x03 = Latency cycles. 0x04 = Latency aborts. 0x20 = REGS - NDL PRI request. 0x21 = REGS - NDL PRI write request. 0x22 = REGS - NDL PRI read request. 0x23 = REGS - PHY PRI request. 0x24 = REGS - PHY PRI write request. 0x25 = REGS - PHY PRI read request. 0x40 = TX - Any flit sent. 0x41 = TX - Header flit sent. 0x42 = TX - AE flit sent. 0x43 = TX - BE flit sent. 0x44 = TX - Data flit sent. 0x45 = TX - Flow control packet. 0x46 = TX - Write.NC. 0x47 = TX - Write.NC 128B. 0x48 = TX - Write.NC 32-96B. 0x49 = TX - Write.NC 1-16B. 0x4A = TX - Write.NC with BE flit. 0x4B = TX - Read. 0x4C = TX - Upgrade. 0x4D = TX - Atomic. 0x4E = TX - Downgrade.

Bits	SCOM	Field Mnemonic: Description
		0x4F = TX - ATSD. 0x50 = TX - Request response, no data. 0x51 = TX - Request response with data. 0x52 = TX - Probe response, no data. 0x53 = TX - Probe response with data. 0x54 = TX - ATR response. 0x55 = TX - TransDone response, no data. 0x56 = TX - TransDone response with data. 0x57 = TX - TransDone response with data 128B. 0x58 = TX - TransDone response with data 32B - 96B. 0x59 = TX - TransDone response with data 1B - 16B. 0x5A = TX - TransDone response with data with BE flit. 0x5B = TX - Not enough CREQ header credits. 0x5C = TX - Not enough DGD header credits. 0x5D = TX - Not enough ATSD header credits. 0x5E = TX - Not enough RSP header credits. 0x5F = TX - Not enough CREQ data credits. 0x60 = TX - Not enough RSP data credits. 0x61 = TX - Not enough replay buffer credits. 0x62 = TX - Not enough asynchronous buffer credits. 0x80 = RX - CREQ header array full. 0x81 = RX - PRB header array full. 0x82 = RX - ATR header array full. 0x83 = RX - RSP header array full. 0x84 = RX - CREQ data array full. 0x85 = RX - RSP data array full. 0x86 = RX - Any flit received. 0x87 = RX - Header flit received. 0x88 = RX - AE flit received. 0x89 = RX - BE flit received. 0x8A = RX - Data flit received. 0x8B = RX - NOP flow control flit received. 0x8C = RX - Write.NC (UT = 0). 0x8D = RX - Write.NC (UT = 1). 0x8E = RX - Write.NC (UT = 0) 128B. 0x8F = RX - Write.NC (UT = 1) 128B. 0x90 = RX - Write.NC (UT = 0) 256B. 0x91 = RX - Write.NC (UT = 1) 256B. 0x92 = RX - Write.NC (UT = 0) 32B - 96B. 0x93 = RX - Write.NC (UT = 1) 32B - 96B. 0x94 = RX - Write.NC (UT = 0) 1B - 16B. 0x95 = RX - Write.NC (UT = 1) 1B - 16B. 0x96 = RX - Write.NC (UT = 0) with BE flit. 0x97 = RX - Write.NC (UT = 1) with BE flit. 0x98 = RX - Write.NC (UT = 0) to MMIO space. 0x99 = RX - Write.NC (UT = 0) to MMIO space and split into multiple requests. 0x9A = RX - Write.NC (UT = 1) and split into multiple requests. 0x9B = RX - Read.NC (UT = 0). 0x9C = RX - Read.NC (UT = 1). 0x9D = RX - Read.NC (UT = 0) 128B. 0x9E = RX - Read.NC (UT = 1) 128B. 0x9F = RX - Read.NC (UT = 0) 256B. 0xA0 = RX - Read.NC (UT = 1) 256B. 0xA1 = RX - Read.NC (UT = 0) 32B - 96B. 0xA2 = RX - Read.NC (UT = 1) 32B - 96B. 0xA3 = RX - Read.NC (UT = 0) 1B - 16B. 0xA4 = RX - Read.NC (UT = 1) 1B - 16B. 0xA5 = RX - Flush. 0xA6 = RX - RMW. 0xA7 = RX - Atomic.NR.

Bits	SCOM	Field Mnemonic: Description
		0xA8 = RX - Atomic.RR. 0xA9 = RX - Probe.I.MO. 0xAA = RX - Probe.I.N. 0xAB = RX - Probe.X.MO. 0xAC = RX - ATR. 0xAD = RX - ReqRsp.ND. 0xAE = RX - ReqRsp.D. 0xAF = RX - DGDRsp. 0xB0 = RX - ATSDRsp. 0xB1 = RX - TransDone.ND. 0xB2 = RX - TransDone.D. 0xB3 = RX - TransDone.D with BE flit. 0xB4 = RX - CREQ non-flush waiting for CQ credit. 0xB5 = RX - CREQ flush waiting for CQ credit. 0xB6 = RX - CREQ waiting for global credit. 0xB7 = RX - CREQ 256B Op waiting for 256B Ops CAM entry. 0xB8 = RX - PRB waiting for CQ credit. 0xB9 = RX - PRB waiting for global credit. 0xBA = RX - ATR waiting for CQ credit. 0xBB = RX - ATR waiting for global credit.
24:31	RW	PERF_CONFIG_EVENT1: Event 1 select (see Event 0 select for encodes).
32:39	RW	PERF_CONFIG_EVENT2: Event 2 select (see Event 0 select for encodes).
40:47	RW	PERF_CONFIG_EVENT3: Event 3 select (see Event 0 select for encodes).
48:50	RW	PERF_CONFIG_LATENCY: Latency select: 0 = Disable. 1 = Read.NC to response. 2 = Write.RR to response. 3 = Atomic.RR to response. 4 = RMW to response. 5 = Flush to response. 6 = Probe to response. 7 = ATR to response.
51:63	RW	PERF_CONFIG_RESERVED: Reserved.

Register Name	NTL Performance Count Register
Mnemonic	NPU.STCK0.NTL1.REGS.PERF_COUNT
Address	00000000050110EF (SCOM)
Description	The NTL Performance Count register holds the performance counts from the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	IDIAL_PERF_COUNT0: Performance counter 0.
16:31	RWX_WCLRREG	IDIAL_PERF_COUNT1: Performance counter 1.
32:47	RWX_WCLRREG	IDIAL_PERF_COUNT2: Performance counter 2.
48:63	RWX_WCLRREG	IDIAL_PERF_COUNT3: Performance counter 3.

Register Name	NTL CREQ Header Array Pointer Register
Mnemonic	NPU.STCK0.NTL1.REGS.CREQ_HA_PTR
Address	00000000050110F0 (SCOM)
Description	The NTL CREQ Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding CREQ header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	CREQ_HA_PTR_RESERVED1: Reserved.
5:11	RW	CREQ_HA_PTR_START: Starting header array location for CREQ headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	CREQ_HA_PTR_RESERVED2: Reserved.
17:23	RW	CREQ_HA_PTR_END: Ending header array location for CREQ headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	NTL PRB Header Array Pointer Register
Mnemonic	NPU.STCK0.NTL1.REGS.PRB_HA_PTR
Address	00000000050110F1 (SCOM)
Description	The NTL PRB Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding PRB header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	PRB_HA_PTR_RESERVED1: Reserved.
5:11	RW	PRB_HA_PTR_START: Starting header array location for PRB headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	PRB_HA_PTR_RESERVED2: Reserved.
17:23	RW	PRB_HA_PTR_END: Ending header array location for PRB headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	NTL ATR Header Array Pointer Register
Mnemonic	NPU.STCK0.NTL1.REGS.ATR_HA_PTR
Address	00000000050110F2 (SCOM)
Description	The NTL ATR Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding ATR header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	ATR_HA_PTR_RESERVED1: Reserved.
5:11	RW	ATR_HA_PTR_START: Starting header array location for ATR headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.

Bits	SCOM	Field Mnemonic: Description
12:16	RW	ATR_HA_PTR_RESERVED2: Reserved.
17:23	RW	ATR_HA_PTR_END: Ending header array location for ATR headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Header Array Pointer Register
Mnemonic	NPU.STCK0.NTL1.REGS.RSP_HA_PTR
Address	00000000050110F3 (SCOM)
Description	The NTL RSP Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding RSP header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	RSP_HA_PTR_RESERVED1: Reserved.
5:11	RW	RSP_HA_PTR_START: Starting header array location for RSP headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	RSP_HA_PTR_RESERVED2: Reserved.
17:23	RW	RSP_HA_PTR_END: Ending header array location for RSP headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL CREQ Data Array Pointer Register
Mnemonic	NPU.STCK0.NTL1.REGS.CREQ_DA_PTR
Address	00000000050110F4 (SCOM)
Description	The NTL CREQ Data Array Pointer register is used to change the start and/or end entry in the NTL data array for holding CREQ data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	CREQ_DA_PTR_RESERVED1: Reserved.
3:11	RW	CREQ_DA_PTR_START: Starting data array location for CREQ data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	CREQ_DA_PTR_RESERVED2: Reserved.
15:23	RW	CREQ_DA_PTR_END: Ending data array location for CREQ data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Data Array Pointer Register
Mnemonic	NPU.STCK0.NTL1.REGS.RSP_DA_PTR
Address	00000000050110F5 (SCOM)
Description	The NTL RSP Data Array Pointer register is used to change the start and/or end entry in the NTL data array for holding RSP data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	RSP_DA_PTR_RESERVED1: Reserved.
3:11	RW	RSP_DA_PTR_START: Starting data array location for RSP data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	RSP_DA_PTR_RESERVED2: Reserved.
15:23	RW	RSP_DA_PTR_END: Ending data array location for RSP data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL Private Register Interface (PRI) Configuration Register
Mnemonic	NPU.STCK0.NTL1.REGS.PRI_CONFIG
Address	00000000050110F6 (SCOM)
Description	The NTL Private Register Interface (PRI) Configuration register is used to set up the PRI settings for this NTL. This register must be configured before any PRI requests are attempted to NDL or PHY registers.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PRI_CONFIG_NDL: NDL indication sent in the PRI read/write access: 00 = NDL 0. 01 = NDL 1. 10 = NDL 2. 11 = Disable (this disables the NTL from decoding the NDL register space).
2:3	RW	PRI_CONFIG_PHY: Indicates if this NTL should decode a PHY register space: 00 = Decode PHY0 register space (only one NTL that is connected to PHY 0 must be set to this value). 01 = Decode PHY1 register space (only one NTL that is connected to PHY 1 must be set to this value). 1X = Do not decode any PHY register space.
4:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	NTL Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK0.NTL1.REGS.CONFIG1
Address	00000000050110F8 (SCOM)
Description	The NVLink transaction layer (NTL) Miscellaneous Configuration 1 register is used to control NVLink packet formatting by the POWER9 processor. It also controls resetting of the POWER9 NTL.

Bits	SCOM	Field Mnemonic: Description
0	RW	COMPRESSED_RSP_ENA: When set to 0b1, the NTL attempts to compress responses that it sends to the GPU whenever possible.
1:3	RW	CONFIG1_RESERVED1: Reserved.

Bits	SCOM	Field Mnemonic: Description
4	RW	CREQ_AE_ALWAYS: When set to 0b1, the NTL always sends an AE flit when it sends a CREQ packet to the GPU.
5	RW	DGD_AE_ALWAYS: When set to 0b1, the NTL always sends an AE flit when it sends a downgrade packet to the GPU.
6	RW	RSP_AE_ALWAYS: When set to 0b1, the NTL always sends an AE flit when it sends a response packet to the GPU.
7	RW	CONFIG1_RESERVED2: Reserved.
8:9	RW	NTL_RESET: This field indicates the NTL reset mode: 00 = Reset disabled. 11 = Reset (fence) both the NTL and the processor bus for this brick. 10 = Reset (fence) only the processor bus for this brick, the NTL is operational. 01 = Reserved. **Note:** The only legal sequence is 00 →11 →10 →00. This field should not be changed unless bits 0:1 in the CQ Fence Status register equals the value in this field.
10:63	RW	CONFIG1_RESERVED3: Reserved.

Register Name	NTL Scratch 1 Register
Mnemonic	NPU.STCK0.NTL1.REGS.SCRATCH1
Address	00000000050110FA (SCOM)
Description	The NTL Scratch 1 register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH1: Scratch register.

Register Name	NTL Low Power Configuration Register
Mnemonic	NPU.STCK0.NTL1.REGS.LOW_PWR
Address	00000000050110FC (SCOM)
Description	The NTL Low Power Configuration register is used to enable the NPU to request that the NVLink interconnect be placed into low-power mode. The register also defines the conditions under which the NPU turns its low-power request on or off.

Bits	SCOM	Field Mnemonic: Description
0	RW	LP_MODE_ENABLE: When set to 0b1, this NTL is allowed to activate the low-power requested signal to NDL when the low-power count is less than or equal to the low-power count threshold.
1	RW	LP_ONLY_MODE: When set to 0b1, this NTL activates the low-power requested signal to NDL continuously. This can be used for lab stress or debug.
2:7	RW	LP_TIMER_TICK_CONFIG: Rate for the low-power timer tick (2^n cycles).
8:19	RW	LP_MIN_CRED_THRESH: Whenever the NDL replay buffer credits is less than this threshold, the low-power requested signal to NDL is deactivated. This value must be greater than 0 and less than the maximum credit threshold.
20:31	RW	LP_MAX_CRED_THRESH: Whenever the NDL replay buffer credits is greater than or equal to this threshold and the low-power timer tick is active, then the low-power count is incremented by 1. This value must be greater than the minimum credit threshold.

Bits	SCOM	Field Mnemonic: Description
32:43	RW	LP_CNT_THRESH: Whenever the low-power count is greater than or equal to this threshold, this NTL activates the low-power requested signal to NDL until the NDL replay buffer credits is less than the low-power minimum credit threshold. This value must be greater than 0.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.CONFIG0
Address	0000000005011100 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0 = Use Read.RWC for DCLAIM/DCBZ to GPU memory. 1 = Use Upgrade.DN for DCLAIM/DCBZ to GPU memory.
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0 = Use Read.RWC for DCBF/DCBFC to GPU memory. 1 = Use Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0 = Use DMA for Write.NC to processor memory. 1 = Use Read-Push for Write.NC to processor memory.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable Vg less than system. 1 = Force all Vg to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc. 1 = Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending dma. 1 = Change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = kChange to _dma.

Bits	SCOM	Field Mnemonic: Description
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp: 0 = 100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7 = 1.5% chance to increase priority.
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD, future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD, future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD, future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD, future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD, future option bit.
22	RW	CONFIG_RESERVED4: Reserved.
23	RW	CONFIG_MACH_CORRENAB: 0 = Disable state machine array ECC correction. 1 = Enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0 = Disable state machine array ECC error inject bit 1. 1 = Enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0 = Disable state machine array ECC error inject bit 2. 1 = Enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0 = Disable ReqRspOut array ECC correction. 1 = Enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0 = Disable PB-Rsp-In array ECC correction. 1 = Enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 1 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.

Bits	SCOM	Field Mnemonic: Description
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0 = Disable NPU processor bus RCMD, PRESP, and CRESP interfaces. 1 = Enable NPU processor bus RCMD, PRESP, and CRESP interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.
40	RW	CONFIG_ENABLE_SNARF_CPM: 0 = Disable Probe.I.MO snarfing a cp_m. 1 = Enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = Preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = Preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = Preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = Preallocate two state machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = Preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode, report local masters as near. 1 = In basic mode, report local masters as local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOs greater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU to PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.

Bits	SCOM	Field Mnemonic: Description
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.CONFIG1
Address	0000000005011101 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non-REQIN events going down the arbiter pipe. After n+1 REQIN events go through the arbiter while a non-CRR event is waiting, REQIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll: 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data: 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	**Power Bus Epsilon Configuration Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.EPSILON_CONFIG
Address	0000000005011102 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/Vg scope CP write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope reads.

Register Name	Timer Configuration Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.XTIMER_CONFIG
Address	0000000005011103 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward-progress timer (2^n cycles).
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). **Note:** This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for SM inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for SM inhibit timer tick1 (default 63 = off). **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV-Response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV response timer (2^n cycles).

Bits	SCOM	Field Mnemonic: Description
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.GPU_BAR
Address	0000000005011104 (SCOM)
Description	Memory BARs. BAR register defining the GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: The base address (1G address) of BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of base address match for the BAR for brick 0: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. **Note:** It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: Base address (1G address) of BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of the base address match for the BAR for brick 1: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 =1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.PHY_BAR
Address	0000000005011106 (SCOM)
Description	BAR register defining the PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2M range mapped to PHY 0 registers. Stack 1 PHY_BAR defines a 2M range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16M range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0 = Disable PHY_BAR. 1 = Enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2M aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2M aligned address of this PHY_BAR's 2M range. **Note:** In stack two, the low three address bits are reserved (16M range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.GENID_BAR
Address	0000000005011107 (SCOM)
Description	ID Registers MMIO BAR. BAR register defining the Generation ID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0 = Disable this BAR. 1 = Enable this BAR.

Bits	SCOM	Field Mnemonic: Description
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128K aligned address of this BAR's 128K range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**Low Water Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.LOW_WATER
Address	0000000005011108 (SCOM)
Description	State machine allocation for low water marks. Each low water mark should be greater than or equal to 1 and the sum of the low marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be >= 8 and <= 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. Can only be changed from 0 to 1 and must stay at 1 once it is set.
52:63	RO	Constant = 0b000000000000

Register Name	**High Water Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.HIGH_WATER
Address	0000000005011109 (SCOM)
Description	State machine allocation for high water marks. Each high water mark should be greater than or equal to the corresponding config_low_water and config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Relaxed Configuration 0 Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.CONFIG_RELAXED0
Address	000000000501110A (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0 = Disable relaxed source 0 for write operations. 1 = Enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0 = Disable relaxed source 0 for read operations. 1 = Enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: Relaxed source 0 tag mask value: 0 = Bit is masked off, the corresponding match bit must be zero. 1 = Bit must equal the corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0 = Disable relaxed source 1 for write operations. 1 = Enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0 = Disable relaxed source 1 for read operations. 1 = Enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CONFIG_RELAXED1
Address	000000000501110B (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0 = Disable relaxed source 2 for write operations. 1 = Enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0 = Disable relaxed source 2 for read operations. 1 = Enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: when config_brazos_mode=0, matches TTAG 2:3,6:21. when config_brazos_mode=1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 2 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CONFIG_RELAXED2
Address	000000000501110C (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.

Bits	SCOM	Field Mnemonic: Description
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F=0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0 = Disable relaxed source 3 for write operations. 1 = Enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0 = Disable relaxed source 3 for read operations. 1 = Enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 3 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.NDT0_BAR
Address	000000000501110D (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	NTL1/NDL1 MMIO BAR Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.NDT1_BAR
Address	000000000501110E (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128K aligned address of BAR for brick 1's 128K range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.PERF_CONFIG
Address	000000000501110F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.INHIBIT_CONFIG
Address	0000000005011110 (SCOM)
Description	This register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0...11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre-frequency 0: 0 = Inhibit timer tick0. 1 = Inverted inhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = Inhibit timer tick1. 1 = Inverted inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_MESSAGE0
Address	0000000005011111 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_MESSAGE1
Address	0000000005011112 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_MESSAGE2
Address	0000000005011113 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_MESSAGE3
Address	0000000005011114 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_MESSAGE4
Address	0000000005011115 (SCOM)
Description	Error message/capture register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.SM_STATUS
Address	0000000005011116 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: Set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: Set to 1 when brick 0 probe allocation is at its idle level.

Bits	SCOM	Field Mnemonic: Description
2	ROX	SM_STATUS_CREQ1: Set to 1 when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: Set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: Set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: Set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: Set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: Set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: Set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: Set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: Set to 1 when the outbound Rn/Vg scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: Set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: Set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: Set to 1 when the outbound brick 1 CREQ request queue is empty.
30	ROX	SM_STATUS_N1DGD: Set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: Set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: Set to 1 the when the outbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: Set to 1 when the outbound processor bus data response/merge operation queue is empty.
34	ROX	SM_STATUS_N0RSP: Set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: Set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: Set to 1 when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: Set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: Set to 1 when free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_FIRST0
Address	0000000005011117 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR First 1 Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_FIRST1
Address	0000000005011118 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD final snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_FIRST2
Address	0000000005011119 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.

Bits	SCOM	Field Mnemonic: Description
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).

Bits	SCOM	Field Mnemonic: Description
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	CERR Mask 0 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_MASK0
Address	000000000501111A (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).

Bits	SCOM	Field Mnemonic: Description
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_MASK1
Address	000000000501111B (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.

Bits	SCOM	Field Mnemonic: Description
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: UE ECC error detected from state machine array.
21	RW	IDIAL_SM_MASK_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: Parity error detected on RCMD TTAG field.
25	RW	IDIAL_SM_MASK_PBP_1: Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: Parity error detected on CRESP TTAG.
27	RW	IDIAL_SM_MASK_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: RCMD TTAG received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: RCMD TTAG received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: CRESP TTAG received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: CRESP TTAG received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 2 Register**
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_MASK2
Address	000000000501111C (SCOM)
Description	c_err_rpt mask register **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate'. but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate.' but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).

Bits	SCOM	Field Mnemonic: Description
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown state.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.

Bits	SCOM	Field Mnemonic: Description
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_HOLD0
Address	000000000501111D (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPU bar.

Bits	SCOM	Field Mnemonic: Description
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_HOLD1
Address	000000000501111E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: UE ECC error detected from state machine array.

Bits	SCOM	Field Mnemonic: Description
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.

Bits	SCOM	Field Mnemonic: Description
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK1.CS.SM0.MISC.CERR_HOLD2
Address	000000000501111F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink mster command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon,' but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.

Bits	SCOM	Field Mnemonic: Description
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout. but not in waiting for NV response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.CONFIG0
Address	0000000005011120 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0 = Use Read.RWC for DCLAIM/DCBZ to GPU memory. 1 = Use Upgrade.DN for DCLAIM/DCBZ to GPU memory.
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0 = Use Read.RWC for DCBF/DCBFC to GPU memory. 1 = Use Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0 = Use DMA for Write.NC to processor memory. 1 = Use Read-Push for Write.NC to processor memory.

Bits	SCOM	Field Mnemonic: Description
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable Vg less than system. 1 = Force all Vg to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc. 1 = Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending dma. 1 = Change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = Change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp. 0 = 100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7 = 1.5% chance to increase priority.
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD, future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD, future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD, future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD, future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD, future option bit.
22	RW	CONFIG_RESERVED4: Reserved.
23	RW	CONFIG_MACH_CORRENAB: 0 = Disable state machine array ECC correction. 1 = Enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0 = Disable state machine array ECC error inject bit 1. 1 = Enable state machine array ECC error inject bit 1.

Bits	SCOM	Field Mnemonic: Description
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0 = Disable state machine array ECC error inject bit 2. 1 = Enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0 = Disable ReqRspOut array ECC correction. 1 = Enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0 = Disable PB-Rsp-In array ECC correction. 1 = Enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 1 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0 = Disable NPU processor bus RCMD, PRESP, and CRESP interfaces. 1 = Enable NPU processor bus RCMD, PRESP, and CRESP interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.
40	RW	CONFIG_ENABLE_SNARF_CPM: 0 = Disable Probe.I.MO snarfing a cp_m. 1 = Enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = Preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = Preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = Preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = Preallocate two state machines to brick 1 PRB channel.

Bits	SCOM	Field Mnemonic: Description
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = Preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode report local masters as near. 1 = In basic mode report local masters as local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOs greater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU to PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.CONFIG1
Address	0000000005011121 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.

Bits	SCOM	Field Mnemonic: Description
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = 1/(2$^{(n+1)}$) cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non-REQIN events going down the arbiter pipe. After n+1 REQIN events go through the arbiter while a non-CRR event is waiting, REQIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll: 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data: 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	Power Bus Epsilon Configuration Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.EPSILON_CONFIG
Address	0000000005011122 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/Vg scope CP write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope reads.

Register Name	Timer Configuration Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.XTIMER_CONFIG
Address	0000000005011123 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward-progress timer (2^n cycles).

Bits	SCOM	Field Mnemonic: Description
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). **Note:** This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for SM inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for SM inhibit timer tick1 (default 63 = off). **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV-Response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.GPU_BAR
Address	0000000005011124 (SCOM)
Description	Memory BARs. BAR register defining the GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: The base address (1G address) of the BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).

Bits	SCOM	Field Mnemonic: Description
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of the base address match for the BAR for brick 0: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. **Note:** It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: The base address (1G address) of the BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of the base address match for the BAR for brick 1: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.PHY_BAR
Address	0000000005011126 (SCOM)
Description	BAR register defining the PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2M range mapped to PHY 0 registers. Stack 1 PHY_BAR r defines a 2M range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16M range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0 = Disable PHY_BAR. 1 = Enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2M aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2M aligned address of this PHY_BAR's 2M range. **Note:** In stack two, the low three address bits are reserved (16M range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.GENID_BAR
Address	0000000005011127 (SCOM)
Description	ID Registers MMIO BAR. BAR register defining Generation ID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0 = Disable this BAR. 1 = Enable this BAR.

Bits	SCOM	Field Mnemonic: Description
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of the 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of the 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128K aligned address of this BAR's 128K range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**Low Water Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.LOW_WATER
Address	0000000005011128 (SCOM)
Description	State machine allocation for low water marks. Each low water mark should be greater than or equal to 1 and the sum of the low water marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be >= 8 and <= 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. Can only be changed from 0 to 1 and must stay at 1 once it is set.
52:63	RO	Constant = 0b000000000000

Register Name	**High Water Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.HIGH_WATER
Address	0000000005011129 (SCOM)
Description	State machine allocation high water marks. Each high water mark should be greater than or equal to the corresponding config_low_water and less than the config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Relaxed Configuration 0 Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.CONFIG_RELAXED0
Address	000000000501112A (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0 = Disable relaxed source 0 for write operations. 1 = Enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0 = Disable relaxed source 0 for read operations. 1 = Enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: Relaxed source 0 tag mask value: 0 = Bit is masked off, corresponding match bit must be zero. 1 = Bit must equal corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0 = Disable relaxed source 1 for write operations. 1 = Enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0 = Disable relaxed source 1 for read operations. 1 = Enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CONFIG_RELAXED1
Address	000000000501112B (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0 = Disable relaxed source 2 for write operations. 1 = Enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0 = Disable relaxed source 2 for read operations. 1 = Enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 2 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CONFIG_RELAXED2
Address	000000000501112C (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.

Bits	SCOM	Field Mnemonic: Description
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F = 0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0 = Disable relaxed source 3 for write operations. 1 = Enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0 = Disable relaxed source 3 for read operations. 1 = Enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 0 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.NDT0_BAR
Address	000000000501112D (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	NTL1/NDL1 MMIO BAR Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.NDT1_BAR
Address	000000000501112E (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128K aligned address of BAR for brick 1's 128K range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.PERF_CONFIG
Address	000000000501112F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.INHIBIT_CONFIG
Address	0000000005011130 (SCOM)
Description	This register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre frequency 0: 0 = Inhibit timer tick0. 1 = Inverted inhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = Inhibit timer tick1. 1 = Inverted inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_MESSAGE0
Address	0000000005011131 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_MESSAGE1
Address	0000000005011132 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_MESSAGE2
Address	0000000005011133 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_MESSAGE3
Address	0000000005011134 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_MESSAGE4
Address	0000000005011135 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.SM_STATUS
Address	0000000005011136 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: Set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: Set to 1 when brick 0 probe allocation is at its idle level.

Bits	SCOM	Field Mnemonic: Description
2	ROX	SM_STATUS_CREQ1: Set to 1 when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: Set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: Set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: Set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: Set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: Set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: Set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: Set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: Set to 1 when the outbound Rn/Vg scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: Set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: Set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: Set to 1 when the outbound brick 1 CREQ request queue is empty.
30	ROX	SM_STATUS_N1DGD: Set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: Set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: Set to 1 when the outbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: Set to 1 when the outbound processor bus data response/merge operation queue is empty.
34	ROX	SM_STATUS_N0RSP: Set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: Set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: Set to 1 when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: Set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: Set to 1 when the free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_FIRST0
Address	0000000005011137 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR First 1 Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_FIRST1
Address	0000000005011138 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_FIRST2
Address	0000000005011139 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate,' but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp-Pocket-Hit event, but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.

Bits	SCOM	Field Mnemonic: Description
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_MASK0
Address	0000000005011 13A (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).

Bits	SCOM	Field Mnemonic: Description
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPU Bar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_MASK1
Address	000000000501113B (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS response.

Bits	SCOM	Field Mnemonic: Description
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: UE ECC error detected from state machine array.
21	RW	IDIAL_SM_MASK_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: Parity error detected on RCMD TTAG field.
25	RW	IDIAL_SM_MASK_PBP_1: Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: Parity error detected on CRESP TTAG.
27	RW	IDIAL_SM_MASK_PBP_3: Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).

Bits	SCOM	Field Mnemonic: Description
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: RCMD TTAG received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: RCMD TTAG received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: CRESP TTAG received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: CRESP TTAG received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 2 Register**
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_MASK2
Address	0000000005011 13C (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate,' but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp-Pocket-Hit event, but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).

Bits	SCOM	Field Mnemonic: Description
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon'. but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown state.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.

Bits	SCOM	Field Mnemonic: Description
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_HOLD0
Address	000000000501113D (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_HOLD1
Address	000000000501113E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK1.CS.SM1.MISC.CERR_HOLD2
Address	000000000501113F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA done event. but not in wait SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.

Bits	SCOM	Field Mnemonic: Description
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.CONFIG0
Address	0000000005011140 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0 = Use Read.RWC for DCLAIM/DCBZ to GPU memory. 1 = Use Upgrade.DN for DCLAIM/DCBZ to GPU memory.

Bits	SCOM	Field Mnemonic: Description
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0 = Use Read.RWC for DCBF/DCBFC to GPU memory. 1 = Use Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0 = Use DMA for Write.NC to processor memory. 1 = Use Read-Push for Write.NC to processor memory.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable Vg less than system. 1 = Force all Vg to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc. 1 = Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending dma. 1 = Change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = Change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp: 0 = 100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7 = 1.5% chance to increase priority.
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD, future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD, future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD, future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD, future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD, future option bit.
22	RW	CONFIG_RESERVED4: Reserved.

Bits	SCOM	Field Mnemonic: Description
23	RW	CONFIG_MACH_CORRENAB: 0 = Disable state machine array ECC correction. 1 = Enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0 = Disable state machine array ECC error inject bit 1. 1 = Enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0 = Disable state machine array ECC error inject bit 2. 1 = Enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0 = Disable ReqRspOut array ECC correction. 1 = Enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0 = Disable PB-Rsp-In array ECC correction. 1 = Enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 0 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0 = Disable NPU processor bus RCMD, PRESP, and CRESP interfaces. 1 = Enable NPU processor bus RCMD, PRESP, and CRESP interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.

Bits	SCOM	Field Mnemonic: Description
40	RW	CONFIG_ENABLE_SNARF_CPM: 0 = Disable Probe.I.MO snarfing a cp_m. 1 = Enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = Preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = Preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = Preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = Preallocate two state machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = Preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode report local masters as near. 1 = In basic mode report local masters as local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOs greater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU to PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.CONFIG1
Address	0000000005011141 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slice times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non-REQIN events going down the arbiter pipe. After n+1 REQIN events go through the arbiter while a non-CRR event is waiting, REQIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.

Bits	SCOM	Field Mnemonic: Description
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll: 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data: 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	**Power Bus Epsilon Configuration Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.EPSILON_CONFIG
Address	0000000005011142 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/Vg scope CP write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope reads.

Register Name	**Timer Configuration Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.XTIMER_CONFIG
Address	0000000005011143 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ *5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward-progress timer (2^n cycles).

Bits	SCOM	Field Mnemonic: Description
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). **Note:** This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for SM inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for SM inhibit timer tick1 (default 63 = off). **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV-Response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV-Response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e -10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.GPU_BAR
Address	0000000005011144 (SCOM)
Description	Memory BARs. BAR register defining the GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: Base address (1G address) of BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).

Bits	SCOM	Field Mnemonic: Description
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of the base address match for the BAR for brick 0: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. **Note:** It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: The base address (1G address) of BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of the base address match for the BAR for brick 1: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.PHY_BAR
Address	0000000005011146 (SCOM)
Description	BAR register defining the PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2M range mapped to PHY 0 registers. Stack 1 PHY_BAR defines a 2M range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16M range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0 = Disable PHY_BAR. 1 = Enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2M aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2M aligned address of this PHY_BAR's 2M range. **Note:** In stack two, the low three address bits are reserved (16M range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.GENID_BAR
Address	0000000005011147 (SCOM)
Description	ID registers MMIO BAR. BAR register defining the Generation ID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0 = Disable this BAR. 1 = Enable this BAR.

Bits	SCOM	Field Mnemonic: Description
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128K aligned address of this BAR's 128K range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**Low Water Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.LOW_WATER
Address	0000000005011148 (SCOM)
Description	State machine allocation for low water marks. Each low water mark should be greater than or equal to 1 and the sum of the low water marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be >= 8 and <= 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. Can only be changed from 0 to 1 and must stay at 1 once it is set.
52:63	RO	Constant = 0b000000000000

Register Name	**High Water Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.HIGH_WATER
Address	0000000005011149 (SCOM)
Description	State machine allocation for high water marks. Each high water mark should be greater than or equal to the corresponding config_low_water and less than the config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Relaxed Configuration 0 Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.CONFIG_RELAXED0
Address	000000000501114A (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0 = Disable relaxed source 0 for write operations. 1 = Enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0 = Disable relaxed source 0 for read operations. 1 = Enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: Relaxed source 0 tag mask value: 0 = Bit is masked off, the corresponding match bit must be 0. 1 = Bit must equal the corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0 = Disable relaxed source 1 for write operations. 1 = Enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0 = Disable relaxed source 1 for read operations. 1 = Enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CONFIG_RELAXED1
Address	000000000501114B (SCOM)
Description	This register configures relaxed ordering/. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0 = Disable relaxed source 2 for write operations. 1 = Enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0 = Disable relaxed source 2 for read operations. 1 = Enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: When config_brazos_mode=0, matches TTAG 2:3,6:21. When config_brazos_mode=1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 2 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CONFIG_RELAXED2
Address	000000000501114C (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally. M

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.

Bits	SCOM	Field Mnemonic: Description
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F=0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0 = Disable relaxed source 3 for write operations. 1 = Enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0 = Disable relaxed source 3 for read operations. 1 = Enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 3 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.NDT0_BAR
Address	000000000501114D (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128K aligned address of the BAR for brick 0's 128K range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	NTL1/NDL1 MMIO BAR Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.NDT1_BAR
Address	000000000501114E (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128K aligned address of the BAR for brick 1 128K range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.PERF_CONFIG
Address	000000000501114F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.INHIBIT_CONFIG
Address	0000000005011150 (SCOM)
Description	This register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre-frequency 0: 0 = Inhibit timer tick0. 1 = Inverted inhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = Inhibit timer tick1. 1 = Inverted inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_MESSAGE0
Address	0000000005011151 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_MESSAGE1
Address	0000000005011152 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_MESSAGE2
Address	0000000005011153 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_MESSAGE3
Address	0000000005011154 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_MESSAGE4
Address	0000000005011155 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.SM_STATUS
Address	0000000005011156 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: Set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: Set to 1 when brick 0 probe allocation is at its idle level.

Bits	SCOM	Field Mnemonic: Description
2	ROX	SM_STATUS_CREQ1: Set to 1 when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: Set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: Set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: Set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: Set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: Set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: Set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: Set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: Set to 1 when the outbound Rn/Vg scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: Set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: Set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: Set to 1 when the outbound brick 1 CREQ request queue is empty.
30	ROX	SM_STATUS_N1DGD: Set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: Set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: Set to 1 when the outbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: Set to 1 when the outbound processor bus data response/merge operation queue is empty.
34	ROX	SM_STATUS_N0RSP: Set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: Set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: Set to 1 when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: Set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: Set to 1 when the free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_FIRST0
Address	0000000005011157 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/length/slignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR First 1 Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_FIRST1
Address	0000000005011158 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_FIRST2
Address	0000000005011159 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: Sart Epsilon, but Epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.

Bits	SCOM	Field Mnemonic: Description
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_MASK0
Address	000000000501115A (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).

Bits	SCOM	Field Mnemonic: Description
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_MASK1
Address	0000000005011158 (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS response.

Bits	SCOM	Field Mnemonic: Description
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting for data time out.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: UE ECC error detected from state machine array.
21	RW	IDIAL_SM_MASK_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: Parity error detected on RCMD TTAG field.
25	RW	IDIAL_SM_MASK_PBP_1: Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: Parity error detected on CRESP TTAG.
27	RW	IDIAL_SM_MASK_PBP_3: Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).

Bits	SCOM	Field Mnemonic: Description
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: RCMD TTAG received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: RCMD TTAG received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: CRESP TTAG received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: CRESP TTAG received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 2 Register**
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_MASK2
Address	0000000005011150 (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).

Bits	SCOM	Field Mnemonic: Description
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown state.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.

Bits	SCOM	Field Mnemonic: Description
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_HOLD0
Address	0000000005011150 (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_HOLD1
Address	000000000501115E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting for data time out.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK1.CS.SM2.MISC.CERR_HOLD2
Address	000000000501115F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT translate response event, but not in wait-translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.

Bits	SCOM	Field Mnemonic: Description
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.CONFIG0
Address	0000000005011160 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0 = Use Read.RWC for DCLAIM/DCBZ to GPU memory. 1 = Use Upgrade.DN for DCLAIM/DCBZ to GPU memory.

Bits	SCOM	Field Mnemonic: Description
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0 = Use Read.RWC for DCBF/DCBFC to GPU memory. 1 = Use Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0 = Use DMA for Write.NC to processor memory. 1 = Use Read-Push for Write.NC to processor memory.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable Vg less than system. 1 = Force all Vg to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc. 1 = Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending dma. 1 = Change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = Change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp: 0 = 100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7 = 1.5% chance to increase priority.
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD, future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD, future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD, future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD, future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD, future option bit.
22	RW	CONFIG_RESERVED4: Reserved.

Bits	SCOM	Field Mnemonic: Description
23	RW	CONFIG_MACH_CORRENAB: 0 = Disable state machine array ECC correction. 1 = Enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0 = Disable state machine array ECC error inject bit 1. 1 = Enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0 = Disable state machine array ECC error inject bit 2. 1 = Enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0 = Disable ReqRspOut array ECC correction. 1 = Enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0 = Disable PB-Rsp-In array ECC correction. 1 = Enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 1 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0 = Disable NPU processor bus RCMD, PRESP, and CRESP interfaces. 1 = Enable NPU processor bus RCMD, PRESP, and CRESP interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.

Bits	SCOM	Field Mnemonic: Description
40	RW	CONFIG_ENABLE_SNARF_CPM: 0 = Disable Probe.I.MO snarfing a cp_m. 1 = Enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = Preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = Preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = Preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = Preallocate two state machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = Preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode report local masters as near. 1 = In basic mode report local masters as near.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOs greater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU to PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.CONFIG1
Address	0000000005011161 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non- REQIN events going down the arbiter pipe. After n+1 REQIN events go through the arbiter while a non-CRR event is waiting, REQIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.

Bits	SCOM	Field Mnemonic: Description
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll: 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data: 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	**Power Bus Epsilon Configuration Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.EPSILON_CONFIG
Address	0000000005011162 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/Vg scope CP write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope reads.

Register Name	**Timer Configuration Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.XTIMER_CONFIG
Address	0000000005011163 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward-progress timer (2^n cycles).

Bits	SCOM	Field Mnemonic: Description
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). **Note:** This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for SM inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for SM inhibit timer tick1 (default 63 = off) **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.GPU_BAR
Address	0000000005011164 (SCOM)
Description	Memory BARs. BAR register defining the GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: The base address (1G address) of the BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).

Bits	SCOM	Field Mnemonic: Description
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of the base address match for the BAR for brick 0: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. **Note:** It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: Base address (1G address) of BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of the base address match for the BAR for brick 1: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.PHY_BAR
Address	0000000005011166 (SCOM)
Description	BAR register defining the PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2M range mapped to PHY 0 registers. Stack 1 PHY_BAR defines a 2M range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16M range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0 = Disable PHY_BAR. 1 = enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2M aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2M aligned address of this PHY_BAR's 2M range. **Note:** In stack two, the low three address bits are reserved (16M range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.GENID_BAR
Address	0000000005011167 (SCOM)
Description	ID registers MMIO BAR. BAR register defining the GenerationID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0 = Disable this BAR. 1 = Enable this BAR.

Bits	SCOM	Field Mnemonic: Description
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of the 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of the 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128K aligned address of this BAR's 128K range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**Low Water Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.LOW_WATER
Address	0000000005011168 (SCOM)
Description	State machine allocation for low water marks. Each low water mark should be greater than or equal to 1 and the sum of the low water marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be >= 8 and <= 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. Can only be changed from 0 to 1 and must stay at 1 once it is set.
52:63	RO	Constant = 0b000000000000

Register Name	**High Water Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.HIGH_WATER
Address	0000000005011169 (SCOM)
Description	State machine allocation for high water marks. Each high water mark should be greater than or equal to the corresponding config_low_water and less than the config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Relaxed Configuration 0 Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.CONFIG_RELAXED0
Address	000000000501116A (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0 = Disable relaxed source 0 for write operations. 1 = Enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0 = Disable relaxed source 0 for read operations. 1 = Enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: Relaxed source 0 tag mask value: 0 = Bit is masked off, corresponding match bit must be 0. 1 = Bit must equal corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0 = Disable relaxed source 1 for write operations. 1 = Enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0 = Disable relaxed source 1 for read operations. 1 = Enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CONFIG_RELAXED1
Address	000000000501116B (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0 = Disable relaxed source 2 for write operations. 1 = Enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0 = Disable relaxed source 2 for read operations. 1 = Enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 2 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CONFIG_RELAXED2
Address	000000000501116C (SCOM)
Description	This register configures relaxed ordering. N**ote:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.

Bits	SCOM	Field Mnemonic: Description
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F=0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0 = Disable relaxed source 3 for write operations. 1 = Enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0 = Disable relaxed source 3 for read operations. 1 = Enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 3 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.NDT0_BAR
Address	000000000501116D (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	NTL1/NDL1 MMIO BAR Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.NDT1_BAR
Address	000000000501116E (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128K aligned address of BAR for brick 1's 128K range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.PERF_CONFIG
Address	000000000501116F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.INHIBIT_CONFIG
Address	0000000005011170 (SCOM)
Description	This register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre frequency 0: 0 = Inhibit timer tick0. 1 = Inverted inhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0...12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = Inhibit timer tick1. 1 = Inverted inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_MESSAGE0
Address	0000000005011171 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_MESSAGE1
Address	0000000005011172 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_MESSAGE2
Address	0000000005011173 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_MESSAGE3
Address	0000000005011174 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_MESSAGE4
Address	0000000005011175 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.SM_STATUS
Address	0000000005011176 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: Set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: Set to 1 when brick 0 probe allocation is at its idle level.

Bits	SCOM	Field Mnemonic: Description
2	ROX	SM_STATUS_CREQ1: Set to 1 when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: Set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: Set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: Set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: Set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: Set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X= Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: Set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: Set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: Set to 1 when the outbound Rn/Vg scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: Set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: Set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: Set to 1 when the outbound brick 1 CREQ request queue is empty.
30	ROX	SM_STATUS_N1DGD: Set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: Set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: Set to 1 when the outbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: Set to 1 when the outbound processor bus data response/merge operation queue is empty.
34	ROX	SM_STATUS_N0RSP: Set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: Set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: Set to 1 when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: Set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: Set to 1 when the free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_FIRST0
Address	0000000005011177 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR First 1 Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_FIRST1
Address	0000000005011178 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_FIRST2
Address	0000000005011179 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.

Bits	SCOM	Field Mnemonic: Description
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_MASK0
Address	000000000501117A (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).

Bits	SCOM	Field Mnemonic: Description
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_MASK1
Address	000000000501117B (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS response.

Bits	SCOM	Field Mnemonic: Description
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting for data time out.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: UE ECC error detected from state machine array.
21	RW	IDIAL_SM_MASK_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: Parity error detected on ECMC TTAG field.
25	RW	IDIAL_SM_MASK_PBP_1: Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: Parity error detected on CRESP TTAG.
27	RW	IDIAL_SM_MASK_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).

Bits	SCOM	Field Mnemonic: Description
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: RCMD TTAG received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: RCMD TTAG received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: CRESP TTAG received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: CRESP TTAG received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 2 Register**
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_MASK2
Address	0000000005011170 (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).

Bits	SCOM	Field Mnemonic: Description
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown state.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.

Bits	SCOM	Field Mnemonic: Description
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_HOLD0
Address	000000000501117D (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_HOLD1
Address	000000000501117E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting for data time out.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK1.CS.SM3.MISC.CERR_HOLD2
Address	000000000501117F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate,' but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.

Bits	SCOM	Field Mnemonic: Description
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_CTL Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK1.CS.CTL.MISC.CONFIG0
Address	0000000005011180 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED0: Reserved. **Note:** This was 1dot0 mode.
1:3	RW	CONFIG1_RESERVED1: Reserved.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.

Bits	SCOM	Field Mnemonic: Description
5:9	RW	CONFIG_GEN_HEAD_DELAY: Number of cycles to wait for generation done when reading a generation head register. **Note:** Setting this field to 0 hangs the NPU.
10	RW	CONFIG_MRBGP_DIV2_COUNT_AT_EXP: 0 = Reset to zero the master retry back-off retry count when the sample period expires for group-pump. 1 = Divide by two the master retry back-off retry count when the sample period expires for group-pump.
11	RW	CONFIG_MRBSP_DIV2_COUNT_AT_EXP: 0 = Reset to zero the master retry back-off retry count when the sample period expires for system-pump. 1 = Divide by two the master retry back-off retry count when the sample period expires for system-pump.
12	RW	CONFIG_MRBGP_DIS_DYN_ADJ: 0 = Enable dynamically adjusting the master retry back-off sample period based on level for group-pump. 1 = Disable dynamically adjusting the master retry back-off sample period based on level for group-pump.
13	RW	CONFIG_MRBSP_DIS_DYN_ADJ: 0 = Enable dynamically adjusting the master retry back-off sample period based on level for system-pump 1 = Disable dynamically adjusting the master retry back-off sample period based on level for system-pump.
14	RW	CONFIG_MRBGP_DIS_DYN_LVL_ADJ: 0 = Enable dynamically adjusting the master retry back-off thresholds based on level for group-pump. 1 = Disable dynamically adjusting the master retry back-off thresholds based on level for group-pump.
15	RW	CONFIG_MRBSP_DIS_DYN_LVL_ADJ: 0 = Enable dynamically adjusting the master retry back-off thresholds based on level for system-pump. 1 = Disable dynamically adjusting the master retry back-off thresholds based on level for system-pump.
16:21	RW	CONFIG_MRBGP_THRESH1: Master retry back-off retry count threshold at which to reduce the level for group-pump.
22:27	RW	CONFIG_MRBGP_THRESH2: Master retry back-off retry count threshold at which to increase the level for group-pump. **Note:** Make sure that thresh2 is greater than thresh1 or the back-off level will only increase.
28:33	RW	CONFIG_MRBSP_THRESH1: Master retry back-off retry count threshold at which to reduce the level for system-pump.
34:39	RW	CONFIG_MRBSP_THRESH2: Master retry back-off retry count threshold at which to increase the level for system-pump. **Note:** Make sure that thresh2 is greater than thresh1 or the back-off level will only increase.
40:43	RW	CONFIG_MRBGP_MAX_LEVEL: Master retry back-off maximum level for group-pump.
44:47	RW	CONFIG_MRBSP_MAX_LEVEL: Master retry back-off maximum level for system-pump.
48	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.
49	RW	CONFIG_DISABLE_PBM_ECC_COR: 0 = Enable ECC correction of MMIO store data. 1 = Disable ECC correction.
50	RW	CONFIG_LAB_RANDOMIZE_PE_01: 0 = Do not randomize PE(0:1). 1 = Randomize PE(0:1).
51	RW	CONFIG_LAB_RANDOMIZE_PE_23: 0 = Do not randomize PE(2:3). 1 = Randomize PE(2:3).
52:63	RW	CONFIG1_RESERVED2: Reserved.

Register Name	Future Configuration 1 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CONFIG1
Address	0000000005011181 (SCOM)
Description	This is currently a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_CONFIG1: Future configuration register.

Register Name	Future Configuration 2 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CONFIG2
Address	0000000005011182 (SCOM)
Description	This is currently a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_CONFIG2: Future configuration register.

Register Name	Future Configuration 3 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CONFIG3
Address	0000000005011183 (SCOM)
Description	This is currently a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_CONFIG3: Future configuration register.

Register Name	Performance Match Configuration Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.PERF_MATCH_CONFIG
Address	0000000005011184 (SCOM)
Description	Performance event field match register.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	PERF_MATCH_NMCMD: NVLink command.
6:10	RW	PERF_MATCH_NMEXCMD: NVLink ExtReqCmd.
11	RW	PERF_MATCH_BE: NVLink byte enables.
12:17	RW	PERF_MATCH_CS: NVLink CS(0:5).
18:33	RW	PERF_MATCH_AECS: NVLink AECS(0:15).
34:37	RW	PERF_MATCH_PE: PE.
38:39	RW	PERF_MATCH_RESERVED1: Reserved.
40:63	RO	Constant = 0b00000000000000000000000

Register Name	Performance Mask Configuration Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.PERF_MASK_CONFIG
Address	0000000005011185 (SCOM)
Description	Performance event field mask register.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	PERF_MASK_NMCMD: NVLink command.
6:10	RW	PERF_MASK_NMEXCMD: NVLink ExtReqCmd.
11	RW	PERF_MASK_BE: NVLink byte enables.
12:17	RW	PERF_MASK_CS: NVLink CS(0:5).
18:33	RW	PERF_MASK_AECS: NVLink AECS(0:15).
34:37	RW	PERF_MASK_PE: PE.
38:39	RW	PERF_MASK_RESERVED1: Reserved.
40:63	RO	Constant = 0b0000000000000000000000000

Register Name	CQ_CTL Performance Count Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.PERF_COUNT
Address	0000000005011186 (SCOM)
Description	PMULet count values register.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	IDIAL_PERF_COUNT0: Performance counter 0.
16:31	RWX_WCLRREG	IDIAL_PERF_COUNT1: Performance counter 1.
32:47	RWX_WCLRREG	IDIAL_PERF_COUNT2: Performance counter 2.
48:63	RWX_WCLRREG	IDIAL_PERF_COUNT3: Performance counter 3.

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.PERF_CONFIG
Address	0000000005011187 (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: PMULet enable (clocks enable).
1	RW	PERF_CONFIG_RESETMODE: 0 = Reset on read. 1 = Reset on write.
2	RW	PERF_CONFIG_FREEZEMODE: 0 = Free run mode. 1 = Freeze on any maximum.
3	RW	PERF_CONFIG_DISABLE_PMISC: 0 = Enable PMISC control of counters. 1 = Disable PMISC control of counters.

Bits	SCOM	Field Mnemonic: Description
4	RW	PERF_CONFIG_PMISC_MODE: 0 = Global PMU PMISC no reset. 1 = Global PMU PMISC reset on enable.
5:7	RW	PERF_CONFIG_CASCADE: PMULet cascade configuration.
8:9	RW	PERF_CONFIG_PRESCALE_C0: Pre-scale configuration for counter 0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: Pre-scale configuration for counter 1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: Pre-scale configuration for counter 2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: Pre-scale configuration for counter 3.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:52	RW	PERF_CONFIG_LATSTART: Latency count start event.
53:57	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
58:62	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
63	RW	PERF_CONFIG_RESERVED: Reserved.

Register Name	**Debug0 Configuration Register**
Mnemonic	NPU.STCK1.CS.CTL.MISC.DEBUG0_CONFIG
Address	0000000005011188 (SCOM)
Description	Configuration register for trace 0 chain.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of trace 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of trace 0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of trace 0.
55:62	RW	DEBUG0_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	Debug1 Configuration Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.DEBUG1_CONFIG
Address	0000000005011189 (SCOM)
Description	Configuration register for trace 1 chain.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of trace 1.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of trace 1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of trace 1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of trace 1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of trace 1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of trace 1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of trace 1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of trace 1.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of trace 1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of trace 1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of trace 1.
55:62	RW	DEBUG1_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	Brick 0 BDF2PE Configuration 0 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.BDF2PE_00_CONFIG
Address	000000000501118A (SCOM)
Description	This register configures BDF-to-PE mapping #0 for brick 0. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_00_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1	RW	CONFIG_BDF2PE_00_WILDCARD: 0 = This BDF-to-PE mapping matches only this BDF. 1 = This BDF-to-PE mapping matches all BDFs.
2:3	RW	CONFIG_BDF2PE_00_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_00_PE: PE associated with this BDF.
8:23	RW	CONFIG_BDF2PE_00_BDF: BDF mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 0 BDF2PE Configuration 1 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.BDF2PE_01_CONFIG
Address	000000000501118B (SCOM)
Description	This register configures BDF-to-PE mapping #1 for brick 0. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_01_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_01_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_01_PE: PE associated with this BDF.
8:23	RW	CONFIG_BDF2PE_01_BDF: BDF mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 0 BDF2PE Configuration 2 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.BDF2PE_02_CONFIG
Address	000000000501118C (SCOM)
Description	This register configures BDF-to-PE mapping #2 for brick 0. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_02_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_02_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_02_PE: PE associated with this BDF.
8:23	RW	CONFIG_BDF2PE_02_BDF: BDF mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 1 BDF2PE Configuration 0 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.BDF2PE_10_CONFIG
Address	000000000501118D (SCOM)
Description	This register configures BDF-to-PE mapping #0 for brick 1. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_10_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1	RW	CONFIG_BDF2PE_10_WILDCARD: 0 = This BDF-to-PE mapping matches only this BDF. 1 = This BDF-to-PE mapping matches all BDFs.
2:3	RW	CONFIG_BDF2PE_10_RESERVED: Reserved.

Bits	SCOM	Field Mnemonic: Description
4:7	RW	CONFIG_BDF2PE_10_PE: PE associated with this BDF.
8:23	RW	CONFIG_BDF2PE_10_BDF: BDF mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 1 BDF2PE Configuration 1 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.BDF2PE_11_CONFIG
Address	000000000501118E (SCOM)
Description	This register configures BDF-to-PE mapping #1 for brick 1. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_11_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_11_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_11_PE: PE associated with this BDF.
8:23	RW	CONFIG_BDF2PE_11_BDF: BDF mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 1 BDF2PE Configuration 2 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.BDF2PE_12_CONFIG
Address	000000000501118F (SCOM)
Description	This register configures BDF-to-PE mapping #2 for brick 1. **Note:** Across all six bricks of an NPU, each BDF can map to at most one PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_12_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_12_RESERVED: Reserved.
4:7	RW	CONFIG_BDF2PE_12_PE: PE associated with this BDF.
8:23	RW	CONFIG_BDF2PE_12_BDF: BDF mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	LPC Threshold Configuration Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.LPCTH_CONFIG
Address	0000000005011190 (SCOM)
Description	Threshold configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_LPCTH_BUSY_ENABLE: 0 = Disable thresholding. 1 = Enable thresholding.
1:3	RW	CONFIG_LPCTH_WINDOW_SELECT: 001 = 256 cycle window. 010 = 512 cycle window. 100 = 1024 cycle window.
4:13	RW	CONFIG_LPCTH_THRESH_0: Busy counter threshold 0. When this threshold is exceeded, the LPC_th field in the partial response ATAG is set to '01'.
14:23	RW	CONFIG_LPCTH_THRESH_1: Busy counter threshold 1. When this threshold is exceeded, the LPC_th field in the partial response ATAG is set to '10'.
24:33	RW	CONFIG_LPCTH_THRESH_2: Busy counter threshold 2. When this threshold is exceeded, the LPC_th field in the partial response ATAG is set to '11'.
34:35	RW	CONFIG_LPCTH_RESERVED1: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.INHIBIT_CONFIG
Address	0000000005011191 (SCOM)
Description	This register configures inhibits for CQ_CTL.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre-frequency 0: 0 = SM0 timer tick. 1 = Inverted SM0 timer tick. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$

Bits	SCOM	Field Mnemonic: Description
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre frequency 0: 0 = SM1 timer tick. 1 = Inverted SM1 timer tick. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CQ_CTL Status Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CTL_STATUS
Address	0000000005011192 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	CTL_STATUS_SM_MMIO0: Set to 1 when SM slice 0 has an MMIO pending.
1	ROX	CTL_STATUS_SM_MMIO1: Set to 1 when SM slice 1 has an MMIO pending.
2	ROX	CTL_STATUS_SM_MMIO2: Set to 1 when SM slice 2 has an MMIO pending.
3	ROX	CTL_STATUS_SM_MMIO3: Set to 1 when SM slice 3 has an MMIO pending.
4:7	ROX	CTL_STATUS_MRBGP: Master retry back-off level for group-pump commands.
8:11	ROX	CTL_STATUS_MRBSP: Master retry back-off level for system-pump commands.
12:15	ROX	CTL_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 1001 = Fenced state, fence sequencing complete. 1100 = Half-fenced state, NTL is not fenced. others = In transition between fenced and not fenced.
16:19	ROX	CTL_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 1001 = Fenced state, fence sequencing complete. 1100 = Half-fenced state, NTL is not fenced. others = In transition between fenced and not fenced.
20:21	ROX	CTL_STATUS_LPCTH: LPC threshold value driven in partial responses.
22:26	ROX	CTL_STATUS_PBM_STATE: PB-MMIO/GenId state (0b00000 = Idle).
27	ROX	CTL_STATUS_BRK0_RLX: Set to 1 when brick 0 Gen-Id/relaxed ordering is idle.
28	ROX	CTL_STATUS_BRK1_RLX: Set to 1 when brick 1 Gen-Id/relaxed ordering is idle.
29	ROX	CTL_STATUS_BRK0_NVL: Set to 1 when brick 0 NVLink flush is idle.
30	ROX	CTL_STATUS_BRK1_NVL: Set to 1 when brick 1 NVLink flush is idle.
31	ROX	CTL_STATUS_ATS_SYNC: Set to 1 when AT sync is idle.
32	ROX	CTL_STATUS_NMMU: Set to 1 when NMMU outbound message is idle.
33	ROX	CTL_STATUS_PBLN: Set to 1 when the outbound processor bus Ln scope queue is empty.

Bits	SCOM	Field Mnemonic: Description
34	ROX	CTL_STATUS_PBNNG: Set to 1 when the outbound processor bus Nn/G scope queue is empty.
35	ROX	CTL_STATUS_PBRNVG: Set to 1 when the outbound processor bus Rn/Vg scope queue is empty.
36	ROX	CTL_STATUS_NVREQ0: Set to 1 when the outbound brick 0 request queue is empty.
37	ROX	CTL_STATUS_NVDGD0: Set to 1 when the outbound brick 0 downgrade queue is empty.
38	ROX	CTL_STATUS_NVREQ1: Set to 1 when the outbound brick 1 request queue is empty.
39	ROX	CTL_STATUS_NVDGD1: Set to 1 when the outbound brick 1 downgrade queue is empty.
40	ROX	CTL_STATUS_ATSREQ: Set to 1 when the outbound ATS TCE translate request queue is empty.
41	ROX	CTL_STATUS_MMIO: Set to 1 when the MMIO/GenId state machine is idle.
42	ROX	CTL_STATUS_PBRS: Set to 1 when the outbound PB response/merge queue is empty.
43	ROX	CTL_STATUS_NVRS0: Set to 1 when the outbound brick 0 response queue is empty.
44	ROX	CTL_STATUS_NVRS1: Set to 1 when the outbound brick 0 response queue is empty.
45	ROX	CTL_STATUS_XARS: Set to 1 when the outbound ATS/MISC response queue is empty.
46	ROX	CTL_STATUS_ATRR: Set to 1 when the outbound ATR response logic is idle.
47	ROX	CTL_STATUS_RESERVED1: Reserved.
48:63	RO	Constant = 0b0000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CERR_MESSAGE0
Address	0000000005011198 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CERR_MESSAGE1
Address	0000000005011199 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CERR_FIRST0
Address	000000000501119A (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_0: NCF0 SM0 NCF error.

Bits	SCOM	Field Mnemonic: Description
1	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_1: NCF1 SM1 NCF error.
2	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_2: NCF2 SM2 NCF error.
3	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_3: NCF3 SM3 NCF error.
4	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_4: NCF4 (Reserved).
5	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_5: NCF5 (Reserved).
6	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_6: NCF6 (Reserved).
7	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_7: NCF7 (Reserved).
8	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_0: NVF0 SM0 NVF error.
9	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_1: NVF1 SM1 NVF error.
10	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_2: NVF2 SM2 NVF error.
11	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_3: NVF3 SM3 NVF error.
12	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_4: NVF4 Illegal Probe.MO: Probe.MO received with illegal probe state.
13	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_5: NVF5 Illegal Probe.N: Probe.N received with illegal probe state.
14	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_6: NVF6 Illegal Atomic: Illegal atomic command for Atomic.NR with red = 1.
15	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_7: NVF7 Illegal Atomic: Atomic.NR with red = 0.
16	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_8: NVF8 Illegal Atomic: Atomic.NR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
17	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_9: NVF9 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 0.
18	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_10: NVF10 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 1.
19	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_11: NVF11 Illegal Atomic: Atomic.RR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
20	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_12: NVF12 Illegal ExCmd for Cmd = ExCmd-CREQ.
21	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_13: NVF13 Illegal ExCmd for Cmd = ExCmd-ATR.
22	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_14: NVF14 Illegal command or RMW with illegal length.
23	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_15: NVF15 BDF-to-PE look-up failed.
24	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_16: NVF16 Received a 256B FO = 1 Write.
25	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_17: NVF17 Received an invalid AddrType field, neither 00 or 11.
26	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_18: NVF18 Received an invalid transaction ID in a NVLink response.
27	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_19: NVF19 Received a rsp_status of target error in an ATSD response.
28	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_20: NVF20 Received a rsp_status of unsupported request in an ATSD response.
29	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_21: NVF21 Received a rsp_status of '11' (reserved value) in an ATSD response.
30	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_22: NVF22 Brick 0 NVF error occurred.
31	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_23: NVF23 Brick 1 NVF error occurred.
32	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_0: RSV10 (Reserved).
33	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_1: RSV11 (Reserved).
34	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_2: RSV12 (Reserved).
35	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_3: RSV13 (Reserved).
36	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_0: ASBE0 SM0 ASBE error.
37	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_1: ASBE1 SM1 ASBE error.

Bits	SCOM	Field Mnemonic: Description
38	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_2: ASBE2 SM2 ASBE error.
39	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_3: ASBE3 SM3 ASBE error.
40	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_4: ASBE4 processor bus MMIO data ECC CE error.
41	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_5: ASBE5 (Reserved).
42	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_6: ASBE6 (Reserved).
43	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_7: ASBE7 (Reserved).
44	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_0: PBR0 SM0 PBR error.
45	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_1: PBR1 SM1 PBR error.
46	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_2: PBR2 SM2 PBR error.
47	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_3: PBR3 SM3 PBR error.
48	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_4: PBR4 (Reserved).
49	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_0: REG0 SM0 REG error.
53	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_1: REG1 SM1 REG error.
54	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_2: REG2 SM2 REG error.
55	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_3: REG3 SM3 REG error.
56	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_0: DUE0 Processor bus MMIO data ECC UE error.
57	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_1: DUE1 Processor bus MMIO data ECC SUE error.
58	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_2: DUE2 (Reserved).
59	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_3: DUE3 (Reserved).
60	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_0: PEF0 Brick 0 received a request to a frozen BDF/PE.
61	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_1: PEF1 Brick 1 received a request to a frozen BDF/PE.
62	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_2: PEF2 (Reserved).
63	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_3: PEF3 (Reserved).

Register Name	CERR First 1 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CERR_FIRST1
Address	000000000501119B (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_0: NLG0 SM0 NLG error.
1	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_1: NLG1 SM1 NLG error.
2	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_2: NLG2 SM2 NLG error.
3	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_3: NLG3 SM3 NLG error.
4	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_4: NLG4 Processor bus MMIO state machine invalid state.
5	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_5: NLG5 Buffer used for PB response before NTL finished writing data.

Bits	SCOM	Field Mnemonic: Description
6	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_6: NLG6 Buffer read before NTL finished writing data.
7	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_7: NLG7 Invalid state in data read state machine.
8	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_8: NLG8 Attempt to send NV request with unknown NMCMD_ command type.
9	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_9: NLG9 Attempt to send NV response with unknown NRTYPE_ response type.
10	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_10: NLG10 Invalid state in XA response state machine.
11	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_11: NLG11 (Reserved).
12	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_12: NLG12 (Reserved).
13	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_13: NLG13 (Reserved).
14	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_14: NLG14 (Reserved).
15	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_15: NLG15 (Reserved).
16	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_0: FWD0 SM0 FWD error.
17	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_1: FWD1 SM1 FWD error.
18	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_2: FWD2 SM2 FWD error.
19	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_3: FWD3 SM3 FWD error.
20	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_4: FWD4 (Reserved).
21	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_5: FWD5 (Reserved).
22	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_6: FWD6 (Reserved).
23	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_7: FWD7 (Reserved).
24	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_0: AUE0 SM0 AUE error.
25	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_1: AUE1 SM1 AUE error.
26	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_2: AUE2 SM2 AUE error.
27	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_3: AUE3 SM3 AUE error.
28	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_4: AUE4 (Reserved).
29	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_5: AUE5 (Reserved).
30	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_6: AUE6 (Reserved).
31	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_7: AUE7 (Reserved).
32	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_0: PBP0 SM0 PBP error.
33	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_1: PBP1 SM1 PBP error.
34	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_2: PBP2 SM2 PBP error.
35	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_3: PBP3 SM3 PBP error.
36	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_4: PBP4 (Reserved).
37	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_5: PBP5 (Reserved).
38	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_6: PBP6 (Reserved).
39	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_7: PBP7 (Reserved).
40	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_0: PBF0 SM0 PBF error.
41	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_1: PBF1 SM1 PBF error.
42	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_2: PBF2 SM2 PBF error.
43	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_3: PBF3 SM3 PBF error.

Bits	SCOM	Field Mnemonic: Description
44	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_4: PBR4 (Reserved).
45	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_5: PBR5 (Reserved).
46	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_6: PBR6 (Reserved).
47	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_7: PBR7 (Reserved).
48	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_0: PBC0 SM0 PBC error.
49	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_1: PBC1 SM1 PBC error.
50	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_2: PBC2 SM2 PBC error.
51	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_3: PBC3 SM3 PBC error.
52	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_4: PBC4 (Reserved).
53	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_5: PBC5 (Reserved).
54	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_6: PBC6 (Reserved).
55	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_7: PBC7 (Reserved).
56	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_0: RSV20 SM0 RSV2 error.
57	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_1: RSV21 SM1 RSV2 error.
58	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_2: RSV22 SM2 RSV2 error.
59	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_3: RSV23 SM3 RSV2 error.
60	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_0: RSV30 (Reserved).
61	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_1: RSV31 (Reserved).
62	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_2: RSV32 (Reserved).
63	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_3: RSV33 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK1.CS.CTL.MISC.CERR_MASK0
Address	000000000501119C (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_CTL_MASK_NCF_0: NCF0 SM0 NCF error.
1	RW	IDIAL_CTL_MASK_NCF_1: NCF1 SM1 NCF error.
2	RW	IDIAL_CTL_MASK_NCF_2: NCF2 SM2 NCF error.
3	RW	IDIAL_CTL_MASK_NCF_3: NCF3 SM3 NCF error.
4	RW	IDIAL_CTL_MASK_NCF_4: NCF4 (Reserved).
5	RW	IDIAL_CTL_MASK_NCF_5: NCF5 (Reserved).
6	RW	IDIAL_CTL_MASK_NCF_6: NCF6 (Reserved).
7	RW	IDIAL_CTL_MASK_NCF_7: NCF7 (Reserved).
8	RW	IDIAL_CTL_MASK_NVF_0: NVF0 SM0 NVF error.
9	RW	IDIAL_CTL_MASK_NVF_1: NVF1 SM1 NVF error.
10	RW	IDIAL_CTL_MASK_NVF_2: NVF2 SM2 NVF error.
11	RW	IDIAL_CTL_MASK_NVF_3: NVF3 SM3 NVF error.

Bits	SCOM	Field Mnemonic: Description
12	RW	IDIAL_CTL_MASK_NVF_4: NVF4 Illegal Probe.MO: Probe.MO received with illegal probe state.
13	RW	IDIAL_CTL_MASK_NVF_5: NVF5 Illegal Probe.N: Probe.N received with illegal probe state.
14	RW	IDIAL_CTL_MASK_NVF_6: NVF6 Illegal Atomic: Illegal atomic command for Atomic.NR with red = 1.
15	RW	IDIAL_CTL_MASK_NVF_7: NVF7 Illegal Atomic: Atomic.NR with red = 0.
16	RW	IDIAL_CTL_MASK_NVF_8: NVF8 Illegal Atomic: Atomic.NR with atomic size /=4 or 8 or with non-4/8 byte-enables.
17	RW	IDIAL_CTL_MASK_NVF_9: NVF9 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 0.
18	RW	IDIAL_CTL_MASK_NVF_10: NVF10 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 1.
19	RW	IDIAL_CTL_MASK_NVF_11: NVF11 Illegal Atomic: Atomic.RR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
20	RW	IDIAL_CTL_MASK_NVF_12: NVF12 Illegal ExCmd for Cmd = ExCmd-CREQ.
21	RW	IDIAL_CTL_MASK_NVF_13: NVF13 Illegal ExCmd for Cmd = ExCmd-ATR.
22	RW	IDIAL_CTL_MASK_NVF_14: NVF14 Illegal command or RMW with illegal length.
23	RW	IDIAL_CTL_MASK_NVF_15: NVF15 BDF-to-PE look-up failed.
24	RW	IDIAL_CTL_MASK_NVF_16: NVF16 Received a 256B FO = 1 write.
25	RW	IDIAL_CTL_MASK_NVF_17: NVF17 Received an invalid AddrType field, neither 00 or 11.
26	RW	IDIAL_CTL_MASK_NVF_18: NVF18 Received an invalid transaction ID in a NVLink response.
27	RW	IDIAL_CTL_MASK_NVF_19: NVF19 Received a rsp_status of target error in an ATSD response.
28	RW	IDIAL_CTL_MASK_NVF_20: NVF20 Received a rsp_status of unsupported request in an ATSD response.
29	RW	IDIAL_CTL_MASK_NVF_21: NVF21 Received a rsp_status of '11' (reserved value) in an ATSD response.
30	RW	IDIAL_CTL_MASK_NVF_22: NVF22 Brick 0 NVF error occurred.
31	RW	IDIAL_CTL_MASK_NVF_23: NVF23 Brick 1 NVF error occurred.
32	RW	IDIAL_CTL_MASK_RSV1_0: RSV10 (Reserved).
33	RW	IDIAL_CTL_MASK_RSV1_1: RSV11 (Reserved).
34	RW	IDIAL_CTL_MASK_RSV1_2: RSV12 (Reserved).
35	RW	IDIAL_CTL_MASK_RSV1_3: RSV13 (Reserved).
36	RW	IDIAL_CTL_MASK_ASBE_0: ASBE0 SM0 ASBE error.
37	RW	IDIAL_CTL_MASK_ASBE_1: ASBE1 SM1 ASBE error.
38	RW	IDIAL_CTL_MASK_ASBE_2: ASBE2 SM2 ASBE error.
39	RW	IDIAL_CTL_MASK_ASBE_3: ASBE3 SM3 ASBE error.
40	RW	IDIAL_CTL_MASK_ASBE_4: ASBE4 processor bus MMIO data ECC CE error.
41	RW	IDIAL_CTL_MASK_ASBE_5: ASBE5 (Reserved).
42	RW	IDIAL_CTL_MASK_ASBE_6: ASBE6 (Reserved).
43	RW	IDIAL_CTL_MASK_ASBE_7: ASBE7 (Reserved).
44	RW	IDIAL_CTL_MASK_PBR_0: PBR0 SM0 PBR error.
45	RW	IDIAL_CTL_MASK_PBR_1: PBR1 SM1 PBR error.
46	RW	IDIAL_CTL_MASK_PBR_2: PBR2 SM2 PBR error.
47	RW	IDIAL_CTL_MASK_PBR_3: PBR3 SM3 PBR error.
48	RW	IDIAL_CTL_MASK_PBR_4: PBR4 (Reserved).
49	RW	IDIAL_CTL_MASK_PBR_5: PBR5 (Reserved).

Bits	SCOM	Field Mnemonic: Description
50	RW	IDIAL_CTL_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_CTL_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_CTL_MASK_REG_0: REG0 SM0 REG error.
53	RW	IDIAL_CTL_MASK_REG_1: REG1 SM1 REG error.
54	RW	IDIAL_CTL_MASK_REG_2: REG2 SM2 REG error.
55	RW	IDIAL_CTL_MASK_REG_3: REG3 SM3 REG error.
56	RW	IDIAL_CTL_MASK_DUE_0: DUE0 Processor bus MMIO data ECC UE error.
57	RW	IDIAL_CTL_MASK_DUE_1: DUE1 Processor bus MMIO data ECC SUE error.
58	RW	IDIAL_CTL_MASK_DUE_2: DUE2 (Reserved).
59	RW	IDIAL_CTL_MASK_DUE_3: DUE3 (Reserved).
60	RW	IDIAL_CTL_MASK_PEF_0: PEF0 Brick 0 received a request to a frozen BDF/PE.
61	RW	IDIAL_CTL_MASK_PEF_1: PEF1 Brick 1 received a request to a frozen BDF/PE.
62	RW	IDIAL_CTL_MASK_PEF_2: PEF2 (Reserved).
63	RW	IDIAL_CTL_MASK_PEF_3: PEF3 (Reserved).

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK1.CS.CTL.MISC.CERR_MASK1
Address	000000000501119D (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_CTL_MASK_NLG_0: NLG0 SM0 NLG error.
1	RW	IDIAL_CTL_MASK_NLG_1: NLG1 SM1 NLG error.
2	RW	IDIAL_CTL_MASK_NLG_2: NLG2 SM2 NLG error.
3	RW	IDIAL_CTL_MASK_NLG_3: NLG3 SM3 NLG error.
4	RW	IDIAL_CTL_MASK_NLG_4: NLG4 Processor bus MMIO state machine invalid state.
5	RW	IDIAL_CTL_MASK_NLG_5: NLG5 Buffer used for PB response before NTL finished writing data.
6	RW	IDIAL_CTL_MASK_NLG_6: NLG6 Buffer read before NTL finished writing data.
7	RW	IDIAL_CTL_MASK_NLG_7: NLG7 Invalid state in data read state machine.
8	RW	IDIAL_CTL_MASK_NLG_8: NLG8 Attempt to send NV request with unknown NMCMD_ command type.
9	RW	IDIAL_CTL_MASK_NLG_9: NLG9 Attempt to send NV response with unknown NRTYPE_ response type.
10	RW	IDIAL_CTL_MASK_NLG_10: NLG10 Invalid state in XA response state machine.
11	RW	IDIAL_CTL_MASK_NLG_11: NLG11 (Reserved).
12	RW	IDIAL_CTL_MASK_NLG_12: NLG12 (Reserved).
13	RW	IDIAL_CTL_MASK_NLG_13: NLG13 (Reserved).
14	RW	IDIAL_CTL_MASK_NLG_14: NLG14 (Reserved).
15	RW	IDIAL_CTL_MASK_NLG_15: NLG15 (Reserved).
16	RW	IDIAL_CTL_MASK_FWD_0: FWD0 SM0 FWD error.
17	RW	IDIAL_CTL_MASK_FWD_1: FWD1 SM1 FWD error.

Bits	SCOM	Field Mnemonic: Description
18	RW	IDIAL_CTL_MASK_FWD_2: FWD2 SM2 FWD error.
19	RW	IDIAL_CTL_MASK_FWD_3: FWD3 SM3 FWD error.
20	RW	IDIAL_CTL_MASK_FWD_4: FWD4 (Reserved).
21	RW	IDIAL_CTL_MASK_FWD_5: FWD5 (Reserved).
22	RW	IDIAL_CTL_MASK_FWD_6: FWD6 (Reserved).
23	RW	IDIAL_CTL_MASK_FWD_7: FWD7 (Reserved).
24	RW	IDIAL_CTL_MASK_AUE_0: AUE0 SM0 AUE error.
25	RW	IDIAL_CTL_MASK_AUE_1: AUE1 SM1 AUE error.
26	RW	IDIAL_CTL_MASK_AUE_2: AUE2 SM2 AUE error.
27	RW	IDIAL_CTL_MASK_AUE_3: AUE3 SM3 AUE error.
28	RW	IDIAL_CTL_MASK_AUE_4: AUE4 (Reserved).
29	RW	IDIAL_CTL_MASK_AUE_5: AUE5 (Reserved).
30	RW	IDIAL_CTL_MASK_AUE_6: AUE6 (Reserved).
31	RW	IDIAL_CTL_MASK_AUE_7: AUE7 (Reserved).
32	RW	IDIAL_CTL_MASK_PBP_0: PBP0 SM0 PBP error.
33	RW	IDIAL_CTL_MASK_PBP_1: PBP1 SM1 PBP error.
34	RW	IDIAL_CTL_MASK_PBP_2: PBP2 SM2 PBP error.
35	RW	IDIAL_CTL_MASK_PBP_3: PBP3 SM3 PBP error.
36	RW	IDIAL_CTL_MASK_PBP_4: PBP4 (Reserved).
37	RW	IDIAL_CTL_MASK_PBP_5: PBP5 (Reserved).
38	RW	IDIAL_CTL_MASK_PBP_6: PBP6 (Reserved).
39	RW	IDIAL_CTL_MASK_PBP_7: PBP7 (Reserved).
40	RW	IDIAL_CTL_MASK_PBF_0: PBF0 SM0 PBF error.
41	RW	IDIAL_CTL_MASK_PBF_1: PBF1 SM1 PBF error.
42	RW	IDIAL_CTL_MASK_PBF_2: PBF2 SM2 PBF error.
43	RW	IDIAL_CTL_MASK_PBF_3: PBF3 SM3 PBF error.
44	RW	IDIAL_CTL_MASK_PBF_4: PBR4 (Reserved).
45	RW	IDIAL_CTL_MASK_PBF_5: PBR5 (Reserved).
46	RW	IDIAL_CTL_MASK_PBF_6: PBR6 (Reserved).
47	RW	IDIAL_CTL_MASK_PBF_7: PBR7 (Reserved).
48	RW	IDIAL_CTL_MASK_PBC_0: PBC0 SM0 PBC error.
49	RW	IDIAL_CTL_MASK_PBC_1: PBC1 SM1 PBC error.
50	RW	IDIAL_CTL_MASK_PBC_2: PBC2 SM2 PBC error.
51	RW	IDIAL_CTL_MASK_PBC_3: PBC3 SM3 PBC error.
52	RW	IDIAL_CTL_MASK_PBC_4: PBC4 (Reserved).
53	RW	IDIAL_CTL_MASK_PBC_5: PBC5 (Reserved).
54	RW	IDIAL_CTL_MASK_PBC_6: PBC6 (Reserved).
55	RW	IDIAL_CTL_MASK_PBC_7: PBC7 (Reserved).
56	RW	IDIAL_CTL_MASK_RSV2_0: RSV20 SM0 RSV2 error.

Bits	SCOM	Field Mnemonic: Description
57	RW	IDIAL_CTL_MASK_RSV2_1: RSV21 SM1 RSV2 error.
58	RW	IDIAL_CTL_MASK_RSV2_2: RSV22 SM2RSV2 error.
59	RW	IDIAL_CTL_MASK_RSV2_3: RSV23 SM3 RSV2 error.
60	RW	IDIAL_CTL_MASK_RSV3_0: RSV30 (Reserved).
61	RW	IDIAL_CTL_MASK_RSV3_1: RSV31 (Reserved).
62	RW	IDIAL_CTL_MASK_RSV3_2: RSV32 (Reserved).
63	RW	IDIAL_CTL_MASK_RSV3_3: RSV33 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CERR_HOLD0
Address	000000000501119E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_0: NCF0 SM0 NCF error.
1	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_1: NCF1 SM1 NCF error.
2	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_2: NCF2 SM2 NCF error.
3	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_3: NCF3 SM3 NCF error.
4	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_4: NCF4 (Reserved).
5	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_5: NCF5 (Reserved).
6	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_6: NCF6 (Reserved).
7	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_7: NCF7 (Reserved).
8	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_0: NVF0 SM0 NVF error.
9	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_1: NVF1 SM1 NVF error.
10	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_2: NVF2 SM2 NVF error.
11	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_3: NVF3 SM3 NVF error.
12	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_4: NVF4 Illegal Probe.MO: Probe.MO received with illegal probe state.
13	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_5: NVF5 Illegal Probe.N: Probe.N received with illegal probe state.
14	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_6: NVF6 Illegal Atomic: Illegal atomic command for Atomic.NR with red = 1.
15	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_7: NVF7 Illegal Atomic: Atomic.NR with red=0.
16	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_8: NVF8 Illegal Atomic: Atomic.NR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
17	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_9: NVF9 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 0.
18	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_10: NVF10 Illegal Atomic: Illegal atomic command for Atomic.RR with red = 1.
19	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_11: NVF11 Illegal Atomic: Atomic.RR with atomic size /= 4 or 8 or with non-4/8 byte-enables.
20	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_12: NVF12 Illegal ExCmd for Cmd=ExCmd-CREQ.
21	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_13: NVF13 Illegal ExCmd for Cmd=ExCmd-ATR.
22	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_14: NVF14 Illegal command or RMW with illegal length.
23	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_15: NVF15 BDF-to-PE look-up failed.

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_16: NVF16 Received a 256B FO = 1 write.
25	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_17: NVF17 Received an invalid AddrType field, neither 00 or 11.
26	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_18: NVF18 Received an invalid transaction ID in a NVLink response.
27	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_19: NVF19 Received a rsp_status of target error in an ATSD response.
28	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_20: NVF20 Received a rsp_status of unsupported request in an ATSD response.
29	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_21: NVF21 Received a rsp_status of '11' (reserved value) in an ATSD response.
30	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_22: NVF22 Brick 0 NVF error occurred.
31	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_23: NVF23 Brick 1 NVF error occurred.
32	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_0: RSV10 (Reserved).
33	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_1: RSV11 (Reserved).
34	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_2: RSV12 (Reserved).
35	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_3: RSV13 (Reserved).
36	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_0: ASBE0 SM0 ASBE error.
37	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_1: ASBE1 SM1 ASBE error.
38	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_2: ASBE2 SM2 ASBE error.
39	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_3: ASBE3 SM3 ASBE error.
40	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_4: ASBE4 processor bus MMIO data ECC CE error.
41	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_5: ASBE5 (Reserved).
42	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_6: ASBE6 (Reserved).
43	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_7: ASBE7 (Reserved).
44	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_0: PBR0 SM0 PBR error.
45	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_1: PBR1 SM1 PBR error.
46	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_2: PBR2 SM2 PBR error.
47	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_3: PBR3 SM3 PBR error.
48	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_4: PBR4 (Reserved).
49	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_0: REG0 SM0 REG error.
53	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_1: REG1 SM1 REG error.
54	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_2: REG2 SM2 REG error.
55	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_3: REG3 SM3 REG error.
56	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_0: DUE0 Processor bus MMIO data ECC UE error.
57	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_1: DUE1 Processor bus MMIO data ECC SUE error.
58	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_2: DUE2 (Reserved).
59	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_3: DUE3 (Reserved).
60	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_0: PEF0 Brick 0 received a request to a frozen BDF/PE.
61	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_1: PEF1 Brick 1 received a request to a frozen BDF/PE.

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_2: PEF2 (Reserved).
63	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_3: PEF3 (Reserved).

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK1.CS.CTL.MISC.CERR_HOLD1
Address	000000000501119F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_0: NLG0 SM0 NLG error.
1	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_1: NLG1 SM1 NLG error.
2	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_2: NLG2 SM2 NLG error.
3	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_3: NLG3 SM3 NLG error.
4	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_4: NLG4 Processor bus MMIO state machine invalid state.
5	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_5: NLG5 Buffer used for PB response before NTL finished writing data.
6	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_6: NLG6 Buffer read before NTL finished writing data.
7	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_7: NLG7 Invalid state in data read state machine.
8	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_8: NLG8 Attempt to send NV request with unknown NMCMD_ command type.
9	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_9: NLG9 Attempt to send NV response with unknown NRTYPE_ response type.
10	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_10: NLG10 Invalid state in XA response state machine.
11	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_11: NLG11 (Reserved).
12	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_12: NLG12 (Reserved).
13	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_13: NLG13 (Reserved).
14	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_14: NLG14 (Reserved).
15	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_15: NLG15 (Reserved).
16	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_0: FWD0 SM0 FWD error.
17	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_1: FWD1 SM1 FWD error.
18	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_2: FWD2 SM2 FWD error.
19	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_3: FWD3 SM3 FWD error.
20	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_4: FWD4 (Reserved).
21	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_5: FWD5 (Reserved).
22	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_6: FWD6 (Reserved).
23	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_7: FWD7 (Reserved).
24	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_0: AUE0 SM0 AUE error.
25	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_1: AUE1 SM1 AUE error.
26	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_2: AUE2 SM2 AUE error.
27	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_3: AUE3 SM3 AUE error.
28	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_4: AUE4 (Reserved).

Bits	SCOM	Field Mnemonic: Description
29	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_5: AUE5 (Reserved).
30	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_6: AUE6 (Reserved).
31	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_7: AUE7 (Reserved).
32	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_0: PBP0 SM0 PBP error.
33	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_1: PBP1 SM1 PBP error.
34	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_2: PBP2 SM2 PBP error.
35	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_3: PBP3 SM3 PBP error.
36	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_4: PBP4 (Reserved).
37	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_5: PBP5 (Reserved).
38	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_6: PBP6 (Reserved).
39	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_7: PBP7 (Reserved).
40	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_0: PBF0 SM0 PBF error.
41	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_1: PBF1 SM1 PBF error.
42	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_2: PBF2 SM2 PBF error.
43	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_3: PBF3 SM3 PBF error.
44	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_4: PBR4 (Reserved).
45	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_5: PBR5 (Reserved).
46	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_6: PBR6 (Reserved).
47	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_7: PBR7 (Reserved).
48	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_0: PBC0 SM0 PBC error.
49	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_1: PBC1 SM1 PBC error.
50	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_2: PBC2 SM2 PBC error.
51	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_3: PBC3 SM3 PBC error.
52	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_4: PBC4 (Reserved).
53	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_5: PBC5 (Reserved).
54	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_6: PBC6 (Reserved).
55	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_7: PBC7 (Reserved).
56	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_0: RSV20 SM0 RSV2 error.
57	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_1: RSV21 SM1 RSV2 error.
58	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_2: RSV22 SM2 RSV2 error.
59	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_3: RSV23 SM3 RSV2 error.
60	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_0: RSV30 (Reserved).
61	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_1: RSV31 (Reserved).
62	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_2: RSV32 (Reserved).
63	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_3: RSV33 (Reserved).

Register Name	CQ_DAT Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK1.DAT.MISC.CONFIG1
Address	00000000050111A1 (SCOM)
Description	CQ_DAT miscellaneous configuration register 1.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG1_MGR_CREDIT: CTL to DAT merge request interface number of credits.
2:4	RW	CONFIG1_MRG_PBTX_NBUF: CTL to DAT merge request Power bus TX interface logic request buffer size.
5:8	RW	CONFIG1_MRG_RDBF_NBUF: CTL to DAT merge request Power bus TX array read logic request buffer size.
9:12	RW	CONFIG1_MRG_IBWR_NBUF: CTL to DAT merge request BE merge/OI loopback/AMO inbound buffer write logic request buffer size.
13:15	RW	CONFIG1_MRG_IBRD_NBUF: CTL to DAT merge request BE merge/IO loopback/AMO inbound buffer read logic request buffer size.
16:18	RW	CONFIG1_MRG_BBRD_NBUF: CTL to DAT merge request BE merge BE buffer read logic request buffer size.
19:21	RW	CONFIG1_MRG_OBRD_NBUF: CTL to DAT merge request BE merge/OI loopback/AMO outbound buffer read logic request buffer size.
22	RW	CONFIG1_MRG_CR_DIS: Writing a 1 disables CQ_DAT to send credits to CTL for merge operations.
23	RW	CONFIG1_MRG_CTLW_CR_DIS: Writing a 1 disables the CQ_DAT to send credits to CTL for inbound buffer write operations.
24:25	RW	CONFIG1_NTLR_PAUSE_THRESH: Specifies the number of outbound buffer NTL port occupation cycles before raising NTL pause request: 00 = 32 cycles. 01 = 16 cycles. 10 = 8 cycles. 11b = Never.
26:27	RW	CONFIG1_CTLR_HP_THRESH: Specifies the number of outbound buffer CTL read wait cycles before giving high priority: 00 = 16 cycles. 01 = 8 cycles 10 = 4 cycles. 11 = Never.
28:29	RW	CONFIG1_NTLW_PAUSE_THRESH: Specifies the number of inbound buffer NTL port occupation cycles before raising NTL pause request: 00 = 16 cycles. 01 = 8 cycles. 10 = 4 cycles. 11 = Never.
30:31	RW	CONFIG1_CTLW_HP_THRESH: Specifies the number of inbound buffer CTL write wait cycles before giving high priority: 00 = 16 cycles. 01 = 8 cycles. 10 = 4 cycles. 11 = Never.
32	RW	CONFIG1_PBTX_REDUCE_RTAG: Writing a 1 has the CQ_DAT limit number of outstanding RTAGs to 1 on PB transmit interface (default is 2).
33	RW	CONFIG1_PBTX_DELAY_BDONE: Writing a 1 has the CQ_DAT PB transmit logic wait until all the OW is presented on the PB before raising BuffDone to CTL.
34	RW	CONFIG1_PBTX_FLIP_IMIN_BIG: Writing a 1 has the CQ_DAT PB transmit logic flip the endian of the integer minimum value on failed inc/dec when e = 0 is specified.

Bits	SCOM	Field Mnemonic: Description
35	RW	CONFIG1_PBTX_FLIP_IMIN_LITTLE: Writing a 1 has the CQ_DAT PB transmit logic flip the endian of the integer minimum value on failed inc/dec when e = 1 is specified.
36	RW	CONFIG1_ALU_SAFE_LATENCY: Writing a 1 has the CQ_DAT wait for one more cycle for ALU output in case x2 phase detection logic goes wrong.
37	RW	CONFIG1_ALU_FLIP_ENDIAN_BIG: Writing a 1 has the CQ_DAT flip the ALU endian when e = 0 is specified.
38	RW	CONFIG1_ALU_FLIP_ENDIAN_LITTLE: Writing a 1 has the CQ_DAT flip the ALU endian when e = 1 is specified.
39	RW	CONFIG1_PBTX_EARLY_AFTAG: Writing a 1 has the CQ_DAT raise BuffDone to CTL earlier for armwf_* operations. CQ_DAT does not wait for fetch data to be presented on the PB. However, CQ_DAT does wait for fetch data to leave the inbound buffer, that is the buffer entry can still be safely reused. This bit can be randomized in verification.
40:63	RW	CONFIG1_RESERVED1: Reserved.

Register Name	**CQ_DAT ECC Configuration Register**
Mnemonic	NPU.STCK1.DAT.MISC.ECC_CONFIG
Address	00000000050111A2 (SCOM)
Description	CQ_DAT ECC configuration register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ECC_CONFIG_PBTX_AMO_IGNORE_XUE: For armwf_inc/dec types, replace PB transmit data with negative maximum value when comparison fails, even if the data has UE or SUE. The negative maximum value is marked with SUE as long as suedis_pt = 0.
1	RW	ECC_CONFIG_SUE_DIS_BR_PERR: Writing a 1 disables marking merge result data with SUE when BE buffer read data latch has parity error.
2	RW	ECC_CONFIG_SUE_DIS_IR_PERR: Writing a 1 disables marking merge result data with SUE when inbound buffer read data latch has parity error.
3	RW	ECC_CONFIG_SUE_DIS_OR_PERR: Writing a 1 disables marking merge result data with SUE when the outbound buffer read data latch has parity error.
4	RW	ECC_CONFIG_CORR_DIS_PT: Writing a 1 disables ECC correction in Power bus TX.
5	RW	ECC_CONFIG_CORR_DIS_PR: Writing a 1 disables ECC correction in Power bus RX.
6	RW	ECC_CONFIG_CORR_DIS_BR: Writing a 1 disables ECC correction in byte enable buffer read.
7	RW	ECC_CONFIG_CORR_DIS_IR: Writing a 1 disables ECC correction in merge operation inbound buffer read.
8	RW	ECC_CONFIG_CORR_DIS_OR: Writing a 1 disables ECC correction in merge operation outbound buffer read.
9	RW	ECC_CONFIG_SUE_DIS_PT: Writing a 1 disables converting ECC UE to SUE in Power bus TX.
10	RW	ECC_CONFIG_SUE_DIS_PR: Writing a 1 disables converting ECC UE to SUE in Power bus RX.
11	RW	ECC_CONFIG_SUE_DIS_BR: Writing a 1 disables converting ECC UE to SUE in byte enable buffer read.
12	RW	ECC_CONFIG_SUE_DIS_IR: Writing a 1 disables converting ECC UE to SUE in merge operation inbound buffer read.
13	RW	ECC_CONFIG_SUE_DIS_OR: Writing a 1 disables converting ECC UE to SUE in merge operation outbound buffer read.
14:31	RW	ECC_CONFIG_RESERVED: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CQ_DAT Scratch 0 Register
Mnemonic	NPU.STCK1.DAT.MISC.SCRATCH0
Address	00000000050111A3 (SCOM)
Description	CQ_DAT scratch register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	SCRATCH0_IDIAL: Scratch register.

Register Name	CQ_DAT CERR ECC Hold Register
Mnemonic	NPU.STCK1.DAT.MISC.CERR_ECC_HOLD
Address	00000000050111A4 (SCOM)
Description	CQ_DAT ECC error c_err_rpt status and clear register.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:13	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PT_UE: ECC UE on Power bus TX data path (4 ECC words).
14:17	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PR_UE: ECC UE on Power bus RX data path (4 ECC words).
18:19	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_BR_UE: ECC UE on byte enable buffer read data path (2 ECC words).
20:23	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_IR_UE: ECC UE on merge operation inbound buffer read data path (4 ECC words).
24:27	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_OR_UE: ECC UE on merge operation outbound buffer read data path (4 ECC words).
28:31	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PT_SUE: ECC SUE on Power bus TX data path (4 ECC words).
32:35	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PR_SUE: ECC SUE on Power bus RX data path (4 ECC words).
36:37	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_BR_SUE: ECC SUE on byte enable buffer read data path (2 ECC words).
38:41	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_IR_SUE: ECC SUE on merge operation inbound buffer read data path (4 ECC words).
42:45	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_OR_SUE: ECC SUE on merge operation outbound buffer read data path (4 ECC words).
46:49	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PT_CE: ECC CE on Power bus TX data path (4 ECC words).
50:53	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PR_CE: ECC CE on Power bus RX data path (4 ECC words).
54:55	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_BR_CE: ECC CE on byte enable buffer read data path (2 ECC words).
56:59	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_IR_CE: ECC CE on merge operation inbound buffer read data path (4 ECC words).
60:63	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_OR_CE: ECC CE on merge operation outbound buffer read data path (4 ECC words).

Register Name	CQ_DAT CERR ECC Mask Register
Mnemonic	NPU.STCK1.DAT.MISC.CERR_ECC_MASK
Address	00000000050111A5 (SCOM)
Description	CQ_DAT ECC error c_err_rpt mask register.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:63	RW	CERR_ECC_MASK_BITS: CQ_DAT ECC error c_err_rpt mask bits.

Register Name	CQ_DAT CERR ECC First Register
Mnemonic	NPU.STCK1.DAT.MISC.CERR_ECC_FIRST
Address	00000000050111A6 (SCOM)
Description	CQ_DAT ECC error c_err_rpt first register.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:63	RWX_WCLEAR	CERR_ECC_FIRST_BITS: CQ_DAT ECC error c_err_rpt first error bits.

Register Name	CQ_DAT CERR Parity Hold Register
Mnemonic	NPU.STCK1.DAT.MISC.CERR_PTY_HOLD
Address	00000000050111A7 (SCOM)
Description	CQ_DAT parity error c_err_rpt status and clear register.

Bits	SCOM	Field Mnemonic: Description
0:36	RO	Constant = 0b000000000000000000000000000000000000
37	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_INHIBIT_CONFIG: Parity error on inhibit configuration register.
38	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_MISC_STATE: Parity error on critical state latches in the miscellaneous subunit.
39	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_MRG_STATE: Parity error on critical state latches in the merge subunit.
40	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_OBUF_STATE: Parity error on critical state latches in the outbound buffer subunit.
41	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_PBTX_STATE: Parity error on critical state latches in the PB transmit subunit.
42	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_RQIN_STATE: Parity error on critical state latches in the merge request buffer subunit.
43	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_IBUF_STATE: Parity error on critical state latches in the inbound buffer subunit.
44	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_ERRINJ: Parity error on ECC ERRINJ register.
45:48	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_PBTX_AMO: Parity error in PB transmit AMO inc/dec data path (4 words).
49:52	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_IBRD: Parity error in merge operation inbound buffer read data path (4 words).
53:56	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_OBRD: Parity error in merge operation outbound buffer read data path (4 words).
57:58	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_BBRD: Parity error in byte enable buffer read data path (2 words).
59	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_PBRX_RTAG: Parity error on received RTAG on the PB receive interface.
60	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_ECC_CONFIG: Parity error on ECC configuration register.
61	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_CONFIG1: Parity error on configuration 1 register.
62	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_DEBUG0_CONFIG: Parity error on debug 0 configuration register.

Bits	SCOM	Field Mnemonic: Description
63	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_DEBUG1_CONFIG: Parity error on debug 1 configuration register.

Register Name	CQ_DAT CERR Parity Mask Register
Mnemonic	NPU.STCK1.DAT.MISC.CERR_PTY_MASK
Address	00000000050111A8 (SCOM)
Description	CQ_DAT parity error c_err_rpt mask register.

Bits	SCOM	Field Mnemonic: Description
0:36	RO	Constant = 0b00000000000000000000000000000000000000
37:63	RW	CERR_PTY_MASK_BITS: CQ_DAT parity error c_err_rpt mask bits.

Register Name	CQ_DAT CERR Parity First Register
Mnemonic	NPU.STCK1.DAT.MISC.CERR_PTY_FIRST
Address	00000000050111A9 (SCOM)
Description	CQ_DAT parity error c_err_rpt first register.

Bits	SCOM	Field Mnemonic: Description
0:36	RO	Constant = 0b00000000000000000000000000000000000000
37:63	RWX_WCLEAR	CERR_PTY_FIRST_BITS: CQ_DAT parity error c_err_rpt first error bits.

Register Name	CQ_DAT CERR Logic Hold Register
Mnemonic	NPU.STCK1.DAT.MISC.CERR_LOG_HOLD
Address	00000000050111AA (SCOM)
Description	CQ_DAT logic error c_err_rpt status and clear register.

Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b00000000000000000000000000000000000000000000000
47	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_BBUF_RDWR: Logic error: Read/write conflict on BE buffer, the same buffer entry was read and written in the same cycle.
48	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_RDWR: Logic error: Read/write conflict on inbound buffer, the same buffer entry was read and written in the same cycle.
49	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_OBUF_RDWR: Logic error: Read/write conflict on outbound buffer, the same buffer entry was read and written in the same cycle.
50:55	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_RQIN_OVF: Logic error: Merge request buffer overflow in a merge pipeline: Bit 0 = Error in PB transmit request pipeline. Bit 1 = Error in PB transmit array read pipeline. Bit 2 = Error in merge inbound buffer write pipeline. Bit 3 = Error in merge inbound buffer read pipeline. Bit 4 = Error in merge BE buffer read pipeline. Bit 5 = Error in merge outbound buffer read pipeline.
56	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_CTL_PIPE: Logic error: inbound buffer CTL write request/data lost due to excessive incoming request.
57	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_PBTX_PIPE: Logic error: Pipeline overflow in PB transmit logic.

Bits	SCOM	Field Mnemonic: Description
58	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_MRG_IR_PIPE: Logic error: Pipeline overflow in merge inbound buffer read logic.
59	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_MRG_OR_PIPE: Logic error: Pipeline overflow in merge outbound buffer read logic.
60	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_AMO_ADDR: Logic error: Invalid address position within OW for armw_cas_t, armwf_inc_b, armwf_inc_e, and armwf_dec_b types.
61	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_PBRX_RTAG: Logic error: Invalid RTAG observed on the PB receive interface.
62	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_WRITE: Logic error: NTL/ CTL wrote inbound buffer entry 0 - 3 cycles after the same entry was read for PB TX.
63	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_WARB: Logic error: More than one write request granted on inbound buffer write port.

Register Name	CQ_DAT CERR Logic Mask Register
Mnemonic	NPU.STCK1.DAT.MISC.CERR_LOG_MASK
Address	00000000050111AB (SCOM)
Description	CQ_DAT logic error c_err_rpt mask register.

Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b00000000000000000000000000000000000000000000000
47:63	RW	CERR_LOG_MASK_BITS: CQ_DAT logic error c_err_rpt mask bits.

Register Name	CQ_DAT CERR Logic First Register
Mnemonic	NPU.STCK1.DAT.MISC.CERR_LOG_FIRST
Address	00000000050111AC (SCOM)
Description	CQ_DAT logic error c_err_rpt first register.

Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b00000000000000000000000000000000000000000000000
47:63	RWX_WCLEAR	CERR_LOG_FIRST_BITS: CQ_DAT logic error c_err_rpt first error bits.

Register Name	CQ_DAT RAS Error Message 0 Register
Mnemonic	NPU.STCK1.DAT.MISC.REM0
Address	00000000050111AD (SCOM)
Description	CQ_DAT RAS error message register.

Bits	SCOM	Field Mnemonic: Description
0:16	RO	Constant = 0b00000000000000000

Bits	SCOM	Field Mnemonic: Description
17:21	ROX	REM0_IBUF_WSRC: Indicates the inbound buffer write requester that caused a read/write conflict: Bit 0 = NTL0 datin immediate write. Bit 1 = NTL1 datin immediate write. Bit 2 = NTL1 datin delayed write. Bit 3 = CTL write. Bit 4 = Merge logic.
22:23	ROX	REM0_IBUF_RSRC: Indicates the inbound buffer read requester that caused read/write conflict: Bit 0 = PBTX transmit. Bit 1 = Merge logic.
24:31	ROX	REM0_IBUF_AIDX: The inbound buffer entry (0 - 255) on which the read/write conflict occurred.
32:33	ROX	REM0_IBUF_ABANK: The inbound buffer array bank (0 - 3) on which read/write conflict occurred.
34:35	ROX	REM0_OBUF_WSRC: Indicates the outbound buffer write requester that caused read/write conflict: bit 0 = PBTX receive. bit 1 = Merge logic I-O loopback.
36:41	ROX	REM0_OBUF_RSRC: Indicates the outbound buffer read requester that caused read/write conflict: Bit 0 = NTL0 datout immediate read. Bit 1 = NTL1 datout immediate read. Bit 2 = NTL0 datout regular read. Bit 3 = NTL1 datout regular read. Bit 4 = Merge logic. Bit 5 = CTL read.
42:49	ROX	REM0_OBUF_AIDX: The outbound buffer entry (0 - 255) on which the read/write conflict occurred.
50:51	ROX	REM0_OBUF_ABANK: The outbound buffer array bank (0 - 3) on which the read/write conflict occurred.
52:53	ROX	REM0_BBUF_WSRC: Indicates the BE buffer write requester that caused the read/write conflict: Bit 0 = NTL datin. Bit 1 = Dispalt logic in MISC.
54:55	ROX	REM0_BBUF_RSRC: Indicates the BE buffer read requester that caused the read/write conflict: Bit 0 = Merge logic. Bit 1 = Dispalt logic in MISC.
56:63	ROX	REM0_BBUF_AIDX: The BE buffer entry (0 - 255) on which the read/write conflict occurred.

Register Name	CQ_DAT RAS Error Message 1 Register
Mnemonic	NPU.STCK1.DAT.MISC.REM1
Address	00000000050111AE (SCOM)
Description	CQ_DAT RAS error message register.

Bits	SCOM	Field Mnemonic: Description
0:33	RO	Constant = 0b000000000000000000000000000000000
34:55	ROX	REM1_PBRX_RTAG: The invalid RTAG observed on PB receive interface.
56:58	ROX	REM1_ALU_ADR: The invalid ALU address in the OW that caused address error (in unit of 4B, 0 - 7).
59:62	ROX	REM1_ALU_TYPE: The ALU optype with which an address error was detected.
63	ROX	REM1_ALU_SZ: The ALU operand size (0:4B, 1:8B) when an address error was detected.

Register Name	CQ_DAT Debug0 Configuration Register
Mnemonic	NPU.STCK1.DAT.MISC.DEBUG0_CONFIG
Address	00000000050111B0 (SCOM)
Description	CQ_DAT debug 0 configuration register.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of trace 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of trace 0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of trace 0.
55:62	RW	DEBUG0_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	CQ_DAT Debug1 Configuration Register
Mnemonic	NPU.STCK1.DAT.MISC.DEBUG1_CONFIG
Address	00000000050111B1 (SCOM)
Description	CQ_DAT debug 1 configuration register.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of trace 0.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of trace 0.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of trace 0.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of trace 0.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of trace 0.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of trace 0.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of trace 0.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of trace 0.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of trace 0.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of trace 0.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of trace 0.
55:62	RW	DEBUG1_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	CQ_DAT Scratch 1 Register
Mnemonic	NPU.STCK1.DAT.MISC.SCRATCH1
Address	00000000050111BC (SCOM)
Description	CQ_DAT scratch register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	SCRATCH1_IDIAL: Scratch register.

Register Name	NTL Miscellaneous Configuration 2 Register
Mnemonic	NPU.STCK1.NTL0.REGS.CONFIG2
Address	00000000050111C0 (SCOM)
Description	The NTL Miscellaneous Configuration 2 register is used to control internal NTL function. It contains mode bits, chicken switches, and thresholds.

Bits	SCOM	Field Mnemonic: Description
0	RW	BRICK_ENABLE: When set to 0b1, this NVLink brick is enabled. This configuration bit is used as a general clock gate for latches in the NTL design.
1	RW	RSP_CTL_CRED_SINGLE_ENA: When set to 0b1, the NTL only gives CQ_CTL one RSP credit at a time, instead of the normal two.
2	RW	CREQ_BE_128: When set to 0b1, the NTL always sends 128 bytes of data when it needs to send a byte enable (BE) flit to the GPU for a CREQ packet. When set to 0b0, the NTL sends the least number of data flits required.
3	RW	DGD_BE_128: When set to 0b1, the NTL always sends 128 bytes of data when it needs to send a byte enable (BE) flit to the GPU for a downgrade packet (BE and data flits are sent in the TransDone packet for the downgrade). When se to 0b0, NTL sends the least number of data flits required.
4	RW	WR_SPLIT_UT0_ENA: When set to 0b1, the NTL splits up the write requests with UT = 0 from the GPU that map to the MMIO space into legal processor bus sizes/alignments. When set to 0b0, the NTL passes all write requests with UT = 0 as is to the CQ.
5	RW	WR_SPLIT_UT1_ENA: When set to 0b1, the NTL splits up the write requests with UT = 1 from the GPU into legal processor bus sizes/alignments. This includes both DMA writes and MMIO writes since there is no way for the NTL to distinguish between them. When set to 0b0, the NTL passes all write requests with UT = 1 as is to the CQ.
6	RW	BRICK_DEBUG_MODE: When set to 0b1, the NTL ignores all incoming NVLink packets from the GPU and throws away all NVLink requests/responses from the CQ destined for the GPU. This mode is used for debug purposes only when the NPU is not connected over NVLink to a GPU.
7	RW	P9_TO_P9_MODE: When set to 0b1, the NTL sets UT = 1 for all incoming read, write, and atomic NVLink packets before sending to the CQ. This mode is used for debug purposes only when the NPU is connected to another/same NPU over NVLink.
8:9	RW	CONFIG2_RESERVED1: Reserved.
10:15	RW	CAM256_MAX_CNT: This field specifies the number of entries in the CAM that holds information to send responses for 256 byte operations that require a response (maximum value = 48).
16	RW	NDL_RX_PARITY_ENA: When set to 0b1, the NTL checks parity on the incoming NDL RX signals.
17	RW	NDL_TX_PARITY_ENA: When set to 0b1, the NTL checks parity on the incoming NDL TX (that is, TX credits) signals.
18	RW	NDL_PRI_PARITY_ENA: When set to 0b1, the NTL checks the parity on the incoming NDL signals.
19	RW	RCV_CREDIT_OVERFLOW_ENA: When set to 0b1, the NTL checks for overflows on any received credits from the GPU, NDL, and NDL wrapper.

Bits	SCOM	Field Mnemonic: Description
20	RW	HDR_ARR_ECC_CORR_ENA: When set to 0b1, the NTL corrects ECC SBEs when reading the RX header array.
21	RW	DAT_ARR_ECC_CORR_ENA: When set to 0b1, the NTL corrects ECC SBEs when reading the RX data array. The NTL only corrects ECC on reads of the RX data array that require the NTL to update the data before sending to CQ_DAT (for example, BE flit or data flits for atomic CAS ops).
22	RW	TX_DATA_ECC_CORR_ENA: When set to 0b1, the NTL corrects ECC SBEs when reading TX data from CQ_DAT.
23	RW	CONFIG2_RESERVED2: Reserved.
24	RW	PARITY_ERROR_SUE_ENA: When set to 0b1, the NTL drives SUE on all data transfers to the CQ_DAT for a packet that has a parity error on an incoming data flit.
25	RW	DATA_POISON_SUE_ENA: When set to 0b1, the NTL drives SUE on all data transfers to the CQ_DAT for a packet that receives LMD = data poison.
26	RW	HDR_ARR_ECC_SUE_ENA: When set to 0b1, the NTL drives SUE on all data transfers to the CQ_DAT for a packet that has an ECC UE/SUE on the header info read from the RX header array.
27	RW	DAT_ARR_ECC_SUE_ENA: When set to 0b1, the NTL drives SUE on all data transfers to the CQ_DAT for a packet that has an ECC UE/SUE on data read from the RX data array. The NTL only checks ECC on reads of the RX data array that require the NTL to update the data before sending to the CQ_DAT (for example, BE flit or data flits for atomic CAS ops).
28	RW	TX_ECC_DATA_POISON_ENA: When set to 0b1, the NTL sends LMD = data poison for an outgoing NVLink packet that encounters an ECC UE/SUE on data read from CQ_DAT.
29:31	RW	CONFIG2_RESERVED3: Reserved.
32	RW	PRI_STATE_MACHINE_RESET: Reset PRI state machine to idle state (debug use only).
33:63	RW	CONFIG2_RESERVED4: Reserved.

Register Name	NTL Miscellaneous Configuration 3 Register
Mnemonic	NPU.STCK1.NTL0.REGS.CONFIG3
Address	00000000050111C1 (SCOM)
Description	The NTL Miscellaneous Configuration 3 register is used for future control of internal NTL functions. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG3_RESERVED1: Reserved.

Register Name	NTL CERR Hold 1 Register
Mnemonic	NPU.STCK1.NTL0.REGS.CERR_HOLD1
Address	00000000050111C2 (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLRREG	NTL_HOLD1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RWX_WCLRREG	NTL_HOLD1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.

Bits	SCOM	Field Mnemonic: Description
3	RWX_WCLRREG	NTL_HOLD1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RWX_WCLRREG	NTL_HOLD1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RWX_WCLRREG	NTL_HOLD1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLRREG	NTL_HOLD1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RWX_WCLRREG	NTL_HOLD1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RWX_WCLRREG	NTL_HOLD1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RWX_WCLRREG	NTL_HOLD1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RWX_WCLRREG	NTL_HOLD1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLRREG	NTL_HOLD1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RWX_WCLRREG	NTL_HOLD1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	RWX_WCLRREG	NTL_HOLD1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RWX_WCLRREG	NTL_HOLD1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RWX_WCLRREG	NTL_HOLD1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RWX_WCLRREG	NTL_HOLD1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RWX_WCLRREG	NTL_HOLD1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLRREG	NTL_HOLD1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLRREG	NTL_HOLD1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLRREG	NTL_HOLD1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLRREG	NTL_HOLD1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLRREG	NTL_HOLD1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLRREG	NTL_HOLD1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLRREG	NTL_HOLD1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RWX_WCLRREG	NTL_HOLD1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RWX_WCLRREG	NTL_HOLD1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RWX_WCLRREG	NTL_HOLD1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RWX_WCLRREG	NTL_HOLD1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RWX_WCLRREG	NTL_HOLD1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RWX_WCLRREG	NTL_HOLD1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RWX_WCLRREG	NTL_HOLD1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RWX_WCLRREG	NTL_HOLD1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RWX_WCLRREG	NTL_HOLD1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.

Bits	SCOM	Field Mnemonic: Description
34	RWX_WCLRREG	NTL_HOLD1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RWX_WCLRREG	NTL_HOLD1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RWX_WCLRREG	NTL_HOLD1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RWX_WCLRREG	NTL_HOLD1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RWX_WCLRREG	NTL_HOLD1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RWX_WCLRREG	NTL_HOLD1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RWX_WCLRREG	NTL_HOLD1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RWX_WCLRREG	NTL_HOLD1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RWX_WCLRREG	NTL_HOLD1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RWX_WCLRREG	NTL_HOLD1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RWX_WCLRREG	NTL_HOLD1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RWX_WCLRREG	NTL_HOLD1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RWX_WCLRREG	NTL_HOLD1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RWX_WCLRREG	NTL_HOLD1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RWX_WCLRREG	NTL_HOLD1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RWX_WCLRREG	NTL_HOLD1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RWX_WCLRREG	NTL_HOLD1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLRREG	NTL_HOLD1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLRREG	NTL_HOLD1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLRREG	NTL_HOLD1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLRREG	NTL_HOLD1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLRREG	NTL_HOLD1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLRREG	NTL_HOLD1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RWX_WCLRREG	NTL_HOLD1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RWX_WCLRREG	NTL_HOLD1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RWX_WCLRREG	NTL_HOLD1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RWX_WCLRREG	NTL_HOLD1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RWX_WCLRREG	NTL_HOLD1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.

Bits	SCOM	Field Mnemonic: Description
62	RWX_WCLRREG	NTL_HOLD1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLRREG	NTL_HOLD1_63: ERROR - NTL RX - Reserved.

Register Name	NTL CERR Mask 1 Register
Mnemonic	NPU.STCK1.NTL0.REGS.CERR_MASK1
Address	00000000050111C3 (SCOM)
Description	c_err_rpt mask latches read-only register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	ROX	NTL_MASK1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	ROX	NTL_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	ROX	NTL_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	ROX	NTL_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	ROX	NTL_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	ROX	NTL_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	ROX	NTL_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	ROX	NTL_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	ROX	NTL_MASK1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	ROX	NTL_MASK1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	ROX	NTL_MASK1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	ROX	NTL_MASK1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT=0 request packet where the address field is valid, and not ATR.
13	ROX	NTL_MASK1_13: ERROR - NTL RX - DatLen /= 16,32,64,128B in an incoming NVLink probe packet.
14	ROX	NTL_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	ROX	NTL_MASK1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	ROX	NTL_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	ROX	NTL_MASK1_17: ERROR - NTL RX - Reserved.
18	ROX	NTL_MASK1_18: ERROR - NTL RX - Reserved.
19	ROX	NTL_MASK1_19: ERROR - NTL RX - Reserved.
20	ROX	NTL_MASK1_20: ERROR - NTL RX - Reserved.

Bits	SCOM	Field Mnemonic: Description
21	ROX	NTL_MASK1_21: ERROR - NTL RX - Reserved.
22	ROX	NTL_MASK1_22: ERROR - NTL RX - Reserved.
23	ROX	NTL_MASK1_23: ERROR - NTL RX - Reserved.
24	ROX	NTL_MASK1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	ROX	NTL_MASK1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	ROX	NTL_MASK1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	ROX	NTL_MASK1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	ROX	NTL_MASK1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	ROX	NTL_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	ROX	NTL_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	ROX	NTL_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	ROX	NTL_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	ROX	NTL_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	ROX	NTL_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	ROX	NTL_MASK1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	ROX	NTL_MASK1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	ROX	NTL_MASK1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	ROX	NTL_MASK1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	ROX	NTL_MASK1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	ROX	NTL_MASK1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	ROX	NTL_MASK1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	ROX	NTL_MASK1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	ROX	NTL_MASK1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	ROX	NTL_MASK1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	ROX	NTL_MASK1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	ROX	NTL_MASK1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	ROX	NTL_MASK1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	ROX	NTL_MASK1_48: ERROR - NTL RX - A CQ global credit was received when 3 were already valid (overflow).
49	ROX	NTL_MASK1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).

Bits	SCOM	Field Mnemonic: Description
50	ROX	NTL_MASK1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	ROX	NTL_MASK1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	ROX	NTL_MASK1_52: ERROR - NTL RX - Reserved.
53	ROX	NTL_MASK1_53: ERROR - NTL RX - Reserved.
54	ROX	NTL_MASK1_54: ERROR - NTL RX - Reserved.
55	ROX	NTL_MASK1_55: ERROR - NTL RX - Reserved.
56	ROX	NTL_MASK1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	ROX	NTL_MASK1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	ROX	NTL_MASK1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	ROX	NTL_MASK1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	ROX	NTL_MASK1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	ROX	NTL_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	ROX	NTL_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	ROX	NTL_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First 1 Register**
Mnemonic	NPU.STCK1.NTL0.REGS.CERR_FIRST1
Address	00000000050111C4 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLEAR	NTL_FIRST1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RWX_WCLEAR	NTL_FIRST1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RWX_WCLEAR	NTL_FIRST1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RWX_WCLEAR	NTL_FIRST1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RWX_WCLEAR	NTL_FIRST1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLEAR	NTL_FIRST1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RWX_WCLEAR	NTL_FIRST1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RWX_WCLEAR	NTL_FIRST1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RWX_WCLEAR	NTL_FIRST1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.

Bits	SCOM	Field Mnemonic: Description
10	RWX_WCLEAR	NTL_FIRST1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLEAR	NTL_FIRST1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RWX_WCLEAR	NTL_FIRST1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT=0 request packet where the address field is valid and not ATR.
13	RWX_WCLEAR	NTL_FIRST1_13: ERROR - NTL RX - DatLen /= 16,32,64,128B in an incoming NVLink probe packet.
14	RWX_WCLEAR	NTL_FIRST1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RWX_WCLEAR	NTL_FIRST1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RWX_WCLEAR	NTL_FIRST1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RWX_WCLEAR	NTL_FIRST1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLEAR	NTL_FIRST1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLEAR	NTL_FIRST1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLEAR	NTL_FIRST1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLEAR	NTL_FIRST1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLEAR	NTL_FIRST1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLEAR	NTL_FIRST1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLEAR	NTL_FIRST1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RWX_WCLEAR	NTL_FIRST1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RWX_WCLEAR	NTL_FIRST1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RWX_WCLEAR	NTL_FIRST1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RWX_WCLEAR	NTL_FIRST1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RWX_WCLEAR	NTL_FIRST1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RWX_WCLEAR	NTL_FIRST1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RWX_WCLEAR	NTL_FIRST1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RWX_WCLEAR	NTL_FIRST1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RWX_WCLEAR	NTL_FIRST1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RWX_WCLEAR	NTL_FIRST1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RWX_WCLEAR	NTL_FIRST1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RWX_WCLEAR	NTL_FIRST1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RWX_WCLEAR	NTL_FIRST1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RWX_WCLEAR	NTL_FIRST1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RWX_WCLEAR	NTL_FIRST1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RWX_WCLEAR	NTL_FIRST1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.

Bits	SCOM	Field Mnemonic: Description
41	RWX_WCLEAR	NTL_FIRST1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RWX_WCLEAR	NTL_FIRST1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RWX_WCLEAR	NTL_FIRST1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RWX_WCLEAR	NTL_FIRST1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RWX_WCLEAR	NTL_FIRST1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RWX_WCLEAR	NTL_FIRST1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RWX_WCLEAR	NTL_FIRST1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RWX_WCLEAR	NTL_FIRST1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RWX_WCLEAR	NTL_FIRST1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RWX_WCLEAR	NTL_FIRST1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLEAR	NTL_FIRST1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLEAR	NTL_FIRST1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLEAR	NTL_FIRST1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLEAR	NTL_FIRST1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLEAR	NTL_FIRST1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLEAR	NTL_FIRST1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RWX_WCLEAR	NTL_FIRST1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RWX_WCLEAR	NTL_FIRST1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RWX_WCLEAR	NTL_FIRST1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RWX_WCLEAR	NTL_FIRST1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RWX_WCLEAR	NTL_FIRST1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLEAR	NTL_FIRST1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLEAR	NTL_FIRST1_63: ERROR - NTL RX - Reserved.

Register Name	NTL CERR First Mask 1 Register
Mnemonic	NPU.STCK1.NTL0.REGS.CERR_FIRST_MASK1
Address	00000000050111C5 (SCOM)
Description	This register mask errors from being captured in the First 1 Error registers and the RAS Error Message registers.

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.

Bits	SCOM	Field Mnemonic: Description
1	RW	NTL_FIRST_MASK1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RW	NTL_FIRST_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RW	NTL_FIRST_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RW	NTL_FIRST_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RW	NTL_FIRST_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RW	NTL_FIRST_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RW	NTL_FIRST_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RW	NTL_FIRST_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RW	NTL_FIRST_MASK1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RW	NTL_FIRST_MASK1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RW	NTL_FIRST_MASK1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RW	NTL_FIRST_MASK1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid, and not ATR.
13	RW	NTL_FIRST_MASK1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RW	NTL_FIRST_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RW	NTL_FIRST_MASK1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RW	NTL_FIRST_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RW	NTL_FIRST_MASK1_17: ERROR - NTL RX - Reserved.
18	RW	NTL_FIRST_MASK1_18: ERROR - NTL RX - Reserved.
19	RW	NTL_FIRST_MASK1_19: ERROR - NTL RX - Reserved.
20	RW	NTL_FIRST_MASK1_20: ERROR - NTL RX - Reserved.
21	RW	NTL_FIRST_MASK1_21: ERROR - NTL RX - Reserved.
22	RW	NTL_FIRST_MASK1_22: ERROR - NTL RX - Reserved.
23	RW	NTL_FIRST_MASK1_23: ERROR - NTL RX - Reserved.
24	RW	NTL_FIRST_MASK1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RW	NTL_FIRST_MASK1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RW	NTL_FIRST_MASK1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RW	NTL_FIRST_MASK1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RW	NTL_FIRST_MASK1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RW	NTL_FIRST_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.

Bits	SCOM	Field Mnemonic: Description
30	RW	NTL_FIRST_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RW	NTL_FIRST_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RW	NTL_FIRST_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RW	NTL_FIRST_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RW	NTL_FIRST_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RW	NTL_FIRST_MASK1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RW	NTL_FIRST_MASK1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RW	NTL_FIRST_MASK1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RW	NTL_FIRST_MASK1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RW	NTL_FIRST_MASK1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RW	NTL_FIRST_MASK1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RW	NTL_FIRST_MASK1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RW	NTL_FIRST_MASK1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RW	NTL_FIRST_MASK1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RW	NTL_FIRST_MASK1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RW	NTL_FIRST_MASK1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RW	NTL_FIRST_MASK1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RW	NTL_FIRST_MASK1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RW	NTL_FIRST_MASK1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RW	NTL_FIRST_MASK1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RW	NTL_FIRST_MASK1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RW	NTL_FIRST_MASK1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RW	NTL_FIRST_MASK1_52: ERROR - NTL RX - Reserved.
53	RW	NTL_FIRST_MASK1_53: ERROR - NTL RX - Reserved.
54	RW	NTL_FIRST_MASK1_54: ERROR - NTL RX - Reserved.
55	RW	NTL_FIRST_MASK1_55: ERROR - NTL RX - Reserved.
56	RW	NTL_FIRST_MASK1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RW	NTL_FIRST_MASK1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.

Bits	SCOM	Field Mnemonic: Description
58	RW	NTL_FIRST_MASK1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RW	NTL_FIRST_MASK1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RW	NTL_FIRST_MASK1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RW	NTL_FIRST_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RW	NTL_FIRST_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RW	NTL_FIRST_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR Hold 2 Register**
Mnemonic	NPU.STCK1.NTL0.REGS.CERR_HOLD2
Address	00000000050111C6 (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RWX_WCLRREG	NTL_HOLD2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RWX_WCLRREG	NTL_HOLD2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RWX_WCLRREG	NTL_HOLD2_3: ERROR - NTL TX – ECC SUE on data(0:63) read from CQ_DAT.
4	RWX_WCLRREG	NTL_HOLD2_4: ERROR - NTL TX – ECC SUE on data(64:127) read from CQ_DAT.
5	RWX_WCLRREG	NTL_HOLD2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RWX_WCLRREG	NTL_HOLD2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLRREG	NTL_HOLD2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLRREG	NTL_HOLD2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLRREG	NTL_HOLD2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLRREG	NTL_HOLD2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLRREG	NTL_HOLD2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLRREG	NTL_HOLD2_12: ERROR - NTL TX - More than one entry in the 256B ops CAM was hit at the same time.
13	RWX_WCLRREG	NTL_HOLD2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RWX_WCLRREG	NTL_HOLD2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RWX_WCLRREG	NTL_HOLD2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLRREG	NTL_HOLD2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLRREG	NTL_HOLD2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLRREG	NTL_HOLD2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLRREG	NTL_HOLD2_19: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
20	RWX_WCLRREG	NTL_HOLD2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLRREG	NTL_HOLD2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLRREG	NTL_HOLD2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLRREG	NTL_HOLD2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLRREG	NTL_HOLD2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RWX_WCLRREG	NTL_HOLD2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RWX_WCLRREG	NTL_HOLD2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLRREG	NTL_HOLD2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLRREG	NTL_HOLD2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLRREG	NTL_HOLD2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLRREG	NTL_HOLD2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLRREG	NTL_HOLD2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLRREG	NTL_HOLD2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RWX_WCLRREG	NTL_HOLD2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RWX_WCLRREG	NTL_HOLD2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RWX_WCLRREG	NTL_HOLD2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RWX_WCLRREG	NTL_HOLD2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RWX_WCLRREG	NTL_HOLD2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RWX_WCLRREG	NTL_HOLD2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RWX_WCLRREG	NTL_HOLD2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RWX_WCLRREG	NTL_HOLD2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	RWX_WCLRREG	NTL_HOLD2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	RWX_WCLRREG	NTL_HOLD2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLRREG	NTL_HOLD2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLRREG	NTL_HOLD2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLRREG	NTL_HOLD2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLRREG	NTL_HOLD2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLRREG	NTL_HOLD2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLRREG	NTL_HOLD2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLRREG	NTL_HOLD2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLRREG	NTL_HOLD2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLRREG	NTL_HOLD2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLRREG	NTL_HOLD2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.

Bits	SCOM	Field Mnemonic: Description
53	RWX_WCLRREG	NTL_HOLD2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RWX_WCLRREG	NTL_HOLD2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RWX_WCLRREG	NTL_HOLD2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RWX_WCLRREG	NTL_HOLD2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RWX_WCLRREG	NTL_HOLD2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RWX_WCLRREG	NTL_HOLD2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RWX_WCLRREG	NTL_HOLD2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RWX_WCLRREG	NTL_HOLD2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLRREG	NTL_HOLD2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLRREG	NTL_HOLD2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLRREG	NTL_HOLD2_63: ERROR - NTL REGS - Reserved.

Register Name	NTL CERR Mask 2 Register
Mnemonic	NPU.STCK1.NTL0.REGS.CERR_MASK2
Address	00000000050111C7 (SCOM)
Description	c_err_rpt mask latches read-only register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	ROX	NTL_MASK2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	ROX	NTL_MASK2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	ROX	NTL_MASK2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	ROX	NTL_MASK2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	ROX	NTL_MASK2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	ROX	NTL_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	ROX	NTL_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	ROX	NTL_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	ROX	NTL_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	ROX	NTL_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	ROX	NTL_MASK2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	ROX	NTL_MASK2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	ROX	NTL_MASK2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	ROX	NTL_MASK2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	ROX	NTL_MASK2_15: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
16	ROX	NTL_MASK2_16: ERROR - NTL TX - Reserved.
17	ROX	NTL_MASK2_17: ERROR - NTL TX - Reserved.
18	ROX	NTL_MASK2_18: ERROR - NTL TX - Reserved.
19	ROX	NTL_MASK2_19: ERROR - NTL TX - Reserved.
20	ROX	NTL_MASK2_20: ERROR - NTL TX - Reserved.
21	ROX	NTL_MASK2_21: ERROR - NTL TX - Reserved.
22	ROX	NTL_MASK2_22: ERROR - NTL TX - Reserved.
23	ROX	NTL_MASK2_23: ERROR - NTL TX - Reserved.
24	ROX	NTL_MASK2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	ROX	NTL_MASK2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	ROX	NTL_MASK2_26: ERROR - NTL TX - Reserved.
27	ROX	NTL_MASK2_27: ERROR - NTL TX - Reserved.
28	ROX	NTL_MASK2_28: ERROR - NTL TX - Reserved.
29	ROX	NTL_MASK2_29: ERROR - NTL TX - Reserved.
30	ROX	NTL_MASK2_30: ERROR - NTL TX - Reserved.
31	ROX	NTL_MASK2_31: ERROR - NTL TX - Reserved.
32	ROX	NTL_MASK2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	ROX	NTL_MASK2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	ROX	NTL_MASK2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	ROX	NTL_MASK2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	ROX	NTL_MASK2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	ROX	NTL_MASK2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	ROX	NTL_MASK2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	ROX	NTL_MASK2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	ROX	NTL_MASK2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	ROX	NTL_MASK2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	ROX	NTL_MASK2_42: ERROR - NTL REGS - Reserved.
43	ROX	NTL_MASK2_43: ERROR - NTL REGS - Reserved.
44	ROX	NTL_MASK2_44: ERROR - NTL REGS - Reserved.
45	ROX	NTL_MASK2_45: ERROR - NTL REGS - Reserved.
46	ROX	NTL_MASK2_46: ERROR - NTL REGS - Reserved.
47	ROX	NTL_MASK2_47: ERROR - NTL REGS - Reserved.
48	ROX	NTL_MASK2_48: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
49	ROX	NTL_MASK2_49: ERROR - NTL REGS - Reserved.
50	ROX	NTL_MASK2_50: ERROR - NTL REGS - Reserved.
51	ROX	NTL_MASK2_51: ERROR - NTL REGS - Reserved.
52	ROX	NTL_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	ROX	NTL_MASK2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	ROX	NTL_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	ROX	NTL_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	ROX	NTL_MASK2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	ROX	NTL_MASK2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	ROX	NTL_MASK2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	ROX	NTL_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	ROX	NTL_MASK2_60: ERROR - NTL REGS - Reserved.
61	ROX	NTL_MASK2_61: ERROR - NTL REGS - Reserved.
62	ROX	NTL_MASK2_62: ERROR - NTL REGS - Reserved.
63	ROX	NTL_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR First 2 Register**
Mnemonic	NPU.STCK1.NTL0.REGS.CERR_FIRST2
Address	00000000050111C8 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RWX_WCLEAR	NTL_FIRST2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RWX_WCLEAR	NTL_FIRST2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RWX_WCLEAR	NTL_FIRST2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RWX_WCLEAR	NTL_FIRST2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RWX_WCLEAR	NTL_FIRST2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RWX_WCLEAR	NTL_FIRST2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLEAR	NTL_FIRST2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLEAR	NTL_FIRST2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLEAR	NTL_FIRST2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLEAR	NTL_FIRST2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLEAR	NTL_FIRST2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.

Bits	SCOM	Field Mnemonic: Description
12	RWX_WCLEAR	NTL_FIRST2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLEAR	NTL_FIRST2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RWX_WCLEAR	NTL_FIRST2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RWX_WCLEAR	NTL_FIRST2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLEAR	NTL_FIRST2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLEAR	NTL_FIRST2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLEAR	NTL_FIRST2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLEAR	NTL_FIRST2_19: ERROR - NTL TX - Reserved.
20	RWX_WCLEAR	NTL_FIRST2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLEAR	NTL_FIRST2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLEAR	NTL_FIRST2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLEAR	NTL_FIRST2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLEAR	NTL_FIRST2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RWX_WCLEAR	NTL_FIRST2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RWX_WCLEAR	NTL_FIRST2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLEAR	NTL_FIRST2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLEAR	NTL_FIRST2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLEAR	NTL_FIRST2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLEAR	NTL_FIRST2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLEAR	NTL_FIRST2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLEAR	NTL_FIRST2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RWX_WCLEAR	NTL_FIRST2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RWX_WCLEAR	NTL_FIRST2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RWX_WCLEAR	NTL_FIRST2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RWX_WCLEAR	NTL_FIRST2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RWX_WCLEAR	NTL_FIRST2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RWX_WCLEAR	NTL_FIRST2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RWX_WCLEAR	NTL_FIRST2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RWX_WCLEAR	NTL_FIRST2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	RWX_WCLEAR	NTL_FIRST2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	RWX_WCLEAR	NTL_FIRST2_42: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
43	RWX_WCLEAR	NTL_FIRST2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLEAR	NTL_FIRST2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLEAR	NTL_FIRST2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLEAR	NTL_FIRST2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLEAR	NTL_FIRST2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLEAR	NTL_FIRST2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLEAR	NTL_FIRST2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLEAR	NTL_FIRST2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLEAR	NTL_FIRST2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLEAR	NTL_FIRST2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RWX_WCLEAR	NTL_FIRST2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RWX_WCLEAR	NTL_FIRST2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RWX_WCLEAR	NTL_FIRST2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RWX_WCLEAR	NTL_FIRST2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RWX_WCLEAR	NTL_FIRST2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RWX_WCLEAR	NTL_FIRST2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RWX_WCLEAR	NTL_FIRST2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RWX_WCLEAR	NTL_FIRST2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLEAR	NTL_FIRST2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLEAR	NTL_FIRST2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLEAR	NTL_FIRST2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR First Mask 2 Register**
Mnemonic	NPU.STCK1.NTL0.REGS.CERR_FIRST_MASK2
Address	00000000050111C9 (SCOM)
Description	This register mask errors from being captured in the First 2 Error registers and the RAS Error Message registers.

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RW	NTL_FIRST_MASK2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RW	NTL_FIRST_MASK2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RW	NTL_FIRST_MASK2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RW	NTL_FIRST_MASK2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RW	NTL_FIRST_MASK2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RW	NTL_FIRST_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RW	NTL_FIRST_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).

Bits	SCOM	Field Mnemonic: Description
8	RW	NTL_FIRST_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RW	NTL_FIRST_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RW	NTL_FIRST_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RW	NTL_FIRST_MASK2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	RW	NTL_FIRST_MASK2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RW	NTL_FIRST_MASK2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RW	NTL_FIRST_MASK2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RW	NTL_FIRST_MASK2_15: ERROR - NTL TX - Reserved.
16	RW	NTL_FIRST_MASK2_16: ERROR - NTL TX - Reserved.
17	RW	NTL_FIRST_MASK2_17: ERROR - NTL TX - Reserved.
18	RW	NTL_FIRST_MASK2_18: ERROR - NTL TX - Reserved.
19	RW	NTL_FIRST_MASK2_19: ERROR - NTL TX - Reserved.
20	RW	NTL_FIRST_MASK2_20: ERROR - NTL TX - Reserved.
21	RW	NTL_FIRST_MASK2_21: ERROR - NTL TX - Reserved.
22	RW	NTL_FIRST_MASK2_22: ERROR - NTL TX - Reserved.
23	RW	NTL_FIRST_MASK2_23: ERROR - NTL TX - Reserved.
24	RW	NTL_FIRST_MASK2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RW	NTL_FIRST_MASK2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RW	NTL_FIRST_MASK2_26: ERROR - NTL TX - Reserved.
27	RW	NTL_FIRST_MASK2_27: ERROR - NTL TX - Reserved.
28	RW	NTL_FIRST_MASK2_28: ERROR - NTL TX - Reserved.
29	RW	NTL_FIRST_MASK2_29: ERROR - NTL TX - Reserved.
30	RW	NTL_FIRST_MASK2_30: ERROR - NTL TX - Reserved.
31	RW	NTL_FIRST_MASK2_31: ERROR - NTL TX - Reserved.
32	RW	NTL_FIRST_MASK2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RW	NTL_FIRST_MASK2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RW	NTL_FIRST_MASK2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RW	NTL_FIRST_MASK2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RW	NTL_FIRST_MASK2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RW	NTL_FIRST_MASK2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.

Bits	SCOM	Field Mnemonic: Description
38	RW	NTL_FIRST_MASK2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RW	NTL_FIRST_MASK2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RW	NTL_FIRST_MASK2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	RW	NTL_FIRST_MASK2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	RW	NTL_FIRST_MASK2_42: ERROR - NTL REGS - Reserved.
43	RW	NTL_FIRST_MASK2_43: ERROR - NTL REGS - Reserved.
44	RW	NTL_FIRST_MASK2_44: ERROR - NTL REGS - Reserved.
45	RW	NTL_FIRST_MASK2_45: ERROR - NTL REGS - Reserved.
46	RW	NTL_FIRST_MASK2_46: ERROR - NTL REGS - Reserved.
47	RW	NTL_FIRST_MASK2_47: ERROR - NTL REGS - Reserved.
48	RW	NTL_FIRST_MASK2_48: ERROR - NTL REGS - Reserved.
49	RW	NTL_FIRST_MASK2_49: ERROR - NTL REGS - Reserved.
50	RW	NTL_FIRST_MASK2_50: ERROR - NTL REGS - Reserved.
51	RW	NTL_FIRST_MASK2_51: ERROR - NTL REGS - Reserved.
52	RW	NTL_FIRST_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RW	NTL_FIRST_MASK2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RW	NTL_FIRST_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RW	NTL_FIRST_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RW	NTL_FIRST_MASK2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RW	NTL_FIRST_MASK2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RW	NTL_FIRST_MASK2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RW	NTL_FIRST_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RW	NTL_FIRST_MASK2_60: ERROR - NTL REGS - Reserved.
61	RW	NTL_FIRST_MASK2_61: ERROR - NTL REGS - Reserved.
62	RW	NTL_FIRST_MASK2_62: ERROR - NTL REGS - Reserved.
63	RW	NTL_FIRST_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL Scratch 2 Register**
Mnemonic	NPU.STCK1.NTL0.REGS.SCRATCH2
Address	00000000050111CA (SCOM)
Description	The NTL Scratch 2 register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH2: Scratch register.

Register Name	NTL Scratch 3 Register
Mnemonic	NPU.STCK1.NTL0.REGS.SCRATCH3
Address	00000000050111CB (SCOM)
Description	The NTL Scratch 3 register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH3: Scratch register.

Register Name	NTL Debug0 Configuration Register
Mnemonic	NPU.STCK1.NTL0.REGS.DEBUG0_CONFIG
Address	00000000050111CC (SCOM)
Description	The NTL Debug Trace 0 Configuration register is used to configure what debug information is sent on the debug trace 0 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of debug trace 0: 0x00 = Debug trace 0 byte 0 inputs. 0x01 = Debug trace 0 byte 1 inputs. 0x02 = Debug trace 0 byte 2 inputs. 0x03 = Debug trace 0 byte 3 inputs. 0x04 = Debug trace 0 byte 4 inputs. 0x05 = Debug trace 0 byte 5 inputs. 0x06 = Debug trace 0 byte 6 inputs. 0x07 = Debug trace 0 byte 7 inputs. 0x08 = Debug trace 0 byte 8 inputs. 0x09 = Debug trace 0 byte 9 inputs. 0x0A = Debug trace 0 byte 10 inputs. 0x0B = RX debug group 0. 0x0C = RX debug group 1. 0x0D = RX debug group 2. 0x0E = RX debug group 3. 0x0F = RX debug group 4. 0x10 = RX debug group 5. 0x11 = RX debug group 6. 0x12 = RX debug group 7. 0x13 = RX debug group 8. 0x14 = TX debug group 0. 0x15 = TX debug group 1. 0x16 = TX debug group 2. 0x17 = TX debug group 3. 0x18 = TX debug group 4. 0x19 = TX debug group 5. 0x1A = TX debug group 6. 0x1B = REGS debug group 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of debug trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of debug trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of debug trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of debug trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of debug trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of debug trace 0.

Bits	SCOM	Field Mnemonic: Description
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of debug trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of debug trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of debug trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of debug trace 0.
55:62	RW	DEBUG0_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	**NTL Debug1 Configuration Register**
Mnemonic	NPU.STCK1.NTL0.REGS.DEBUG1_CONFIG
Address	00000000050111CD (SCOM)
Description	The NTL Debug Trace 1 Configuration register is used to configure what debug information is sent on the debug trace 1 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of debug trace 1: 0x00 = Debug trace 1 byte 0 inputs. 0x01 = Debug trace 1 byte 1 inputs. 0x02 = Debug trace 1 byte 2 inputs. 0x03 = Debug trace 1 byte 3 inputs. 0x04 = Debug trace 1 byte 4 inputs. 0x05 = Debug trace 1 byte 5 inputs. 0x06 = Debug trace 1 byte 6 inputs. 0x07 = Debug trace 1 byte 7 inputs. 0x08 = Debug trace 1 byte 8 inputs. 0x09 = Debug trace 1 byte 9 inputs. 0x0A = Debug trace 1 byte 10 inputs. 0x0B = RX debug group 0. 0x0C = RX debug group 1. 0x0D = RX debug group 2. 0x0E = RX debug group 3. 0x0F = RX debug group 4. 0x10 = RX debug group 5. 0x11 = RX debug group 6. 0x12 = RX debug group 7. 0x13 = RX debug group 8. 0x14 = TX debug group 0. 0x15 = TX debug group 1. 0x16 = TX debug group 2. 0x17 = TX debug group 3. 0x18 = TX debug group 4. 0x19 = TX debug group 5. 0x1A = TX debug group 6. 0x1B = REGS debug group 0.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of debug trace 1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of debug trace 1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of debug trace 1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of debug trace 1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of debug trace 1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of debug trace 1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of debug trace 1.

Bits	SCOM	Field Mnemonic: Description
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of debug trace 1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of debug trace 1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of debug trace 1.
55:62	RW	DEBUG1_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	**NTL Performance Configuration Register**
Mnemonic	NPU.STCK1.NTL0.REGS.PERF_CONFIG
Address	00000000050111CE (SCOM)
Description	The NTL Performance Configuration register is used to configure what information is counted by the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: PMULet enable (clocks enable).
1	RW	PERF_CONFIG_RESETMODE: 0 = Reset on read. 1 = Reset on write.
2	RW	PERF_CONFIG_FREEZEMODE: 0 = Free run mode. 1 = Freeze on any maximum.
3	RW	PERF_CONFIG_DISABLE_PMISC: 0 = Enable PMISC control of counters. 1 = Disable PMISC control of counters.
4	RW	PERF_CONFIG_PMISC_MODE: 0 = Global PMU PMISC no reset. 1 = Global PMU PMISC reset on enable.
5:7	RW	PERF_CONFIG_CASCADE: PMULet cascade configuration.
8:9	RW	PERF_CONFIG_PRESCALE_C0: Pre-scale configuration for counter 0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: Pre-scale configuration for counter 1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: Pre-scale configuration for counter 2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: Pre-scale configuration for counter 3.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select: 0x00 = Disable. 0x01 = Cycles. 0x02 = Latency events. 0x03 = Latency cycles. 0x04 = Latency aborts. 0x20 = REGS - NDL PRI request. 0x21 = REGS - NDL PRI write request. 0x22 = REGS - NDL PRI read request. 0x23 = REGS - PHY PRI request. 0x24 = REGS - PHY PRI write request. 0x25 = REGS - PHY PRI read request. 0x40 = TX - Any flit sent. 0x41 = TX - Header flit sent. 0x42 = TX - AE flit sent.

Bits	SCOM	Field Mnemonic: Description
		0x43 = TX - BE flit sent. 0x44 = TX - Data flit sent. 0x45 = TX - Flow control packet. 0x46 = TX - Write.NC. 0x47 = TX - Write.NC 128B. 0x48 = TX - Write.NC 32B - 96B. 0x49 = TX - Write.NC 1B - 16B. 0x4A = TX - Write.NC with BE flit. 0x4B = TX - Read. 0x4C = TX - Upgrade. 0x4D = TX - Atomic. 0x4E = TX - Downgrade. 0x4F = TX - ATSD. 0x50 = TX - Request response, no data. 0x51 = TX - Request response with data. 0x52 = TX - Probe response, no data. 0x53 = TX - Probe response with data. 0x54 = TX - ATR response. 0x55 = TX - TransDone response, no data. 0x56 = TX - TransDone response with data. 0x57 = TX - TransDone response with data 128B. 0x58 = TX - TransDone response with data 32B - 96B. 0x59 = TX - TransDone response with data 1B - 16B. 0x5A = TX - TransDone response with data with BE flit. 0x5B = TX - Not enough CREQ header credits. 0x5C = TX - Not enough DGD header credits. 0x5D = TX - Not enough ATSD header credits. 0x5E = TX - Not enough RSP header credits. 0x5F = TX - Not enough CREQ data credits. 0x60 = TX - Not enough RSP data credits. 0x61 = TX - Not enough replay buffer credits. 0x62 = TX - Not enough asynchronous buffer credits. 0x80 = RX - CREQ header array full. 0x81 = RX - PRB header array full. 0x82 = RX - ATR header array full. 0x83 = RX - RSP header array full. 0x84 = RX - CREQ data array full. 0x85 = RX - RSP data array full. 0x86 = RX - Any flit received. 0x87 = RX - Header flit received. 0x88 = RX - AE flit received. 0x89 = RX - BE flit received. 0x8A = RX - Data flit received. 0x8B = RX - NOP flow control flit received. 0x8C = RX - Write.NC (UT = 0). 0x8D = RX - Write.NC (UT = 1). 0x8E = RX - Write.NC (UT = 0) 128B. 0x8F = RX - Write.NC (UT = 1) 128B. 0x90 = RX - Write.NC (UT = 0) 256B. 0x91 = RX - Write.NC (UT = 1) 256B. 0x92 = RX - Write.NC (UT = 0) 32B - 96B. 0x93 = RX - Write.NC (UT = 1) 32B - 96B. 0x94 = RX - Write.NC (UT = 0) 1B - 16B. 0x95 = RX - Write.NC (UT = 1) 1B - 16B. 0x96 = RX - Write.NC (UT = 0) with BE flit. 0x97 = RX - Write.NC (UT = 1) with BE flit. 0x98 = RX - Write.NC (UT = 0) to MMIO space. 0x99 = RX - Write.NC (UT = 0) to MMIO space and split into multiple requests. 0x9A = RX - Write.NC (UT = 1) and split into multiple requests. 0x9B = RX - Read.NC (UT = 0).

Bits	SCOM	Field Mnemonic: Description
		0x9C = RX - Read.NC (UT = 1). 0x9D = RX - Read.NC (UT = 0) 128B. 0x9E = RX - Read.NC (UT = 1) 128B. 0x9F = RX - Read.NC (UT = 0) 256B. 0xA0 = RX - Read.NC (UT = 1) 256B. 0xA1 = RX - Read.NC (UT = 0) 32B - 96B. 0xA2 = RX - Read.NC (UT = 1) 32B - 96B. 0xA3 = RX - Read.NC (UT = 0) 1B - 16B. 0xA4 = RX - Read.NC (UT = 1) 1B - 16B. 0xA5 = RX - Flush. 0xA6 = RX - RMW. 0xA7 = RX - Atomic.NR. 0xA8 = RX - Atomic.RR. 0xA9 = RX - Probe.I.MO. 0xAA = RX - Probe.I.N. 0xAB = RX - Probe.X.MO. 0xAC = RX - ATR. 0xAD = RX - ReqRsp.ND. 0xAE = RX - ReqRsp.D. 0xAF = RX - DGDRsp. 0xB0 = RX - ATSDRsp. 0xB1 = RX - TransDone.ND. 0xB2 = RX - TransDone.D. 0xB3 = RX - TransDone.D with BE flit. 0xB4 = RX - CREQ non-flush waiting for CQ credit. 0xB5 = RX - CREQ flush waiting for CQ credit. 0xB6 = RX - CREQ waiting for global credit. 0xB7 = RX - CREQ 256B Op waiting for 256B Ops CAM entry. 0xB8 = RX - PRB waiting for CQ credit. 0xB9 = RX - PRB waiting for global credit. 0xBA = RX - ATR waiting for CQ credit. 0xBB = RX - ATR waiting for global credit.
24:31	RW	PERF_CONFIG_EVENT1: Event 1 select (see Event 0 select for encodes).
32:39	RW	PERF_CONFIG_EVENT2: Event 2 select (see Event 0 select for encodes).
40:47	RW	PERF_CONFIG_EVENT3: Event 3 select (see Event 0 select for encodes).
48:50	RW	PERF_CONFIG_LATENCY: Latency select: 0 = Disable. 1 = Read.NC to response. 2 = Write.RR to response. 3 = Atomic.RR to response. 4 = RMW to response. 5 = Flush to response. 6 = Probe to response. 7 = ATR to response.
51:63	RW	PERF_CONFIG_RESERVED: Reserved.

Register Name	NTL Performance Count Register
Mnemonic	NPU.STCK1.NTL0.REGS.PERF_COUNT
Address	00000000050111CF (SCOM)
Description	The NTL Performance Count register holds the performance counts from the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	IDIAL_PERF_COUNT0: Performance counter 0.

Bits	SCOM	Field Mnemonic: Description
16:31	RWX_WCLRREG	IDIAL_PERF_COUNT1: Performance counter 1.
32:47	RWX_WCLRREG	IDIAL_PERF_COUNT2: Performance counter 2.
48:63	RWX_WCLRREG	IDIAL_PERF_COUNT3: Performance counter 3.

Register Name	NTL CREQ Header Array Pointer Register
Mnemonic	NPU.STCK1.NTL0.REGS.CREQ_HA_PTR
Address	00000000050111D0 (SCOM)
Description	The NTL CREQ Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding CREQ header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	CREQ_HA_PTR_RESERVED1: Reserved.
5:11	RW	CREQ_HA_PTR_START: Starting header array location for CREQ headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	CREQ_HA_PTR_RESERVED2: Reserved.
17:23	RW	CREQ_HA_PTR_END: Ending header array location for CREQ headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL PRB Header Array Pointer Register
Mnemonic	NPU.STCK1.NTL0.REGS.PRB_HA_PTR
Address	00000000050111D1 (SCOM)
Description	The NTL PRB Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding PRB header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	PRB_HA_PTR_RESERVED1: Reserved.
5:11	RW	PRB_HA_PTR_START: Starting header array location for PRB headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	PRB_HA_PTR_RESERVED2: Reserved.
17:23	RW	PRB_HA_PTR_END: Ending header array location for PRB headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL ATR Header Array Pointer Register
Mnemonic	NPU.STCK1.NTL0.REGS.ATR_HA_PTR
Address	00000000050111D2 (SCOM)
Description	The NTL ATR Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding ATR header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	ATR_HA_PTR_RESERVED1: Reserved.
5:11	RW	ATR_HA_PTR_START: Starting header array location for ATR headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	ATR_HA_PTR_RESERVED2: Reserved.
17:23	RW	ATR_HA_PTR_END: Ending header array location for ATR headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Header Array Pointer Register
Mnemonic	NPU.STCK1.NTL0.REGS.RSP_HA_PTR
Address	00000000050111D3 (SCOM)
Description	The NTL RSP Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding RSP header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	RSP_HA_PTR_RESERVED1: Reserved.
5:11	RW	RSP_HA_PTR_START: Starting header array location for RSP headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	RSP_HA_PTR_RESERVED2: Reserved.
17:23	RW	RSP_HA_PTR_END: Ending header array location for RSP headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL CREQ Data Array Pointer Register
Mnemonic	NPU.STCK1.NTL0.REGS.CREQ_DA_PTR
Address	00000000050111D4 (SCOM)
Description	The NTL CREQ Data Array Pointer register is used to change the start and/or end entry in the NTL data array for holding CREQ data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	CREQ_DA_PTR_RESERVED1: Reserved.
3:11	RW	CREQ_DA_PTR_START: Starting data array location for CREQ data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	CREQ_DA_PTR_RESERVED2: Reserved.
15:23	RW	CREQ_DA_PTR_END: Ending data array location for CREQ data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Data Array Pointer Register
Mnemonic	NPU.STCK1.NTL0.REGS.RSP_DA_PTR
Address	00000000050111D5 (SCOM)
Description	The NTL RSP Data Array Pointer register is used to change the start and/or end entry in the NTL data array for holding RSP data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	RSP_DA_PTR_RESERVED1: Reserved.
3:11	RW	RSP_DA_PTR_START: Starting data array location for RSP data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	RSP_DA_PTR_RESERVED2: Reserved.
15:23	RW	RSP_DA_PTR_END: Ending data array location for RSP data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL Private Register Interface (PRI) Configuration Register
Mnemonic	NPU.STCK1.NTL0.REGS.PRI_CONFIG
Address	00000000050111D6 (SCOM)
Description	The NTL Private Register Interface (PRI) Configuration register is used to set up the PRI settings for this NTL. This register must be configured before any PRI requests are attempted to NDL or PHY registers.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PRI_CONFIG_NDL: NDL indication sent in the PRI read/write access: 00 = NDL 0. 01 = NDL 1. 10 = NDL 2. 11 = Disable (this disables the NTL from decoding the NDL register space).
2:3	RW	PRI_CONFIG_PHY: Indicates if this NTL should decode a PHY register space: 00 = Decode PHY 0 register space (only one NTL that is connected to PHY 0 must be set to this value). 01 = Decode PHY 1 register space (only one NTL that is connected to PHY 1 must be set to this value). 1X = Do not decode any PHY register space.
4:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	NTL Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK1.NTL0.REGS.CONFIG1
Address	00000000050111D8 (SCOM)
Description	The NTL Miscellaneous Configuration 1 register is used to control NVLink packet formatting by the POWER9 processor. It also controls resetting of the POWER9 NTL.

Bits	SCOM	Field Mnemonic: Description
0	RW	COMPRESSED_RSP_ENA: When set to 0b1, the NTL attempts to compress responses that it sends to the GPU whenever possible.
1:3	RW	CONFIG1_RESERVED1: Reserved.

Bits	SCOM	Field Mnemonic: Description
4	RW	CREQ_AE_ALWAYS: When set to 0b1, the NTL always sends an AE flit when it sends a CREQ packet to the GPU.
5	RW	DGD_AE_ALWAYS: When set to 0b1, the NTL always sends an AE flit when it sends a downgrade packet to the GPU.
6	RW	RSP_AE_ALWAYS: When set to 0b1, the NTL always sends an AE flit when it sends a response packet to the GPU.
7	RW	CONFIG1_RESERVED2: Reserved.
8:9	RW	NTL_RESET: This field indicates the NTL reset mode: 00 = Reset disabled. 11 = Reset (fence) both NTL and the processor bus for this brick. 10 = Reset (fence) only the processor bus for this brick, the NTL is operational. 01 = Reserved. **Note:** The only legal sequence is 00 →11 →10 →00. This field should not be changed unless bits 0:1 in the CQ Fence Status register equals the value in this field.
10:63	RW	CONFIG1_RESERVED3: Reserved.

Register Name	NTL Scratch 1 Register
Mnemonic	NPU.STCK1.NTL0.REGS.SCRATCH1
Address	00000000050111DA (SCOM)
Description	The NTL scratch 1 register is provided in case a new control function is required in the future. This register has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH1: Scratch register.

Register Name	NTL Low Power Register
Mnemonic	NPU.STCK1.NTL0.REGS.LOW_PWR
Address	00000000050111DC (SCOM)
Description	The NTL Low Power Configuration register is used to enable the NPU to request that the NVLink interconnect be placed into low-power mode. The register also defines the conditions under which the NPU turns its low-power request on or off.

Bits	SCOM	Field Mnemonic: Description
0	RW	LP_MODE_ENABLE: When set to 0b1, this NTL is allowed to activate the low-power requested signal to NDL when the low-power count is greater than or equal to the low-power count threshold.
1	RW	LP_ONLY_MODE: When set to 0b1, this NTL activates the low-power requested signal to NDL continuously. This can be used for lab stress or debug.
2:7	RW	LP_TIMER_TICK_CONFIG: Rate for the low-power timer tick (2^n cycles).
8:19	RW	LP_MIN_CRED_THRESH: Whenever the NDL replay buffer credits is greater than this threshold, the low-power requested signal to NDL is deactivated. This value must be greater than 0 and less than the maximum credit threshold.
20:31	RW	LP_MAX_CRED_THRESH: Whenever the NDL replay buffer credits is greater than or equal to this threshold and the low-power timer tick is active, then the low-power count is incremented by 1. This value must be greater than the minimum credit threshold.

Bits	SCOM	Field Mnemonic: Description
32:43	RW	LP_CNT_THRESH: Whenever the low-power count is greater than or equal to this threshold, this NTL activates the low-power requested signal to NDL until the NDL replay buffer credits is less than the low-power minimum credit threshold. This value must be greater than 0.
44:63	RO	Constant = 0b00000000000000000000

Register Name	NTL Miscellaneous Configuration 2 Register
Mnemonic	NPU.STCK1.NTL1.REGS.CONFIG2
Address	00000000050111E0 (SCOM)
Description	The NTL Miscellaneous Configuration 2 register is used to control internal NTL function. It contains mode bits, chicken switches, and thresholds.

Bits	SCOM	Field Mnemonic: Description
0	RW	BRICK_ENABLE: When set to 0b1, this NVLink brick is enabled. This configuration bit is used as a general clock gate for latches in the NTL design.
1	RW	RSP_CTL_CRED_SINGLE_ENA: When set to 0b1, the NTL only gives the CQ_CTL one RSP credit at a time, instead of the normal 2.
2	RW	CREQ_BE_128: When set to 0b1, the NTL always sends 128 bytes of data when it needs to send a byte enable (BE) flit to the GPU for a CREQ packet. When set to 0b0, the NTL sends the least number of data flits required.
3	RW	DGD_BE_128: When set to 0b1, the NTL always sends 128 bytes of data when it needs to send a byte enable (BE) flit to the GPU for a downgrade packet (BE and data flits are sent in the TransDone packet for the downgrade). When set to 0b0, the NTL sends the least number of data flits required.
4	RW	WR_SPLIT_UT0_ENA: When set to 0b1, the NTL splits up write requests with UT = 0 from the GPU that map to the MMIO space into legal processor bus sizes/alignments. When set to 0b0, the NTL passes all write requests with UT = 0 as is to the CQ.
5	RW	WR_SPLIT_UT1_ENA: When set to 0b1, the NTL splits up write requests with UT = 1 from the GPU into legal processor bus sizes/alignments. This includes both DMA writes and MMIO writes since there is no way for the NTL to distinguish between them. When set to 0b0, the NTL passes all write requests with UT = 1 as is to the CQ.
6	RW	BRICK_DEBUG_MODE: When set to 0b1, the NTL ignores all incoming NVLink packets from the GPU and throws away all NVLink requests/responses from the CQ destined for the GPU. This mode is used for debug purposes only when the NPU is not connected over NVLink to a GPU.
7	RW	P9_TO_P9_MODE: When set to 0b1, the NTL sets UT = 1 for all incoming read, write, and atomic NVLink packets before sending to the CQ. This mode is used for debug purposes only when the NPU is connected to another/same NPU over NVLink.
8:9	RW	CONFIG2_RESERVED1: Reserved.
10:15	RW	CAM256_MAX_CNT: This field specifies the number of entries in the CAM that holds information to send responses for 256 byte operations that require a response (maximum value = 48).
16	RW	NDL_RX_PARITY_ENA: When set to 0b1, the NTL checks the parity on the incoming NDL RX signals.
17	RW	NDL_TX_PARITY_ENA: When set to 0b1, the NTL checks the parity on the incoming NDL TX (that is, TX credits) signals.
18	RW	NDL_PRI_PARITY_ENA: When set to 0b1, the NTL checks the parity on the incoming NDL signals.
19	RW	RCV_CREDIT_OVERFLOW_ENA: When set to 0b1, the NTL checks for overflows on any received credits from the GPU, NDL, and NDL wrapper.
20	RW	HDR_ARR_ECC_CORR_ENA: When set to 0b1, the NTL corrects ECC SBEs when reading the RX header array.

Bits	SCOM	Field Mnemonic: Description
21	RW	DAT_ARR_ECC_CORR_ENA: When set to 0b1, the NTL corrects ECC SBEs when reading the RX data array. The NTL only corrects ECC on reads of the RX data array that require the NTL to update the data before sending to CQ_DAT (for example, BE flit or data flits for atomic CAS ops).
22	RW	TX_DATA_ECC_CORR_ENA: When set to 0b1, the NTL corrects ECC SBEs when reading TX data from CQ_DAT.
23	RW	CONFIG2_RESERVED2: Reserved.
24	RW	PARITY_ERROR_SUE_ENA: When set to 0b1, the NTL drives SUE on all data transfers to CQ_DAT for a packet that has a parity error on an incoming data flit.
25	RW	DATA_POISON_SUE_ENA: When set to 0b1, the NTL drives SUE on all data transfers to CQ_DAT for a packet that receives LMD = data poison.
26	RW	HDR_ARR_ECC_SUE_ENA: When set to 0b1, the NTL drives SUE on all data transfers to CQ_DAT for a packet that has an ECC UE/SUE on the header info read from the RC header array.
27	RW	DAT_ARR_ECC_SUE_ENA: When set to 0b1, the NTL drives SUE on all data transfers to CQ_DAT for a packet that has an ECC UE/SUE on data read from the RX data array. The NTL only checks ECC on reads of the RX data array that require the NTL to update the data before sending to CQ_DAT (for example, BE flit or data flits for atomic CAS ops).
28	RW	TX_ECC_DATA_POISON_ENA: When set to 0b1, the NTL sends LMD = data poison for an outgoing NVLink packet that encounters an ECC UE/SUE on data read from CQ_DAT.
29:31	RW	CONFIG2_RESERVED3: Reserved.
32	RW	PRI_STATE_MACHINE_RESET: Reset PRI state machine to idle state (debug use only).
33:63	RW	CONFIG2_RESERVED4: Reserved.

Register Name	NTL Miscellaneous Configuration 3 Register
Mnemonic	NPU.STCK1.NTL1.REGS.CONFIG3
Address	00000000050111E1 (SCOM)
Description	The NTL Miscellaneous Configuration 3 register is used for future control of internal NTL functions. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG3_RESERVED1: Reserved.

Register Name	NTL CERR Hold 1 Register
Mnemonic	NPU.STCK1.NTL1.REGS.CERR_HOLD1
Address	00000000050111E2 (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLRREG	NTL_HOLD1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RWX_WCLRREG	NTL_HOLD1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RWX_WCLRREG	NTL_HOLD1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.

Bits	SCOM	Field Mnemonic: Description
4	RWX_WCLRREG	NTL_HOLD1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RWX_WCLRREG	NTL_HOLD1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLRREG	NTL_HOLD1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RWX_WCLRREG	NTL_HOLD1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RWX_WCLRREG	NTL_HOLD1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RWX_WCLRREG	NTL_HOLD1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RWX_WCLRREG	NTL_HOLD1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLRREG	NTL_HOLD1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RWX_WCLRREG	NTL_HOLD1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	RWX_WCLRREG	NTL_HOLD1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RWX_WCLRREG	NTL_HOLD1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RWX_WCLRREG	NTL_HOLD1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RWX_WCLRREG	NTL_HOLD1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RWX_WCLRREG	NTL_HOLD1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLRREG	NTL_HOLD1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLRREG	NTL_HOLD1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLRREG	NTL_HOLD1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLRREG	NTL_HOLD1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLRREG	NTL_HOLD1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLRREG	NTL_HOLD1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLRREG	NTL_HOLD1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RWX_WCLRREG	NTL_HOLD1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RWX_WCLRREG	NTL_HOLD1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RWX_WCLRREG	NTL_HOLD1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RWX_WCLRREG	NTL_HOLD1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RWX_WCLRREG	NTL_HOLD1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RWX_WCLRREG	NTL_HOLD1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RWX_WCLRREG	NTL_HOLD1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RWX_WCLRREG	NTL_HOLD1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RWX_WCLRREG	NTL_HOLD1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RWX_WCLRREG	NTL_HOLD1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLRREG	NTL_HOLD1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RWX_WCLRREG	NTL_HOLD1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RWX_WCLRREG	NTL_HOLD1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RWX_WCLRREG	NTL_HOLD1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RWX_WCLRREG	NTL_HOLD1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RWX_WCLRREG	NTL_HOLD1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RWX_WCLRREG	NTL_HOLD1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RWX_WCLRREG	NTL_HOLD1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RWX_WCLRREG	NTL_HOLD1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RWX_WCLRREG	NTL_HOLD1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	RWX_WCLRREG	NTL_HOLD1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RWX_WCLRREG	NTL_HOLD1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RWX_WCLRREG	NTL_HOLD1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RWX_WCLRREG	NTL_HOLD1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RWX_WCLRREG	NTL_HOLD1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RWX_WCLRREG	NTL_HOLD1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLRREG	NTL_HOLD1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLRREG	NTL_HOLD1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLRREG	NTL_HOLD1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLRREG	NTL_HOLD1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLRREG	NTL_HOLD1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLRREG	NTL_HOLD1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RWX_WCLRREG	NTL_HOLD1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RWX_WCLRREG	NTL_HOLD1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RWX_WCLRREG	NTL_HOLD1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RWX_WCLRREG	NTL_HOLD1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RWX_WCLRREG	NTL_HOLD1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLRREG	NTL_HOLD1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.

Bits	SCOM	Field Mnemonic: Description
63	RWX_WCLRREG	NTL_HOLD1_63: ERROR - NTL RX - Reserved.

Register Name	NTL CERR Mask 1 Register
Mnemonic	NPU.STCK1.NTL1.REGS.CERR_MASK1
Address	00000000050111E3 (SCOM)
Description	c_err_rpt mask latches read-only register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	ROX	NTL_MASK1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	ROX	NTL_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	ROX	NTL_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	ROX	NTL_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	ROX	NTL_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	ROX	NTL_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	ROX	NTL_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	ROX	NTL_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	ROX	NTL_MASK1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	ROX	NTL_MASK1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	ROX	NTL_MASK1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	ROX	NTL_MASK1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	ROX	NTL_MASK1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	ROX	NTL_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	ROX	NTL_MASK1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	ROX	NTL_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	ROX	NTL_MASK1_17: ERROR - NTL RX - Reserved.
18	ROX	NTL_MASK1_18: ERROR - NTL RX - Reserved.
19	ROX	NTL_MASK1_19: ERROR - NTL RX - Reserved.
20	ROX	NTL_MASK1_20: ERROR - NTL RX - Reserved.
21	ROX	NTL_MASK1_21: ERROR - NTL RX - Reserved.

Bits	SCOM	Field Mnemonic: Description
22	ROX	NTL_MASK1_22: ERROR - NTL RX - Reserved.
23	ROX	NTL_MASK1_23: ERROR - NTL RX - Reserved.
24	ROX	NTL_MASK1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	ROX	NTL_MASK1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	ROX	NTL_MASK1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	ROX	NTL_MASK1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	ROX	NTL_MASK1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	ROX	NTL_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	ROX	NTL_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	ROX	NTL_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	ROX	NTL_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	ROX	NTL_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	ROX	NTL_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	ROX	NTL_MASK1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	ROX	NTL_MASK1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	ROX	NTL_MASK1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	ROX	NTL_MASK1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	ROX	NTL_MASK1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	ROX	NTL_MASK1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	ROX	NTL_MASK1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	ROX	NTL_MASK1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	ROX	NTL_MASK1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	ROX	NTL_MASK1_44: ERROR - NTL RX - More than one VC tried to write the header and/or data array on the same cycle.
45	ROX	NTL_MASK1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	ROX	NTL_MASK1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	ROX	NTL_MASK1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	ROX	NTL_MASK1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	ROX	NTL_MASK1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	ROX	NTL_MASK1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.

Bits	SCOM	Field Mnemonic: Description
51	ROX	NTL_MASK1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	ROX	NTL_MASK1_52: ERROR - NTL RX - Reserved.
53	ROX	NTL_MASK1_53: ERROR - NTL RX - Reserved.
54	ROX	NTL_MASK1_54: ERROR - NTL RX - Reserved.
55	ROX	NTL_MASK1_55: ERROR - NTL RX - Reserved.
56	ROX	NTL_MASK1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	ROX	NTL_MASK1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	ROX	NTL_MASK1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	ROX	NTL_MASK1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	ROX	NTL_MASK1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	ROX	NTL_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	ROX	NTL_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	ROX	NTL_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First 1 Register**
Mnemonic	NPU.STCK1.NTL1.REGS.CERR_FIRST1
Address	00000000050111E4 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLEAR	NTL_FIRST1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.
2	RWX_WCLEAR	NTL_FIRST1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RWX_WCLEAR	NTL_FIRST1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RWX_WCLEAR	NTL_FIRST1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RWX_WCLEAR	NTL_FIRST1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLEAR	NTL_FIRST1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RWX_WCLEAR	NTL_FIRST1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RWX_WCLEAR	NTL_FIRST1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RWX_WCLEAR	NTL_FIRST1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RWX_WCLEAR	NTL_FIRST1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	NTL_FIRST1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RWX_WCLEAR	NTL_FIRST1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT=0 request packet where the address field is valid and not ATR.
13	RWX_WCLEAR	NTL_FIRST1_13: ERROR - NTL RX - DatLen /= 16,32,64,128B in an incoming NVLink probe packet.
14	RWX_WCLEAR	NTL_FIRST1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RWX_WCLEAR	NTL_FIRST1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RWX_WCLEAR	NTL_FIRST1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RWX_WCLEAR	NTL_FIRST1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLEAR	NTL_FIRST1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLEAR	NTL_FIRST1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLEAR	NTL_FIRST1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLEAR	NTL_FIRST1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLEAR	NTL_FIRST1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLEAR	NTL_FIRST1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLEAR	NTL_FIRST1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RWX_WCLEAR	NTL_FIRST1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RWX_WCLEAR	NTL_FIRST1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RWX_WCLEAR	NTL_FIRST1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RWX_WCLEAR	NTL_FIRST1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RWX_WCLEAR	NTL_FIRST1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RWX_WCLEAR	NTL_FIRST1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RWX_WCLEAR	NTL_FIRST1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.
32	RWX_WCLEAR	NTL_FIRST1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RWX_WCLEAR	NTL_FIRST1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RWX_WCLEAR	NTL_FIRST1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RWX_WCLEAR	NTL_FIRST1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RWX_WCLEAR	NTL_FIRST1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RWX_WCLEAR	NTL_FIRST1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RWX_WCLEAR	NTL_FIRST1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RWX_WCLEAR	NTL_FIRST1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RWX_WCLEAR	NTL_FIRST1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RWX_WCLEAR	NTL_FIRST1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.

Bits	SCOM	Field Mnemonic: Description
42	RWX_WCLEAR	NTL_FIRST1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RWX_WCLEAR	NTL_FIRST1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RWX_WCLEAR	NTL_FIRST1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or data array on the same cycle.
45	RWX_WCLEAR	NTL_FIRST1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RWX_WCLEAR	NTL_FIRST1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RWX_WCLEAR	NTL_FIRST1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RWX_WCLEAR	NTL_FIRST1_48: ERROR - NTL RX - A CQ global credit was received when three were already valid (overflow).
49	RWX_WCLEAR	NTL_FIRST1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RWX_WCLEAR	NTL_FIRST1_50: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLEAR	NTL_FIRST1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLEAR	NTL_FIRST1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLEAR	NTL_FIRST1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLEAR	NTL_FIRST1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLEAR	NTL_FIRST1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLEAR	NTL_FIRST1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RWX_WCLEAR	NTL_FIRST1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RWX_WCLEAR	NTL_FIRST1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RWX_WCLEAR	NTL_FIRST1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.
60	RWX_WCLEAR	NTL_FIRST1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RWX_WCLEAR	NTL_FIRST1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLEAR	NTL_FIRST1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLEAR	NTL_FIRST1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First Mask 1 Register**
Mnemonic	NPU.STCK1.NTL1.REGS.CERR_FIRST_MASK1
Address	00000000050111E5 (SCOM)
Description	Mask errors from being captured in the First1 Error registers and the RAS Error Message registers.

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RW	NTL_FIRST_MASK1_1: ERROR - NTL RX - AN /= 1 in an incoming NVLink packet where RX Vld = 1 and RX Hdr Vld = 1.

Bits	SCOM	Field Mnemonic: Description
2	RW	NTL_FIRST_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the address field is valid.
3	RW	NTL_FIRST_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the address field is valid.
4	RW	NTL_FIRST_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink read, write, atomic, or RMW request packet.
5	RW	NTL_FIRST_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RW	NTL_FIRST_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid and not read or write.
7	RW	NTL_FIRST_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink request/response with data packet.
8	RW	NTL_FIRST_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink atomic CAS packet.
9	RW	NTL_FIRST_MASK1_9: ERROR - NTL RX - Compressed responses not populated in the order CR0, CR1, and CR2 in an incoming NVLink response packet.
10	RW	NTL_FIRST_MASK1_10: ERROR - NTL RX - Compressed response with an invalid/reserved TD/IVC combination in an incoming NVLink response packet.
11	RW	NTL_FIRST_MASK1_11: ERROR - NTL RX - Address(63:49) /= 0 in an incoming NVLink request packet where the address field is valid.
12	RW	NTL_FIRST_MASK1_12: ERROR - NTL RX - Address(48:47) /= 0 in an incoming NVLink UT = 0 request packet where the address field is valid and not ATR.
13	RW	NTL_FIRST_MASK1_13: ERROR - NTL RX - DatLen /= 16, 32, 64, or 128B in an incoming NVLink probe packet.
14	RW	NTL_FIRST_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink request/response with data packet.
15	RW	NTL_FIRST_MASK1_15: ERROR - NTL RX - AtomicSz /= 4B or 8B in an incoming NVLink atomic packet.
16	RW	NTL_FIRST_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink atomic packet where no BE flit exists.
17	RW	NTL_FIRST_MASK1_17: ERROR - NTL RX - Reserved.
18	RW	NTL_FIRST_MASK1_18: ERROR - NTL RX - Reserved.
19	RW	NTL_FIRST_MASK1_19: ERROR - NTL RX - Reserved.
20	RW	NTL_FIRST_MASK1_20: ERROR - NTL RX - Reserved.
21	RW	NTL_FIRST_MASK1_21: ERROR - NTL RX - Reserved.
22	RW	NTL_FIRST_MASK1_22: ERROR - NTL RX - Reserved.
23	RW	NTL_FIRST_MASK1_23: ERROR - NTL RX - Reserved.
24	RW	NTL_FIRST_MASK1_24: ERROR - NTL RX - ECC UE on data(0:63) read from the header array.
25	RW	NTL_FIRST_MASK1_25: ERROR - NTL RX - ECC UE on data(64:127) read from the header array.
26	RW	NTL_FIRST_MASK1_26: ERROR - NTL RX - ECC UE on data(128:167) read from the header array.
27	RW	NTL_FIRST_MASK1_27: ERROR - NTL RX - ECC UE on data(0:63) read from the data array.
28	RW	NTL_FIRST_MASK1_28: ERROR - NTL RX - ECC UE on data(64:127) read from the data array.
29	RW	NTL_FIRST_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL RX Vld and Hdr_Vld signals.
30	RW	NTL_FIRST_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL RX LMD and CRC signals.
31	RW	NTL_FIRST_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL RX header flit signals.

Bits	SCOM	Field Mnemonic: Description
32	RW	NTL_FIRST_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL RX AE flit signals.
33	RW	NTL_FIRST_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL RX data flit signals.
34	RW	NTL_FIRST_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = data poison.
35	RW	NTL_FIRST_MASK1_35: ERROR - NTL RX - New CREQ header flit from NVLink received when the CREQ header array is full.
36	RW	NTL_FIRST_MASK1_36: ERROR - NTL RX - New CREQ data flit from NVLink received when the CREQ data array is full.
37	RW	NTL_FIRST_MASK1_37: ERROR - NTL RX - CREQ data flit was attempted to be read from the CREQ data array when it was empty.
38	RW	NTL_FIRST_MASK1_38: ERROR - NTL RX - New RSP header flit from NVLink received when the RSP header array is full.
39	RW	NTL_FIRST_MASK1_39: ERROR - NTL RX - New RSP data flit from NVLink received when the RSP data array is full.
40	RW	NTL_FIRST_MASK1_40: ERROR - NTL RX - RSP data flit was attempted to be read from the RSP data array when it was empty.
41	RW	NTL_FIRST_MASK1_41: ERROR - NTL RX - New PRB header flit from NVLink received when the PRB header array is full.
42	RW	NTL_FIRST_MASK1_42: ERROR - NTL RX - New ATR header flit from NVLink received when the ATR header array is full.
43	RW	NTL_FIRST_MASK1_43: ERROR - NTL RX - A new NVLink header flit was received when NTL was still expecting data flits for the previous packet.
44	RW	NTL_FIRST_MASK1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or data array on the same cycle.
45	RW	NTL_FIRST_MASK1_45: ERROR - NTL RX - A CQ slice credit was received when one was already valid (overflow).
46	RW	NTL_FIRST_MASK1_46: ERROR - NTL RX - A CQ ATR credit was received when one was already valid (overflow).
47	RW	NTL_FIRST_MASK1_47: ERROR - NTL RX - A CQ flush credit was received when 15 were already valid (overflow).
48	RW	NTL_FIRST_MASK1_48: ERROR - NTL RX - A CQ global credit was received when 3 were already valid (overflow).
49	RW	NTL_FIRST_MASK1_49: ERROR - NTL RX - A CQ response credit was received when one was already valid (overflow).
50	RW	NTL_FIRST_MASK1_50: ERROR - NTL RX – A send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RW	NTL_FIRST_MASK1_51: ERROR - NTL RX - A send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RW	NTL_FIRST_MASK1_52: ERROR - NTL RX - Reserved.
53	RW	NTL_FIRST_MASK1_53: ERROR - NTL RX - Reserved.
54	RW	NTL_FIRST_MASK1_54: ERROR - NTL RX - Reserved.
55	RW	NTL_FIRST_MASK1_55: ERROR - NTL RX - Reserved.
56	RW	NTL_FIRST_MASK1_56: ERROR - NTL RX - ECC CE on data(0:63) read from the header array.
57	RW	NTL_FIRST_MASK1_57: ERROR - NTL RX - ECC CE on data(64:127) read from the header array.
58	RW	NTL_FIRST_MASK1_58: ERROR - NTL RX - ECC CE on data(128:167) read from the header array.
59	RW	NTL_FIRST_MASK1_59: ERROR - NTL RX - ECC CE on data(0:63) read from the data array.

Bits	SCOM	Field Mnemonic: Description
60	RW	NTL_FIRST_MASK1_60: ERROR - NTL RX - ECC CE on data(64:127) read from the data array.
61	RW	NTL_FIRST_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RW	NTL_FIRST_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RW	NTL_FIRST_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR Hold 2 Register**
Mnemonic	NPU.STCK1.NTL1.REGS.CERR_HOLD2
Address	00000000050111E6 (SCOM)
Description	c_err_rpt hold latches read-write-clear registers.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RWX_WCLRREG	NTL_HOLD2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RWX_WCLRREG	NTL_HOLD2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RWX_WCLRREG	NTL_HOLD2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RWX_WCLRREG	NTL_HOLD2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RWX_WCLRREG	NTL_HOLD2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RWX_WCLRREG	NTL_HOLD2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLRREG	NTL_HOLD2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLRREG	NTL_HOLD2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLRREG	NTL_HOLD2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLRREG	NTL_HOLD2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLRREG	NTL_HOLD2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLRREG	NTL_HOLD2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLRREG	NTL_HOLD2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RWX_WCLRREG	NTL_HOLD2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RWX_WCLRREG	NTL_HOLD2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLRREG	NTL_HOLD2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLRREG	NTL_HOLD2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLRREG	NTL_HOLD2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLRREG	NTL_HOLD2_19: ERROR - NTL TX - Reserved.
20	RWX_WCLRREG	NTL_HOLD2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLRREG	NTL_HOLD2_21: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
22	RWX_WCLRREG	NTL_HOLD2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLRREG	NTL_HOLD2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLRREG	NTL_HOLD2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RWX_WCLRREG	NTL_HOLD2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RWX_WCLRREG	NTL_HOLD2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLRREG	NTL_HOLD2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLRREG	NTL_HOLD2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLRREG	NTL_HOLD2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLRREG	NTL_HOLD2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLRREG	NTL_HOLD2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLRREG	NTL_HOLD2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RWX_WCLRREG	NTL_HOLD2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RWX_WCLRREG	NTL_HOLD2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RWX_WCLRREG	NTL_HOLD2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RWX_WCLRREG	NTL_HOLD2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RWX_WCLRREG	NTL_HOLD2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RWX_WCLRREG	NTL_HOLD2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RWX_WCLRREG	NTL_HOLD2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RWX_WCLRREG	NTL_HOLD2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	RWX_WCLRREG	NTL_HOLD2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	RWX_WCLRREG	NTL_HOLD2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLRREG	NTL_HOLD2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLRREG	NTL_HOLD2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLRREG	NTL_HOLD2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLRREG	NTL_HOLD2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLRREG	NTL_HOLD2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLRREG	NTL_HOLD2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLRREG	NTL_HOLD2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLRREG	NTL_HOLD2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLRREG	NTL_HOLD2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLRREG	NTL_HOLD2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RWX_WCLRREG	NTL_HOLD2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RWX_WCLRREG	NTL_HOLD2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.

Bits	SCOM	Field Mnemonic: Description
55	RWX_WCLRREG	NTL_HOLD2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RWX_WCLRREG	NTL_HOLD2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RWX_WCLRREG	NTL_HOLD2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RWX_WCLRREG	NTL_HOLD2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RWX_WCLRREG	NTL_HOLD2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RWX_WCLRREG	NTL_HOLD2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLRREG	NTL_HOLD2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLRREG	NTL_HOLD2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLRREG	NTL_HOLD2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR Mask 2 Register**
Mnemonic	NPU.STCK1.NTL1.REGS.CERR_MASK2
Address	00000000050111E7 (SCOM)
Description	c_err_rpt mask latches read-only register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	ROX	NTL_MASK2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	ROX	NTL_MASK2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	ROX	NTL_MASK2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	ROX	NTL_MASK2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	ROX	NTL_MASK2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	ROX	NTL_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	ROX	NTL_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	ROX	NTL_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	ROX	NTL_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	ROX	NTL_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	ROX	NTL_MASK2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	ROX	NTL_MASK2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	ROX	NTL_MASK2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	ROX	NTL_MASK2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	ROX	NTL_MASK2_15: ERROR - NTL TX - Reserved.
16	ROX	NTL_MASK2_16: ERROR - NTL TX - Reserved.
17	ROX	NTL_MASK2_17: ERROR - NTL TX - Reserved.
18	ROX	NTL_MASK2_18: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
19	ROX	NTL_MASK2_19: ERROR - NTL TX - Reserved.
20	ROX	NTL_MASK2_20: ERROR - NTL TX - Reserved.
21	ROX	NTL_MASK2_21: ERROR - NTL TX - Reserved.
22	ROX	NTL_MASK2_22: ERROR - NTL TX - Reserved.
23	ROX	NTL_MASK2_23: ERROR - NTL TX - Reserved.
24	ROX	NTL_MASK2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	ROX	NTL_MASK2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	ROX	NTL_MASK2_26: ERROR - NTL TX - Reserved.
27	ROX	NTL_MASK2_27: ERROR - NTL TX - Reserved.
28	ROX	NTL_MASK2_28: ERROR - NTL TX - Reserved.
29	ROX	NTL_MASK2_29: ERROR - NTL TX - Reserved.
30	ROX	NTL_MASK2_30: ERROR - NTL TX - Reserved.
31	ROX	NTL_MASK2_31: ERROR - NTL TX - Reserved.
32	ROX	NTL_MASK2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	ROX	NTL_MASK2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	ROX	NTL_MASK2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	ROX	NTL_MASK2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	ROX	NTL_MASK2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	ROX	NTL_MASK2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	ROX	NTL_MASK2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	ROX	NTL_MASK2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	ROX	NTL_MASK2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	ROX	NTL_MASK2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	ROX	NTL_MASK2_42: ERROR - NTL REGS - Reserved.
43	ROX	NTL_MASK2_43: ERROR - NTL REGS - Reserved.
44	ROX	NTL_MASK2_44: ERROR - NTL REGS - Reserved.
45	ROX	NTL_MASK2_45: ERROR - NTL REGS - Reserved.
46	ROX	NTL_MASK2_46: ERROR - NTL REGS - Reserved.
47	ROX	NTL_MASK2_47: ERROR - NTL REGS - Reserved.
48	ROX	NTL_MASK2_48: ERROR - NTL REGS - Reserved.
49	ROX	NTL_MASK2_49: ERROR - NTL REGS - Reserved.
50	ROX	NTL_MASK2_50: ERROR - NTL REGS - Reserved.
51	ROX	NTL_MASK2_51: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
52	ROX	NTL_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	ROX	NTL_MASK2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	ROX	NTL_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	ROX	NTL_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	ROX	NTL_MASK2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	ROX	NTL_MASK2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	ROX	NTL_MASK2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	ROX	NTL_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	ROX	NTL_MASK2_60: ERROR - NTL REGS - Reserved.
61	ROX	NTL_MASK2_61: ERROR - NTL REGS - Reserved.
62	ROX	NTL_MASK2_62: ERROR - NTL REGS - Reserved.
63	ROX	NTL_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR First 2 Register**
Mnemonic	NPU.STCK1.NTL1.REGS.CERR_FIRST2
Address	00000000050111E8 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RWX_WCLEAR	NTL_FIRST2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RWX_WCLEAR	NTL_FIRST2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RWX_WCLEAR	NTL_FIRST2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RWX_WCLEAR	NTL_FIRST2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RWX_WCLEAR	NTL_FIRST2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RWX_WCLEAR	NTL_FIRST2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLEAR	NTL_FIRST2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLEAR	NTL_FIRST2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLEAR	NTL_FIRST2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLEAR	NTL_FIRST2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLEAR	NTL_FIRST2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLEAR	NTL_FIRST2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLEAR	NTL_FIRST2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.

Bits	SCOM	Field Mnemonic: Description
14	RWX_WCLEAR	NTL_FIRST2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RWX_WCLEAR	NTL_FIRST2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLEAR	NTL_FIRST2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLEAR	NTL_FIRST2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLEAR	NTL_FIRST2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLEAR	NTL_FIRST2_19: ERROR - NTL TX - Reserved.
20	RWX_WCLEAR	NTL_FIRST2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLEAR	NTL_FIRST2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLEAR	NTL_FIRST2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLEAR	NTL_FIRST2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLEAR	NTL_FIRST2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RWX_WCLEAR	NTL_FIRST2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RWX_WCLEAR	NTL_FIRST2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLEAR	NTL_FIRST2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLEAR	NTL_FIRST2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLEAR	NTL_FIRST2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLEAR	NTL_FIRST2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLEAR	NTL_FIRST2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLEAR	NTL_FIRST2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RWX_WCLEAR	NTL_FIRST2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RWX_WCLEAR	NTL_FIRST2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RWX_WCLEAR	NTL_FIRST2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RWX_WCLEAR	NTL_FIRST2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RWX_WCLEAR	NTL_FIRST2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RWX_WCLEAR	NTL_FIRST2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RWX_WCLEAR	NTL_FIRST2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.
40	RWX_WCLEAR	NTL_FIRST2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	RWX_WCLEAR	NTL_FIRST2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	RWX_WCLEAR	NTL_FIRST2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLEAR	NTL_FIRST2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLEAR	NTL_FIRST2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLEAR	NTL_FIRST2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLEAR	NTL_FIRST2_46: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
47	RWX_WCLEAR	NTL_FIRST2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLEAR	NTL_FIRST2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLEAR	NTL_FIRST2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLEAR	NTL_FIRST2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLEAR	NTL_FIRST2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLEAR	NTL_FIRST2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RWX_WCLEAR	NTL_FIRST2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RWX_WCLEAR	NTL_FIRST2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RWX_WCLEAR	NTL_FIRST2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RWX_WCLEAR	NTL_FIRST2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RWX_WCLEAR	NTL_FIRST2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RWX_WCLEAR	NTL_FIRST2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RWX_WCLEAR	NTL_FIRST2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RWX_WCLEAR	NTL_FIRST2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLEAR	NTL_FIRST2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLEAR	NTL_FIRST2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLEAR	NTL_FIRST2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR First Mask 2 Register**
Mnemonic	NPU.STCK1.NTL1.REGS.CERR_FIRST_MASK2
Address	00000000050111E9 (SCOM)
Description	This register masks errors from being captured in the First 2 Error registers and the RAS Error Message registers.

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL TX credit signals.
1	RW	NTL_FIRST_MASK2_1: ERROR - NTL TX - ECC UE on data(0:63) read from CQ_DAT.
2	RW	NTL_FIRST_MASK2_2: ERROR - NTL TX - ECC UE on data(64:127) read from CQ_DAT.
3	RW	NTL_FIRST_MASK2_3: ERROR - NTL TX - ECC SUE on data(0:63) read from CQ_DAT.
4	RW	NTL_FIRST_MASK2_4: ERROR - NTL TX - ECC SUE on data(64:127) read from CQ_DAT.
5	RW	NTL_FIRST_MASK2_5: ERROR - NTL TX - Read or atomic request with a length that is not a power of 2.
6	RW	NTL_FIRST_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RW	NTL_FIRST_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RW	NTL_FIRST_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RW	NTL_FIRST_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).

Bits	SCOM	Field Mnemonic: Description
10	RW	NTL_FIRST_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RW	NTL_FIRST_MASK2_11: ERROR - NTL TX - More than one type of flit was attempted to be sent to NDL at the same time.
12	RW	NTL_FIRST_MASK2_12: ERROR - NTL TX - More than one entry in the 256B Ops CAM was hit at the same time.
13	RW	NTL_FIRST_MASK2_13: ERROR - NTL TX - More than one entry in the CREQ sticky CAM was hit at the same time.
14	RW	NTL_FIRST_MASK2_14: ERROR - NTL TX - More than one entry in the DGD sticky CAM was hit at the same time.
15	RW	NTL_FIRST_MASK2_15: ERROR - NTL TX - Reserved.
16	RW	NTL_FIRST_MASK2_16: ERROR - NTL TX - Reserved.
17	RW	NTL_FIRST_MASK2_17: ERROR - NTL TX - Reserved.
18	RW	NTL_FIRST_MASK2_18: ERROR - NTL TX - Reserved.
19	RW	NTL_FIRST_MASK2_19: ERROR - NTL TX - Reserved.
20	RW	NTL_FIRST_MASK2_20: ERROR - NTL TX - Reserved.
21	RW	NTL_FIRST_MASK2_21: ERROR - NTL TX - Reserved.
22	RW	NTL_FIRST_MASK2_22: ERROR - NTL TX - Reserved.
23	RW	NTL_FIRST_MASK2_23: ERROR - NTL TX - Reserved.
24	RW	NTL_FIRST_MASK2_24: ERROR - NTL TX - ECC CE on data(0:63) read from CQ_DAT.
25	RW	NTL_FIRST_MASK2_25: ERROR - NTL TX - ECC CE on data(64:127) read from CQ_DAT.
26	RW	NTL_FIRST_MASK2_26: ERROR - NTL TX - Reserved.
27	RW	NTL_FIRST_MASK2_27: ERROR - NTL TX - Reserved.
28	RW	NTL_FIRST_MASK2_28: ERROR - NTL TX - Reserved.
29	RW	NTL_FIRST_MASK2_29: ERROR - NTL TX - Reserved.
30	RW	NTL_FIRST_MASK2_30: ERROR - NTL TX - Reserved.
31	RW	NTL_FIRST_MASK2_31: ERROR - NTL TX - Reserved.
32	RW	NTL_FIRST_MASK2_32: ERROR - NTL REGS - CREQ header credits received from the GPU are greater than maximum value.
33	RW	NTL_FIRST_MASK2_33: ERROR - NTL REGS - DGD header credits received from the GPU are greater than maximum value.
34	RW	NTL_FIRST_MASK2_34: ERROR - NTL REGS - ATSD header credits received from the GPU are greater than maximum value.
35	RW	NTL_FIRST_MASK2_35: ERROR - NTL REGS - RSP header credits received from the GPU are greater than maximum value.
36	RW	NTL_FIRST_MASK2_36: ERROR - NTL REGS - CREQ data credits received from the GPU are greater than maximum value.
37	RW	NTL_FIRST_MASK2_37: ERROR - NTL REGS - RSP data credits received from the GPU are greater than maximum value.
38	RW	NTL_FIRST_MASK2_38: ERROR - NTL REGS - Replay buffer credits received from NDL are greater than 512.
39	RW	NTL_FIRST_MASK2_39: ERROR - NTL REGS - Asynchronous buffer credits received from the NDL wrapper are greater than 64.

Bits	SCOM	Field Mnemonic: Description
40	RW	NTL_FIRST_MASK2_40: ERROR - NTL REGS - Multiple PRI requests are active at the same time for different NTLs.
41	RW	NTL_FIRST_MASK2_41: ERROR - NTL REGS - Multiple PRI requests are active at the same time for the same NTL.
42	RW	NTL_FIRST_MASK2_42: ERROR - NTL REGS - Reserved.
43	RW	NTL_FIRST_MASK2_43: ERROR - NTL REGS - Reserved.
44	RW	NTL_FIRST_MASK2_44: ERROR - NTL REGS - Reserved.
45	RW	NTL_FIRST_MASK2_45: ERROR - NTL REGS - Reserved.
46	RW	NTL_FIRST_MASK2_46: ERROR - NTL REGS - Reserved.
47	RW	NTL_FIRST_MASK2_47: ERROR - NTL REGS - Reserved.
48	RW	NTL_FIRST_MASK2_48: ERROR - NTL REGS - Reserved.
49	RW	NTL_FIRST_MASK2_49: ERROR - NTL REGS - Reserved.
50	RW	NTL_FIRST_MASK2_50: ERROR - NTL REGS - Reserved.
51	RW	NTL_FIRST_MASK2_51: ERROR - NTL REGS - Reserved.
52	RW	NTL_FIRST_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a PRI response.
53	RW	NTL_FIRST_MASK2_53: ERROR - NTL REGS - NDL error indication received on a PRI response.
54	RW	NTL_FIRST_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a PRI response.
55	RW	NTL_FIRST_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a PRI response.
56	RW	NTL_FIRST_MASK2_56: ERROR - NTL REGS - Parity error indication received on a PRI response.
57	RW	NTL_FIRST_MASK2_57: ERROR - NTL REGS - Protocol error indication received on a PRI response.
58	RW	NTL_FIRST_MASK2_58: ERROR - NTL REGS - PRI acknowledgment signal from NDL wrapper went invalid in the middle of a PRI response.
59	RW	NTL_FIRST_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL PRI response signals.
60	RW	NTL_FIRST_MASK2_60: ERROR - NTL REGS - Reserved.
61	RW	NTL_FIRST_MASK2_61: ERROR - NTL REGS - Reserved.
62	RW	NTL_FIRST_MASK2_62: ERROR - NTL REGS - Reserved.
63	RW	NTL_FIRST_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	NTL Scratch 2 Register
Mnemonic	NPU.STCK1.NTL1.REGS.SCRATCH2
Address	00000000050111EA (SCOM)
Description	The NTL Scratch 2 register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH2: Scratch register.

Register Name	NTL Scratch 3 Register
Mnemonic	NPU.STCK1.NTL1.REGS.SCRATCH3
Address	00000000050111EB (SCOM)
Description	The NTL Scratch 3 Register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH3: Scratch register.

Register Name	NTL Debug0 Configuration Register
Mnemonic	NPU.STCK1.NTL1.REGS.DEBUG0_CONFIG
Address	00000000050111EC (SCOM)
Description	The NTL Debug Trace 0 Configuration register is used to configure what debug information is sent on the debug trace 0 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of debug trace 0: 0x00 = Debug trace 0 byte 0 inputs. 0x01 = Debug trace 0 byte 1 inputs. 0x02 = Debug trace 0 byte 2 inputs. 0x03 = Debug trace 0 byte 3 inputs. 0x04 = Debug trace 0 byte 4 inputs. 0x05 = Debug trace 0 byte 5 inputs. 0x06 = Debug trace 0 byte 6 inputs. 0x07 = Debug trace 0 byte 7 inputs. 0x08 = Debug trace 0 byte 8 inputs. 0x09 = Debug trace 0 byte 9 inputs. 0x0A = Debug trace 0 byte 10 inputs. 0x0B = RX debug group 0. 0x0C = RX debug group 1. 0x0D = RX debug group 2. 0x0E = RX debug group 3. 0x0F = RX debug group 4. 0x10 = RX debug group 5. 0x11 = RX debug group 6. 0x12 = RX debug group 7. 0x13 = RX debug group 8. 0x14 = TX debug group 0. 0x15 = TX debug group 1. 0x16 = TX debug group 2. 0x17 = TX debug group 3. 0x18 = TX debug group 4. 0x19 = TX debug group 5. 0x1A = TX debug group 6. 0x1B = REGS debug group 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of debug trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of debug trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of debug trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of debug trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of debug trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of debug trace 0.

Bits	SCOM	Field Mnemonic: Description
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of debug trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of debug trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of debug trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of debug trace 0.
55:62	RW	DEBUG0_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	**NTL Debug1 Configuration Register**
Mnemonic	NPU.STCK1.NTL1.REGS.DEBUG1_CONFIG
Address	00000000050111ED (SCOM)
Description	The NTL Debug Trace 1 Configuration register is used to configure what debug information is sent on the debug trace 1 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of debug trace 1: 0x00 = Debug trace 1 byte 0 inputs. 0x01 = Debug trace 1 byte 1 inputs. 0x02 = Debug trace 1 byte 2 inputs. 0x03 = Debug trace 1 byte 3 inputs. 0x04 = Debug trace 1 byte 4 inputs. 0x05 = Debug trace 1 byte 5 inputs. 0x06 = Debug trace 1 byte 6 inputs. 0x07 = Debug trace 1 byte 7 inputs. 0x08 = Debug trace 1 byte 8 inputs. 0x09 = Debug trace 1 byte 9 inputs. 0x0A = Debug trace 1 byte 10 inputs. 0x0B = RX debug group 0. 0x0C = RX debug group 1. 0x0D = RX debug group 2. 0x0E = RX debug group 3. 0x0F = RX debug group 4. 0x10 = RX debug group 5. 0x11 = RX debug group 6. 0x12 = RX debug group 7. 0x13 = RX debug group 8. 0x14 = TX debug group 0. 0x15 = TX debug group 1. 0x16 = TX debug group 2. 0x17 = TX debug group 3. 0x18 = TX debug group 4. 0x19 = TX debug group 5. 0x1A = TX debug group 6. 0x1B = REGS debug group 0.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of debug trace 1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of debug trace 1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of debug trace 1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of debug trace 1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of debug trace 1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of debug trace 1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of debug trace 1.

Bits	SCOM	Field Mnemonic: Description
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of debug trace 1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of debug trace 1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of debug trace 1.
55:62	RW	DEBUG1_CONFIG_RESERVED1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for debug trace latches.

Register Name	**NTL Performance Configuration Register**
Mnemonic	NPU.STCK1.NTL1.REGS.PERF_CONFIG
Address	00000000050111EE (SCOM)
Description	The NTL Performance Configuration register is used to configure what information is counted by the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: PMULet enable (clocks enable).
1	RW	PERF_CONFIG_RESETMODE: 0 = Reset on read. 1 = Reset on write.
2	RW	PERF_CONFIG_FREEZEMODE: 0 = Free run mode. 1 =Freeze on any maximum.
3	RW	PERF_CONFIG_DISABLE_PMISC: 0 = Enable PMISC control of counters. 1 = Disable PMISC control of counters.
4	RW	PERF_CONFIG_PMISC_MODE: 0 = Global PMU PMISC no reset. 1 = Global PMU PMISC reset on enable.
5:7	RW	PERF_CONFIG_CASCADE: PMULet cascade configuration.
8:9	RW	PERF_CONFIG_PRESCALE_C0: Pre-scale configuration for counter 0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: Pre-scale configuration for counter 1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: Pre-scale configuration for counter 2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: Pre-scale configuration for counter 3.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select: 0x00 = Disable. 0x01 = Cycles. 0x02 = Latency events. 0x03 = Latency cycles. 0x04 = Latency aborts. 0x20 = REGS - NDL PRI request. 0x21 = REGS - NDL PRI write request. 0x22 = REGS - NDL PRI read request. 0x23 = REGS - PHY PRI request. 0x24 = REGS - PHY PRI write request. 0x25 = REGS - PHY PRI read request. 0x40 = TX - Any flit sent. 0x41 = TX - Header flit sent. 0x42 = TX - AE flit sent.

Bits	SCOM	Field Mnemonic: Description
		0x43 = TX - BE flit sent. 0x44 = TX - Data flit sent. 0x45 = TX - Flow control packet. 0x46 = TX - Write.NC. 0x47 = TX - Write.NC 128B. 0x48 = TX - Write.NC 32B - 96B. 0x49 = TX - Write.NC 1B - 16B. 0x4A = TX - Write.NC with BE flit. 0x4B = TX - Read. 0x4C = TX - Upgrade. 0x4D = TX - Atomic. 0x4E = TX - Downgrade. 0x4F = TX - ATSD. 0x50 = TX - Request response, no data. 0x51 = TX - Request response with data. 0x52 = TX - Probe response, no data. 0x53 = TX - Probe response with data. 0x54 = TX - ATR response. 0x55 = TX - TransDone response, no data. 0x56 = TX - TransDone response with data. 0x57 = TX - TransDone response with data 128B. 0x58 = TX - TransDone response with data 32B - 96B. 0x59 = TX - TransDone response with data 1B - 16B. 0x5A = TX - TransDone response with data with BE flit. 0x5B = TX - Not enough CREQ header credits. 0x5C = TX - Not enough DGD header credits. 0x5D = TX - Not enough ATSD header credits. 0x5E = TX - Not enough RSP header credits. 0x5F = TX - Not enough CREQ data credits. 0x60 = TX - Not enough RSP data credits. 0x61 = TX - Not enough replay buffer credits. 0x62 = TX - Not enough asynchronous buffer credits. 0x80 = RX - CREQ header array full. 0x81 = RX - PRB header array full. 0x82 = RX - ATR header array full. 0x83 = RX - RSP header array full. 0x84 = RX - CREQ data array full. 0x85 = RX - RSP data array full. 0x86 = RX - Any flit received. 0x87 = RX - Header flit received. 0x88 = RX - AE flit received. 0x89 = RX - BE flit received. 0x8A = RX - Data flit received. 0x8B = RX - NOP flow control flit received. 0x8C = RX - Write.NC (UT = 0). 0x8D = RX - Write.NC (UT = 1). 0x8E = RX - Write.NC (UT = 0) 128B. 0x8F = RX - Write.NC (UT = 1) 128B. 0x90 = RX - Write.NC (UT = 0) 256B. 0x91 = RX - Write.NC (UT = 1) 256B. 0x92 = RX - Write.NC (UT = 0) 32B - 96B. 0x93 = RX - Write.NC (UT = 1) 32B - 96B. 0x94 = RX - Write.NC (UT = 0) 1B - 16B. 0x95 = RX - Write.NC (UT = 1) 1B - 16B. 0x96 = RX - Write.NC (UT = 0) with BE flit. 0x97 = RX - Write.NC (UT = 1) with BE flit. 0x98 = RX - Write.NC (UT = 0) to MMIO space. 0x99 = RX - Write.NC (UT = 0) to MMIO space and split into multiple requests. 0x9A = RX - Write.NC (UT = 1) and split into multiple requests. 0x9B = RX - Read.NC (UT = 0).

Bits	SCOM	Field Mnemonic: Description
		0x9C = RX - Read.NC (UT = 1). 0x9D = RX - Read.NC (UT = 0) 128B. 0x9E = RX - Read.NC (UT = 1) 128B. 0x9F = RX - Read.NC (UT = 0) 256B. 0xA0 = RX - Read.NC (UT = 1) 256B. 0xA1 = RX - Read.NC (UT = 0) 32B - 96B. 0xA2 = RX - Read.NC (UT = 1) 32B - 96B. 0xA3 = RX - Read.NC (UT = 0) 1B - 16B. 0xA4 = RX - Read.NC (UT =1) 1B - 16B. 0xA5 = RX - Flush. 0xA6 = RX - RMW. 0xA7 = RX - Atomic.NR. 0xA8 = RX - Atomic.RR. 0xA9 = RX - Probe.I.MO. 0xAA = RX - Probe.I.N. 0xAB = RX - Probe.X.MO. 0xAC = RX - ATR. 0xAD = RX - ReqRsp.ND. 0xAE = RX - ReqRsp.D. 0xAF = RX - DGDRsp. 0xB0 = RX - ATSDRsp. 0xB1 = RX - TransDone.ND. 0xB2 = RX - TransDone.D. 0xB3 = RX - TransDone.D with BE flit. 0xB4 = RX - CREQ non-flush waiting for CQ credit. 0xB5 = RX - CREQ flush waiting for CQ credit. 0xB6 = RX - CREQ waiting for global credit. 0xB7 = RX - CREQ 256B Op waiting for 256B Ops CAM entry. 0xB8 = RX - PRB waiting for CQ credit. 0xB9 = RX - PRB waiting for global credit. 0xBA = RX - ATR waiting for CQ credit. 0xBB = RX - ATR waiting for global credit.
24:31	RW	PERF_CONFIG_EVENT1: Event 1 select (see Event 0 select for encodes).
32:39	RW	PERF_CONFIG_EVENT2: Event 2 select (see Event 0 select for encodes).
40:47	RW	PERF_CONFIG_EVENT3: Event 3 select (see Event 0 select for encodes).
48:50	RW	PERF_CONFIG_LATENCY: Latency select: 0 = Disable. 1 = Read.NC to response. 2 = Write.RR to response. 3 = Atomic.RR to response. 4 = RMW to response. 5 = Flush to response. 6 = Probe to response. 7 = ATR to response.
51:63	RW	PERF_CONFIG_RESERVED: Reserved.

Register Name	NTL Performance Count Register
Mnemonic	NPU.STCK1.NTL1.REGS.PERF_COUNT
Address	00000000050111EF (SCOM)
Description	The NTL Performance Count register holds the performance counts from the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	IDIAL_PERF_COUNT0: Performance counter 0.

Bits	SCOM	Field Mnemonic: Description
16:31	RWX_WCLRREG	IDIAL_PERF_COUNT1: Performance counter 1.
32:47	RWX_WCLRREG	IDIAL_PERF_COUNT2: Performance counter 2.
48:63	RWX_WCLRREG	IDIAL_PERF_COUNT3: Performance counter 3.

Register Name	NTL CREQ Header Array Pointer Register
Mnemonic	NPU.STCK1.NTL1.REGS.CREQ_HA_PTR
Address	00000000050111F0 (SCOM)
Description	The NTL CREQ Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding CREQ header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	CREQ_HA_PTR_RESERVED1: Reserved.
5:11	RW	CREQ_HA_PTR_START: Starting header array location for CREQ headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	CREQ_HA_PTR_RESERVED2: Reserved.
17:23	RW	CREQ_HA_PTR_END: Ending header array location for CREQ headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL PRB Header Array Pointer Register
Mnemonic	NPU.STCK1.NTL1.REGS.PRB_HA_PTR
Address	00000000050111F1 (SCOM)
Description	The NTL PRB Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding PRB header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	PRB_HA_PTR_RESERVED1: Reserved.
5:11	RW	PRB_HA_PTR_START: Starting header array location for PRB headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	PRB_HA_PTR_RESERVED2: Reserved.
17:23	RW	PRB_HA_PTR_END: Ending header array location for PRB headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL ATR Header Array Pointer Register
Mnemonic	NPU.STCK1.NTL1.REGS.ATR_HA_PTR
Address	00000000050111F2 (SCOM)
Description	The NTL ATR Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding ATR header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	ATR_HA_PTR_RESERVED1: Reserved.
5:11	RW	ATR_HA_PTR_START: Starting header array location for ATR headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	ATR_HA_PTR_RESERVED2: Reserved.
17:23	RW	ATR_HA_PTR_END: Ending header array location for ATR headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Header Array Pointer Register
Mnemonic	NPU.STCK1.NTL1.REGS.RSP_HA_PTR
Address	00000000050111F3 (SCOM)
Description	The NTL RSP Header Array Pointer register is used to change the start and/or end entry in the NTL header array for holding RSP header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	RSP_HA_PTR_RESERVED1: Reserved.
5:11	RW	RSP_HA_PTR_START: Starting header array location for RSP headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	RSP_HA_PTR_RESERVED2: Reserved.
17:23	RW	RSP_HA_PTR_END: Ending header array location for RSP headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL CREQ Data Array Pointer Register
Mnemonic	NPU.STCK1.NTL1.REGS.CREQ_DA_PTR
Address	00000000050111F4 (SCOM)
Description	The NTL CREQ Data Array Pointer register is used to change the start and/or end entry in the NTL data array for holding CREQ data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	CREQ_DA_PTR_RESERVED1: Reserved.
3:11	RW	CREQ_DA_PTR_START: Starting data array location for CREQ data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	CREQ_DA_PTR_RESERVED2: Reserved.
15:23	RW	CREQ_DA_PTR_END: Ending data array location for CREQ data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Data Array Pointer Register
Mnemonic	NPU.STCK1.NTL1.REGS.RSP_DA_PTR
Address	00000000050111F5 (SCOM)
Description	The NTL RSP Data Array Pointer register is used to change the start and/or end entry in the NTL data array for holding RSP data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	RSP_DA_PTR_RESERVED1: Reserved.
3:11	RW	RSP_DA_PTR_START: Starting data array location for RSP data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	RSP_DA_PTR_RESERVED2: Reserved.
15:23	RW	RSP_DA_PTR_END: Ending data array location for RSP data flits received from the GPU. The data array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b000000000000000000000000000000000000000000000000

Register Name	NTL Private Register Interface (PRI) Configuration Register
Mnemonic	NPU.STCK1.NTL1.REGS.PRI_CONFIG
Address	00000000050111F6 (SCOM)
Description	The NTL Private Register Interface (PRI) Configuration register is used to set up the PRI settings for this NTL. This register must be configured before any PRI requests are attempted to NDL or PHY registers.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PRI_CONFIG_NDL: NDL indication sent in the PRI read/write access: 00 = NDL 0. 01 = NDL 1. 10 = NDL 2. 11 = Disable (this disables the NTL from decoding the NDL register space).
2:3	RW	PRI_CONFIG_PHY: Indicates if this NTL should decode a PHY register space: 00 = Decode PHY 0 register space (only one NTL that is connected to PHY 0 must be set to this value). 01 = Decode PHY 1 register space (only one NTL that is connected to PHY 1 must be set to this value). 1X = Do not decode any PHY register space.
4:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	NTL Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK1.NTL1.REGS.CONFIG1
Address	00000000050111F8 (SCOM)
Description	The NTL Miscellaneous Configuration 1 register is used to control NVLink packet formatting by the POWER9 processor. It also controls resetting of the POWER9 NTL.

Bits	SCOM	Field Mnemonic: Description
0	RW	COMPRESSED_RSP_ENA: When set to 0b1, the NTL attempts to compress responses that it sends to the GPU whenever possible.
1:3	RW	CONFIG1_RESERVED1: Reserved.

Bits	SCOM	Field Mnemonic: Description
4	RW	CREQ_AE_ALWAYS: When set to 0b1, the NTL always sends an AE flit when it sends a CREQ packet to the GPU.
5	RW	DGD_AE_ALWAYS: When set to 0b1, the NTL always sends an AE flit when it sends a downgrade packet to the GPU.
6	RW	RSP_AE_ALWAYS: When set to 0b1, the NTL always sends an AE flit when it sends a response packet to the GPU.
7	RW	CONFIG1_RESERVED2: Reserved.
8:9	RW	NTL_RESET: This field indicates the NTL reset mode: 00 = Reset disabled. 11 = Reset (fence) both NTL and the processor bus for this brick. 10 = Reset (fence) only the processor bus for this brick, the NTL is operational. 01 = Reserved. **Note:** The only legal sequence is 00 →11 →10 →00. This field should not be changed unless bits 0:1 in the CQ Fence Status register equals the value in this field.
10:63	RW	CONFIG1_RESERVED3: Reserved.

Register Name	NTL Scratch 1 Register
Mnemonic	NPU.STCK1.NTL1.REGS.SCRATCH1
Address	00000000050111FA (SCOM)
Description	The NTL Scratch 1 register is provided in case a new control function is required in the future. This register has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH1: Scratch register.

Register Name	NTL Low Power Register
Mnemonic	NPU.STCK1.NTL1.REGS.LOW_PWR
Address	00000000050111FC (SCOM)
Description	The NTL Low Power Configuration register is used to enable the NPU to request that the NVLink interconnect be placed into low-power mode. The register also defines the conditions under which the NPU turns its low-power request on or off.

Bits	SCOM	Field Mnemonic: Description
0	RW	LP_MODE_ENABLE: When set to 0b1, this NTL is allowed to activate the low-power requested signal to NDL when the low-power count is greater than or equal to the low-power count threshold.
1	RW	LP_ONLY_MODE: When set to 0b1, this NTL activates the low-power requested signal to NDL continuously. This can be used for lab stress or debug.
2:7	RW	LP_TIMER_TICK_CONFIG: Rate for the low-power timer tick (2^n cycles).
8:19	RW	LP_MIN_CRED_THRESH: Whenever the NDL replay buffer credits is less than this threshold, the low-power requested signal to NDL is deactivated. This value must be greater than 0 and less than the maximum credit threshold.
20:31	RW	LP_MAX_CRED_THRESH: Whenever the NDL replay buffer credits is greater than or equal to this threshold and the low-power timer tick is active, then the low-power count is incremented by 1. This value must be greater than the minimum credit threshold.

Bits	SCOM	Field Mnemonic: Description
32:43	RW	LP_CNT_THRESH: Whenever the low-power count is greater than or equal to this threshold, this NTL activates the low-power requested signal to NDL until the NDL replay buffer credits is less than the low-power minimum credit threshold. This value must be greater than 0.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.CONFIG0
Address	0000000005011200 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0 = Use Read.RWC for DCLAIM/DCBZ to GPU memory. 1 = Use Upgrade.DN for DCLAIM/DCBZ to GPU memory.
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0 = Use Read.RWC for DCBF/DCBFC to GPU memory. 1 = Use Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0 = Use DMA for Write.NC to processor memory. 1 = Use Read-Push for Write.NC to processor memory.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable Vg less than system. 1 = Force all Vg to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc / Skip G on rty_inc. 1 = Allow G on rty_inc / Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending dma. 1 = Change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = Change to _dma.

Bits	SCOM	Field Mnemonic: Description
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp. 0 = 100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7 = 1.5% chance to increase priority.
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD, future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD, future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD, future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD, future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD, future option bit.
22	RW	CONFIG_RESERVED4: Reserved.
23	RW	CONFIG_MACH_CORRENAB: 0 = Disable state machine array ECC correction. 1 = Enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0 = Disable state machine array ECC error inject bit 1. 1 = Enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0 = Disable state machine array ECC error inject bit 2. 1 = Enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0 = Disable ReqRspOut array ECC correction. 1 = Enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0 = Disable PB-Rsp-In array ECC correction. 1 = Enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 1 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.

Bits	SCOM	Field Mnemonic: Description
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0 = Disable NPU processor bus RCMD, PRESP, and CRESP interfaces. 1 = Enable NPU processor bus RCMD, PRESP, and CRESP interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.
40	RW	CONFIG_ENABLE_SNARF_CPM: 0 = Disable Probe.I.MO snarfing a cp_m. 1 = Enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = Preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = Preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = Preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = Preallocate two state machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = Preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode report local masters as near. 1 = In basic mode report local masters as near.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOs greater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU to PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.

Bits	SCOM	Field Mnemonic: Description
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.CONFIG1
Address	0000000005011201 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slice times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non-REQIN events going down the arbiter pipe. After n+1 REQIN events go through the arbiter while a non-CRR event is waiting, REQIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll: 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data: 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	**Power Bus Epsilon Configuration Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.EPSILON_CONFIG
Address	0000000005011202 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/Vg scope CP write.

Bits	SCOM	Field Mnemonic: Description
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope reads.

Register Name	**Timer Configuration Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.XTIMER_CONFIG
Address	0000000005011203 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward progress timer (2^n cycles).
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). **Note:** This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for SM inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for SM inhibit timer tick1 (default 63 = off). **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.GPU_BAR
Address	0000000005011204 (SCOM)
Description	Memory BARs. BAR register defining the GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0 = Disable BAR for brick 0. 0 = Enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: The base address (1G address) of the BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of base address match for the BAR for brick 0: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. Note: It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.

Bits	SCOM	Field Mnemonic: Description
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: The base address (1G address) of the BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of the base address match for the BAR for brick 1: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	**PHY0/PHY1/NPU MMIO BAR Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.PHY_BAR
Address	0000000005011206 (SCOM)
Description	BAR register defining the PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2M range mapped to PHY 0 registers. Stack 1 PHY_BAR defines a 2M range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16M range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0 = Disable PHY_BAR. 1 = Enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2M aligned address of this PHY_BAR.

Bits	SCOM	Field Mnemonic: Description
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2M aligned address of this PHY_BAR's 2M range. **Note:** In stack two, the low three address bits are reserved (16M range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.GENID_BAR
Address	0000000005011207 (SCOM)
Description	ID Registers MMIO BAR. BAR register defining the Generation ID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0 = Disable this BAR. 1 = Enable this BAR.
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of the 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of the128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128K aligned address of this BAR's 128K range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Low Water Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.LOW_WATER
Address	0000000005011208 (SCOM)
Description	State machine allocation for low water marks. Each low water mark should be greater than or equal to 1 and the sum of the low water marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.

Bits	SCOM	Field Mnemonic: Description
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be >= 8 and <= 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. Can only be changed from 0 to 1 and must stay at 1 once it is set.
52:63	RO	Constant = 0b000000000000

Register Name	**High Water Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.HIGH_WATER
Address	0000000005011209 (SCOM)
Description	State machine allocation for high water marks. Each high water mark should be greater than or equal to the corresponding config_low_water and config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Relaxed Configuration 0 Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.CONFIG_RELAXED0
Address	000000005011120A (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0 = Disable relaxed source 0 for write operations. 1 = Enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0 = Disable relaxed source 0 for read operations. 1 = Enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.

Bits	SCOM	Field Mnemonic: Description
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: Relaxed source 0 tag mask value: 0 = Bit is masked off, corresponding match bit must be zero. 1 = Bit must equal corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0 = Disable relaxed source 1 for write operations. 1 = Enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0 = Disable relaxed source 1 for read operations. 1 = Enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CONFIG_RELAXED1
Address	000000000501120B (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0 = Disable relaxed source 2 for write operations. 1 = Enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0 = Disable relaxed source 2 for read operations. 1 = Enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 2 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CONFIG_RELAXED2
Address	000000000501120C (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.

Bits	SCOM	Field Mnemonic: Description
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F=0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0 = Disable relaxed source 3 for write operations. 1 = Enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0 = Disable relaxed source 3 for read operations. 1 = Enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 3 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.NDT0_BAR
Address	000000000501120D (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.

Bits	SCOM	Field Mnemonic: Description
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**NTL1/NDL1 MMIO BAR Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.NDT1_BAR
Address	000000000501120E (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128K aligned address of BAR for brick 1's 128K range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**Performance Configuration Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.PERF_CONFIG
Address	000000000501120F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.INHIBIT_CONFIG
Address	0000000005011210 (SCOM)
Description	This register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0...11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre-frequency 0: 0 = Inhibit timer tick0. 1 = Inverted inhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0...12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = Inhibit timer tick1. 1 = Inverted inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_MESSAGE0
Address	0000000005011211 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_MESSAGE1
Address	0000000005011212 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_MESSAGE2
Address	0000000005011213 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_MESSAGE3
Address	0000000005011214 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_MESSAGE4
Address	0000000005011215 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.SM_STATUS
Address	0000000005011216 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: Set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: Set to 1 when brick 0 probe allocation is at its idle level.
2	ROX	SM_STATUS_CREQ1: 1Set to when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: Set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: Set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: Set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: Set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: Set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X= Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: Set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: Set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: 1Set to when the outbound Rn/Vg scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: Set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: Set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: Set to 1 when the outbound brick 1 CREQ request queue is empty.
30	ROX	SM_STATUS_N1DGD: Set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: Set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: Set to 1 when o the utbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: Set to 1 when the outbound processor bus data-response/merge-operation queue is empty.
34	ROX	SM_STATUS_N0RSP: Set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: Set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: Set to 1 when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: Set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: Set to 1 when the free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_FIRST0
Address	0000000005011217 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.

Bits	SCOM	Field Mnemonic: Description
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.

Bits	SCOM	Field Mnemonic: Description
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 1 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_FIRST1
Address	0000000005011218 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting for data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_FIRST2
Address	0000000005011219 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate,' but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.

Bits	SCOM	Field Mnemonic: Description
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad nex step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).

Bits	SCOM	Field Mnemonic: Description
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_MASK0
Address	000000000501121A (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT =1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).

Bits	SCOM	Field Mnemonic: Description
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_MASK1
Address	000000000501121B (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting for data time out.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: UE ECC error detected from state machine array.
21	RW	IDIAL_SM_MASK_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: Parity error detected on RCMD TTAG field.
25	RW	IDIAL_SM_MASK_PBP_1: Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: Parity error detected on CRESP TTAG.
27	RW	IDIAL_SM_MASK_PBP_3: Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).

Bits	SCOM	Field Mnemonic: Description
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: RCMD TTAG received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: RCMD TTAG received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: CRESP TTAG received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: CRESP TTAG received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 2 Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_MASK2
Address	000000000501121C (SCOM)
Description	c_err_rpt mask register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.

Bits	SCOM	Field Mnemonic: Description
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.

Bits	SCOM	Field Mnemonic: Description
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown state.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_HOLD0
Address	000000000501121D (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.

Bits	SCOM	Field Mnemonic: Description
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).

Bits	SCOM	Field Mnemonic: Description
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU memory received.

Bits	SCOM	Field Mnemonic: Description
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_HOLD1
Address	000000000501121E (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD pre-snoop table look-up missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD final-snoop table look-up missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD pre-snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).

Bits	SCOM	Field Mnemonic: Description
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting for data time out.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: UE ECC error detected from state machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: Parity error detected on RCMD TTAG field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: Parity error detected on CRESP TTAG.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: Error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: Error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: Error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: Not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data, but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or TAG) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: RCMD TTAG received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: RCMD TTAG received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: CRESP TTAG received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: CRESP TTAG received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Hold 2 Register**
Mnemonic	NPU.STCK2.CS.SM0.MISC.CERR_HOLD2
Address	000000000501121F (SCOM)
Description	c_err_rpt hold latches read-write-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD event received, but state machine is not idle.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket hit event, but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table look-up missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: Start Epsilon, but Epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate', but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: Bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: Snoop CRESP received, but not in M_WT_CRESP state.
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp pocket hit event, but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table look-up missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state did not match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: Start Epsilon, but Epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: Bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: Bad next step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: Bad next step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: Bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: Master CRESP received, but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT translate response event, but not in wait translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT translate response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA done event, but not in wait SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: Bad next step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink master command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event, but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown NV master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RSPLN event, but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon in progress, but Epsilon counter clock is not the Epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon', but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: Bad next step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired, but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND, but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table look-up missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from DSA table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown state.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND, but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown NV master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: Impossible command/CRESP.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: Impossible command/CRESP.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: Impossible command/CRESP.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected error state (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry, but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry, but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout, but not in waiting for NV response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.CONFIG0
Address	0000000005011220 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_RESERVED1: Reserved.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 01 = Use Read.RWC for DCLAIM/DCBZ to GPU memory. 1 = Use Upgrade.DN for DCLAIM/DCBZ to GPU memory.
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0 = Use Read.RWC for DCBF/DCBFC to GPU memory. 1 = Use Upgrade.DN for DCBF/DCBFC to GPU memory.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0 = Use DMA for Write.NC to processor memory. 1 = Use Read-Push for Write.NC to processor memory.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0 = Large system mode. 1 = Small system mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0 = Enable Nn and Rn scopes. 1 = Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0 = Enable Vg less than system. 1 = Force all Vg to system.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0 = Enable G scope. 1 = Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0 = Enable Ln scope. 1 = Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0 = Allow G on rty_inc. 1 = Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0 = Increase scope on rty_inc to dma_w. 1 = Use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type CRESP: 0 = Keep sending dma. 1 = Change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type CRESP: 0 = Keep sending inj. 1 = Change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp. 0 = 100% chance to increase priority. 1 = 50% chance to increase priority. 2 = 25% chance to increase priority. 3 = 12.5% chance to increase priority. 4 = 6% chance to increase priority. 5 = 3% chance to increase priority. 6, 7 = 1.5% chance to increase priority.

Bits	SCOM	Field Mnemonic: Description
16	RW	CONFIG1_RESERVED2: Reserved.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD, future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD, future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD, future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD, future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD, future option bit.
22	RW	CONFIG_RESERVED4: Reserved.
23	RW	CONFIG_MACH_CORRENAB: 0 = Disable state machine array ECC correction. 1 = Enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0 = Disable state machine array ECC error inject bit 1. 1 = DEnable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0 = Disable state machine array ECC error inject bit 2. 1 = Enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0 = Disable ReqRspOut array ECC correction. 1 = Enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0 = Disable ReqRspOut array ECC error inject bit 1. 1 = Enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0 = Disable PB-Rsp-In array ECC correction. 1 = Enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0 = Disable PB-Rsp-Ine array ECC error inject bit 1. 1 = Enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = Partial respond to DCLAIM to GPU memory with lpc_ack. 1 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lost_claim. 2 = Partial respond to DCLAIM to GPU memory with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0 = Non-relaxed dma_w use Read.RWC to acquire pocket cache state/data. 1 = Non-relaxed dma_w use Upgrade.DN to acquire pocket cache state/data.
35	RW	CONFIG_EVAPORATE_BY_LCO: 0 = Just free the state machine without LCO. 1 = Evaporate pocket cache entries by LCO.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0 = Master retry back-off group-pump track only this stack's retry responses. 1 = Master retry back-off group-pump track all this chip's retry responses.

Bits	SCOM	Field Mnemonic: Description
37	RW	CONFIG_MRBSP_TRACK_ALL: 0 = Master retry back-off system-pump track only this stack's retry responses. 1 = Master retry back-off system-pump track all this chip's retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0 = Disable NPU processor bus RCMD, PRESP, and CRESP interfaces. 1 = Enable NPU processor bus RCMD, PRESP, and CRESP interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0 = Non-brazos 4-group; 2-chip mode. 1 = Brazos 2-group; 4-chip mode.
40	RW	CONFIG_ENABLE_SNARF_CPM: 0 = Disable Probe.I.MO snarfing a cp_m. 1 = Enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = Preallocate two state machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = Preallocate two state machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = Preallocate two state machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = Preallocate two state machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = Preallocate two state machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0 = Enable sending cl,pr_dma_inj. 1 = Disable sending cl,pr_dma_inj. **Note:** To disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj config_ma_dsa_opt_rp_mode
47	RW	CONFIG_DCACHE_MODE: 0 = Drive data bus DCACHE field in basic mode. 1 = Drive data bus DCACHE field in CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0 = In basic mode, report local masters as near. 1 = In basic mode, report local masters as local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0 = Enable RSI PB data in fastpath. 1 = Disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0 = Valid pocket cache entries, do not block probes. 1 = Probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0 = Normal operation. 1 = Run in special lab bring-up GPUless POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0 = Allow GPU to PB MMIOs greater than 32 bytes. 1 = Flag error and brick fence on MMIOs greater than 32 bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0 = Allow GPU to PB atomics to MMIO space. 1 = Flag error and brick fence on atomics to MMIO space.
54	RW	CONFIG_OPT_SNOOP_CP: 0 = Snoop POWER9 memory cp_* type commands. 1 = Do not snoop cp_* type commands.
55:63	RW	CONFIG0_RESERVED3: Reserved.

Register Name	CQ_SM Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CONFIG1
Address	0000000005011221 (SCOM)
Description	Miscellaneous configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry back-off: 0000 = 0 - 15 base random duration. 0001 = 0 - 31 base random duration. 0011 = 0 - 63 base random duration. 0111 = 0 - 127 base random duration. 1111 = 0 - 255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for the slowdown of NTL CREQ credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for the slowdown of NTL probe credits during chgrate.hang. 'n' = $1/(2^{(n+1)})$ cycles average rate. **Note:** For a single processor bus ramp, the rate is actually eight times faster since there are four RCMD slices times two NTL bricks that get CREQ credits. This field is the rate for one brick receiving credit from one RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-CRESP/non- REQIN events going down the arbiter pipe. After n+1 REQIN events go through the arbiter while a non-CRR event is waiting, REQIN events are blocked to give non-CRR events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: Epsilon count for Ln scope CP write.
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll. 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data. 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_RESERVED: Reserved.

Register Name	Power Bus Epsilon Configuration Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.EPSILON_CONFIG
Address	0000000005011222 (SCOM)
Description	Processor bus Epsilon configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = Decrement Epsilon count at 1:1 nest_gckn. ... 15 = Epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: Epsilon count for Nn/G scope CP write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: Epsilon count for Rn/Vg scope CP write.

Bits	SCOM	Field Mnemonic: Description
28:39	RW	CONFIG_EPSILON_R0_COUNT: Epsilon count for Ln scope reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: Epsilon count for Nn/G scope reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: Epsilon count for Rn/Vg scope reads.

Register Name	**Timer Configuration Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.XTIMER_CONFIG
Address	0000000005011223 (SCOM)
Description	Timer configuration register. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the pocket cache with data entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for pocket cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for pocket cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward-progress timer (2^n cycles).
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). **Note:** This field can/should have different values in each instance.
26:31	RW	CONFIG_INH0_TICK: Rate for SM inhibit timer tick0 (default 63 = off). **Note:** This field can/should have different values in each instance.
32:37	RW	CONFIG_INH1_TICK: Rate for SM inhibit timer tick1 (default 63 = off). **Note:** This field can/should have different values in each instance.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV-Response timer. The timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds, where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV-Response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the pocket cache dataless entries. The pocket cache timer is used to evaporate pocket cache entries which are not claimed. The long timer duration is f(Rate-1) * $2^{(Rate-2)}$ * 5e - 10 seconds. The short timer duration is f(Rate-1) * $2^{(Rate-3)}$ * 5e - 10 seconds. Where f(Rate-1) is: f(0b00) = 7 f(0b01) = 63 f(0b10) = 511 f(0b11) = 4095
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.GPU_BAR
Address	0000000005011224 (SCOM)
Description	BAR register defining the GPU memory addresses serviced by bricks 0 and 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. **Note:** It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: Group field of the base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: The base address (1G address) of the BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_RESERVED: Reserved.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of base address match for the BAR for brick 0: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. **Note:** It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: Group field of the base address of BAR for brick 1.

Bits	SCOM	Field Mnemonic: Description
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: The base address (1G address) of the BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_RESERVED: Reserved.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = Hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = Hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of base address match for the BAR for brick 1: 0 = 1G 1 = 2G 2 = 4G ... 9 = 512G 10 = 1T 11 = 2T 12 = 4T >12 = Reserved.
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in address/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	**PHY0/PHY1/NPU MMIO BAR Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.PHY_BAR
Address	0000000005011226 (SCOM)
Description	BAR register defining PHY0/PHY1/NPU MMIO range. Stack 0 PHY_BAR defines a 2M range mapped to PHY 0 registers. Stack 1 PHY_BAR defines a 2M range mapped to PHY 1 registers. Stack 2 PHY_BAR defines a 16M range mapped to all NPU registers. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0 = Disable PHY_BAR. 1 = Enable PHY_BAR.
1:2	RW	PHY_RESERVED1: Reserved.
3:6	RW	CONFIG_PHY_BAR_GROUP: Group field of the 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: Chip field of the 2M aligned address of this PHY_BAR.

Bits	SCOM	Field Mnemonic: Description
10:30	RW	CONFIG_PHY_BAR_ADDR: The 2M aligned address of this PHY_BAR;s 2M range. **Note:** In stack two, the low three address bits are reserved (16M range).
31	RW	PHY_RESERVED2: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.GENID_BAR
Address	0000000005011227 (SCOM)
Description	BAR register defining the Generation ID register for this stack/ramp. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0 = Disable this BAR. 1 = Enable this BAR.
1:2	RW	GENID_RESERVED1: Reserved.
3:6	RW	CONFIG_GENID_BAR_GROUP: Group field of the 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: Chip field of the 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: The 128K aligned address of this BAR's 128K range.
35	RW	GENID_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Low Water Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.LOW_WATER
Address	0000000005011228 (SCOM)
Description	State machine allocation for low water marks. Each low water mark should be greater than or equal to 1 and the sum of the low water marks must be less than config_max_machines. Low water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once it is set to 1. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low water mark for processor bus CP (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low water mark for NVLink brick 0 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low water mark for NVLink brick 0 probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low water mark for NVLink brick 1 non-probe requests. Can only be changed while config_enable_machine_alloc = 0.

Bits	SCOM	Field Mnemonic: Description
36:41	RW	CONFIG_LOW_WATER_PRB1: Low water mark for NVLink brick 1 probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state machines to be used. Must be >= 8 and <= 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_RESERVED1: Reserved.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state machine allocation. Can only be changed from 0 to 1 and must stay at 1 once it is set.
52:63	RO	Constant = 0b000000000000

Register Name	**High Water Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.HIGH_WATER
Address	0000000005011229 (SCOM)
Description	State machine allocation for high water marks. Each high water mark should be greater than or equal to the corresponding config_low_water and less than the config_max_machines. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High water mark for processor bus CP (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High water mark for NVLink brick 0 non-probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High water mark for NVLink brick 0 probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High water mark for NVLink brick 1 non-probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High water mark for NVLink brick 1 probe requests.
42:43	RW	HIGH_WATER_RESERVED1: Reserved.
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Relaxed Configuration 0 Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.CONFIG_RELAXED0
Address	000000005011122A (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0 = Disable relaxed source 0 for write operations. 1 = Enable relaxed source 0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0 = Disable relaxed source 0 for read operations. 1 = Enable relaxed source 0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: Relaxed source 0 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.

Bits	SCOM	Field Mnemonic: Description
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: Relaxed source 0 tag mask value: 0 = Bit is masked off, the corresponding match bit must be zero. 1 = Bit must equal corresponding match bit.
38:39	RW	CONFIG_RELAXED_RESERVED0: Reserved.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0 = Disable relaxed source 1 for write operations. 1 = Enable relaxed source 1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0 = Disable relaxed source 1 for read operations. 1 = Enable relaxed source 1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: Relaxed source 1 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CONFIG_RELAXED1
Address	000000000501122B (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: Relaxed source 1 tag mask value.
18:19	RW	CONFIG_RELAXED_RESERVED1: Reserved.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0 = Disable relaxed source 2 for write operations. 1 = Enable relaxed source 2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0 = Disable relaxed source 2 for read operations. 1 = Enable relaxed source 2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: Relaxed source 2 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: Relaxed source 2 tag mask value.
58:59	RW	CONFIG_RELAXED_RESERVED2: Reserved.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CONFIG_RELAXED2
Address	000000000501122C (SCOM)
Description	This register configures relaxed ordering. **Note:** This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.

Bits	SCOM	Field Mnemonic: Description
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F=0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0 = Disable relaxed source 3 for write operations. 1 = Enable relaxed source 3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0 = Disable relaxed source 3 for read operations. 1 = Enable relaxed source 3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: Relaxed source 3 tag match value: When config_brazos_mode = 0, matches TTAG 2:3,6:21. When config_brazos_mode = 1, matches TTAG 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: Relaxed source 3 tag mask value.
62:63	RW	CONFIG_RELAXED_RESERVED3: Reserved.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.NDT0_BAR
Address	000000000501122D (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 0 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0 = Disable BAR for brick 0. 1 = Enable BAR for brick 0.
1:2	RW	NDT0_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT0_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: The 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**NTL1/NDL1 MMIO BAR Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.NDT1_BAR
Address	000000000501122E (SCOM)
Description	BAR register defining the NDL/NTL MMIO range for brick 1 connected to this stack. **Note:** This register should be set to the same value for each brick/stack.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0 = Disable BAR for brick 1. 1 = Enable BAR for brick 1.
1:2	RW	NDT1_RESERVED1: Reserved.
3:6	RW	CONFIG_NDT1_BAR_GROUP: Group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: Chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: The 128K aligned address of BAR for brick 1's 128K range.
35	RW	NDT1_RESERVED2: Reserved.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**Performance Configuration Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.PERF_CONFIG
Address	000000000501122F (SCOM)
Description	Performance event selection register.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_RESERVED2: Reserved.

Bits	SCOM	Field Mnemonic: Description
63	RW	PERF_CONFIG_ACT: Enable clock gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.INHIBIT_CONFIG
Address	0000000005011230 (SCOM)
Description	The register configures inhibits for CQ_SM.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0...11 = $1/2^{(n+1)}$ 12 = $1/2^{14}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre frequency 0: 0 = Inhibit timer tick0. 1 = Inverted inhibit timer tick0. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0 = Disable blocky mode. 1 = Enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0 = Continuous mode. 1 = One shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0...12 = $1/2^{(n+1)}$ 13 = $1/2^{16}$ 14 = $1/2^{18}$ 15 = $1/2^{20}$
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre-frequency 0: 0 = Inhibit timer tick1. 1 = Inverted inhibit timer tick1. 2 = LFSR. 3 = Inverted LFSR (1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0 = Disable blocky mode. 1 = Enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0 = Continuous mode. 1 = One shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_MESSAGE0
Address	0000000005011231 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_MESSAGE1
Address	0000000005011232 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_MESSAGE2
Address	0000000005011233 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_MESSAGE3
Address	0000000005011234 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_MESSAGE4
Address	0000000005011235 (SCOM)
Description	Error message/capture register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.SM_STATUS
Address	0000000005011236 (SCOM)
Description	Status reporting register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: Set to 1 when brick 0 CREQ allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: Set to 1 when brick 0 probe allocation is at its idle level.
2	ROX	SM_STATUS_CREQ1: Set to 1 when brick 1 CREQ allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: Set to 1 when brick 1 probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: Set to 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: Set to 1 when processor bus (non-CP*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: Set to 1 when processor bus (CP*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: Set to 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master retry back-off level for group-pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master retry back-off level for system-pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick 0 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X = Flushing pocket cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick 1 fence sequencing state: 0000 = Idle state, completely unfenced. 0XXX = In transition between fenced and not fenced. 0111 = Fenced state, fence sequencing complete. 100X= Flushing pocket cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: Set to 1 when the outbound Ln scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: Set to 1 when the outbound Nn/G scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: Set to 1 when the outbound Rn/Vg scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: Set to 1 when the outbound brick 0 CREQ request queue is empty.
28	ROX	SM_STATUS_N0DGD: Set to 1 when the outbound brick 0 downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: Set to 1 when the outbound brick 1 CREQ request queue is empty.
30	ROX	SM_STATUS_N1DGD: Set to 1 when the outbound brick 1 downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: Set to 1 when the outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: Set to 1 when the outbound ATS TCE translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: Set to 1 when the outbound processor bus data response/merge operation queue is empty.
34	ROX	SM_STATUS_N0RSP: Set to 1 when the outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: Set to 1 when the outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: Set to 1 when the outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: Set to 1 when the same address collision check queue is empty.
38	ROX	SM_STATUS_FREE: Set to 1 when the free state machine queue is empty.
39	ROX	SM_STATUS_RESERVED1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_FIRST0
Address	0000000005011237 (SCOM)
Description	c_err_rpt first latches read-write-1-clear register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink response.

Bits	SCOM	Field Mnemonic: Description
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPU bar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from state machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU bkill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/length/alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR First 1 Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_FIRST1
Address	0000000005011238 (SCOM)
Description	This c_err_rpt register is read/write. Writing a '1' clears the register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD pre-snoop table lookup missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD final-snoop table lookup missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD Pre-snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD Final-snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).

Bits	SCOM	Field Mnemonic: Description
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: AUE0 UE ECC error detected from the state-machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: AUE1 UE ECC error detected from the Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: AUE2 UE ECC error detected from the processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: PBP0 Parity error detected on the RCMD ttag field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: PBP2 Parity error detected on CRESP ttag.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).

Bits	SCOM	Field Mnemonic: Description
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP -- Error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP -- Error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP -- Error CRESP received for a bkill.
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP -- ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL -- Not all segments or OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA -- Received data but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN -- Received data with data_stat = Poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: Atag contains out-of-range group (HPC or Tag) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: Atag contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: PBC4 RCMD TTag received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: PBC5 RCMD TTag received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: PBC6 CRESP TTag received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: PBC7 CRESP TTag received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_FIRST2
Address	0000000005011239 (SCOM)
Description	2 latches c_err_rpt first latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD Event received but state machine is not IDLE.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket-Hit event but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table lookup missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: start epsilon, but epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: snoop CRESP received but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp-Pocket-Hit event but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table lookup missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state didn't match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: start epsilon, but epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: bad next-step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: bad next-step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: master CRESP received but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT-translate-Response event but not in wait-translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT-translate-Response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA-Done event but not in wait-SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next-step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink Master Command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.

Bits	SCOM	Field Mnemonic: Description
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown nv-master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon-In-Progress, but epsilon counter clock is not the epsilon clock.
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: bad next-step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown Event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table lookup missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from dsa table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown State.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown nv-master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: impossible command/CRESP.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: impossible command/CRESP.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: impossible command/CRESP.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout but not in waiting-NV-response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).

Bits	SCOM	Field Mnemonic: Description
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_MASK0
Address	0000000005011234A (SCOM)
Description	c_err_rpt mask register. Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad cmd/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done Response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad cmd/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).

Bits	SCOM	Field Mnemonic: Description
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPUBar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from State-machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU BKill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU Memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/Length/Alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Mask 1 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_MASK1
Address	000000000501123B (SCOM)
Description	c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD Pre-Snoop table lookup missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD Final-Snoop table lookup missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS-response.
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD Pre-Snoop table impossible cmd.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD Final-Snoop table impossible cmd.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: AUE0 UE ECC error detected from State-machine array.
21	RW	IDIAL_SM_MASK_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: PBP0 Parity error detected on RCMD ttag field.
25	RW	IDIAL_SM_MASK_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: PBP2 Parity error detected on CRESP ttag.
27	RW	IDIAL_SM_MASK_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: error CRESP received for a command.

Bits	SCOM	Field Mnemonic: Description
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = Poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: Atag contains out-of-range group (HPC or Tag) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: Atag contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: PBC4 RCMD TTag received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: PBC5 RCMD TTag received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: PBC6 CRESP TTag received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: PBC7 CRESP TTag received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Mask 2 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_MASK2
Address	000000000501123C (SCOM)
Description	2 latches c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD Event received but state machine is not IDLE.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket-Hit event but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table lookup missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: start epsilon, but epsilon already in progress.

Bits	SCOM	Field Mnemonic: Description
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: snoop CRESP received but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp-Pocket-Hit event but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table lookup missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state didn't match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: start epsilon, but epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: bad next-step for bkill (ack-done).
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: bad next-step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: master CRESP received but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT-translate-Response event but not in wait-translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT-translate-Response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA-Done event but not in wait-SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next-step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink Master Command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown nv-master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon-In-Progress, but epsilon counter clock is not the epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: bad next-step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown Event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table lookup missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from dsa table.

Bits	SCOM	Field Mnemonic: Description
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown State.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown nv-master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: impossible command/cresp.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: impossible command/cresp.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: impossible command/cresp.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry but not in retry-abbks collision state.
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout but not in waiting-NV-response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_HOLD0
Address	000000000501123D (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.

Bits	SCOM	Field Mnemonic: Description
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad cmd/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done Response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad cmd/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).

Bits	SCOM	Field Mnemonic: Description
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPUBar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from state-machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU BKill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU Memory received.

Bits	SCOM	Field Mnemonic: Description
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/Length/Alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_HOLD1
Address	0000000005011 23E (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD Pre-snoop table lookup missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD Final-snoop table lookup missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS-response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD Pre-snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD Final-snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).

Bits	SCOM	Field Mnemonic: Description
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: AUE0 UE ECC error detected from State-machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: PBP0 Parity error detected on RCMD ttag field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: PBP2 Parity error detected on CRESP ttag.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = Poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: Atag contains out-of-range group (HPC or Tag) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: Atag contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: PBC4 RCMD TTag received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: PBC5 RCMD TTag received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: PBC6 CRESP TTag received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: PBC7 CRESP TTag received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK2.CS.SM1.MISC.CERR_HOLD2
Address	000000000501123F (SCOM)
Description	2 latches c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD Event received but state machine is not IDLE.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket-Hit event but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table lookup missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: start epsilon, but epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: snoop CRESP received but not in M_WT_CRESP state.
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp-Pocket-Hit event but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table lookup missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state didn't match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: start epsilon, but epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: bad next-step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: bad next-step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: master CRESP received but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT-translate-Response event but not in wait-translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT-translate-Response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA-Done event but not in wait-SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next-step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink Master Command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown nv-master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon-In-Progress, but epsilon counter clock is not the epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.

Bits	SCOM	Field Mnemonic: Description
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: bad next-step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown Event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table lookup missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from dsa table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown State.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown nv-master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: impossible command/cresp.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: impossible command/cresp.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: impossible command/cresp.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout but not in waiting-NV-response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK2.CS.SM2.MISC.CONFIG0
Address	0000000005011240 (SCOM)
Description	Misc Configuration Register Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0/1 = use Read.RWC/Upgrade.DN for dclaim/dcbz to GPU Mem.
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0/1 = use Read.RWC/Upgrade.DN for dcbf/dcbfc to GPU Mem.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0/1 = use DMA/Read-Push for Write.NC to Proc Mem.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0/1 = large-system-mode/small-system-mode.
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0/1 = Enable Nn and Rn scopes / Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0/1 = Enable Vg less than sys / Force all Vg to sys.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0/1 = Enable G scope / Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0/1 = Enable Ln scope / Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0/1 = Allow G on rty_inc / Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0/1 = increase scope on rty_inc to dma_w / use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type cresp, 0/1 = keep sending dma/change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type cresp, 0/1 = keep sending inj/change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp. 0: 100% chance to increase priority. 1: 50% chance to increase priority. 2: 25% chance to increase priority. 3: 12.5% chance to increase priority. 4: 6% chance to increase priority. 5: 3% chance to increase priority. 6,7: 1.5% chance to increase priority.
16	RW	CONFIG1_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD future option bit.
22	RW	CONFIG_Reserved4: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.

Bits	SCOM	Field Mnemonic: Description
23	RW	CONFIG_MACH_CORRENAB: 0/1 = Disable/enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0/1 = Disable/enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0/1 = Disable/enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0/1 = Disable/enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0/1 = Disable/enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0/1 = Disable/enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0/1 = Disable/enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0/1 = Disable/enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0/1 = Disable/enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = partial-respond to dclaim to GPU Mem with lpc_ack. 1 = partial-respond to dclaim to GPU Mem with lpc_ack+rty_lost_claim. 2 = partial-respond to dclaim to GPU Mem with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0/1 = non-relaxed dma_w use Read.RWC/Upgrade.DN to acquire pocket-cache state/data.
35	RW	CONFIG_EVAPORATE_BY_LCO: 0/1 = just free the state-machine without lco/evaporate pocket-cache entries by lco.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0/1 = master-retry-backoff group-pump track only this stack's/all-this-chips retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0/1 = master-retry-backoff system-pump track only this stack's/all-this-chips retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0/1 = Disable NPU processor bus RCMD, PResp, and CRESP interfaces / enable these interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0/1 = non-brazos 4-group;2-chip mode / brazos 2-group;4-chip mode.
40	RW	CONFIG_ENABLE_SNARF_CPM: 0/1 = Disable/enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = pre-allocate 2 state-machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = pre-allocate 2 state-machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = pre-allocate 2 state-machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = pre-allocate 2 state-machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = pre-allocate 2 state-machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0/1 = Enable sending cl,pr_dma_inj / disable sending cl,pr_dma_inj. Note: to truly disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj. config_ma_dsa_opt_rp_mode.
47	RW	CONFIG_DCACHE_MODE: 0/1 = drive data-bus dcache field in basic mode / CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0/1 = in basic mode, report local masters as near / local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0/1 = Enable rsi PB data-in fastpath/disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0/1 = valid pocket-cache entries do not block probes / probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0/1 = normal operation / run in special lab-bringup GPU-less POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0/1 = Allow GPU->PB MMIOs > 32-bytes / flag-error and brick-fence on MMIOs > 32-bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0/1 = Allow GPU->PB atomics to MMIO space / flag-error and brick-fence on atomics to MMIO space.

Bits	SCOM	Field Mnemonic: Description
54	RW	CONFIG_OPT_SNOOP_CP: 0/1 = Snoop POWER9-Mem cp_* type commands / don't snoop cp_* type commands.
55:63	RW	CONFIG0_Reserved3: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK2.CS.SM2.MISC.CONFIG1
Address	0000000005011241 (SCOM)
Description	Misc Configuration Register Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry backoff. 0000 -> 0-15 base random duration. 0001 -> 0-31 base random duration. 0011 -> 0-63 base random duration. 0111 -> 0-127 base random duration. 1111 -> 0-255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for for the slowdown of NTL CReq credits during chgrate.hang. 'n' -> 1/(2^(n+1)) cycles average rate. Note that for a single processor bus ramp, the rate is actually 8 times faster since there are 4 RCMD slice x 2 NTL Bricks that get CReq credits. This field is the rate for 1 brick receiving credit from 1 RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for for the slowdown of NTL Probe credits during chgrate.hang. 'n' -> 1/(2^(n+1)) cycles average rate. Note that for a single processor bus ramp, the rate is actually 8 times faster since there are 4 RCMD slice x 2 NTL Bricks that get CReq credits. This field is the rate for 1 brick receiving credit from 1 RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-cresp/non-reqin events going down the arb pipe. after N+1 reqin events go through the arbiter while a non-crr event is waiting, reqin events are blocked to give non-crr events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: epsilon count for Ln scope CP-Write.
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll. 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data. 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_Reserved: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.

Register Name	Power Bus Epsilon Configuration Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.EPSILON_CONFIG
Address	0000000005011242 (SCOM)
Description	Pprocessor bus Epsilon Configuration Register Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = decrement epsilon count at 1:1 nest_gckn. ... 15 = epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: epsilon count for Nn/G scope CP-Write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: epsilon count for Rn/Vg scope CP-Write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: epsilon count for Ln scope Reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: epsilon count for Nn/G scope Reads.
52:63	RW	CONFIG_EPSILON_R2_COUNT: epsilon count for Rn/Vg scope Reads.

Register Name	Timer Configuration Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.XTIMER_CONFIG
Address	0000000005011243 (SCOM)
Description	Timer Configuration Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the Pocket-Cache w/ Data entries. The Pocket-Cache timer is used to evaporate pocket-cache entries which are not claimed. The Long timer duration is f(Rate-1)*2^(Rate-2)*5e-10 seconds and. the Short timer duration is f(Rate-1)*2^(Rate-3)*5e-10 seconds where f(Rate-1) is: f(0b00) = 7. f(0b01) = 63. f(0b10) = 511. f(0b11) = 4095.
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for Pocket-Cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for Pocket-Cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward-progress timer (2^n cycles).
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
26:31	RW	CONFIG_INH0_TICK: Rate for SM-Inhibit timer tick0 (default 63 = off). Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
32:37	RW	CONFIG_INH1_TICK: Rate for SM-Inhibit timer tick1 (default 63 = off). Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.

Bits	SCOM	Field Mnemonic: Description
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV-Response timer. The timer duration is f(Rate-1)*2^(Rate-2)*5e-10 seconds. f(0b00) = 7. f(0b01) = 63. f(0b10) = 511. f(0b11) = 4095.
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV-Response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the Pocket-Cache Dataless entries. The Pocket-Cache timer is used to evaporate pocket-cache entries which are not claimed. The Long timer duration is f(Rate-1)*2^(Rate-2)*5e-10 seconds and. the Short timer duration is f(Rate-1)*2^(Rate-3)*5e-10 seconds where f(Rate-1) is: f(0b00) = 7. f(0b01) = 63. f(0b10) = 511. f(0b11) = 4095.
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.GPU_BAR
Address	0000000005011244 (SCOM)
Description	Memory BARs BAR register defining GPU Mem addresses serviced by bricks 0 and 1 connected to this stack. Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0/1 = Disable/enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. Note: It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: group field of the Base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the Base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: Base address (1G address) of BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_Reserved: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of Base Address match for the BAR for brick 0. 0 = 1G. 1 = 2G. 2 = 4G. ... 9 = 512G. 10 = 1T. 11 = 2T. 12 = 4T. >12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in addr/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0/1 = Disable/enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. Note: It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: group field of the Base address of BAR for brick 1.
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the Base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: Base address (1G address) of BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_Reserved: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of Base Address match for the BAR for brick 1. 0 = 1G. 1 = 2G. 2 = 4G. ... 9 = 512G. 10 = 1T. 11 = 2T. 12 = 4T. >12 = Reserved.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in addr/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.PHY_BAR
Address	0000000005011246 (SCOM)
Description	BAR register defining PHY0/PHY1/NPU MMIO range stack 0 phy_bar defines a 2M range mapped to PHY-0 registers stack 1 phy_bar defines a 2M range mapped to PHY-1 registers stack 2 phy_bar defines a 16M range mapped to all NPU registers Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0/1 = Disable/enable PHY_BAR.
1:2	RW	PHY_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
3:6	RW	CONFIG_PHY_BAR_GROUP: group field of 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: chip field of 2M aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: 2M aligned address of this PHY_BARs 2M range. (in stack 2 the low 3 address bits are Reserved -> 16M range).
31	RW	PHY_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.GENID_BAR
Address	0000000005011247 (SCOM)
Description	ID Registers MMIO BAR BAR register defining Generation-ID register for this stack/ramp Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0/1 = Disable/enable this BAR.
1:2	RW	GENID_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
3:6	RW	CONFIG_GENID_BAR_GROUP: group field of 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: chip field of 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: 128K aligned address of this BARs 128K range.
35	RW	GENID_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**Low Water Register**
Mnemonic	NPU.STCK2.CS.SM2.MISC.LOW_WATER
Address	0000000005011248 (SCOM)
Description	Water Marks State-Machine allocation Low-Water Marks Each Low-Water mark should be > = 1 and the sum of the Low-Water marks must be less than config_max_machines Low-Water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once set to 1 Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low-Water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.
6:11	RW	CONFIG_LOW_WATER_PWR0: Low-Water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low-Water mark for processor bus cp (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low-Water mark for NVLink brick-0 non-Probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low-Water mark for NVLink brick-0 Probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low-Water mark for NVLink brick-1 non-Probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low-Water mark for NVLink brick-1 Probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state-machines to be used. Must be > = 8 and < = 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state-machine allocation. Can only be changed 0->1, must stay 1 once set.

Bits	SCOM	Field Mnemonic: Description
52:63	RO	Constant = 0b000000000000

Register Name	High Water Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.HIGH_WATER
Address	0000000005011249 (SCOM)
Description	Water Marks State-Machine allocation High-Water Marks Each High-Water mark should be > = corresponding config_low_water and < config_max_machines Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High-Water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High-Water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High-Water mark for processor bus cp (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High-Water mark for NVLink brick-0 non-Probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High-Water mark for NVLink brick-0 Probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High-Water mark for NVLink brick-1 non-Probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High-Water mark for NVLink brick-1 Probe requests.
42:43	RW	HIGH_WATER_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
44:63	RO	Constant = 0b00000000000000000000

Register Name	Relaxed Configuration 0 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CONFIG_RELAXED0
Address	000000000501124A (SCOM)
Description	Ordering Config0 Configure relaxed-ordering Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0/1 = Disable/enable relaxed source0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0/1 = Disable/enable relaxed source0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: relaxed source0 tag match value. when config_brazos_mode = 0, matches TTag 2:3,6:21. when config_brazos_mode = 1, matches TTag 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: relaxed source0 tag mask value. 0 = bit is masked off, corresponding match bit must be zero. 1 = bit must equal corresponding match bit.
38:39	RW	CONFIG_RELAXED_Reserved0: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0/1 = Disable/enable relaxed source1 for write operations.

Bits	SCOM	Field Mnemonic: Description
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0/1 = Disable/enable relaxed source1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: relaxed source1 tag match value. when config_brazos_mode = 0, matches TTag 2:3,6:21. when config_brazos_mode = 1, matches TTag 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CONFIG_RELAXED1
Address	000000000501124B (SCOM)
Description	Ordering Config1 Configure relaxed-ordering Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: relaxed source1 tag mask value.
18:19	RW	CONFIG_RELAXED_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0/1 = Disable/enable relaxed source2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0/1 = Disable/enable relaxed source2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: relaxed source2 tag match value. when config_brazos_mode = 0, matches TTag 2:3,6:21. when config_brazos_mode = 1, matches TTag 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: relaxed source0 tag mask value.
58:59	RW	CONFIG_RELAXED_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CONFIG_RELAXED2
Address	000000000501124C (SCOM)
Description	Ordering Config2 Configure relaxed-ordering Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.

Bits	SCOM	Field Mnemonic: Description
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F = 0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0/1 = Disable/enable relaxed source3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0/1 = Disable/enable relaxed source3 for read operations.
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: relaxed source3 tag match value. when config_brazos_mode = 0, matches TTag 2:3,6:21. when config_brazos_mode = 1, matches TTag 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: relaxed source0 tag mask value.
62:63	RW	CONFIG_RELAXED_Reserved3: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.

Register Name	NTL0/NDL0 MMIO BAR Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.NDT0_BAR
Address	000000000501124D (SCOM)
Description	BAR register defining NDL/NTL MMIO range for brick 0 connected to this stack Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0/1 = Disable/enable BAR for brick 0.
1:2	RW	NDT0_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
3:6	RW	CONFIG_NDT0_BAR_GROUP: group field of the address for this BAR.

Bits	SCOM	Field Mnemonic: Description
7:9	RW	CONFIG_NDT0_BAR_CHIP: chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**NTL1/NDL1 MMIO BAR Register**
Mnemonic	NPU.STCK2.CS.SM2.MISC.NDT1_BAR
Address	000000000501124E (SCOM)
Description	BAR register defining NDL/NTL MMIO range for brick 1 connected to this stack Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0/1 = Disable/enable BAR for brick 1.
1:2	RW	NDT1_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
3:6	RW	CONFIG_NDT1_BAR_GROUP: group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: 128K aligned address of BAR for brick 1's 128K range.
35	RW	NDT1_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**Performance Configuration Register**
Mnemonic	NPU.STCK2.CS.SM2.MISC.PERF_CONFIG
Address	000000000501124F (SCOM)
Description	Performance Event selection

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_Reserved2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock-gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.INHIBIT_CONFIG
Address	0000000005011250 (SCOM)
Description	Configures Inhibits for CQ_SM

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = 1/2^(n+1). 12 = 1/2^14. 13 = 1/2^16. 14 = 1/2^18. 15 = 1/2^20.
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre frequency 0: 0 = Inhibit timer tick0. 1 = inverted Inhibit timer tick0. 2 = LFSR. 3 = inverted LFSR (-> 1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0/1 = Disable blocky mode / enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0/1 = continus mode / one-shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..12 = 1/2^(n+1). 13 = 1/2^16. 14 = 1/2^18. 15 = 1/2^20.
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre frequency 0: 0 = Inhibit timer tick1. 1 = inverted Inhibit timer tick1. 2 = LFSR. 3 = inverted LFSR (-> 1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0/1 = Disable blocky mode / enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0/1 = continus mode / one-shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_MESSAGE0
Address	0000000005011251 (SCOM)
Description	Error message/capture register 0

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_MESSAGE1
Address	0000000005011252 (SCOM)
Description	Error message/capture register 1

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_MESSAGE2
Address	0000000005011253 (SCOM)
Description	2 latches Error message/capture register 2

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_MESSAGE3
Address	0000000005011254 (SCOM)
Description	3 latches Error message/capture register 3

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_MESSAGE4
Address	0000000005011255 (SCOM)
Description	4 latches Error message/capture register 4

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.SM_STATUS
Address	0000000005011256 (SCOM)
Description	Status reporting register

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: 1 when brick 0 CReq allocation is at its idle level.

Bits	SCOM	Field Mnemonic: Description
1	ROX	SM_STATUS_PRB0: 1 when brick 0 Probe allocation is at its idle level.
2	ROX	SM_STATUS_CREQ1: 1 when brick 1 CReq allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: 1 when brick 1 Probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: 1 when processor bus (non-cp*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: 1 when processor bus (cp*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master-Retry backoff level for Group-Pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master-Retry backoff level for System-Pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick-0 Fence sequencing state. 0b0000 = Idle state, completely unfenced. 0b0xxx = In transition between fenced and not-fenced. 0b0111 = Fenced state, fence sequencing complete. 0b100x = Flushing pocket-cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick-1 Fence sequencing state. 0b0000 = Idle state, completely unfenced. 0b0xxx = In transition between fenced and not-fenced. 0b0111 = Fenced state, fence sequencing complete. 0b100x = Flushing pocket-cache entries prior to exiting fence.
24	ROX	SM_STATUS_PBLN: 1 when outbound Ln-scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: 1 when outbound Nn/G-scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: 1 when outbound Rn/Vg-scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: 1 when outbound brick 0 CReq request queue is empty.
28	ROX	SM_STATUS_N0DGD: 1 when outbound brick 0 Downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: 1 when outbound brick 1 CReq request queue is empty.
30	ROX	SM_STATUS_N1DGD: 1 when outbound brick 1 Downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: 1 when outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: 1 when outbound ATS-TCE-Translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: 1 when outbound processor bus data-response/merge-operation queue is empty.
34	ROX	SM_STATUS_N0RSP: 1 when outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: 1 when outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: 1 when outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: 1 when Same-Address Collision-Check queue is empty.
38	ROX	SM_STATUS_FREE: 1 when Free state machine queue is empty.
39	ROX	SM_STATUS_Reserved1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	**CERR First 0 Register**
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_FIRST0
Address	0000000005011257 (SCOM)
Description	c_err_rpt first latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done Response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPUBar.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from State-machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU BKill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU Memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/Length/Alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR First 1 Register**
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_FIRST1
Address	0000000005011258 (SCOM)
Description	c_err_rpt first latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD Pre-Snoop table lookup missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD Final-Snoop table lookup missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS-response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD Pre-Snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD Final-Snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: AUE0 UE ECC error detected from State-machine array.
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: PBP0 Parity error detected on RCMD ttag field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: PBP2 Parity error detected on CRESP ttag.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: error CRESP received for a bkill.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = Poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: Atag contains out-of-range group (HPC or Tag) for NPU +/- brazos mode.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: Atag contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: PBC4 RCMD TTag received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: PBC5 RCMD TTag received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: PBC6 CRESP TTag received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: PBC7 CRESP TTag received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_FIRST2
Address	0000000005011259 (SCOM)
Description	2 latches c_err_rpt first latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD Event received but state machine is not IDLE.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket-Hit event but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table lookup missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: start epsilon, but epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: snoop CRESP received but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp-Pocket-Hit event but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table lookup missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state didn't match early protection state.
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: start epsilon, but epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: bad next-step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: bad next-step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: master CRESP received but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT-translate-Response event but not in wait-translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT-translate-Response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA-Done event but not in wait-SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next-step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink Master Command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown nv-master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon-In-Progress, but epsilon counter clock is not the epsilon clock.
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.

Bits	SCOM	Field Mnemonic: Description
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: bad next-step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown Event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table lookup missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from dsa table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown State.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown nv-master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: impossible command/cresp.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: impossible command/cresp.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: impossible command/cresp.
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout but not in waiting-NV-response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_MASK0
Address	000000000501125A (SCOM)
Description	c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done Response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.

Bits	SCOM	Field Mnemonic: Description
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPUBar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from State-machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU BKill request.
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU Memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/Length/Alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Mask 1 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_MASK1
Address	000000000501125B (SCOM)
Description	c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD Pre-Snoop table lookup missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD Final-Snoop table lookup missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS-response.
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD Pre-Snoop table impossible command.

Bits	SCOM	Field Mnemonic: Description
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD Final-Snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).
20	RW	IDIAL_SM_MASK_AUE_0: AUE0 UE ECC error detected from State-machine array.
21	RW	IDIAL_SM_MASK_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: PBP0 Parity error detected on RCMD ttag field.
25	RW	IDIAL_SM_MASK_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: PBP2 Parity error detected on CRESP ttag.
27	RW	IDIAL_SM_MASK_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = Poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: Atag contains out-of-range group (HPC or Tag) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: Atag contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: PBC4 RCMD TTag received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: PBC5 RCMD TTag received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: PBC6 CRESP TTag received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: PBC7 CRESP TTag received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 2 Register**
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_MASK2
Address	000000000501125C (SCOM)
Description	2 latches c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD Event received but state machine is not IDLE.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket-Hit event but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table lookup missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: start epsilon, but epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: snoop CRESP received but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp-Pocket-Hit event but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table lookup missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state didn't match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: start epsilon, but epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: bad scenario code from ma_mcresp table.

Bits	SCOM	Field Mnemonic: Description
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: bad next-step for bkill (ack-done).
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: bad next-step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: master CRESP received but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT-translate-Response event but not in wait-translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT-translate-Response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA-Done event but not in wait-SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next-step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink Master Command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown nv-master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon-In-Progress, but epsilon counter clock is not the epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: bad next-step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown Event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table lookup missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from dsa table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown State.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown nv-master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: impossible command/cresp.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: impossible command/cresp.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: impossible command/cresp.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry but not in retry-abbks collision state.

Bits	SCOM	Field Mnemonic: Description
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout but not in waiting-NV-response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_HOLD0
Address	000000000501125D (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done Response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPUBar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from State-machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU BKill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU Memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/Length/Alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_HOLD1
Address	000000000501125E (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD Pre-Snoop table lookup missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD Final-Snoop table lookup missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS-response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD Pre-Snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD Final-Snoop table impossible command.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: AUE0 UE ECC error detected from State-machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: PBP0 Parity error detected on RCMD ttag field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: PBP2 Parity error detected on CRESP ttag.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = Poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).

Bits	SCOM	Field Mnemonic: Description
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: Atag contains out-of-range group (HPC or Tag) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: Atag contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: PBC4 RCMD TTag received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: PBC5 RCMD TTag received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: PBC6 CRESP TTag received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: PBC7 CRESP TTag received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 2 Register
Mnemonic	NPU.STCK2.CS.SM2.MISC.CERR_HOLD2
Address	000000000501125F (SCOM)
Description	2 latches c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD Event received but state machine is not IDLE.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket-Hit event but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table lookup missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: start epsilon, but epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: snoop CRESP received but not in M_WT_CRESP state.

Bits	SCOM	Field Mnemonic: Description
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp-Pocket-Hit event but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table lookup missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state didn't match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: start epsilon, but epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: bad next-step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: bad next-step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: master CRESP received but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT-translate-Response event but not in wait-translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT-translate-Response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA-Done event but not in wait-SA state.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next-step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink Master Command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown nv-master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon-In-Progress, but epsilon counter clock is not the epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: bad next-step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown Event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table lookup missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from dsa table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown State.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown nv-master command for Fence-Fill-SUE response.

Bits	SCOM	Field Mnemonic: Description
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: impossible command/cresp.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: impossible command/cresp.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: impossible command/cresp.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout but not in waiting-NV-response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_SM Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK2.CS.SM3.MISC.CONFIG0
Address	0000000005011260 (SCOM)
Description	Misc Configuration Register Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
1	RW	CONFIG_MA_DSA_OPT_CLAIM_UR: 0/1 = use Read.RWC/Upgrade.DN for dclaim/dcbz to GPU Mem.
2	RW	CONFIG_MA_DSA_OPT_FLUSH_UR: 0/1 = use Read.RWC/Upgrade.DN for dcbf/dcbfc to GPU Mem.
3	RW	CONFIG_MA_DSA_OPT_RP_MODE: 0/1 = use DMA/Read-Push for Write.NC to Proc Mem.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0/1 = large-system-mode/small-system-mode.

Bits	SCOM	Field Mnemonic: Description
5	RW	CONFIG_DISABLE_NN_RN: Processor bus scope: 0/1 = Enable Nn and Rn scopes / Disable Nn and Rn scopes.
6	RW	CONFIG_DISABLE_VG_NOT_SYS: Processor bus scope: 0/1 = Enable Vg less than sys / Force all Vg to sys.
7	RW	CONFIG_DISABLE_G: Processor bus scope: 0/1 = Enable G scope / Disable G scope.
8	RW	CONFIG_DISABLE_LN: Processor bus scope: 0/1 = Enable Ln scope / Disable Ln scope.
9	RW	CONFIG_SKIP_G: Processor bus scope: 0/1 = Allow G on rty_inc / Skip G on rty_inc.
10	RW	CONFIG_MA_MCRESP_OPT_WRP: 0/1 = increase scope on rty_inc to dma_w / use write-read-push on rty_inc to dma_w.
11	RW	CONFIG_MA_MCRESP_OPT_RTY_INJ: On a rty_inj type cresp, 0/1 = keep sending dma/change to _inj.
12	RW	CONFIG_MA_MCRESP_OPT_RTY_DMA: On a rty_dma type cresp, 0/1 = keep sending inj/change to _dma.
13:15	RW	CONFIG_INC_PRI_MASK: Mask select for priority increase due to rty_drp. 0: 100% chance to increase priority. 1: 50% chance to increase priority. 2: 25% chance to increase priority. 3: 12.5% chance to increase priority. 4: 6% chance to increase priority. 5: 3% chance to increase priority. 6,7: 1.5% chance to increase priority.
16	RW	CONFIG1_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
17	RW	CONFIG_MA_RSNOOP_OPT_B: TBD future option bit.
18	RW	CONFIG_MA_RSNOOP_OPT_C: TBD future option bit.
19	RW	CONFIG_MA_SCRESP_OPT_A: TBD future option bit.
20	RW	CONFIG_MA_SCRESP_OPT_B: TBD future option bit.
21	RW	CONFIG_MA_SCRESP_OPT_C: TBD future option bit.
22	RW	CONFIG_Reserved4: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
23	RW	CONFIG_MACH_CORRENAB: 0/1 = Disable/enable state machine array ECC correction.
24	RW	CONFIG_MACH_INJECT_ENABLE1: 0/1 = Disable/enable state machine array ECC error inject bit 1.
25	RW	CONFIG_MACH_INJECT_ENABLE2: 0/1 = Disable/enable state machine array ECC error inject bit 2.
26	RW	CONFIG_RXO_CORRENAB: 0/1 = Disable/enable ReqRspOut array ECC correction.
27	RW	CONFIG_RXO_INJECT_ENABLE1: 0/1 = Disable/enable ReqRspOut array ECC error inject bit 1.
28	RW	CONFIG_RXO_INJECT_ENABLE2: 0/1 = Disable/enable ReqRspOut array ECC error inject bit 1.
29	RW	CONFIG_RSI_CORRENAB: 0/1 = Disable/enable PB-Rsp-In array ECC correction.
30	RW	CONFIG_RSI_INJECT_ENABLE1: 0/1 = Disable/enable PB-Rsp-Ine array ECC error inject bit 1.
31	RW	CONFIG_RSI_INJECT_ENABLE2: 0/1 = Disable/enable PB-Rsp-Ine array ECC error inject bit 1.
32:33	RW	CONFIG_MA_RSNOOP_OPT_DCLAIM: 0 = partial-respond to dclaim to GPU Mem with lpc_ack. 1 = partial-respond to dclaim to GPU Mem with lpc_ack+rty_lost_claim. 2 = partial-respond to dclaim to GPU Mem with lpc_ack+rty_lpc+start pocket cache. 3 = Reserved.
34	RW	CONFIG_MA_DSA_OPT_DMA_UPG: 0/1 = non-relaxed dma_w use Read.RWC/Upgrade.DN to acquire pocket-cache state/data.

Bits	SCOM	Field Mnemonic: Description
35	RW	CONFIG_EVAPORATE_BY_LCO: 0/1 = just free the state-machine without lco/evaporate pocket-cache entries by lco.
36	RW	CONFIG_MRBGP_TRACK_ALL: 0/1 = master-retry-backoff group-pump track only this stack's/all-this-chips retry responses.
37	RW	CONFIG_MRBSP_TRACK_ALL: 0/1 = master-retry-backoff system-pump track only this stack's/all-this-chips retry responses.
38	RW	CONFIG_ENABLE_PBUS: 0/1 = Disable NPU processor bus RCMD, PResp, and CRESP interfaces / enable these interfaces.
39	RW	CONFIG_BRAZOS_MODE: 0/1 = non-brazos 4-group;2-chip mode / brazos 2-group;4-chip mode.
40	RW	CONFIG_ENABLE_SNARF_CPM: 0/1 = Disable/enable Probe.I.MO snarfing a cp_m.
41	RW	CONFIG_PREALLOC2_REQ0: 0/1 = pre-allocate 2 state-machines to brick 0 CREQ channel.
42	RW	CONFIG_PREALLOC2_PRB0: 0/1 = pre-allocate 2 state-machines to brick 0 PRB channel.
43	RW	CONFIG_PREALLOC2_REQ1: 0/1 = pre-allocate 2 state-machines to brick 1 CREQ channel.
44	RW	CONFIG_PREALLOC2_PRB1: 0/1 = pre-allocate 2 state-machines to brick 1 PRB channel.
45	RW	CONFIG_PREALLOC2_XATS: 0/1 = pre-allocate 2 state-machines to XATS interface.
46	RW	CONFIG_DISABLE_INJECT: 0/1 = Enable sending cl,pr_dma_inj / disable sending cl,pr_dma_inj. Note: to truly disable sending _inj commands, the following bits must also be set to '0': config_ma_mcresp_opt_rty_inj. config_ma_dsa_opt_rp_mode.
47	RW	CONFIG_DCACHE_MODE: 0/1 = drive data-bus dcache field in basic mode / CAPP mode.
48	RW	CONFIG_DCACHE_REPORTS_PHYSICAL: 0/1 = in basic mode, report local masters as near / local.
49	RW	CONFIG_RSI_DISABLE_DATIN_FASTPATH: 0/1 = Enable rsi PB data-in fastpath/disable fastpath.
50	RW	CONFIG_PCKT_BLK_PRB: 0/1 = valid pocket-cache entries do not block probes / probes are blocked.
51	RW	CONFIG_P9P9_MODE: 0/1 = normal operation / run in special lab-bringup GPU-less POWER9-to-POWER9 mode.
52	RW	CONFIG_FORBID_MMIO_READ_GT_32: 0/1 = Allow GPU->PB MMIOs > 32-bytes / flag-error and brick-fence on MMIOs > 32-bytes.
53	RW	CONFIG_FORBID_MMIO_ATOMIC: 0/1 = Allow GPU->PB atomics to MMIO space / flag-error and brick-fence on atomics to MMIO space.
54	RW	CONFIG_OPT_SNOOP_CP: 0/1 = Snoop POWER9-Mem cp_* type commands / don't snoop cp_* type commands.
55:63	RW	CONFIG0_Reserved3: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.

Register Name	**CQ_SM Miscellaneous Configuration 1 Register**
Mnemonic	NPU.STCK2.CS.SM3.MISC.CONFIG1
Address	0000000005011261 (SCOM)
Description	Misc Configuration Register Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_RANDOM_BACKOFF_DUR_MASK: Mask for the base random duration of a random retry backoff. 0000 -> 0-15 base random duration. 0001 -> 0-31 base random duration. 0011 -> 0-63 base random duration. 0111 -> 0-127 base random duration. 1111 -> 0-255 base random duration.
4:7	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_REQ: Mask for for the slowdown of NTL CReq credits during chgrate.hang. 'n' -> 1/(2^(n+1)) cycles average rate. Note that for a single processor bus ramp, the rate is actually 8 times faster since there are 4 RCMD slice x 2 NTL Bricks that get CReq credits. This field is the rate for 1 brick receiving credit from 1 RCMD slice.
8:11	RW	CONFIG_CHGRATE_HANG_SLOWDOWN_PRB: Mask for for the slowdown of NTL Probe credits during chgrate.hang. 'n' -> 1/(2^(n+1)) cycles average rate. Note that for a single processor bus ramp, the rate is actually 8 times faster since there are 4 RCMD slice x 2 NTL Bricks that get CReq credits. This field is the rate for 1 brick receiving credit from 1 RCMD slice.
12:15	RW	CONFIG_ARB_NONCRR_SAFETY: Safety valve for non-cresp/non-reqin events going down the arb pipe. after N+1 reqin events go through the arbiter while a non-crr event is waiting, reqin events are blocked to give non-crr events a chance.
16:27	RW	CONFIG_EPSILON_WLN_COUNT: epsilon count for Ln scope CP-Write.
28:31	RW	CONFIG_SCALE_RPT_HANG_POLL: Scaling factor for rpt_hang.poll. 0 = 1:1 processor bus rpt_hang.polls received. 1 = 1:2 processor bus rpt_hang.polls received. ... 15 = 1:16 processor bus rpt_hang.polls received.
32:35	RW	CONFIG_SCALE_RPT_HANG_DATA: Scaling factor for rpt_hang.data. 0 = 1:1 processor bus rpt_hang.datas received. 1 = 1:2 processor bus rpt_hang.datas received. ... 15 = 1:16 processor bus rpt_hang.datas received.
36:63	RW	CONFIG1_Reserved: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.

Register Name	**Power Bus Epsilon Configuration Register**
Mnemonic	NPU.STCK2.CS.SM3.MISC.EPSILON_CONFIG
Address	0000000005011262 (SCOM)
Description	Processor bus Epsilon Configuration Register Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_EPSILON_RATE: 0 = decrement epsilon count at 1:1 nest_gckn. ... 15 = epsilon count at 1/16 nest_gckn.
4:15	RW	CONFIG_EPSILON_W0_COUNT: epsilon count for Nn/G scope CP-Write.
16:27	RW	CONFIG_EPSILON_W1_COUNT: epsilon count for Rn/Vg scope CP-Write.
28:39	RW	CONFIG_EPSILON_R0_COUNT: epsilon count for Ln scope Reads.
40:51	RW	CONFIG_EPSILON_R1_COUNT: epsilon count for Nn/G scope Reads.

Bits	SCOM	Field Mnemonic: Description
52:63	RW	CONFIG_EPSILON_R2_COUNT: epsilon count for Rn/Vg scope Reads.

Register Name	Timer Configuration Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.XTIMER_CONFIG
Address	0000000005011263 (SCOM)
Description	Timer Configuration Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_POCKET_RATE1: Rate-1 for the Pocket-Cache w/ Data entries. The Pocket-Cache timer is used to evaporate pocket-cache entries which are not claimed. The Long timer duration is f(Rate-1)*2^(Rate-2)*5e-10 seconds and. the Short timer duration is f(Rate-1)*2^(Rate-3)*5e-10 seconds where f(Rate-1) is: f(0b00) = 7. f(0b01) = 63. f(0b10) = 511. f(0b11) = 4095.
2:7	RW	CONFIG_POCKET_RATE2: Rate-2 for the long timer for Pocket-Cache entries (2^n cycles).
8:13	RW	CONFIG_POCKET_RATE3: Rate-3 for the short timer for Pocket-Cache entries (2^n cycles).
14:19	RW	CONFIG_FWD_PROG_RATE2: Rate-2 for the forward-progress timer (2^n cycles).
20:25	RW	CONFIG_CTL_TICK: Rate for CTL timer tick (default 63 = off). Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
26:31	RW	CONFIG_INH0_TICK: Rate for SM-Inhibit timer tick0 (default 63 = off). Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
32:37	RW	CONFIG_INH1_TICK: Rate for SM-Inhibit timer tick1 (default 63 = off). Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
38:39	RW	CONFIG_NV_RESP_RATE1: Rate-1 for NV-Response timer. The timer duration is f(Rate-1)*2^(Rate-2)*5e-10 seconds. f(0b00) = 7. f(0b01) = 63. f(0b10) = 511. f(0b11) = 4095.
40:45	RW	CONFIG_NV_RESP_RATE2: Rate-2 for the NV-Response timer (2^n cycles).
46:47	RW	CONFIG_POCKET_ND_RATE1: Rate-1 for the Pocket-Cache Dataless entries. The Pocket-Cache timer is used to evaporate pocket-cache entries which are not claimed. The Long timer duration is f(Rate-1)*2^(Rate-2)*5e-10 seconds and. the Short timer duration is f(Rate-1)*2^(Rate-3)*5e-10 seconds where f(Rate-1) is: f(0b00) = 7. f(0b01) = 63. f(0b10) = 511. f(0b11) = 4095.
48:63	RO	Constant = 0b0000000000000000

Register Name	GPU BAR Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.GPU_BAR
Address	0000000005011264 (SCOM)
Description	Memory BARs BAR register defining GPU Mem addresses serviced by bricks 0 and 1 connected to this stack. Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GPU0_BAR_ENABLE: 0/1 = Disable/enable BAR for brick 0.
1:2	RW	CONFIG_GPU0_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 0. Note: It is illegal to set this field to 0b11.
3:6	RW	CONFIG_GPU0_BAR_GROUP: group field of the Base address of BAR for brick 0.
7:9	RW	CONFIG_GPU0_BAR_CHIP: Chip field of the Base address of BAR for brick 0.
10:21	RW	CONFIG_GPU0_BAR_ADDR: Base address (1G address) of BAR for brick 0. Must be aligned on the size of the BAR mask.
22	RW	CONFIG_GPU0_BAR_Reserved: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
23	RW	CONFIG_GPU0_BAR_GRANULE: Hash boundary for brick 0: 0 = hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
24:27	RW	CONFIG_GPU0_BAR_SIZE: Size of Base Address match for the BAR for brick 0. 0 = 1G. 1 = 2G. 2 = 4G. ... 9 = 512G. 10 = 1T. 11 = 2T. 12 = 4T. >12 = Reserved.
28:31	RW	CONFIG_GPU0_BAR_MODE: Hash mode of the BAR for brick 0: 0 = (single) match on all address in addr/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.
32	RW	CONFIG_GPU1_BAR_ENABLE: 0/1 = Disable/enable BAR for brick 1.
33:34	RW	CONFIG_GPU1_BAR_MEMTYPE: Memory type bits (addr(13:14)) needed to match this BAR for brick 1. Note: It is illegal to set this field to 0b11.
35:38	RW	CONFIG_GPU1_BAR_GROUP: group field of the Base address of BAR for brick 1.

Bits	SCOM	Field Mnemonic: Description
39:41	RW	CONFIG_GPU1_BAR_CHIP: Chip field of the Base address of BAR for brick 1.
42:53	RW	CONFIG_GPU1_BAR_ADDR: Base address (1G address) of BAR for brick 1. Must be aligned on the size of the BAR mask.
54	RW	CONFIG_GPU1_BAR_Reserved: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
55	RW	CONFIG_GPU1_BAR_GRANULE: Hash boundary for brick 1: 0 = hash on 512B boundary (hashbits(0:7) = addr(47:54)). 1 = hash on 1024B boundary (hashbits(0:7) = addr(46:53)).
56:59	RW	CONFIG_GPU1_BAR_SIZE: Size of Base Address match for the BAR for brick 1. 0 = 1G. 1 = 2G. 2 = 4G. ... 9 = 512G. 10 = 1T. 11 = 2T. 12 = 4T. >12 = Reserved.
60:63	RW	CONFIG_GPU1_BAR_MODE: Hash mode of the BAR for brick 1: 0 = (single) match on all address in addr/size. 1 = (dual.0) match if hashbits(7) = 0. 2 = (dual.1) match if hashbits(7) = 1. 3 = (triple.0) match if hashbits%3 = 0. 4 = (triple.1) match if hashbits%3 = 1. 5 = (triple.2) match if hashbits%3 = 2. 6 = (quad.0) match if hashbits(6:7) = 0. 7 = (quad.1) match if hashbits(6:7) = 1. 8 = (quad.2) match if hashbits(6:7) = 2. 9 = (quad.3) match if hashbits(6:7) = 3. 10 = (six.0) match if hashbits%3 = 0 and hashbits(7) = 0. 11 = (six.1) match if hashbits%3 = 0 and hashbits(7) = 1. 12 = (six.2) match if hashbits%3 = 1 and hashbits(7) = 0. 13 = (six.3) match if hashbits%3 = 1 and hashbits(7) = 1. 14 = (six.4) match if hashbits%3 = 2 and hashbits(7) = 0. 15 = (six.5) match if hashbits%3 = 2 and hashbits(7) = 1.

Register Name	PHY0/PHY1/NPU MMIO BAR Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.PHY_BAR
Address	0000000005011266 (SCOM)
Description	BAR register defining PHY0/PHY1/NPU MMIO range stack 0 phy_bar defines a 2M range mapped to PHY-0 registers stack 1 phy_bar defines a 2M range mapped to PHY-1 registers stack 2 phy_bar defines a 16M range mapped to all NPU registers Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_PHY_BAR_ENABLE: 0/1 = Disable/enable PHY_BAR.
1:2	RW	PHY_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.

Bits	SCOM	Field Mnemonic: Description
3:6	RW	CONFIG_PHY_BAR_GROUP: group field of 2M aligned address of this PHY_BAR.
7:9	RW	CONFIG_PHY_BAR_CHIP: chip field of 2M aligned address of this PHY_BAR.
10:30	RW	CONFIG_PHY_BAR_ADDR: 2M aligned address of this PHY_BARs 2M range. (in stack 2 the low 3 address bits are Reserved -> 16M range).
31	RW	PHY_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Generation ID BAR Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.GENID_BAR
Address	0000000005011267 (SCOM)
Description	ID Registers MMIO BAR BAR register defining Generation-ID register for this stack/ramp Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_GENID_BAR_ENABLE: 0/1 = Disable/enable this BAR.
1:2	RW	GENID_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
3:6	RW	CONFIG_GENID_BAR_GROUP: group field of 128K aligned address of this GENID_BAR.
7:9	RW	CONFIG_GENID_BAR_CHIP: chip field of 128K aligned address of this GENID_BAR.
10:34	RW	CONFIG_GENID_BAR_ADDR: 128K aligned address of this BARs 128K range.
35	RW	GENID_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
36:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Low Water Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.LOW_WATER
Address	0000000005011268 (SCOM)
Description	Water Marks State-Machine allocation Low-Water Marks Each Low-Water mark should be > = 1 and the sum of the Low-Water marks must be less than config_max_machines Low-Water marks must not be changed after config_enable_machine_alloc is set to 1 and config_enable_machine_alloc must remain at 1 once set to 1 Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_LOW_WATER_XATS: Low-Water mark for XTS/MISC processor bus requests. Can only be changed while config_enable_machine_alloc = 0.

Bits	SCOM	Field Mnemonic: Description
6:11	RW	CONFIG_LOW_WATER_PWR0: Low-Water mark for processor bus rd/dclaim/atomic/etc. requests. Can only be changed while config_enable_machine_alloc = 0.
12:17	RW	CONFIG_LOW_WATER_PWR1: Low-Water mark for processor bus cp (castout-push) requests. Can only be changed while config_enable_machine_alloc = 0.
18:23	RW	CONFIG_LOW_WATER_REQ0: Low-Water mark for NVLink brick-0 non-Probe requests. Can only be changed while config_enable_machine_alloc = 0.
24:29	RW	CONFIG_LOW_WATER_PRB0: Low-Water mark for NVLink brick-0 Probe requests. Can only be changed while config_enable_machine_alloc = 0.
30:35	RW	CONFIG_LOW_WATER_REQ1: Low-Water mark for NVLink brick-1 non-Probe requests. Can only be changed while config_enable_machine_alloc = 0.
36:41	RW	CONFIG_LOW_WATER_PRB1: Low-Water mark for NVLink brick-1 Probe requests. Can only be changed while config_enable_machine_alloc = 0.
42:47	RW	CONFIG_MAX_MACHINES: Maximum number of state-machines to be used. Must be > = 8 and < = 62. Can only be changed while config_enable_machine_alloc = 0.
48:50	RW	LOW_WATER_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
51	RW	CONFIG_ENABLE_MACHINE_ALLOC: Enable state-machine allocation. Can only be changed 0->1, must stay 1 once set.
52:63	RO	Constant = 0b000000000000

Register Name	High Water Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.HIGH_WATER
Address	0000000005011269 (SCOM)
Description	Water Marks State-Machine allocation High-Water Marks Each High-Water mark should be > = corresponding config_low_water and < config_max_machines Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_HIGH_WATER_XATS: High-Water mark for XTS/MISC processor bus requests.
6:11	RW	CONFIG_HIGH_WATER_PWR0: High-Water mark for processor bus rd/dclaim/atomic/etc. requests.
12:17	RW	CONFIG_HIGH_WATER_PWR1: High-Water mark for processor bus cp (castout-push) requests.
18:23	RW	CONFIG_HIGH_WATER_REQ0: High-Water mark for NVLink brick-0 non-Probe requests.
24:29	RW	CONFIG_HIGH_WATER_PRB0: High-Water mark for NVLink brick-0 Probe requests.
30:35	RW	CONFIG_HIGH_WATER_REQ1: High-Water mark for NVLink brick-1 non-Probe requests.
36:41	RW	CONFIG_HIGH_WATER_PRB1: High-Water mark for NVLink brick-1 Probe requests.
42:43	RW	HIGH_WATER_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
44:63	RO	Constant = 0b00000000000000000000

Register Name	Relaxed Configuration 0 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CONFIG_RELAXED0
Address	000000000501126A (SCOM)
Description	Ordering Config0 Configure relaxed-ordering Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_SOURCE0_WRENA: 0/1 = Disable/enable relaxed source0 for write operations.
1	RW	CONFIG_RELAXED_SOURCE0_RDENA: 0/1 = Disable/enable relaxed source0 for read operations.
2:19	RW	CONFIG_RELAXED_SOURCE0_MATCH: relaxed source0 tag match value. when config_brazos_mode = 0, matches TTag 2:3,6:21. when config_brazos_mode = 1, matches TTag 3,5:21.
20:37	RW	CONFIG_RELAXED_SOURCE0_MASK: relaxed source0 tag mask value. 0 = bit is masked off, corresponding match bit must be zero. 1 = bit must equal corresponding match bit.
38:39	RW	CONFIG_RELAXED_Reserved0: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
40	RW	CONFIG_RELAXED_SOURCE1_WRENA: 0/1 = Disable/enable relaxed source1 for write operations.
41	RW	CONFIG_RELAXED_SOURCE1_RDENA: 0/1 = Disable/enable relaxed source1 for read operations.
42:59	RW	CONFIG_RELAXED_SOURCE1_MATCH: relaxed source1 tag match value. when config_brazos_mode = 0, matches TTag 2:3,6:21. when config_brazos_mode = 1, matches TTag 3,5:21.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 1 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CONFIG_RELAXED1
Address	000000000501126B (SCOM)
Description	Ordering Config1 Configure relaxed-ordering Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:17	RW	CONFIG_RELAXED_SOURCE1_MASK: relaxed source1 tag mask value.
18:19	RW	CONFIG_RELAXED_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
20	RW	CONFIG_RELAXED_SOURCE2_WRENA: 0/1 = Disable/enable relaxed source2 for write operations.
21	RW	CONFIG_RELAXED_SOURCE2_RDENA: 0/1 = Disable/enable relaxed source2 for read operations.
22:39	RW	CONFIG_RELAXED_SOURCE2_MATCH: relaxed source2 tag match value. when config_brazos_mode = 0, matches TTag 2:3,6:21. when config_brazos_mode = 1, matches TTag 3,5:21.
40:57	RW	CONFIG_RELAXED_SOURCE2_MASK: relaxed source0 tag mask value.

Bits	SCOM	Field Mnemonic: Description
58:59	RW	CONFIG_RELAXED_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
60:63	RO	Constant = 0b0000

Register Name	Relaxed Configuration 2 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CONFIG_RELAXED2
Address	0000000005011260 (SCOM)
Description	Ordering Config2 Configure relaxed-ordering Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_RELAXED_CMD_CL_DMA_W: Enable relaxed ordering for cl_dma_w.
1	RW	CONFIG_RELAXED_CMD_CL_DMA_W_HP: Enable relaxed ordering for cl_dma_w_hp.
2	RW	CONFIG_RELAXED_CMD_CL_DMA_INJ: Enable relaxed ordering for cl_dma_inj.
3	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_U: Enable relaxed ordering for armw_cas_imax_u.
4	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMAX_S: Enable relaxed ordering for armw_cas_imax_s.
5	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_U: Enable relaxed ordering for armw_cas_imin_u.
6	RW	CONFIG_RELAXED_CMD_ARMW_CAS_IMIN_S: Enable relaxed ordering for armw_cas_imin_s.
7	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_U: Enable relaxed ordering for armwf_cas_imax_u.
8	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMAX_S: Enable relaxed ordering for armwf_cas_imax_s.
9	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_U: Enable relaxed ordering for armwf_cas_imin_u.
10	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_IMIN_S: Enable relaxed ordering for armwf_cas_imin_s.
11	RW	CONFIG_RELAXED_CMD_PR_DMA_INJ: Enable relaxed ordering for pr_dma_inj.
12	RW	CONFIG_RELAXED_CMD_DMA_PR_W: Enable relaxed ordering for dma_pr_w.
13	RW	CONFIG_RELAXED_CMD_ARMW_ADD: Enable relaxed ordering for armw_add.
14	RW	CONFIG_RELAXED_CMD_ARMW_AND: Enable relaxed ordering for armw_and.
15	RW	CONFIG_RELAXED_CMD_ARMW_OR: Enable relaxed ordering for armw_or.
16	RW	CONFIG_RELAXED_CMD_ARMW_XOR: Enable relaxed ordering for armw_xor.
17	RW	CONFIG_RELAXED_CMD_ARMWF_ADD: Enable relaxed ordering for armwf_add.
18	RW	CONFIG_RELAXED_CMD_ARMWF_AND: Enable relaxed ordering for armwf_and.
19	RW	CONFIG_RELAXED_CMD_ARMWF_OR: Enable relaxed ordering for armwf_or.
20	RW	CONFIG_RELAXED_CMD_ARMWF_XOR: Enable relaxed ordering for armwf_xor.
21	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_E: Enable relaxed ordering for armwf_cas_e.
22	RW	CONFIG_RELAXED_CMD_ARMWF_CAS_U: Enable relaxed ordering for armwf_cas_u.
23	RW	CONFIG_RELAXED_CMD_CL_RD_NC_F0: Enable relaxed ordering for cl_rd_nc(F = 0).
24	RW	CONFIG_RELAXED_SOURCE3_WRENA: 0/1 = Disable/enable relaxed source3 for write operations.
25	RW	CONFIG_RELAXED_SOURCE3_RDENA: 0/1 = Disable/enable relaxed source3 for read operations.

Bits	SCOM	Field Mnemonic: Description
26:43	RW	CONFIG_RELAXED_SOURCE3_MATCH: relaxed source3 tag match value. when config_brazos_mode = 0, matches TTag 2:3,6:21. when config_brazos_mode = 1, matches TTag 3,5:21.
44:61	RW	CONFIG_RELAXED_SOURCE3_MASK: relaxed source0 tag mask value.
62:63	RW	CONFIG_RELAXED_Reserved3: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.

Register Name	**NTL0/NDL0 MMIO BAR Register**
Mnemonic	NPU.STCK2.CS.SM3.MISC.NDT0_BAR
Address	000000000501126D (SCOM)
Description	BAR register defining NDL/NTL MMIO range for brick 0 connected to this stack Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT0_BAR_ENABLE: 0/1 = Disable/enable BAR for brick 0.
1:2	RW	NDT0_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
3:6	RW	CONFIG_NDT0_BAR_GROUP: group field of the address for this BAR.
7:9	RW	CONFIG_NDT0_BAR_CHIP: chip field of the address for this BAR.
10:34	RW	CONFIG_NDT0_BAR_ADDR: 128K aligned address of BAR for brick 0's 128K range.
35	RW	NDT0_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	**NTL1/NDL1 MMIO BAR Register**
Mnemonic	NPU.STCK2.CS.SM3.MISC.NDT1_BAR
Address	000000000501126E (SCOM)
Description	BAR register defining NDL/NTL MMIO range for brick 1 connected to this stack Note: This register should be set to the same value for each brick/stack. MDials have been created at NPU_STACK_WRAP for this register's IDials

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_NDT1_BAR_ENABLE: 0/1 = Disable/enable BAR for brick 1.
1:2	RW	NDT1_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
3:6	RW	CONFIG_NDT1_BAR_GROUP: group field of the address for this BAR.
7:9	RW	CONFIG_NDT1_BAR_CHIP: chip field of the address for this BAR.
10:34	RW	CONFIG_NDT1_BAR_ADDR: 128K aligned address of BAR for brick 1's 128K range.

Bits	SCOM	Field Mnemonic: Description
35	RW	NDT1_Reserved2: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.PERF_CONFIG
Address	000000000501126F (SCOM)
Description	Performance Event selection

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PERF_CONFIG_LATSTART: Latency count start event.
8:15	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:55	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
56:62	RW	PERF_CONFIG_Reserved2: Reserved.
63	RW	PERF_CONFIG_ACT: Enable clock-gates for performance monitor latches.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.INHIBIT_CONFIG
Address	0000000005011270 (SCOM)
Description	Configures Inhibits for CQ_SM

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = 1/2^(n+1). 12 = 1/2^14. 13 = 1/2^16. 14 = 1/2^18. 15 = 1/2^20.
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre frequency 0: 0 = Inhibit timer tick0. 1 = inverted Inhibit timer tick0. 2 = LFSR. 3 = inverted LFSR (-> 1/2, 3/4, 7/8, ...).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0/1 = Disable blocky mode / enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0/1 = continus mode / one-shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.

Bits	SCOM	Field Mnemonic: Description
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..12 = 1/2^(n+1). 13 = 1/2^16. 14 = 1/2^18. 15 = 1/2^20.
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre frequency 0: 0 = Inhibit timer tick1. 1 = inverted Inhibit timer tick1. 2 = LFSR. 3 = inverted LFSR (-> 1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0/1 = Disable blocky mode / enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0/1 = continus mode / one-shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_MESSAGE0
Address	0000000005011271 (SCOM)
Description	Error message/capture register 0

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_MESSAGE1
Address	0000000005011272 (SCOM)
Description	Error message/capture register 1

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR Message 2 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_MESSAGE2
Address	0000000005011273 (SCOM)
Description	2 latches Error message/capture register 2

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS2: Reserved.

Register Name	CERR Message 3 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_MESSAGE3
Address	0000000005011274 (SCOM)
Description	3 latches Error message/capture register 3

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS3: Reserved.

Register Name	CERR Message 4 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_MESSAGE4
Address	0000000005011275 (SCOM)
Description	4 latches Error message/capture register 4

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS4: Reserved.

Register Name	CQ_SM Status Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.SM_STATUS
Address	0000000005011276 (SCOM)
Description	Status reporting register

Bits	SCOM	Field Mnemonic: Description
0	ROX	SM_STATUS_CREQ0: 1 when brick 0 CReq allocation is at its idle level.
1	ROX	SM_STATUS_PRB0: 1 when brick 0 Probe allocation is at its idle level.
2	ROX	SM_STATUS_CREQ1: 1 when brick 1 CReq allocation is at its idle level.
3	ROX	SM_STATUS_PRB1: 1 when brick 1 Probe allocation is at its idle level.
4	ROX	SM_STATUS_XATS: 1 when ATS/MISC allocation is at its idle level.
5	ROX	SM_STATUS_PWR0: 1 when processor bus (non-cp*) allocation is at its idle level.
6	ROX	SM_STATUS_PWR1: 1 when processor bus (cp*) allocation is at its idle level.
7	ROX	SM_STATUS_CHGRATE: 1 when chgrate.hang slowdown is being applied to machine allocation.
8:11	ROX	SM_STATUS_MRBGP: Master-Retry backoff level for Group-Pump commands.
12:15	ROX	SM_STATUS_MRBSP: Master-Retry backoff level for System-Pump commands.
16:19	ROX	SM_STATUS_FENCE0: Brick-0 Fence sequencing state. 0000 = Idle state, completely unfenced. 0xxx = In transition between fenced and not-fenced. 0111 = Fenced state, fence sequencing complete. 100x = Flushing pocket-cache entries prior to exiting fence.
20:23	ROX	SM_STATUS_FENCE1: Brick-1 Fence sequencing state. 0000 = Idle state, completely unfenced. 0xxx = In transition between fenced and not-fenced. 0111 = Fenced state, fence sequencing complete. 100x = Flushing pocket-cache entries prior to exiting fence.

Bits	SCOM	Field Mnemonic: Description
24	ROX	SM_STATUS_PBLN: 1 when outbound Ln-scope processor bus request queue is empty.
25	ROX	SM_STATUS_PBNNG: 1 when outbound Nn/G-scope processor bus request queue is empty.
26	ROX	SM_STATUS_PBRNVG: 1 when outbound Rn/Vg-scope processor bus request queue is empty.
27	ROX	SM_STATUS_N0REQ: 1 when outbound brick 0 CReq request queue is empty.
28	ROX	SM_STATUS_N0DGD: 1 when outbound brick 0 Downgrade request queue is empty.
29	ROX	SM_STATUS_N1REQ: 1 when outbound brick 1 CReq request queue is empty.
30	ROX	SM_STATUS_N1DGD: 1 when outbound brick 1 Downgrade request queue is empty.
31	ROX	SM_STATUS_MMIO: 1 when outbound MMIO/GenId request queue is empty.
32	ROX	SM_STATUS_ATSXLATE: 1 when outbound ATS-TCE-Translation request queue is empty.
33	ROX	SM_STATUS_PBRSP: 1 when outbound processor bus data-response/merge-operation queue is empty.
34	ROX	SM_STATUS_N0RSP: 1 when outbound brick 0 response queue is empty.
35	ROX	SM_STATUS_N1RSP: 1 when outbound brick 1 response queue is empty.
36	ROX	SM_STATUS_XARSP: 1 when outbound ATS/MISC response queue is empty.
37	ROX	SM_STATUS_SACOLL: 1 when Same-Address Collision-Check queue is empty.
38	ROX	SM_STATUS_FREE: 1 when Free state machine queue is empty.
39	ROX	SM_STATUS_Reserved1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_FIRST0
Address	0000000005011277 (SCOM)
Description	c_err_rpt first latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
9	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Response.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done Response.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_22: NVF22 (Reserved).
23	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_23: NVF23 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_24: NVF24 (Reserved).
25	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_25: NVF25 (Reserved).
26	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_26: NVF26 (Reserved).
27	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_27: NVF27 (Reserved).
28	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_28: NVF28 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_29: NVF29 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_0: NCF0 An NVLink probe did not match its GPUBar.

Bits	SCOM	Field Mnemonic: Description
33	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_1: NCF1 (Reserved).
34	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_2: NCF2 (Reserved).
35	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_3: NCF3 (Reserved).
36	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_4: NCF4 (Reserved).
37	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_5: NCF5 (Reserved).
38	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_0: ASBE0 SBE ECC error detected from State-machine array.
41	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLEAR	IDIAL_SM_FIRST_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU BKill request.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_2: PBR2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_3: PBR3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_4: PBR4 Illegal command to GPU Memory received.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_REG_0: REG0 s3: Address/Length/Alignment error on MMIO/GenId access.
53	RWX_WCLEAR	IDIAL_SM_FIRST_REG_1: REG1 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_REG_2: REG2 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 1 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_FIRST1
Address	0000000005011278 (SCOM)
Description	c_err_rpt first latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_0: NLGX0 RCMD Pre-Snoop table lookup missed the table.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_1: NLGX1 RCMD Final-Snoop table lookup missed the table.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_2: NLGX2 Req-in logic dropped an ATS-response.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_3: NLGX3 RCMD Pre-Snoop table impossible command.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_4: NLGX4 RCMD Final-Snoop table impossible command.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_2: FWD2 (Reserved).
19	RWX_WCLEAR	IDIAL_SM_FIRST_FWD_3: FWD3 (Reserved).
20	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_0: AUE0 UE ECC error detected from State-machine array.

Bits	SCOM	Field Mnemonic: Description
21	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLEAR	IDIAL_SM_FIRST_AUE_3: AUE3 (Reserved).
24	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_0: PBP0 Parity error detected on RCMD ttag field.
25	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_2: PBP2 Parity error detected on CRESP ttag.
27	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_4: PBP4 (Reserved).
29	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_5: PBP5 (Reserved).
30	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_6: PBP6 (Reserved).
31	RWX_WCLEAR	IDIAL_SM_FIRST_PBP_7: PBP7 (Reserved).
32	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_0: PBF0 s3: M_WT_CRESP: error CRESP received for a command.
33	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_1: PBF1 s3: PC_WT_CRESP: error CRESP received for a command.
34	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_2: PBF2 s3: PC_BK_WT_CRESP: error CRESP received for a bkill.
35	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_4: PBF4 s3: M_RCV_DATA_PTL: not all segments/OWs were received.
37	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_5: PBF5 s3: PC_RCV_DATA: Received data but none is valid.
38	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = Poison.
39	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_7: PBF7 (Reserved).
40	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_8: PBF8 (Reserved).
41	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_9: PBF9 (Reserved).
42	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_10: PBF10 (Reserved).
43	RWX_WCLEAR	IDIAL_SM_FIRST_PBF_11: PBF11 (Reserved).
44	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_0: PBC0 s3: PC_WT_CRESP: Atag contains out-of-range group (HPC or Tag) for NPU +/- brazos mode.

Bits	SCOM	Field Mnemonic: Description
45	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_1: PBC1 s3: PC_WT_CRESP: Atag contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_2: PBC2 (Reserved).
47	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_3: PBC3 (Reserved).
48	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_4: PBC4 RCMD TTag received with illegal group ID.
49	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_5: PBC5 RCMD TTag received with illegal chip ID.
50	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_6: PBC6 CRESP TTag received with illegal group ID.
51	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_7: PBC7 CRESP TTag received with illegal chip ID.
52	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_8: PBC8 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_9: PBC9 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_10: PBC10 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR First 2 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_FIRST2
Address	0000000005011279 (SCOM)
Description	2 latches c_err_rpt first latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_0: NLG0 s3: RCMD Event received but state machine is not IDLE.
1	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_1: NLG1 s3: Pocket-Hit event but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table lookup missed.
3	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_3: NLG3 s3: M_WT_CRESP: start epsilon, but epsilon already in progress.
4	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_6: NLG6 s3: M_WT_CRESP: bad scenario code from ma_scresp table.
7	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_7: NLG7 s3: snoop CRESP received but not in M_WT_CRESP state.
8	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_8: NLG8 s3: MCResp-Pocket-Hit event but not in PC_* state.
9	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table lookup missed.
10	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state didn't match early protection state.

Bits	SCOM	Field Mnemonic: Description
11	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_11: NLG11 s3: PC_WT_CRESP: start epsilon, but epsilon already in progress.
12	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_12: NLG12 s3: PC_WT_CRESP: bad scenario code from ma_mcresp table.
13	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_13: NLG13 s3: PC_BK_WT_CRESP: bad next-step for bkill (ack-done).
14	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_14: NLG14 s3: PC_BK_WT_CRESP: bad next-step for bkill (retry).
15	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_15: NLG15 s3: PC_BK_WT_CRESP: bad CRESP for a bkill.
16	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_16: NLG16 s3: master CRESP received but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_19: NLG19 s3: AT-translate-Response event but not in wait-translate state.
20	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_20: NLG20 s3: AT-translate-Response event had bad translate status, but command not recognized.
21	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_21: NLG21 s3: SA-Done event but not in wait-SA state.
22	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next-step for PB data transmit.
23	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink Master Command.
24	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_25: NLG25 s3: NC_WT_RESP: Unknown nv-master command for NVLink response.
26	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_27: NLG27 s3: Epsilon-In-Progress, but epsilon counter clock is not the epsilon clock.
28	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.
29	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_29: NLG29 s3: PC_WT_BK_RBACK: bad next-step for bkill.
30	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_34: NLG34 s3: Unknown Event type received.
35	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table lookup missed.
36	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from dsa table.
37	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_37: NLG37 s4: Unknown State.
38	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND but master state is not PCKT_WAIT_HIT.
39	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown nv-master command for Fence-Fill-SUE response.
41	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_41: NLG41 s3: M_WT_CRESP: impossible command/cresp.
42	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_42: NLG42 s3: PC_WT_CRESP: impossible command/cresp.
43	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_43: NLG43 s3: M_EVAL_DIR: impossible command/cresp.

Bits	SCOM	Field Mnemonic: Description
44	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_45: NLG45 s3: sfstat-retry but not in retry-abbks collision state.
46	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_46: NLG46 s3: *cond*-retry but not in retry-abbks collision state.
47	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_48: NLG48 s3: NVLink response timeout but not in waiting-NV-response state.
49	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_51: NLG51 (Reserved).
52	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_52: NLG52 (Reserved).
53	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_53: NLG53 (Reserved).
54	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_54: NLG54 (Reserved).
55	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_55: NLG55 (Reserved).
56	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_56: NLG56 (Reserved).
57	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_57: NLG57 (Reserved).
58	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_58: NLG58 (Reserved).
59	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_59: NLG59 (Reserved).
60	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_60: NLG60 (Reserved).
61	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_61: NLG61 (Reserved).
62	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_62: NLG62 (Reserved).
63	RWX_WCLEAR	IDIAL_SM_FIRST_NLG_63: NLG63 (Reserved).

Register Name	CERR Mask 0 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_MASK0
Address	000000000501127A (SCOM)
Description	c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RW	IDIAL_SM_MASK_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RW	IDIAL_SM_MASK_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RW	IDIAL_SM_MASK_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RW	IDIAL_SM_MASK_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RW	IDIAL_SM_MASK_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RW	IDIAL_SM_MASK_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RW	IDIAL_SM_MASK_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RW	IDIAL_SM_MASK_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
9	RW	IDIAL_SM_MASK_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RW	IDIAL_SM_MASK_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RW	IDIAL_SM_MASK_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RW	IDIAL_SM_MASK_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RW	IDIAL_SM_MASK_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RW	IDIAL_SM_MASK_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RW	IDIAL_SM_MASK_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RW	IDIAL_SM_MASK_NVF_16: NVF16 s3: NVLink response timeout.
17	RW	IDIAL_SM_MASK_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).
18	RW	IDIAL_SM_MASK_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RW	IDIAL_SM_MASK_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Response.
20	RW	IDIAL_SM_MASK_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done Response.
21	RW	IDIAL_SM_MASK_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RW	IDIAL_SM_MASK_NVF_22: NVF22 (Reserved).
23	RW	IDIAL_SM_MASK_NVF_23: NVF23 (Reserved).
24	RW	IDIAL_SM_MASK_NVF_24: NVF24 (Reserved).
25	RW	IDIAL_SM_MASK_NVF_25: NVF25 (Reserved).
26	RW	IDIAL_SM_MASK_NVF_26: NVF26 (Reserved).
27	RW	IDIAL_SM_MASK_NVF_27: NVF27 (Reserved).
28	RW	IDIAL_SM_MASK_NVF_28: NVF28 (Reserved).
29	RW	IDIAL_SM_MASK_NVF_29: NVF29 (Reserved).
30	RW	IDIAL_SM_MASK_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RW	IDIAL_SM_MASK_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RW	IDIAL_SM_MASK_NCF_0: NCF0 An NVLink probe did not match its GPUBar.
33	RW	IDIAL_SM_MASK_NCF_1: NCF1 (Reserved).
34	RW	IDIAL_SM_MASK_NCF_2: NCF2 (Reserved).
35	RW	IDIAL_SM_MASK_NCF_3: NCF3 (Reserved).
36	RW	IDIAL_SM_MASK_NCF_4: NCF4 (Reserved).
37	RW	IDIAL_SM_MASK_NCF_5: NCF5 (Reserved).
38	RW	IDIAL_SM_MASK_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RW	IDIAL_SM_MASK_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RW	IDIAL_SM_MASK_ASBE_0: ASBE0 SBE ECC error detected from State-machine array.
41	RW	IDIAL_SM_MASK_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.
42	RW	IDIAL_SM_MASK_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RW	IDIAL_SM_MASK_ASBE_3: ASBE3 (Reserved).
44	RW	IDIAL_SM_MASK_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RW	IDIAL_SM_MASK_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU BKill request.

Bits	SCOM	Field Mnemonic: Description
46	RW	IDIAL_SM_MASK_PBR_2: PBR2 (Reserved).
47	RW	IDIAL_SM_MASK_PBR_3: PBR3 (Reserved).
48	RW	IDIAL_SM_MASK_PBR_4: PBR4 Illegal command to GPU Memory received.
49	RW	IDIAL_SM_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_SM_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_SM_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_SM_MASK_REG_0: REG0 s3: Address/Length/Alignment error on MMIO/GenId access.
53	RW	IDIAL_SM_MASK_REG_1: REG1 (Reserved).
54	RW	IDIAL_SM_MASK_REG_2: REG2 (Reserved).
55	RW	IDIAL_SM_MASK_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**c_err_rpt maskCERR Mask 1 Register**
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_MASK1
Address	0000000005011278 (SCOM)
Description	c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLGX_0: NLGX0 RCMD Pre-Snoop table lookup missed the table.
1	RW	IDIAL_SM_MASK_NLGX_1: NLGX1 RCMD Final-Snoop table lookup missed the table.
2	RW	IDIAL_SM_MASK_NLGX_2: NLGX2 Req-in logic dropped an ATS-response.
3	RW	IDIAL_SM_MASK_NLGX_3: NLGX3 RCMD Pre-Snoop table impossible command.
4	RW	IDIAL_SM_MASK_NLGX_4: NLGX4 RCMD Final-Snoop table impossible command.
5	RW	IDIAL_SM_MASK_NLGX_5: NLGX5 (Reserved).
6	RW	IDIAL_SM_MASK_NLGX_6: NLGX6 (Reserved).
7	RW	IDIAL_SM_MASK_NLGX_7: NLGX7 (Reserved).
8	RW	IDIAL_SM_MASK_NLGX_8: NLGX8 (Reserved).
9	RW	IDIAL_SM_MASK_NLGX_9: NLGX9 (Reserved).
10	RW	IDIAL_SM_MASK_NLGX_10: NLGX10 (Reserved).
11	RW	IDIAL_SM_MASK_NLGX_11: NLGX11 (Reserved).
12	RW	IDIAL_SM_MASK_NLGX_12: NLGX12 (Reserved).
13	RW	IDIAL_SM_MASK_NLGX_13: NLGX13 (Reserved).
14	RW	IDIAL_SM_MASK_NLGX_14: NLGX14 (Reserved).
15	RW	IDIAL_SM_MASK_NLGX_15: NLGX15 (Reserved).
16	RW	IDIAL_SM_MASK_FWD_0: FWD0 s3: Forward progress timer expired.
17	RW	IDIAL_SM_MASK_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RW	IDIAL_SM_MASK_FWD_2: FWD2 (Reserved).
19	RW	IDIAL_SM_MASK_FWD_3: FWD3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
20	RW	IDIAL_SM_MASK_AUE_0: AUE0 UE ECC error detected from State-machine array.
21	RW	IDIAL_SM_MASK_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RW	IDIAL_SM_MASK_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RW	IDIAL_SM_MASK_AUE_3: AUE3 (Reserved).
24	RW	IDIAL_SM_MASK_PBP_0: PBP0 Parity error detected on RCMD ttag field.
25	RW	IDIAL_SM_MASK_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RW	IDIAL_SM_MASK_PBP_2: PBP2 Parity error detected on CRESP ttag.
27	RW	IDIAL_SM_MASK_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RW	IDIAL_SM_MASK_PBP_4: PBP4 (Reserved).
29	RW	IDIAL_SM_MASK_PBP_5: PBP5 (Reserved).
30	RW	IDIAL_SM_MASK_PBP_6: PBP6 (Reserved).
31	RW	IDIAL_SM_MASK_PBP_7: PBP7 (Reserved).
32	RW	IDIAL_SM_MASK_PBF_0: PBF0 s3: M_WT_CRESP: error CRESP received for a command.
33	RW	IDIAL_SM_MASK_PBF_1: PBF1 s3: PC_WT_CRESP: error CRESP received for a command.
34	RW	IDIAL_SM_MASK_PBF_2: PBF2 s3: PC_BK_WT_CRESP: error CRESP received for a bkill.
35	RW	IDIAL_SM_MASK_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RW	IDIAL_SM_MASK_PBF_4: PBF4 s3: M_RCV_DATA_PTL: not all segments/OWs were received.
37	RW	IDIAL_SM_MASK_PBF_5: PBF5 s3: PC_RCV_DATA: Received data but none is valid.
38	RW	IDIAL_SM_MASK_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = Poison.
39	RW	IDIAL_SM_MASK_PBF_7: PBF7 (Reserved).
40	RW	IDIAL_SM_MASK_PBF_8: PBF8 (Reserved).
41	RW	IDIAL_SM_MASK_PBF_9: PBF9 (Reserved).
42	RW	IDIAL_SM_MASK_PBF_10: PBF10 (Reserved).
43	RW	IDIAL_SM_MASK_PBF_11: PBF11 (Reserved).
44	RW	IDIAL_SM_MASK_PBC_0: PBC0 s3: PC_WT_CRESP: Atag contains out-of-range group (HPC or Tag) for NPU +/- brazos mode.
45	RW	IDIAL_SM_MASK_PBC_1: PBC1 s3: PC_WT_CRESP: Atag contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RW	IDIAL_SM_MASK_PBC_2: PBC2 (Reserved).
47	RW	IDIAL_SM_MASK_PBC_3: PBC3 (Reserved).
48	RW	IDIAL_SM_MASK_PBC_4: PBC4 RCMD TTag received with illegal group ID.
49	RW	IDIAL_SM_MASK_PBC_5: PBC5 RCMD TTag received with illegal chip ID.
50	RW	IDIAL_SM_MASK_PBC_6: PBC6 CRESP TTag received with illegal group ID.
51	RW	IDIAL_SM_MASK_PBC_7: PBC7 CRESP TTag received with illegal chip ID.
52	RW	IDIAL_SM_MASK_PBC_8: PBC8 (Reserved).
53	RW	IDIAL_SM_MASK_PBC_9: PBC9 (Reserved).
54	RW	IDIAL_SM_MASK_PBC_10: PBC10 (Reserved).
55	RW	IDIAL_SM_MASK_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Mask 2 Register**
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_MASK2
Address	0000000005011270 (SCOM)
Description	2 latches c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_SM_MASK_NLG_0: NLG0 s3: RCMD Event received but state machine is not IDLE.
1	RW	IDIAL_SM_MASK_NLG_1: NLG1 s3: Pocket-Hit event but not in M_PCKT_WAIT_HIT state.
2	RW	IDIAL_SM_MASK_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table lookup missed.
3	RW	IDIAL_SM_MASK_NLG_3: NLG3 s3: M_WT_CRESP: start epsilon, but epsilon already in progress.
4	RW	IDIAL_SM_MASK_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RW	IDIAL_SM_MASK_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RW	IDIAL_SM_MASK_NLG_6: NLG6 s3: M_WT_CRESP: bad scenario code from ma_scresp table.
7	RW	IDIAL_SM_MASK_NLG_7: NLG7 s3: snoop CRESP received but not in M_WT_CRESP state.
8	RW	IDIAL_SM_MASK_NLG_8: NLG8 s3: MCResp-Pocket-Hit event but not in PC_* state.
9	RW	IDIAL_SM_MASK_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table lookup missed.
10	RW	IDIAL_SM_MASK_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state didn't match early protection state.
11	RW	IDIAL_SM_MASK_NLG_11: NLG11 s3: PC_WT_CRESP: start epsilon, but epsilon already in progress.
12	RW	IDIAL_SM_MASK_NLG_12: NLG12 s3: PC_WT_CRESP: bad scenario code from ma_mcresp table.
13	RW	IDIAL_SM_MASK_NLG_13: NLG13 s3: PC_BK_WT_CRESP: bad next-step for bkill (ack-done).
14	RW	IDIAL_SM_MASK_NLG_14: NLG14 s3: PC_BK_WT_CRESP: bad next-step for bkill (retry).
15	RW	IDIAL_SM_MASK_NLG_15: NLG15 s3: PC_BK_WT_CRESP: bad CRESP for a bkill.
16	RW	IDIAL_SM_MASK_NLG_16: NLG16 s3: master CRESP received but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RW	IDIAL_SM_MASK_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RW	IDIAL_SM_MASK_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RW	IDIAL_SM_MASK_NLG_19: NLG19 s3: AT-translate-Response event but not in wait-translate state.
20	RW	IDIAL_SM_MASK_NLG_20: NLG20 s3: AT-translate-Response event had bad translate status, but command not recognized.
21	RW	IDIAL_SM_MASK_NLG_21: NLG21 s3: SA-Done event but not in wait-SA state.
22	RW	IDIAL_SM_MASK_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next-step for PB data transmit.
23	RW	IDIAL_SM_MASK_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink Master Command.
24	RW	IDIAL_SM_MASK_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RW	IDIAL_SM_MASK_NLG_25: NLG25 s3: NC_WT_RESP: Unknown nv-master command for NVLink response.
26	RW	IDIAL_SM_MASK_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.

Bits	SCOM	Field Mnemonic: Description
27	RW	IDIAL_SM_MASK_NLG_27: NLG27 s3: Epsilon-In-Progress, but epsilon counter clock is not the epsilon clock.
28	RW	IDIAL_SM_MASK_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.
29	RW	IDIAL_SM_MASK_NLG_29: NLG29 s3: PC_WT_BK_RBACK: bad next-step for bkill.
30	RW	IDIAL_SM_MASK_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RW	IDIAL_SM_MASK_NLG_31: NLG31 s3: Bad epclock value.
32	RW	IDIAL_SM_MASK_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RW	IDIAL_SM_MASK_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RW	IDIAL_SM_MASK_NLG_34: NLG34 s3: Unknown Event type received.
35	RW	IDIAL_SM_MASK_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table lookup missed.
36	RW	IDIAL_SM_MASK_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from dsa table.
37	RW	IDIAL_SM_MASK_NLG_37: NLG37 s4: Unknown State.
38	RW	IDIAL_SM_MASK_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND but master state is not PCKT_WAIT_HIT.
39	RW	IDIAL_SM_MASK_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RW	IDIAL_SM_MASK_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown nv-master command for Fence-Fill-SUE response.
41	RW	IDIAL_SM_MASK_NLG_41: NLG41 s3: M_WT_CRESP: impossible command/cresp.
42	RW	IDIAL_SM_MASK_NLG_42: NLG42 s3: PC_WT_CRESP: impossible command/cresp.
43	RW	IDIAL_SM_MASK_NLG_43: NLG43 s3: M_EVAL_DIR: impossible command/cresp.
44	RW	IDIAL_SM_MASK_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RW	IDIAL_SM_MASK_NLG_45: NLG45 s3: sfstat-retry but not in retry-abbks collision state.
46	RW	IDIAL_SM_MASK_NLG_46: NLG46 s3: *cond*-retry but not in retry-abbks collision state.
47	RW	IDIAL_SM_MASK_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RW	IDIAL_SM_MASK_NLG_48: NLG48 s3: NVLink response timeout but not in waiting-NV-response state.
49	RW	IDIAL_SM_MASK_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RW	IDIAL_SM_MASK_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RW	IDIAL_SM_MASK_NLG_51: NLG51 (Reserved).
52	RW	IDIAL_SM_MASK_NLG_52: NLG52 (Reserved).
53	RW	IDIAL_SM_MASK_NLG_53: NLG53 (Reserved).
54	RW	IDIAL_SM_MASK_NLG_54: NLG54 (Reserved).
55	RW	IDIAL_SM_MASK_NLG_55: NLG55 (Reserved).
56	RW	IDIAL_SM_MASK_NLG_56: NLG56 (Reserved).
57	RW	IDIAL_SM_MASK_NLG_57: NLG57 (Reserved).
58	RW	IDIAL_SM_MASK_NLG_58: NLG58 (Reserved).
59	RW	IDIAL_SM_MASK_NLG_59: NLG59 (Reserved).
60	RW	IDIAL_SM_MASK_NLG_60: NLG60 (Reserved).
61	RW	IDIAL_SM_MASK_NLG_61: NLG61 (Reserved).

Bits	SCOM	Field Mnemonic: Description
62	RW	IDIAL_SM_MASK_NLG_62: NLG62 (Reserved).
63	RW	IDIAL_SM_MASK_NLG_63: NLG63 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_HOLD0
Address	000000000501127D (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_0: NVF0 s3: NV-Rsp to Read.RWC was not a ReqRsp.D.E.128.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_1: NVF1 s3: NV-Rsp to Upgrade.DN was not a ReqRsp.ND.E.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_2: NVF2 s3: NV-Rsp to Write.NC{N}P was not a ReqRsp.ND.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_3: NVF3 s3: NV-Rsp to reduction atomic was not a ReqRsp.ND.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_4: NVF4 s3: NV-Rsp to non-reduction atomic was not a ReqRsp.D.AtmLen.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_5: NVF5 s3: NV-Rsp to Downgrade.XD.128 was not a DgdRsp(.ND).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_6: NVF6 s3: NV-Rsp to Downgrade.XD.64L was not a DgdRsp(.ND).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_7: NVF7 s3: NV-Rsp to Downgrade.XD.64H was not a DgdRsp(.ND).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_8: NVF8 s3: NV-Rsp to Downgrade.ID.128 was not a DgdRsp(.ND).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_9: NVF9 s3: NV-Rsp to Downgrade.ID.64L was not a DgdRsp(.ND).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_10: NVF10 s3: NV-Rsp to Downgrade.ID.64H was not a DgdRsp(.ND).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_11: NVF11 s3: NV-Rsp to Downgrade.ID.DMA was not a DgdRsp(.ND).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_12: NVF12 s3: NV-Rsp to Downgrade.ID.CI was not a DgdRsp(.ND).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_13: NVF13 s3: NV-Rsp to Downgrade.IND was not a DgdRsp(.ND).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_14: NVF14 s3: NV-Rsp to Read.NCP was not a ReqRsp.D.128.
15	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_15: NVF15 s3: UT = 1 to MMIO space bad command/length/alignment.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_16: NVF16 s3: NVLink response timeout.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_17: NVF17 s3: NV-Rsp to Downgrade.ID.ATM was not a DgdRsp(.ND).

Bits	SCOM	Field Mnemonic: Description
18	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_18: NVF18 s3: NV-Rsp to Downgrade.ID.2AT was not a DgdRsp(.ND).
19	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_19: NVF19 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Response.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_20: NVF20 s3: Target-Error/Unsupported-Request/Reserved Rsp_Status received in NVLink Trans-Done Response.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_21: NVF21 s3: UT = 0 to MMIO space bad command/length/alignment.
22	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_22: NVF22 (Reserved).
23	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_23: NVF23 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_24: NVF24 (Reserved).
25	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_25: NVF25 (Reserved).
26	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_26: NVF26 (Reserved).
27	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_27: NVF27 (Reserved).
28	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_28: NVF28 (Reserved).
29	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_29: NVF29 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_30: NVF30 NVLink NVF error for brick 0 occurred.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NVF_31: NVF31 NVLink NVF error for brick 1 occurred.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_0: NCF0 An NVLink probe did not match its GPUBar.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_1: NCF1 (Reserved).
34	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_2: NCF2 (Reserved).
35	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_3: NCF3 (Reserved).
36	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_4: NCF4 (Reserved).
37	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_5: NCF5 (Reserved).
38	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_6: NCF6 NVLink NCF error for brick 0 occurred.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NCF_7: NCF7 NVLink NCF error for brick 1 occurred.
40	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_0: ASBE0 SBE ECC error detected from State-machine array.
41	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_1: ASBE1 SBE ECC error detected from Rq/Rs output queue array.

Bits	SCOM	Field Mnemonic: Description
42	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_2: ASBE2 SBE ECC error detected from processor bus data flit combiner array.
43	RWX_WCLRREG	IDIAL_SM_HOLD_ASBE_3: ASBE3 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_0: PBR0 s3: PC_WT_CRESP: abort_trm(_ed) CRESP received to NPU request.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_1: PBR1 s3: PC_BK_WT_CRESP: abort_trm CRESP received to NPU BKill request.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_2: PBR2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_3: PBR3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_4: PBR4 Illegal command to GPU Memory received.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_REG_0: REG0 s3: Address/Length/Alignment error on MMIO/GenId access.
53	RWX_WCLRREG	IDIAL_SM_HOLD_REG_1: REG1 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_REG_2: REG2 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_REG_3: REG3 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_HOLD1
Address	000000000501127E (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_0: NLGX0 RCMD Pre-Snoop table lookup missed the table.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_1: NLGX1 RCMD Final-Snoop table lookup missed the table.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_2: NLGX2 Req-in logic dropped an ATS-response.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_3: NLGX3 RCMD Pre-Snoop table impossible command.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_4: NLGX4 RCMD Final-Snoop table impossible command.

Bits	SCOM	Field Mnemonic: Description
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_5: NLGX5 (Reserved).
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_6: NLGX6 (Reserved).
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_7: NLGX7 (Reserved).
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_8: NLGX8 (Reserved).
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_9: NLGX9 (Reserved).
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_10: NLGX10 (Reserved).
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_11: NLGX11 (Reserved).
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_12: NLGX12 (Reserved).
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_13: NLGX13 (Reserved).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_14: NLGX14 (Reserved).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLGX_15: NLGX15 (Reserved).
16	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_0: FWD0 s3: Forward progress timer expired.
17	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_1: FWD1 s3: rpt_hang.data waiting-for-data timeout.
18	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_2: FWD2 (Reserved).
19	RWX_WCLRREG	IDIAL_SM_HOLD_FWD_3: FWD3 (Reserved).
20	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_0: AUE0 UE ECC error detected from State-machine array.
21	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_1: AUE1 UE ECC error detected from Rq/Rs output queue array.
22	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_2: AUE2 UE ECC error detected from processor bus data flit combiner array.
23	RWX_WCLRREG	IDIAL_SM_HOLD_AUE_3: AUE3 (Reserved).
24	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_0: PBP0 Parity error detected on RCMD ttag field.
25	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_1: PBP1 Parity error detected on RCMD address field.
26	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_2: PBP2 Parity error detected on CRESP ttag.
27	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_3: PBP3 Parity error detected on CRESP ATAG.
28	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_4: PBP4 (Reserved).

Bits	SCOM	Field Mnemonic: Description
29	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_5: PBP5 (Reserved).
30	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_6: PBP6 (Reserved).
31	RWX_WCLRREG	IDIAL_SM_HOLD_PBP_7: PBP7 (Reserved).
32	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_0: PBF0 s3: M_WT_CRESP: error CRESP received for a command.
33	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_1: PBF1 s3: PC_WT_CRESP: error CRESP received for a command.
34	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_2: PBF2 s3: PC_BK_WT_CRESP: error CRESP received for a bkill.
35	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_3: PBF3 s3: PC_BK_WT_CRESP: ack_dead CRESP received for a bkill.
36	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_4: PBF4 s3: M_RCV_DATA_PTL: not all segments/OWs were received.
37	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_5: PBF5 s3: PC_RCV_DATA: Received data but none is valid.
38	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_6: PBF6 s3: SM_EV_DATIN: Received data with data_stat = Poison.
39	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_7: PBF7 (Reserved).
40	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_8: PBF8 (Reserved).
41	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_9: PBF9 (Reserved).
42	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_10: PBF10 (Reserved).
43	RWX_WCLRREG	IDIAL_SM_HOLD_PBF_11: PBF11 (Reserved).
44	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_0: PBC0 s3: PC_WT_CRESP: ATAG contains out-of-range group (HPC or Tag) for NPU +/- brazos mode.
45	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_1: PBC1 s3: PC_WT_CRESP: ATAG contains out-of-range group (LPC) for NPU +/- brazos mode.
46	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_2: PBC2 (Reserved).
47	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_3: PBC3 (Reserved).
48	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_4: PBC4 RCMD TTag received with illegal group ID.
49	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_5: PBC5 RCMD TTag received with illegal chip ID.
50	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_6: PBC6 CRESP TTag received with illegal group ID.
51	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_7: PBC7 CRESP TTag received with illegal chip ID.
52	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_8: PBC8 (Reserved).

Bits	SCOM	Field Mnemonic: Description
53	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_9: PBC9 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_10: PBC10 (Reserved).
55	RWX_WCLRREG	IDIAL_SM_HOLD_PBC_11: PBC11 (Reserved).
56:63	RO	Constant = 0b00000000

Register Name	**CERR Hold 2 Register**
Mnemonic	NPU.STCK2.CS.SM3.MISC.CERR_HOLD2
Address	000000000501127F (SCOM)
Description	2 latches c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_0: NLG0 s3: RCMD Event received but state machine is not IDLE.
1	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_1: NLG1 s3: Pocket-Hit event but not in M_PCKT_WAIT_HIT state.
2	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_2: NLG2 s3: M_WT_CRESP: ma_scresp table lookup missed.
3	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_3: NLG3 s3: M_WT_CRESP: start epsilon, but epsilon already in progress.
4	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_4: NLG4 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have NV modified data.
5	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_5: NLG5 s3: M_WT_CRESP: ma_scresp indicated 'evaporate' but have PB modified data.
6	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_6: NLG6 s3: M_WT_CRESP: bad scenario code from ma_scresp table.
7	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_7: NLG7 s3: snoop CRESP received but not in M_WT_CRESP state.
8	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_8: NLG8 s3: MCResp-Pocket-Hit event but not in PC_* state.
9	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_9: NLG9 s3: PC_WT_CRESP: ma_mcresp table lookup missed.
10	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_10: NLG10 s3: PC_WT_CRESP: Write coll state didn't match early protection state.
11	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_11: NLG11 s3: PC_WT_CRESP: start epsilon, but epsilon already in progress.
12	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_12: NLG12 s3: PC_WT_CRESP: bad scenario code from ma_mcresp table.
13	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_13: NLG13 s3: PC_BK_WT_CRESP: bad next-step for bkill (ack-done).
14	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_14: NLG14 s3: PC_BK_WT_CRESP: bad next-step for bkill (retry).
15	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_15: NLG15 s3: PC_BK_WT_CRESP: bad CRESP for a bkill.
16	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_16: NLG16 s3: master CRESP received but not in PC_WT_CRESP/PC_BK_WT_CRESP states.
17	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_17: NLG17 s3: M_IDLE: Invalid DATALEN[3:0] for data command.
18	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_18: NLG18 s3: M_IDLE: Invalid command type received.
19	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_19: NLG19 s3: AT-translate-Response event but not in wait-translate state.
20	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_20: NLG20 s3: AT-translate-Response event had bad translate status, but command not recognized.
21	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_21: NLG21 s3: SA-Done event but not in wait-SA state.

Bits	SCOM	Field Mnemonic: Description
22	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_22: NLG22 s3: PC_WAIT_DATADONE: bad next-step for PB data transmit.
23	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_23: NLG23 s3: TD_WAIT_DATADONE: Unknown NVLink Master Command.
24	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_24: NLG24 s3: BuffDone event but not in PB/PC/MG/NR/XATS/TD_WAIT_DATADONE state.
25	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_25: NLG25 s3: NC_WT_RESP: Unknown nv-master command for NVLink response.
26	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_26: NLG26 s3: RspIn event but not in RG_WT_RESP or NC_WT_RESP state.
27	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_27: NLG27 s3: Epsilon-In-Progress, but epsilon counter clock is not the epsilon clock.
28	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_28: NLG28 s3: Epsilon counter clock is 'epsilon' but epsilon_ip is not set.
29	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_29: NLG29 s3: PC_WT_BK_RBACK: bad next-step for bkill.
30	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_30: NLG30 s3: M/RR_BACK timer expired but not in PC_WT(_BK)_RBACK state.
31	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_31: NLG31 s3: Bad epclock value.
32	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_32: NLG32 s3: coll_state is POCKET_RCOLL_ND but master state is not PCKT_WAIT_HIT.
33	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_33: NLG33 s3: Unknown sm_master_state in ESCAN_LCAO event.
34	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_34: NLG34 s3: Unknown Event type received.
35	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_35: NLG35 s4: M_EVAL_DIR: ma_dsa table lookup missed.
36	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_36: NLG36 s4: M_EVAL_DIR: Unknown merge opcode from dsa table.
37	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_37: NLG37 s4: Unknown State.
38	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_38: NLG38 s3: coll_state is POCKET_RCOLL_OND but master state is not PCKT_WAIT_HIT.
39	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_39: NLG39 s3: Unknown sm_master_state in ESCAN_FENCE event.
40	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_40: NLG40 s3: FENCE_WT_RESP_FILL: Unknown nv-master command for Fence-Fill-SUE response.
41	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_41: NLG41 s3: M_WT_CRESP: impossible command/cresp.
42	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_42: NLG42 s3: PC_WT_CRESP: impossible command/cresp.
43	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_43: NLG43 s3: M_EVAL_DIR: impossible command/cresp.
44	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_44: NLG44 s4: Unexpected Error State (bad sub-sequence return).
45	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_45: NLG45 s3: sfstat-retry but not in retry-abbks collision state.
46	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_46: NLG46 s3: *cond*-retry but not in retry-abbks collision state.
47	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_47: NLG47 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
48	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_48: NLG48 s3: NVLink response timeout but not in waiting-NV-response state.
49	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_49: NLG49 s4: M_EVAL_DIR: Unsupported NVLink command for POWER9-to-POWER9 mode.
50	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_50: NLG50 s3: Request from CTL/NTL caused bad MMIO alignment, but command not recognized.
51	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_51: NLG51 (Reserved).
52	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_52: NLG52 (Reserved).
53	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_53: NLG53 (Reserved).
54	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_54: NLG54 (Reserved).

Bits	SCOM	Field Mnemonic: Description
55	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_55: NLG55 (Reserved).
56	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_56: NLG56 (Reserved).
57	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_57: NLG57 (Reserved).
58	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_58: NLG58 (Reserved).
59	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_59: NLG59 (Reserved).
60	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_60: NLG60 (Reserved).
61	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_61: NLG61 (Reserved).
62	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_62: NLG62 (Reserved).
63	RWX_WCLRREG	IDIAL_SM_HOLD_NLG_63: NLG63 (Reserved).

Register Name	**CQ_CTL Miscellaneous Configuration 0 Register**
Mnemonic	NPU.STCK2.CS.CTL.MISC.CONFIG0
Address	0000000005011280 (SCOM)
Description	Misc Configuration Register Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG1_Reserved0: Reserved - was 1dot0 mode. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
1:3	RW	CONFIG1_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
4	RW	CONFIG_ADR_BAR_MODE: Processor bus adr_bar: 0/1 = large-system-mode/small-system-mode.
5:9	RW	CONFIG_GEN_HEAD_DELAY: Number of cycles to wait for generation-done when reading a generation-head register. Note: setting this to zero will hang the NPU.
10	RW	CONFIG_MRBGP_DIV2_COUNT_AT_EXP: Master-retry-backoff retry count when the sample period expires for group-pump. 0 = reset-to-zero 1 = divide-by-two
11	RW	CONFIG_MRBSP_DIV2_COUNT_AT_EXP: Master-retry-backoff retry count when the sample period expires for system-pump 0 = reset-to-zero 1 = divide-by-two
12	RW	CONFIG_MRBGP_DIS_DYN_ADJ: Dynamically adjust the master-retry-backoff sample period based on level for the group-pump. 0 = Enable 1 = Disable
13	RW	CONFIG_MRBSP_DIS_DYN_ADJ: Dynamically adjust the master-retry-backoff sample period based on level for the system-pump. 0 = Enable 1 = Disable

Bits	SCOM	Field Mnemonic: Description
14	RW	CONFIG_MRBGP_DIS_DYN_LVL_ADJ: 0/1 = Adjust the master-retry-backoff thresholds based on level for group-pump. 0 = Enable 1 = Disable
15	RW	CONFIG_MRBSP_DIS_DYN_LVL_ADJ: Adjust the master-retry-backoff thresholds based on level for system-pump. 0 = Enable 1 = Disable
16:21	RW	CONFIG_MRBGP_THRESH1: Master-retry-backoff retry-count threshold at which to reduce the level for group-pump.
22:27	RW	CONFIG_MRBGP_THRESH2: Master-retry-backoff retry-count threshold at which to increase the level for group-pump. Note: make sure that thresh2 > thresh1, or backoff level will only increase.
28:33	RW	CONFIG_MRBSP_THRESH1: Master-retry-backoff retry-count threshold at which to reduce the level for system-pump.
34:39	RW	CONFIG_MRBSP_THRESH2: Master-retry-backoff retry-count threshold at which to increase the level for system-pump. Note: make sure that thresh2 > thresh1, or backoff level will only increase.
40:43	RW	CONFIG_MRBGP_MAX_LEVEL: Master-retry-backoff maximum level for group-pump.
44:47	RW	CONFIG_MRBSP_MAX_LEVEL: Master-retry-backoff maximum level for system-pump.
48	RW	CONFIG_BRAZOS_MODE: 0/1 = non-brazos 4-group;2-chip mode / brazos 2-group;4-chip mode.
49	RW	CONFIG_DISABLE_PBM_ECC_COR: 0/1 = Enable ECC correction of MMIO store data / disable ECC correction.
50	RW	CONFIG_LAB_RANDOMIZE_PE_01: 0 = Don't randomize PE(0:1). 1 = Randomize PE(0:1).
51	RW	CONFIG_LAB_RANDOMIZE_PE_23: 0 = Don't randomize PE(2:3). 1 = Randomize PE(2:3).
52:63	RW	CONFIG1_Reserved2: Reserved. Note: This field can/should have different values in each instance.

Register Name	Future Configuration 1 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CONFIG1
Address	0000000005011281 (SCOM)
Description	Currently reserved register. Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_CONFIG1: Future configuration register.

Register Name	Future Configuration 2 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CONFIG2
Address	0000000005011282 (SCOM)
Description	Currently reserved register. Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_CONFIG2: Future configuration register.

Register Name	Future Configuration 3 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CONFIG3
Address	0000000005011283 (SCOM)
Description	Currently Reserved register. Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_CONFIG3: Future configuration register.

Register Name	Performance Match Configuration Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.PERF_MATCH_CONFIG
Address	0000000005011284 (SCOM)
Description	Performance Event Field Match

Bits	SCOM	Field Mnemonic: Description
0:5	RW	PERF_MATCH_NMCMD: NVLink Command.
6:10	RW	PERF_MATCH_NMEXCMD: NVLink ExtReqCmd.
11	RW	PERF_MATCH_BE: NVLink byte enables.
12:17	RW	PERF_MATCH_CS: NVLink CS(0:5).
18:33	RW	PERF_MATCH_AECS: NVLink AECS(0:15).
34:37	RW	PERF_MATCH_PE: PE.
38:39	RW	PERF_MATCH_Reserved1: Reserved.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	Performance Mask Configuration Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.PERF_MASK_CONFIG
Address	0000000005011285 (SCOM)
Description	Performance Event Field Mask

Bits	SCOM	Field Mnemonic: Description
0:5	RW	PERF_MASK_NMCMD: NVLink Command.
6:10	RW	PERF_MASK_NMEXCMD: NVLink ExtReqCmd.
11	RW	PERF_MASK_BE: NVLink byte enables.
12:17	RW	PERF_MASK_CS: NVLink CS(0:5).
18:33	RW	PERF_MASK_AECS: NVLink AECS(0:15).
34:37	RW	PERF_MASK_PE: PE.
38:39	RW	PERF_MASK_Reserved1: Reserved.

Bits	SCOM	Field Mnemonic: Description
40:63	RO	Constant = 0b000000000000000000000000

Register Name	CQ_CTL Performance Count Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.PERF_COUNT
Address	0000000005011286 (SCOM)
Description	PMULet Count values

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	IDIAL_PERF_COUNT0: Performance Counter 0.
16:31	RWX_WCLRREG	IDIAL_PERF_COUNT1: Performance Counter 1.
32:47	RWX_WCLRREG	IDIAL_PERF_COUNT2: Performance Counter 2.
48:63	RWX_WCLRREG	IDIAL_PERF_COUNT3: Performance Counter 3.

Register Name	Performance Configuration Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.PERF_CONFIG
Address	0000000005011287 (SCOM)
Description	Performance Event selection

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: PMULet Enable (clocks enable).
1	RW	PERF_CONFIG_RESETMODE: 0/1 = reset-on-read/reset-on-write.
2	RW	PERF_CONFIG_FREEZEMODE: 0/1 = freerun-mode/freeze-on-any-max.
3	RW	PERF_CONFIG_DISABLE_PMISC: 0/1 = enable-pmisc/disable-pmisc control of counters.
4	RW	PERF_CONFIG_PMISC_MODE: 0/1 = global pmu pmisc no reset/global pmu miscellaneous reset-on-enable.
5:7	RW	PERF_CONFIG_CASCADE: pmulet cascade config.
8:9	RW	PERF_CONFIG_PRESCALE_C0: prescale config for counter 0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: prescale config for counter 1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: prescale config for counter 2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: prescale config for counter 3.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select.
24:31	RW	PERF_CONFIG_EVENT1: Event 0 select.
32:39	RW	PERF_CONFIG_EVENT2: Event 0 select.
40:47	RW	PERF_CONFIG_EVENT3: Event 0 select.
48:52	RW	PERF_CONFIG_LATSTART: Latency count start event.
53:57	RW	PERF_CONFIG_LATCANCEL: Latency count abort event.
58:62	RW	PERF_CONFIG_LATFINISH: Latency count finish event.
63	RW	PERF_CONFIG_Reserved: Reserved.

Register Name	Debug0 Configuration Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.DEBUG0_CONFIG
Address	0000000005011288 (SCOM)
Description	Config register for trace-0 chain

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of trace-0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of trace-0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of trace-0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of trace-0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of trace-0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of trace-0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of trace-0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of trace-0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of trace-0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of trace-0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of trace-0.
55:62	RW	DEBUG0_CONFIG_Reserved1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock-gates for debug trace latches.

Register Name	Debug1 Configuration Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.DEBUG1_CONFIG
Address	0000000005011289 (SCOM)
Description	Config register for trace-1 chain

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of trace-1.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of trace-1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of trace-1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of trace-1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of trace-1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of trace-1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of trace-1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of trace-1.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of trace-1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of trace-1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of trace-1.
55:62	RW	DEBUG1_CONFIG_Reserved1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock-gates for debug trace latches.

Register Name	Brick 0 BDF2PE Configuration 0 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.BDF2PE_00_CONFIG
Address	000000000501128A (SCOM)
Description	to-PE map 0 Configured BDF-to-PE mapping #0 for brick 0 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_00_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1	RW	CONFIG_BDF2PE_00_WILDCARD: 0/1 = This BDF-to-PE mapping matches only this BDF/matches all BDFs.
2:3	RW	CONFIG_BDF2PE_00_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_00_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_00_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 0 BDF2PE Configuration 1 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.BDF2PE_01_CONFIG
Address	000000000501128B (SCOM)
Description	to-PE map 1 Configured BDF-to-PE mapping #1 for brick 0 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_01_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_01_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_01_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_01_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 0 BDF2PE Configuration 2 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.BDF2PE_02_CONFIG
Address	000000000501128C (SCOM)
Description	to-PE map 2 Configured BDF-to-PE mapping #2 for brick 0 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_02_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_02_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_02_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_02_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 1 BDF2PE Configuration 0 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.BDF2PE_10_CONFIG
Address	000000000501128D (SCOM)
Description	to-PE map 0 Configured BDF-to-PE mapping #0 for brick 1 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_10_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1	RW	CONFIG_BDF2PE_10_WILDCARD: 0/1 = This BDF-to-PE mapping matches only this BDF/matches all BDFs.
2:3	RW	CONFIG_BDF2PE_10_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_10_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_10_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 1 BDF2PE Configuration 1 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.BDF2PE_11_CONFIG
Address	000000000501128E (SCOM)
Description	to-PE map 1 Configured BDF-to-PE mapping #1 for brick 1 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_11_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_11_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_11_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_11_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 1 BDF2PE Configuration 2 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.BDF2PE_12_CONFIG
Address	000000000501128F (SCOM)
Description	to-PE map 2 Configured BDF-to-PE mapping #2 for brick 1 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_12_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_12_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_12_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_12_BDF: BDF (Bus-Device-Function) mapped to this PE.

Bits	SCOM	Field Mnemonic: Description
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	LPC Threshold Configuration Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.LPCTH_CONFIG
Address	0000000005011290 (SCOM)
Description	Threshold configuration register processor bus spec E.2 Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_LPCTH_BUSY_ENABLE: 0/1 = Disable thresholding/enable thresholding.
1:3	RW	CONFIG_LPCTH_WINDOW_SELECT: 001 = 256 cycle window. 010 = 512 cycle window. 100 = 1024 cycle window.
4:13	RW	CONFIG_LPCTH_THRESH_0: Busy counter threshold 0. When this threshold is exceeded, the LPC_th field in the partial response ATAG is set to '01'.
14:23	RW	CONFIG_LPCTH_THRESH_1: Busy counter threshold 1. When this threshold is exceeded, the LPC_th field in the partial response ATAG is set to '10'.
24:33	RW	CONFIG_LPCTH_THRESH_2: Busy counter threshold 2. When this threshold is exceeded, the LPC_th field in the partial response ATAG is set to '11'.
34:35	RW	CONFIG_LPCTH_Reserved1: Reserved. Note: This field can/should have different values in each instance. No MDials have been created for this field's IDials.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	Inhibit Configuration Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.INHIBIT_CONFIG
Address	0000000005011291 (SCOM)
Description	Configures Inhibits for CQ_CTL

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ0: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$. 12 = $1/2^{14}$. 13 = $1/2^{16}$. 14 = $1/2^{18}$. 15 = $1/2^{20}$.
4:5	RW	CONFIG_INHIBIT_PFREQ0: Selects pre frequency 0: 0 = SM0 timer tick. 1 = inverted SM0 timer tick. 2 = LFSR. 3 = inverted LFSR (-> 1/2, 3/4, 7/8, and so on).
6	RW	CONFIG_INHIBIT_BLOCKY0: 0/1 = Disable blocky mode / enable blocky mode.
7	RW	CONFIG_INHIBIT_ONESHOT0: 0/1 = Continuous mode / one-shot mode.
8:15	RW	CONFIG_INHIBIT_DEST0: Selects the destination of the inhibit.

Bits	SCOM	Field Mnemonic: Description
16:19	RW	CONFIG_INHIBIT_LFREQ1: Base LFSR frequency 0: 0..11 = $1/2^{(n+1)}$. 12 = $1/2^{14}$. 13 = $1/2^{16}$. 14 = $1/2^{18}$. 15 = $1/2^{20}$.
20:21	RW	CONFIG_INHIBIT_PFREQ1: Selects pre frequency 0: 0 = SM1 timer tick. 1 = inverted SM1 timer tick. 2 = LFSR. 3 = inverted LFSR (-> 1/2, 3/4, 7/8, ...).
22	RW	CONFIG_INHIBIT_BLOCKY1: 0/1 = Disable blocky mode / enable blocky mode.
23	RW	CONFIG_INHIBIT_ONESHOT1: 0/1 = Continus mode / one-shot mode.
24:31	RW	CONFIG_INHIBIT_DEST1: Selects the destination of the inhibit.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CQ_CTL Status Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CTL_STATUS
Address	0000000005011292 (SCOM)
Description	Status reporting register

Bits	SCOM	Field Mnemonic: Description
0	ROX	CTL_STATUS_SM_MMIO0: 1 when SM slice 0 has an MMIO pending.
1	ROX	CTL_STATUS_SM_MMIO1: 1 when SM slice 1 has an MMIO pending.
2	ROX	CTL_STATUS_SM_MMIO2: 1 when SM slice 2 has an MMIO pending.
3	ROX	CTL_STATUS_SM_MMIO3: 1 when SM slice 3 has an MMIO pending.
4:7	ROX	CTL_STATUS_MRBGP: Master-retry backoff level for Group-Pump commands.
8:11	ROX	CTL_STATUS_MRBSP: Master-retry backoff level for System-Pump commands.
12:15	ROX	CTL_STATUS_FENCE0: Brick-0 Fence sequencing state. 0b0000 = Idle state, completely unfenced. 0b1001 = Fenced state, fence sequencing complete. 0b1100 = Half-Fenced state, NTL is un-fenced. others = in transition between fenced and not-fenced.
16:19	ROX	CTL_STATUS_FENCE1: Brick-1 Fence sequencing state. 0b0000 = Idle state, completely unfenced. 0b1001 = Fenced state, fence sequencing complete. 0b1100 = Half-Fenced state, NTL is un-fenced. others = in transition between fenced and not-fenced.
20:21	ROX	CTL_STATUS_LPCTH: LPC-Threshold value driven in partial-responses.
22:26	ROX	CTL_STATUS_PBM_STATE: PB-MMIO/GenId state (0b00000 = Idle).
27	ROX	CTL_STATUS_BRK0_RLX: 1 when brick-0 Gen-Id/relaxed-ordering is idle.
28	ROX	CTL_STATUS_BRK1_RLX: 1 when brick-1 Gen-Id/relaxed-ordering is idle.
29	ROX	CTL_STATUS_BRK0_NVL: 1 when brick-0 NVLink-Flush is idle.
30	ROX	CTL_STATUS_BRK1_NVL: 1 when brick-1 NVLink-Flush is idle.
31	ROX	CTL_STATUS_ATS_SYNC: 1 when ATS-Sync is idle.

Bits	SCOM	Field Mnemonic: Description
32	ROX	CTL_STATUS_NMMU: 1 when NMMU outbound-message is idle.
33	ROX	CTL_STATUS_PBLN: 1 when outbound processor bus Ln-scope queue is empty.
34	ROX	CTL_STATUS_PBNNG: 1 when outbound processor bus Nn/G-scope queue is empty.
35	ROX	CTL_STATUS_PBRNVG: 1 when outbound processor bus Rn/Vg-scope queue is empty.
36	ROX	CTL_STATUS_NVREQ0: 1 when outbound brick 0 request queue is empty.
37	ROX	CTL_STATUS_NVDGD0: 1 when outbound brick 0 downgrade queue is empty.
38	ROX	CTL_STATUS_NVREQ1: 1 when outbound brick 1 request queue is empty.
39	ROX	CTL_STATUS_NVDGD1: 1 when outbound brick 1 downgrade queue is empty.
40	ROX	CTL_STATUS_ATSREQ: 1 when outbound ATS-TCE-Translate request queue is empty.
41	ROX	CTL_STATUS_MMIO: 1 when MMIO/GenId state machine is idle.
42	ROX	CTL_STATUS_PBRS: 1 when outbound PB-Response/Merge queue is empty.
43	ROX	CTL_STATUS_NVRS0: 1 when outbound brick 0 response queue is empty.
44	ROX	CTL_STATUS_NVRS1: 1 when outbound brick 0 response queue is empty.
45	ROX	CTL_STATUS_XARS: 1 when outbound ATS/MISC response queue is empty.
46	ROX	CTL_STATUS_ATRR: 1 when outbound ATR-Response logic is idle.
47	ROX	CTL_STATUS_Reserved1: Reserved.
48:63	RO	Constant = 0b0000000000000000

Register Name	CERR Message 0 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CERR_MESSAGE0
Address	0000000005011298 (SCOM)
Description	Error message/capture register 0

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS0: Reserved.

Register Name	CERR Message 1 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CERR_MESSAGE1
Address	0000000005011299 (SCOM)
Description	Error message/capture register 1

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	CERR_MESSAGE_BITS1: Reserved.

Register Name	CERR First 0 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CERR_FIRST0
Address	000000000501129A (SCOM)
Description	This register is read and write, write of a ‘1’ clears the bit.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_0: NCF0 SM0 NCF error.
1	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_1: NCF1 SM1 NCF error.
2	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_2: NCF2 SM2 NCF error.
3	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_3: NCF3 SM3 NCF error.
4	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_4: NCF4 (Reserved).
5	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_5: NCF5 (Reserved).
6	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_6: NCF6 (Reserved).
7	RWX_WCLEAR	IDIAL_CTL_FIRST_NCF_7: NCF7 (Reserved).
8	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_0: NVF0 SM0 NCF error.
9	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_1: NVF1 SM1 NCF error.
10	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_2: NVF2 SM2 NCF error.
11	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_3: NVF3 SM3 NCF error.
12	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_4: NVF4 Illegal Probe.MO: Probe.MO received with illegal ProbeState.
13	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_5: NVF5 Illegal Probe.N: Probe.N received with illegal ProbeState.
14	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_6: NVF6 Illegal Atomic: Illegal AtomicCmd for Atomic.NR with Red = 1.
15	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_7: NVF7 Illegal Atomic: Atomic.NR with Red = 0.
16	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_8: NVF8 Illegal Atomic: Atomic.NR with AtomicSize/ = 4 or 8 or with non-4/8 byte-enables.
17	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_9: NVF9 Illegal Atomic: Illegal AtomicCmd for Atomic.RR w/ Red = 0.
18	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_10: NVF10 Illegal Atomic: Illegal AtomicCmd for Atomic.RR w/ Red = 1.
19	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_11: NVF11 Illegal Atomic: Atomic.RR w/ AtomicSize/ = 4 or 8 or w/ non-4/8 byte-enables.
20	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_12: NVF12 Illegal ExCmd for command = ExCmd-CReq.
21	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_13: NVF13 Illegal ExCmd for command = ExCmd-ATR.
22	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_14: NVF14 Illegal command or RMW w/ illegal len.
23	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_15: NVF15 BDF-to-PE lookup failed.
24	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_16: NVF16 Received a 256 B FO = 1 Write.
25	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_17: NVF17 Received an invalid AddrType field - neither 00 or 11.
26	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_18: NVF18 Received an invalid transaction-ID in a NVLink response.
27	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_19: NVF19 Received a rsp_status of target-error in an ATSD response.
28	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_20: NVF20 Received a rsp_status of unsupported-request in an ATSD response.
29	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_21: NVF21 Received a rsp_status of '11' - Reserved value - in an ATSD response.
30	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_22: NVF22 Brick 0 NVF error occurred.
31	RWX_WCLEAR	IDIAL_CTL_FIRST_NVF_23: NVF23 Brick 1 NVF error occurred.
32	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_0: RSV10 (Reserved).
33	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_1: RSV11 (Reserved).
34	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_2: RSV12 (Reserved).
35	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV1_3: RSV13 (Reserved).
36	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_0: ASBE0 SM0 asbe error.

Bits	SCOM	Field Mnemonic: Description
37	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_1: ASBE1 SM1 asbe error.
38	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_2: ASBE2 SM2 asbe error.
39	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_3: ASBE3 SM3 asbe error.
40	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_4: ASBE4 processor bus MMIO Data Ecc CE Error.
41	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_5: ASBE5 (Reserved).
42	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_6: ASBE6 (Reserved).
43	RWX_WCLEAR	IDIAL_CTL_FIRST_ASBE_7: ASBE7 (Reserved).
44	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_0: PBR0 SM0 pbr error.
45	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_1: PBR1 SM1 pbr error.
46	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_2: PBR2 SM2 pbr error.
47	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_3: PBR3 SM3 pbr error.
48	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_4: PBR4 (Reserved).
49	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_5: PBR5 (Reserved).
50	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_6: PBR6 (Reserved).
51	RWX_WCLEAR	IDIAL_CTL_FIRST_PBR_7: PBR7 (Reserved).
52	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_0: REG0 SM0 reg error.
53	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_1: REG1 SM1 reg error.
54	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_2: REG2 SM2 reg error.
55	RWX_WCLEAR	IDIAL_CTL_FIRST_REG_3: REG3 SM3 reg error.
56	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_0: DUE0 processor bus MMIO Data Ecc UE Error.
57	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_1: DUE1 processor bus MMIO Data Ecc SUE Error.
58	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_2: DUE2 (Reserved).
59	RWX_WCLEAR	IDIAL_CTL_FIRST_DUE_3: DUE3 (Reserved).
60	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_0: PEF0 Brick 0 received a request to a frozen bdf/pe.
61	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_1: PEF1 Brick 1 received a request to a frozen bdf/pe.
62	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_2: PEF2 (Reserved).
63	RWX_WCLEAR	IDIAL_CTL_FIRST_PEF_3: PEF3 (Reserved).

Register Name	CERR First 1 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CERR_FIRST1
Address	0000000005011298 (SCOM)
Description	c_err_rpt first latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_0: NLG0 SM0 nlg error.
1	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_1: NLG1 SM1 nlg error.
2	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_2: NLG2 SM2 nlg error.
3	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_3: NLG3 SM3 nlg error.
4	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_4: NLG4 processor bus MMIO state machine invalid state.

Bits	SCOM	Field Mnemonic: Description
5	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_5: NLG5 buffer used for PB response before NTL finished writing data.
6	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_6: NLG6 buffer read before NTL finished writing data.
7	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_7: NLG7 Invalid state in dat-read state machine.
8	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_8: NLG8 Attempt to send NV Req with unknown NMCMD_ command type.
9	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_9: NLG9 Attempt to send NV Resp with unknown NRTYPE_ response type.
10	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_10: NLG10 Invalid state in XA-Response state machine.
11	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_11: NLG11 (Reserved).
12	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_12: NLG12 (Reserved).
13	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_13: NLG13 (Reserved).
14	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_14: NLG14 (Reserved).
15	RWX_WCLEAR	IDIAL_CTL_FIRST_NLG_15: NLG15 (Reserved).
16	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_0: FWD0 SM0 fwd error.
17	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_1: FWD1 SM1 fwd error.
18	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_2: FWD2 SM2 fwd error.
19	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_3: FWD3 SM3 fwd error.
20	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_4: FWD4 (Reserved).
21	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_5: FWD5 (Reserved).
22	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_6: FWD6 (Reserved).
23	RWX_WCLEAR	IDIAL_CTL_FIRST_FWD_7: FWD7 (Reserved).
24	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_0: AUE0 SM0 aue error.
25	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_1: AUE1 SM1 aue error.
26	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_2: AUE2 SM2 aue error.
27	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_3: AUE3 SM3 aue error.
28	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_4: AUE4 (Reserved).
29	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_5: AUE5 (Reserved).
30	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_6: AUE6 (Reserved).
31	RWX_WCLEAR	IDIAL_CTL_FIRST_AUE_7: AUE7 (Reserved).
32	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_0: PBP0 SM0 pbp error.
33	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_1: PBP1 SM1 pbp error.
34	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_2: PBP2 SM2 pbp error.
35	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_3: PBP3 SM3 pbp error.
36	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_4: PBP4 (Reserved).
37	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_5: PBP5 (Reserved).
38	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_6: PBP6 (Reserved).
39	RWX_WCLEAR	IDIAL_CTL_FIRST_PBP_7: PBP7 (Reserved).
40	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_0: PBF0 SM0 pbf error.
41	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_1: PBF1 SM1 pbf error.
42	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_2: PBF2 SM2 pbf error.
43	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_3: PBF3 SM3 pbf error.

Bits	SCOM	Field Mnemonic: Description
44	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_4: PBR4 (Reserved).
45	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_5: PBR5 (Reserved).
46	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_6: PBR6 (Reserved).
47	RWX_WCLEAR	IDIAL_CTL_FIRST_PBF_7: PBR7 (Reserved).
48	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_0: PBC0 SM0 pbc error.
49	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_1: PBC1 SM1 pbc error.
50	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_2: PBC2 SM2 pbc error.
51	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_3: PBC3 SM3 pbc error.
52	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_4: PBC4 (Reserved).
53	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_5: PBC5 (Reserved).
54	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_6: PBC6 (Reserved).
55	RWX_WCLEAR	IDIAL_CTL_FIRST_PBC_7: PBC7 (Reserved).
56	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_0: RSV20 SM0 rsv2 error.
57	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_1: RSV21 SM1 rsv2 error.
58	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_2: RSV22 SM2 rsv2 error.
59	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV2_3: RSV23 SM3 rsv2 error.
60	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_0: RSV30 (Reserved).
61	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_1: RSV31 (Reserved).
62	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_2: RSV32 (Reserved).
63	RWX_WCLEAR	IDIAL_CTL_FIRST_RSV3_3: RSV33 (Reserved).

Register Name	**CERR Mask 0 Register**
Mnemonic	NPU.STCK2.CS.CTL.MISC.CERR_MASK0
Address	000000000501129C (SCOM)
Description	c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_CTL_MASK_NCF_0: NCF0 SM0 ncf error.
1	RW	IDIAL_CTL_MASK_NCF_1: NCF1 SM1 ncf error.
2	RW	IDIAL_CTL_MASK_NCF_2: NCF2 SM2 ncf error.
3	RW	IDIAL_CTL_MASK_NCF_3: NCF3 SM3 ncf error.
4	RW	IDIAL_CTL_MASK_NCF_4: NCF4 (Reserved).
5	RW	IDIAL_CTL_MASK_NCF_5: NCF5 (Reserved).
6	RW	IDIAL_CTL_MASK_NCF_6: NCF6 (Reserved).
7	RW	IDIAL_CTL_MASK_NCF_7: NCF7 (Reserved).
8	RW	IDIAL_CTL_MASK_NVF_0: NVF0 SM0 nvf error.
9	RW	IDIAL_CTL_MASK_NVF_1: NVF1 SM1 nvf error.
10	RW	IDIAL_CTL_MASK_NVF_2: NVF2 SM2 nvf error.

Bits	SCOM	Field Mnemonic: Description
11	RW	IDIAL_CTL_MASK_NVF_3: NVF3 SM3 nvf error.
12	RW	IDIAL_CTL_MASK_NVF_4: NVF4 Illegal Probe.MO: Probe.MO received with illegal ProbeState.
13	RW	IDIAL_CTL_MASK_NVF_5: NVF5 Illegal Probe.N: Probe.N received with illegal ProbeState.
14	RW	IDIAL_CTL_MASK_NVF_6: NVF6 Illegal Atomic: Illegal AtomicCmd for Atomic.NR w/ Red = 1.
15	RW	IDIAL_CTL_MASK_NVF_7: NVF7 Illegal Atomic: Atomic.NR w/ Red = 0.
16	RW	IDIAL_CTL_MASK_NVF_8: NVF8 Illegal Atomic: Atomic.NR w/ AtomicSize/ = 4 or 8 or w/ non-4/8 byte-enables.
17	RW	IDIAL_CTL_MASK_NVF_9: NVF9 Illegal Atomic: Illegal AtomicCmd for Atomic.RR w/ Red = 0.
18	RW	IDIAL_CTL_MASK_NVF_10: NVF10 Illegal Atomic: Illegal AtomicCmd for Atomic.RR w/ Red = 1.
19	RW	IDIAL_CTL_MASK_NVF_11: NVF11 Illegal Atomic: Atomic.RR w/ AtomicSize/ = 4 or 8 or w/ non-4/8 byte-enables.
20	RW	IDIAL_CTL_MASK_NVF_12: NVF12 Illegal ExCmd for command = ExCmd-CReq.
21	RW	IDIAL_CTL_MASK_NVF_13: NVF13 Illegal ExCmd for command = ExCmd-ATR.
22	RW	IDIAL_CTL_MASK_NVF_14: NVF14 Illegal command or RMW w/ illegal len.
23	RW	IDIAL_CTL_MASK_NVF_15: NVF15 BDF-to-PE lookup failed.
24	RW	IDIAL_CTL_MASK_NVF_16: NVF16 Received a 256B FO = 1 Write.
25	RW	IDIAL_CTL_MASK_NVF_17: NVF17 Received an invalid AddrType field - neither 00 or 11.
26	RW	IDIAL_CTL_MASK_NVF_18: NVF18 Received an invalid transaction-ID in a NVLink response.
27	RW	IDIAL_CTL_MASK_NVF_19: NVF19 Received a rsp_status of target-error in an ATSD response.
28	RW	IDIAL_CTL_MASK_NVF_20: NVF20 Received a rsp_status of unsupported-request in an ATSD response.
29	RW	IDIAL_CTL_MASK_NVF_21: NVF21 Received a rsp_status of '11' - Reserved value - in an ATSD response.
30	RW	IDIAL_CTL_MASK_NVF_22: NVF22 Brick 0 NVF error occurred.
31	RW	IDIAL_CTL_MASK_NVF_23: NVF23 Brick 1 NVF error occurred.
32	RW	IDIAL_CTL_MASK_RSV1_0: RSV10 (Reserved).
33	RW	IDIAL_CTL_MASK_RSV1_1: RSV11 (Reserved).
34	RW	IDIAL_CTL_MASK_RSV1_2: RSV12 (Reserved).
35	RW	IDIAL_CTL_MASK_RSV1_3: RSV13 (Reserved).
36	RW	IDIAL_CTL_MASK_ASBE_0: ASBE0 SM0 asbe error.
37	RW	IDIAL_CTL_MASK_ASBE_1: ASBE1 SM1 asbe error.
38	RW	IDIAL_CTL_MASK_ASBE_2: ASBE2 SM2 asbe error.
39	RW	IDIAL_CTL_MASK_ASBE_3: ASBE3 SM3 asbe error.
40	RW	IDIAL_CTL_MASK_ASBE_4: ASBE4 processor bus MMIO Data Ecc CE Error.
41	RW	IDIAL_CTL_MASK_ASBE_5: ASBE5 (Reserved).
42	RW	IDIAL_CTL_MASK_ASBE_6: ASBE6 (Reserved).
43	RW	IDIAL_CTL_MASK_ASBE_7: ASBE7 (Reserved).
44	RW	IDIAL_CTL_MASK_PBR_0: PBR0 SM0 pbr error.
45	RW	IDIAL_CTL_MASK_PBR_1: PBR1 SM1 pbr error.
46	RW	IDIAL_CTL_MASK_PBR_2: PBR2 SM2 pbr error.
47	RW	IDIAL_CTL_MASK_PBR_3: PBR3 SM3 pbr error.
48	RW	IDIAL_CTL_MASK_PBR_4: PBR4 (Reserved).

Bits	SCOM	Field Mnemonic: Description
49	RW	IDIAL_CTL_MASK_PBR_5: PBR5 (Reserved).
50	RW	IDIAL_CTL_MASK_PBR_6: PBR6 (Reserved).
51	RW	IDIAL_CTL_MASK_PBR_7: PBR7 (Reserved).
52	RW	IDIAL_CTL_MASK_REG_0: REG0 SM0 reg error.
53	RW	IDIAL_CTL_MASK_REG_1: REG1 SM1 reg error.
54	RW	IDIAL_CTL_MASK_REG_2: REG2 SM2 reg error.
55	RW	IDIAL_CTL_MASK_REG_3: REG3 SM3 reg error.
56	RW	IDIAL_CTL_MASK_DUE_0: DUE0 processor bus MMIO Data Ecc UE Error.
57	RW	IDIAL_CTL_MASK_DUE_1: DUE1 processor bus MMIO Data Ecc SUE Error.
58	RW	IDIAL_CTL_MASK_DUE_2: DUE2 (Reserved).
59	RW	IDIAL_CTL_MASK_DUE_3: DUE3 (Reserved).
60	RW	IDIAL_CTL_MASK_PEF_0: PEF0 Brick 0 received a request to a frozen bdf/pe.
61	RW	IDIAL_CTL_MASK_PEF_1: PEF1 Brick 1 received a request to a frozen bdf/pe.
62	RW	IDIAL_CTL_MASK_PEF_2: PEF2 (Reserved).
63	RW	IDIAL_CTL_MASK_PEF_3: PEF3 (Reserved).

Register Name	**CERR Mask 1 Register**
Mnemonic	NPU.STCK2.CS.CTL.MISC.CERR_MASK1
Address	000000000501129D (SCOM)
Description	c_err_rpt mask reg Note: This register should be set to the same value globally.

Bits	SCOM	Field Mnemonic: Description
0	RW	IDIAL_CTL_MASK_NLG_0: NLG0 SM0 nlg error.
1	RW	IDIAL_CTL_MASK_NLG_1: NLG1 SM1 nlg error.
2	RW	IDIAL_CTL_MASK_NLG_2: NLG2 SM2 nlg error.
3	RW	IDIAL_CTL_MASK_NLG_3: NLG3 SM3 nlg error.
4	RW	IDIAL_CTL_MASK_NLG_4: NLG4 processor bus MMIO state machine invalid state.
5	RW	IDIAL_CTL_MASK_NLG_5: NLG5 buffer used for PB response before NTL finished writing data.
6	RW	IDIAL_CTL_MASK_NLG_6: NLG6 buffer read before NTL finished writing data.
7	RW	IDIAL_CTL_MASK_NLG_7: NLG7 Invalid state in dat-read state machine.
8	RW	IDIAL_CTL_MASK_NLG_8: NLG8 Attempt to send NV Req with unknown NMCMD_ command type.
9	RW	IDIAL_CTL_MASK_NLG_9: NLG9 Attempt to send NV Resp with unknown NRTYPE_ response type.
10	RW	IDIAL_CTL_MASK_NLG_10: NLG10 Invalid state in XA-Response state machine.
11	RW	IDIAL_CTL_MASK_NLG_11: NLG11 (Reserved).
12	RW	IDIAL_CTL_MASK_NLG_12: NLG12 (Reserved).
13	RW	IDIAL_CTL_MASK_NLG_13: NLG13 (Reserved).
14	RW	IDIAL_CTL_MASK_NLG_14: NLG14 (Reserved).
15	RW	IDIAL_CTL_MASK_NLG_15: NLG15 (Reserved).

Bits	SCOM	Field Mnemonic: Description
16	RW	IDIAL_CTL_MASK_FWD_0: FWD0 SM0 fwd error.
17	RW	IDIAL_CTL_MASK_FWD_1: FWD1 SM1 fwd error.
18	RW	IDIAL_CTL_MASK_FWD_2: FWD2 SM2 fwd error.
19	RW	IDIAL_CTL_MASK_FWD_3: FWD3 SM3 fwd error.
20	RW	IDIAL_CTL_MASK_FWD_4: FWD4 (Reserved).
21	RW	IDIAL_CTL_MASK_FWD_5: FWD5 (Reserved).
22	RW	IDIAL_CTL_MASK_FWD_6: FWD6 (Reserved).
23	RW	IDIAL_CTL_MASK_FWD_7: FWD7 (Reserved).
24	RW	IDIAL_CTL_MASK_AUE_0: AUE0 SM0 aue error.
25	RW	IDIAL_CTL_MASK_AUE_1: AUE1 SM1 aue error.
26	RW	IDIAL_CTL_MASK_AUE_2: AUE2 SM2 aue error.
27	RW	IDIAL_CTL_MASK_AUE_3: AUE3 SM3 aue error.
28	RW	IDIAL_CTL_MASK_AUE_4: AUE4 (Reserved).
29	RW	IDIAL_CTL_MASK_AUE_5: AUE5 (Reserved).
30	RW	IDIAL_CTL_MASK_AUE_6: AUE6 (Reserved).
31	RW	IDIAL_CTL_MASK_AUE_7: AUE7 (Reserved).
32	RW	IDIAL_CTL_MASK_PBP_0: PBP0 SM0 pbp error.
33	RW	IDIAL_CTL_MASK_PBP_1: PBP1 SM1 pbp error.
34	RW	IDIAL_CTL_MASK_PBP_2: PBP2 SM2 pbp error.
35	RW	IDIAL_CTL_MASK_PBP_3: PBP3 SM3 pbp error.
36	RW	IDIAL_CTL_MASK_PBP_4: PBP4 (Reserved).
37	RW	IDIAL_CTL_MASK_PBP_5: PBP5 (Reserved).
38	RW	IDIAL_CTL_MASK_PBP_6: PBP6 (Reserved).
39	RW	IDIAL_CTL_MASK_PBP_7: PBP7 (Reserved).
40	RW	IDIAL_CTL_MASK_PBF_0: PBF0 SM0 pbf error.
41	RW	IDIAL_CTL_MASK_PBF_1: PBF1 SM1 pbf error.
42	RW	IDIAL_CTL_MASK_PBF_2: PBF2 SM2 pbf error.
43	RW	IDIAL_CTL_MASK_PBF_3: PBF3 SM3 pbf error.
44	RW	IDIAL_CTL_MASK_PBF_4: PBR4 (Reserved).
45	RW	IDIAL_CTL_MASK_PBF_5: PBR5 (Reserved).
46	RW	IDIAL_CTL_MASK_PBF_6: PBR6 (Reserved).
47	RW	IDIAL_CTL_MASK_PBF_7: PBR7 (Reserved).
48	RW	IDIAL_CTL_MASK_PBC_0: PBC0 SM0 pbc error.
49	RW	IDIAL_CTL_MASK_PBC_1: PBC1 SM1 pbc error.
50	RW	IDIAL_CTL_MASK_PBC_2: PBC2 SM2 pbc error.
51	RW	IDIAL_CTL_MASK_PBC_3: PBC3 SM3 pbc error.
52	RW	IDIAL_CTL_MASK_PBC_4: PBC4 (Reserved).
53	RW	IDIAL_CTL_MASK_PBC_5: PBC5 (Reserved).
54	RW	IDIAL_CTL_MASK_PBC_6: PBC6 (Reserved).

Bits	SCOM	Field Mnemonic: Description
55	RW	IDIAL_CTL_MASK_PBC_7: PBC7 (Reserved).
56	RW	IDIAL_CTL_MASK_RSV2_0: RSV20 SM0 rsv2 error.
57	RW	IDIAL_CTL_MASK_RSV2_1: RSV21 SM1 rsv2 error.
58	RW	IDIAL_CTL_MASK_RSV2_2: RSV22 SM2 rsv2 error.
59	RW	IDIAL_CTL_MASK_RSV2_3: RSV23 SM3 rsv2 error.
60	RW	IDIAL_CTL_MASK_RSV3_0: RSV30 (Reserved).
61	RW	IDIAL_CTL_MASK_RSV3_1: RSV31 (Reserved).
62	RW	IDIAL_CTL_MASK_RSV3_2: RSV32 (Reserved).
63	RW	IDIAL_CTL_MASK_RSV3_3: RSV33 (Reserved).

Register Name	CERR Hold 0 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CERR_HOLD0
Address	000000000501129E (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_0: NCF0 SM0 ncf error.
1	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_1: NCF1 SM1 ncf error.
2	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_2: NCF2 SM2 ncf error.
3	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_3: NCF3 SM3 ncf error.
4	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_4: NCF4 (Reserved).
5	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_5: NCF5 (Reserved).
6	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_6: NCF6 (Reserved).
7	RWX_WCLRREG	IDIAL_CTL_HOLD_NCF_7: NCF7 (Reserved).
8	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_0: NVF0 SM0 nvf error.
9	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_1: NVF1 SM1 nvf error.
10	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_2: NVF2 SM2 nvf error.
11	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_3: NVF3 SM3 nvf error.
12	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_4: NVF4 Illegal Probe.MO: Probe.MO received with illegal ProbeState.
13	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_5: NVF5 Illegal Probe.N: Probe.N received with illegal ProbeState.
14	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_6: NVF6 Illegal Atomic: Illegal AtomicCmd for Atomic.NR w/ Red = 1.
15	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_7: NVF7 Illegal Atomic: Atomic.NR w/ Red = 0.
16	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_8: NVF8 Illegal Atomic: Atomic.NR w/ AtomicSize/ = 4 or 8 or w/ non-4/8 byte-enables.
17	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_9: NVF9 Illegal Atomic: Illegal AtomicCmd for Atomic.RR w/ Red = 0.
18	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_10: NVF10 Illegal Atomic: Illegal AtomicCmd for Atomic.RR w/ Red = 1.
19	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_11: NVF11 Illegal Atomic: Atomic.RR w/ AtomicSize/ = 4 or 8 or w/ non-4/8 byte-enables.
20	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_12: NVF12 Illegal ExCmd for command = ExCmd-CReq.
21	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_13: NVF13 Illegal ExCmd for command = ExCmd-ATR.

Bits	SCOM	Field Mnemonic: Description
22	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_14: NVF14 Illegal command or RMW w/ illegal len.
23	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_15: NVF15 BDF-to-PE lookup failed.
24	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_16: NVF16 Received a 256B FO = 1 Write.
25	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_17: NVF17 Received an invalid AddrType field - neither 00 or 11.
26	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_18: NVF18 Received an invalid transaction-ID in a NVLink response.
27	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_19: NVF19 Received a rsp_status of target-error in an ATSD response.
28	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_20: NVF20 Received a rsp_status of unsupported-request in an ATSD response.
29	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_21: NVF21 Received a rsp_status of '11' - Reserved value - in an ATSD response.
30	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_22: NVF22 Brick 0 NVF error occurred.
31	RWX_WCLRREG	IDIAL_CTL_HOLD_NVF_23: NVF23 Brick 1 NVF error occurred.
32	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_0: RSV10 (Reserved).
33	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_1: RSV11 (Reserved).
34	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_2: RSV12 (Reserved).
35	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV1_3: RSV13 (Reserved).
36	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_0: ASBE0 SM0 asbe error.
37	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_1: ASBE1 SM1 asbe error.
38	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_2: ASBE2 SM2 asbe error.
39	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_3: ASBE3 SM3 asbe error.
40	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_4: ASBE4 processor bus MMIO Data Ecc CE Error.
41	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_5: ASBE5 (Reserved).
42	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_6: ASBE6 (Reserved).
43	RWX_WCLRREG	IDIAL_CTL_HOLD_ASBE_7: ASBE7 (Reserved).
44	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_0: PBR0 SM0 pbr error.
45	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_1: PBR1 SM1 pbr error.
46	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_2: PBR2 SM2 pbr error.
47	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_3: PBR3 SM3 pbr error.
48	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_4: PBR4 (Reserved).
49	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_5: PBR5 (Reserved).
50	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_6: PBR6 (Reserved).
51	RWX_WCLRREG	IDIAL_CTL_HOLD_PBR_7: PBR7 (Reserved).
52	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_0: REG0 SM0 reg error.
53	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_1: REG1 SM1 reg error.
54	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_2: REG2 SM2 reg error.
55	RWX_WCLRREG	IDIAL_CTL_HOLD_REG_3: REG3 SM3 reg error.
56	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_0: DUE0 processor bus MMIO Data Ecc UE Error.
57	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_1: DUE1 processor bus MMIO Data Ecc SUE Error.
58	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_2: DUE2 (Reserved).
59	RWX_WCLRREG	IDIAL_CTL_HOLD_DUE_3: DUE3 (Reserved).

Bits	SCOM	Field Mnemonic: Description
60	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_0: PEF0 Brick 0 received a request to a frozen bdf/pe.
61	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_1: PEF1 Brick 1 received a request to a frozen bdf/pe.
62	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_2: PEF2 (Reserved).
63	RWX_WCLRREG	IDIAL_CTL_HOLD_PEF_3: PEF3 (Reserved).

Register Name	CERR Hold 1 Register
Mnemonic	NPU.STCK2.CS.CTL.MISC.CERR_HOLD1
Address	000000000501129F (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_0: NLG0 SM0 nlg error.
1	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_1: NLG1 SM1 nlg error.
2	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_2: NLG2 SM2 nlg error.
3	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_3: NLG3 SM3 nlg error.
4	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_4: NLG4 processor bus MMIO state machine invalid state.
5	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_5: NLG5 buffer used for PB response before NTL finished writing data.
6	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_6: NLG6 buffer read before NTL finished writing data.
7	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_7: NLG7 Invalid state in dat-read state machine.
8	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_8: NLG8 Attempt to send NV Req with unknown NMCMD_ command type.
9	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_9: NLG9 Attempt to send NV Resp with unknown NRTYPE_ response type.
10	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_10: NLG10 Invalid state in XA-Response state machine.
11	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_11: NLG11 (Reserved).
12	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_12: NLG12 (Reserved).
13	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_13: NLG13 (Reserved).
14	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_14: NLG14 (Reserved).
15	RWX_WCLRREG	IDIAL_CTL_HOLD_NLG_15: NLG15 (Reserved).
16	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_0: FWD0 SM0 fwd error.
17	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_1: FWD1 SM1 fwd error.
18	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_2: FWD2 SM2 fwd error.
19	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_3: FWD3 SM3 fwd error.
20	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_4: FWD4 (Reserved).
21	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_5: FWD5 (Reserved).
22	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_6: FWD6 (Reserved).
23	RWX_WCLRREG	IDIAL_CTL_HOLD_FWD_7: FWD7 (Reserved).
24	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_0: AUE0 SM0 aue error.
25	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_1: AUE1 SM1 aue error.
26	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_2: AUE2 SM2 aue error.
27	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_3: AUE3 SM3 aue error.

Bits	SCOM	Field Mnemonic: Description
28	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_4: AUE4 (Reserved).
29	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_5: AUE5 (Reserved).
30	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_6: AUE6 (Reserved).
31	RWX_WCLRREG	IDIAL_CTL_HOLD_AUE_7: AUE7 (Reserved).
32	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_0: PBP0 SM0 pbp error.
33	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_1: PBP1 SM1 pbp error.
34	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_2: PBP2 SM2 pbp error.
35	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_3: PBP3 SM3 pbp error.
36	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_4: PBP4 (Reserved).
37	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_5: PBP5 (Reserved).
38	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_6: PBP6 (Reserved).
39	RWX_WCLRREG	IDIAL_CTL_HOLD_PBP_7: PBP7 (Reserved).
40	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_0: PBF0 SM0 pbf error.
41	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_1: PBF1 SM1 pbf error.
42	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_2: PBF2 SM2 pbf error.
43	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_3: PBF3 SM3 pbf error.
44	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_4: PBR4 (Reserved).
45	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_5: PBR5 (Reserved).
46	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_6: PBR6 (Reserved).
47	RWX_WCLRREG	IDIAL_CTL_HOLD_PBF_7: PBR7 (Reserved).
48	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_0: PBC0 SM0 pbc error.
49	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_1: PBC1 SM1 pbc error.
50	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_2: PBC2 SM2 pbc error.
51	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_3: PBC3 SM3 pbc error.
52	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_4: PBC4 (Reserved).
53	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_5: PBC5 (Reserved).
54	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_6: PBC6 (Reserved).
55	RWX_WCLRREG	IDIAL_CTL_HOLD_PBC_7: PBC7 (Reserved).
56	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_0: RSV20 SM0 rsv2 error.
57	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_1: RSV21 SM1 rsv2 error.
58	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_2: RSV22 SM2 rsv2 error.
59	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV2_3: RSV23 SM3 rsv2 error.
60	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_0: RSV30 (Reserved).
61	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_1: RSV31 (Reserved).
62	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_2: RSV32 (Reserved).
63	RWX_WCLRREG	IDIAL_CTL_HOLD_RSV3_3: RSV33 (Reserved).

Register Name	CQ_DAT Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK2.DAT.MISC.CONFIG1
Address	00000000050112A1 (SCOM)
Description	CQ_DAT Misc configuration register #1

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG1_MGR_CREDIT: CTL->DAT merge request interface number of credits.
2:4	RW	CONFIG1_MRG_PBTX_NBUF: CTL->DAT merge request Powerbus TX interface logic request buffer size.
5:8	RW	CONFIG1_MRG_RDBF_NBUF: CTL->DAT merge request Powerbus TX array read logic request buffer size.
9:12	RW	CONFIG1_MRG_IBWR_NBUF: CTL->DAT merge request BE merge/OI-loopback/AMO I-buf write logic request buffer size.
13:15	RW	CONFIG1_MRG_IBRD_NBUF: CTL->DAT merge request BE merge/IO-loopback/AMO I-buf read logic request buffer size.
16:18	RW	CONFIG1_MRG_BBRD_NBUF: CTL->DAT merge request BE merge B-buf read logic request buffer size.
19:21	RW	CONFIG1_MRG_OBRD_NBUF: CTL->DAT merge request BE merge/OI-loopback/AMO O-buf read logic request buffer size.
22	RW	CONFIG1_MRG_CR_DIS: Writing a 1 disables CQ_DAT to send credits to CTL for merge operations.
23	RW	CONFIG1_MRG_CTLW_CR_DIS: Writing a 1 disables CQ_DAT to send credits to CTL for inbound buffer write operations.
24:25	RW	CONFIG1_NTLR_PAUSE_THRESH: Specifies number of O-buf NTL port occupation cycles before raising NTL pause request(00b = > 32cyc, 01b = > 16cyc, 10b = > 8cyc, 11b = > never).
26:27	RW	CONFIG1_CTLR_HP_THRESH: Specifies number of O-buf CTL read wait cycles before giving high priority(00b = > 16cyc, 01b = > 8cyc, 10b = > 4cyc, 11b = > never).
28:29	RW	CONFIG1_NTLW_PAUSE_THRESH: Specifies number of I-buf NTL port occupation cycles before raising NTL pause request(00b = > 16cyc, 01b = > 8cyc, 10b = > 4cyc, 11b = > never).
30:31	RW	CONFIG1_CTLW_HP_THRESH: Specifies number of I-buf CTL write wait cycles before giving high priority(00b = > 16cyc, 01b = > 8cyc, 10b = > 4cyc, 11b = > never).
32	RW	CONFIG1_PBTX_REDUCE_RTAG: Writing a 1 have CQ_DAT limit number of outstanding RTAGs to 1 on PB transmit interface (default is 2).
33	RW	CONFIG1_PBTX_DELAY_BDONE: Writing a 1 have CQ_DAT PB transmit logic wait until all the OW is presented on the PB before raising buffdone to CTL.
34	RW	CONFIG1_PBTX_FLIP_IMIN_BIG: Writing a 1 have CQ_DAT PB transmit logic flip the endian of the integer minimum value on failed inc/dec when e = 0 is specified.
35	RW	CONFIG1_PBTX_FLIP_IMIN_LITTLE: Writing a 1 have CQ_DAT PB transmit logic flip the endian of the integer minimum value on failed inc/dec when e = 1 is specified.
36	RW	CONFIG1_ALU_SAFE_LATENCY: Writing a 1 have CQ_DAT wait for 1 more cycle for ALU output in case x2 phase detection logic goes wrong.
37	RW	CONFIG1_ALU_FLIP_ENDIAN_BIG: Writing a 1 have CQ_DAT flip the ALU endian when e = 0 is specified.
38	RW	CONFIG1_ALU_FLIP_ENDIAN_LITTLE: Writing a 1 have CQ_DAT flip the ALU endian when e = 1 is specified.
39	RW	CONFIG1_PBTX_EARLY_AFTAG: Writing a 1 have CQ_DAT raise buffdone to CTL earlier for armwf_* operations. CQ_DAT does not wait for fetch data to be presented on the PB. However CQ_DAT does wait for fetch data to leave the I-buf that is, the buffer entry can still be safely reused. This bit can be randomized in verification.
40:63	RW	CONFIG1_Reserved1: Reserved.

Register Name	CQ_DAT ECC Configuration Register
Mnemonic	NPU.STCK2.DAT.MISC.ECC_CONFIG
Address	00000000050112A2 (SCOM)
Description	CQ_DAT ECC configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	ECC_CONFIG_PBTX_AMO_IGNORE_XUE: For armwf_inc/dec ttypes, replace PB transmit data with negative max value when comparison fails, even if the data has UE or SUE. The negative max value will be marked with SUE as long as suedis_pt = 0.
1	RW	ECC_CONFIG_SUE_DIS_BR_PERR: Writing a 1 disables marking merge result data with SUE when BE-buf read data latch has parity error.
2	RW	ECC_CONFIG_SUE_DIS_IR_PERR: Writing a 1 disables marking merge result data with SUE when Inbound-buf read data latch has parity error.
3	RW	ECC_CONFIG_SUE_DIS_OR_PERR: Writing a 1 disables marking merge result data with SUE when Outbound-buf read data latch has parity error.
4	RW	ECC_CONFIG_CORR_DIS_PT: Writing a 1 disables ECC correction in Power Bus TX.
5	RW	ECC_CONFIG_CORR_DIS_PR: Writing a 1 disables ECC correction in Power Bus RX.
6	RW	ECC_CONFIG_CORR_DIS_BR: Writing a 1 disables ECC correction in Byte Enable buffer read.
7	RW	ECC_CONFIG_CORR_DIS_IR: Writing a 1 disables ECC correction in Merge operation inbound buffer read.
8	RW	ECC_CONFIG_CORR_DIS_OR: Writing a 1 disables ECC correction in Merge operation outbound buffer read.
9	RW	ECC_CONFIG_SUE_DIS_PT: Writing a 1 disables converting ECC UE to SUE in Power Bus TX.
10	RW	ECC_CONFIG_SUE_DIS_PR: Writing a 1 disables converting ECC UE to SUE in Power Bus RX.
11	RW	ECC_CONFIG_SUE_DIS_BR: Writing a 1 disables converting ECC UE to SUE in Byte Enable buffer read.
12	RW	ECC_CONFIG_SUE_DIS_IR: Writing a 1 disables converting ECC UE to SUE in Merge operation inbound buffer read.
13	RW	ECC_CONFIG_SUE_DIS_OR: Writing a 1 disables converting ECC UE to SUE in Merge operation outbound buffer read.
14:31	RW	ECC_CONFIG_Reserved: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CQ_DAT Scratch 0 Register
Mnemonic	NPU.STCK2.DAT.MISC.SCRATCH0
Address	00000000050112A3 (SCOM)
Description	CQ_DAT Scratch Register 0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	SCRATCH0_IDIAL: Scratch register.

Register Name	CQ_DAT CERR ECC Hold Register
Mnemonic	NPU.STCK2.DAT.MISC.CERR_ECC_HOLD
Address	00000000050112A4 (SCOM)
Description	CQ_DAT ECC error c_err_rpt status and clear register

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:13	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PT_UE: ECC ue on Power Bus TX data path (4 ECC words).
14:17	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PR_UE: ECC ue on Power Bus RX data path (4 ECC words).
18:19	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_BR_UE: ECC ue on Byte Enable buffer read data path (2 ECC words).
20:23	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_IR_UE: ECC ue on Merge operation inbound buffer read data path (4 ECC words).
24:27	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_OR_UE: ECC ue on Merge operation outbound buffer read data path (4 ECC words).
28:31	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PT_SUE: ECC sue on Power Bus TX data path (4 ECC words).
32:35	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PR_SUE: ECC sue on Power Bus RX data path (4 ECC words).
36:37	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_BR_SUE: ECC sue on Byte Enable buffer read data path (2 ECC words).
38:41	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_IR_SUE: ECC sue on Merge operation inbound buffer read data path (4 ECC words).
42:45	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_OR_SUE: ECC sue on Merge operation outbound buffer read data path (4 ECC words).
46:49	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PT_CE: ECC ce on Power Bus TX data path (4 ECC words).
50:53	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_PR_CE: ECC ce on Power Bus RX data path (4 ECC words).
54:55	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_BR_CE: ECC ce on Byte Enable buffer read data path (2 ECC words).
56:59	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_IR_CE: ECC ce on Merge operation inbound buffer read data path (4 ECC words).
60:63	RWX_WCLEAR	IDIAL_CERR_ECC_HOLD_OR_CE: ECC ce on Merge operation outbound buffer read data path (4 ECC words).

Register Name	CQ_DAT CERR ECC Mask Register
Mnemonic	NPU.STCK2.DAT.MISC.CERR_ECC_MASK
Address	00000000050112A5 (SCOM)
Description	CQ_DAT ECC error c_err_rpt mask register

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:63	RW	CERR_ECC_MASK_BITS: CQ_DAT ECC error c_err_rpt mask bits.

Register Name	CQ_DAT CERR ECC First Register
Mnemonic	NPU.STCK2.DAT.MISC.CERR_ECC_FIRST
Address	00000000050112A6 (SCOM)
Description	CQ_DAT ECC error c_err_rpt first register

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:63	RWX_WCLEAR	CERR_ECC_FIRST_BITS: CQ_DAT ECC error c_err_rpt first error bits.

Register Name	CQ_DAT CERR Parity Hold Register
Mnemonic	NPU.STCK2.DAT.MISC.CERR_PTY_HOLD
Address	00000000050112A7 (SCOM)
Description	CQ_DAT parity error c_err_rpt status and clear register

Bits	SCOM	Field Mnemonic: Description
0:36	RO	Constant = 0b000000000000000000000000000000000000
37	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_INHIBIT_CONFIG: Parity error on inhibit configuration register.
38	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_MISC_STATE: Parity error on critical state latches in the miscellaneous subunit.
39	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_MRG_STATE: Parity error on critical state latches in the merge subunit.
40	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_OBUF_STATE: Parity error on critical state latches in the O-buf subunit.
41	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_PBTX_STATE: Parity error on critical state latches in the PB transmit subunit.
42	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_RQIN_STATE: Parity error on critical state latches in the merge request buffer subunit.
43	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_IBUF_STATE: Parity error on critical state latches in the I-buf subunit.
44	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_ERRINJ: Parity error on ecc_errinj register.
45:48	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_PBTX_AMO: Parity error in PB transmit AMO inc/dec data path (4 words).
49:52	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_IBRD: Parity error in Merge operation inbound buffer read data path (4 words).
53:56	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_OBRD: Parity error in Merge operation outbound buffer read data path (4 words).
57:58	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_BBRD: Parity error in Byte enable buffer read data path (2 words).
59	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_PBRX_RTAG: Parity error on received RTAG on the PB receive interface.
60	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_ECC_CONFIG: Parity error on ecc_config register.
61	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_CONFIG1: Parity error on config1 register.
62	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_DEBUG0_CONFIG: Parity error on debug0_config register.
63	RWX_WCLEAR	IDIAL_CERR_PTY_HOLD_DEBUG1_CONFIG: Parity error on debug1_config register.

Register Name	CQ_DAT CERR Parity Mask Register
Mnemonic	NPU.STCK2.DAT.MISC.CERR_PTY_MASK
Address	00000000050112A8 (SCOM)
Description	CQ_DAT parity error c_err_rpt mask register

Bits	SCOM	Field Mnemonic: Description
0:36	RO	Constant = 0b000000000000000000000000000000000000
37:63	RW	CERR_PTY_MASK_BITS: CQ_DAT parity error c_err_rpt mask bits.

Register Name	CQ_DAT CERR Parity First Register
Mnemonic	NPU.STCK2.DAT.MISC.CERR_PTY_FIRST
Address	00000000050112A9 (SCOM)
Description	CQ_DAT parity error c_err_rpt first register

Bits	SCOM	Field Mnemonic: Description
0:36	RO	Constant = 0b00000000000000000000000000000000000000
37:63	RWX_WCLEAR	CERR_PTY_FIRST_BITS: CQ_DAT parity error c_err_rpt first error bits.

Register Name	CQ_DAT CERR Logic Hold Register
Mnemonic	NPU.STCK2.DAT.MISC.CERR_LOG_HOLD
Address	00000000050112AA (SCOM)
Description	CQ_DAT logic error c_err_rpt status and clear register

Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b00000000000000000000000000000000000000000000000
47	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_BBUF_RDWR: Logic error: Read-write conflict on B-buf, the same buffer entry was read and written in the same cycle.
48	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_RDWR: Logic error: Read-write conflict on I-buf, the same buffer entry was read and written in the same cycle.
49	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_OBUF_RDWR: Logic error: Read-write conflict on O-buf, the same buffer entry was read and written in the same cycle.
50:55	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_RQIN_OVF: Logic error: Merge request buffer overflow in a merge pipeline: bit 0: Error in PB transmit request pipeline. bit 1: Error in PB transmit array read pipeline. bit 2: Error in merge I-buf write pipeline. bit 3: Error in merge I-buf read pipeline. bit 4: Error in merge B-buf read pipeline. bit 5: Error in merge O-buf read pipeline.
56	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_CTL_PIPE: Logic error: I-buf CTL write request/data lost due to excessive incoming request.
57	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_PBTX_PIPE: Logic error: Pipeline overflow in PB transmit logic.
58	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_MRG_IR_PIPE: Logic error: Pipeline overflow in Merge I-buf read logic.
59	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_MRG_OR_PIPE: Logic error: Pipeline overflow in Merge O-buf read logic.
60	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_AMO_ADDR: Logic error: Invalid address position withn OW for armw_cas_t, armwf_inc_b, armwf_inc_e, and armwf_dec_b ttypes.
61	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_PBRX_RTAG: Logic error: Invalid RTAG observed on the PB receive interface.
62	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_WRITE: Logic error: NTL/ CTL wrote I-buf entry 0-3 cycles after the same entry was read for PB TX.
63	RWX_WCLEAR	IDIAL_CERR_LOG_HOLD_IBUF_WARB: Logic error: More than 1 write requests granted on I-buf write port.

Register Name	CQ_DAT CERR Logic Mask Register
Mnemonic	NPU.STCK2.DAT.MISC.CERR_LOG_MASK
Address	00000000050112AB (SCOM)
Description	CQ_DAT logic error c_err_rpt mask register

Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000
47:63	RW	CERR_LOG_MASK_BITS: CQ_DAT logic error c_err_rpt mask bits.

Register Name	CQ_DAT CERR Logic First Register
Mnemonic	NPU.STCK2.DAT.MISC.CERR_LOG_FIRST
Address	00000000050112AC (SCOM)
Description	CQ_DAT logic error c_err_rpt first register

Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000
47:63	RWX_WCLEAR	CERR_LOG_FIRST_BITS: CQ_DAT logic error c_err_rpt first error bits.

Register Name	CQ_DAT RAS Error Message 0 Register
Mnemonic	NPU.STCK2.DAT.MISC.REM0
Address	00000000050112AD (SCOM)
Description	CQ_DAT RAS Error Message 0

Bits	SCOM	Field Mnemonic: Description
0:16	RO	Constant = 0b00000000000000000
17:21	ROX	REM0_IBUF_WSRC: Indicates the I-buf write requestor that caused read-write conflict. bit 0 : NTL0 datin immediate write. bit 1 : NTL1 datin immediate write. bit 2 : NTL1 datin delayed write. bit 3 : CTL write. bit 4 : Merge logic.
22:23	ROX	REM0_IBUF_RSRC: Indicates the I-buf read requestor that caused read-write conflict. bit 0 : PBTX transmit. bit 1 : Merge logic.
24:31	ROX	REM0_IBUF_AIDX: The I-buf entry (0-255) on which read-write conflict occurred.
32:33	ROX	REM0_IBUF_ABANK: The I-buf array bank (0-3) on which read-write conflict occurred.
34:35	ROX	REM0_OBUF_WSRC: Indicates the O-buf write requestor that caused read-write conflict. bit 0 : PBTX receive. bit 1 : Merge logic I-O loopback.
36:41	ROX	REM0_OBUF_RSRC: Indicates the O-buf read requestor that caused read-write conflict. bit 0 : NTL0 datout immedate read. bit 1 : NTL1 datout immedate read. bit 2 : NTL0 datout regular read. bit 3 : NTL1 datout regular read. bit 4 : Merge logic. bit 5 : CTL read.

Bits	SCOM	Field Mnemonic: Description
42:49	ROX	REM0_OBUF_AIDX: The O-buf entry (0-255) on which read-write conflict occurred.
50:51	ROX	REM0_OBUF_ABANK: The O-buf array bank (0-3) on which read-write conflict occurred.
52:53	ROX	REM0_BBUF_WSRC: Indicates the B-buf write requestor that caused read-write conflict. bit 0 : NTL datin. bit 1 : Dispalt logic in MISC.
54:55	ROX	REM0_BBUF_RSRC: Indicates the B-buf read requestor that caused read-write conflict. bit 0 : Merge logic. bit 1 : Dispalt logic in MISC.
56:63	ROX	REM0_BBUF_AIDX: The B-buf entry (0-255) on which read-write conflict occurred.

Register Name	CQ_DAT RAS Error Message 1 Register
Mnemonic	NPU.STCK2.DAT.MISC.REM1
Address	00000000050112AE (SCOM)
Description	CQ_DAT RAS Error Message 1

Bits	SCOM	Field Mnemonic: Description
0:33	RO	Constant = 0b00000000000000000000000000000000
34:55	ROX	REM1_PBRX_RTAG: The invalid RTAG observed on PB receive interface.
56:58	ROX	REM1_ALU_ADR: The invalid ALU address in the OW that caused address error (in unit of 4B, 0 to 7).
59:62	ROX	REM1_ALU_TYPE: The ALU optype with which an address error was detected.
63	ROX	REM1_ALU_SZ: The ALU operand size (0:4B, 1:8B) when an address error was detected.

Register Name	CQ_DAT Debug0 Configuration Register
Mnemonic	NPU.STCK2.DAT.MISC.DEBUG0_CONFIG
Address	00000000050112B0 (SCOM)
Description	CQ_DAT Debug0 configuration register

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of trace-0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of trace-0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of trace-0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of trace-0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of trace-0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of trace-0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of trace-0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of trace-0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of trace-0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of trace-0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of trace-0.
55:62	RW	DEBUG0_CONFIG_Reserved1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock-gates for debug trace latches.

Register Name	CQ_DAT Debug1 Configuration Register
Mnemonic	NPU.STCK2.DAT.MISC.DEBUG1_CONFIG
Address	00000000050112B1 (SCOM)
Description	CQ_DAT Debug1 configuration register

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of trace-0.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of trace-0.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of trace-0.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of trace-0.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of trace-0.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of trace-0.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of trace-0.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of trace-0.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of trace-0.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of trace-0.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of trace-0.
55:62	RW	DEBUG1_CONFIG_Reserved1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock-gates for debug trace latches.

Register Name	CQ_DAT Scratch 1 Register
Mnemonic	NPU.STCK2.DAT.MISC.SCRATCH1
Address	00000000050112BC (SCOM)
Description	CQ_DAT scratch register 1

Bits	SCOM	Field Mnemonic: Description
0:63	RW	SCRATCH1_IDIAL: Scratch register.

Register Name	NTL Miscellaneous Configuration 2 Register
Mnemonic	NPU.STCK2.NTL0.REGS.CONFIG2
Address	00000000050112C0 (SCOM)
Description	The NTL Miscellaneous Configuration 2 Register is used to control internal NTL function. It contains mode bits, chicken switches, and thresholds.

Bits	SCOM	Field Mnemonic: Description
0	RW	BRICK_ENABLE: When 0b1, this NVLink brick is enabled. This configuration bit will be used as a general clock gate for latches in the NTL design.
1	RW	RSP_CTL_CRED_SINGLE_ENA: When 0b1, NTL will only give CQ_CTL 1 RSP credit at a time, instead of the normal 2.
2	RW	CREQ_BE_128: When 0b1, NTL will always send 128 bytes of data when it needs to send a Byte Enable (BE) flit to the GPU for a CREQ packet. When 0b0, NTL will send the least number of data flits required.

Bits	SCOM	Field Mnemonic: Description
3	RW	DGD_BE_128: When 0b1, NTL will always send 128 bytes of data when it needs to send a Byte Enable (BE) flit to the GPU for a Downgrade packet (BE and data flits are sent in the TransDone packet for the Downgrade). When 0b0, NTL will send the least number of data flits required.
4	RW	WR_SPLIT_UT0_ENA: When 0b1, NTL will split up Write requests with UT = 0 from the GPU that map to MMIO space into legal processor bus sizes/alignments. When 0b0, NTL will pass all Write requests with UT = 0 as is to CQ.
5	RW	WR_SPLIT_UT1_ENA: When 0b1, NTL will split up Write requests with UT = 1 from the GPU into legal processor bus sizes/alignments. This will include both DMA Writes and MMIO Writes since there is no way for NTL to distinguish between them. When 0b0, NTL will pass all Write requests with UT = 1 as is to CQ.
6	RW	BRICK_DEBUG_MODE: When 0b1, NTL will ignore all incoming NVLink packets from the GPU and will throw away all NVLink requests/responses from CQ destined for the GPU. This mode is used for debug purposes only when the NPU is not connected over NVLink to a GPU.
7	RW	P9_TO_P9_MODE: When 0b1, NTL will set UT = 1 for all incoming Read, Write, and Atomic NVLink packets before sending to CQ. This mode is used for debug purposes only when the NPU is connected to another/same NPU over NVLink.
8:9	RW	CONFIG2_Reserved1: Reserved.
10:15	RW	CAM256_MAX_CNT: This field specifies the number of entries in the CAM that holds information to send Responses for 256 byte operations that require a Response. (max value = 48).
16	RW	NDL_RX_PARITY_ENA: When 0b1, NTL will check parity on the incoming NDL RX signals.
17	RW	NDL_TX_PARITY_ENA: When 0b1, NTL will check parity on the incoming NDL TX (that is, TX Credits) signals.
18	RW	NDL_PRI_PARITY_ENA: When 0b1, NTL will check parity on the incoming NDL Priority Register Interface signals.
19	RW	RCV_CREDIT_OVERFLOW_ENA: When 0b1, NTL will check for overflows on any Received Credits from the GPU, NDL, and NDL Wrapper.
20	RW	HDR_ARR_ECC_CORR_ENA: When 0b1, NTL will correct ECC SBEs when reading the Rx Header Array.
21	RW	DAT_ARR_ECC_CORR_ENA: When 0b1, NTL will correct ECC SBEs when reading the Rx Data Array. NTL will only correct ECC on reads of the Rx Data Array that require NTL to update the data before sending to CQ_DAT (for example, BE flit or Data flits for Atomic CAS ops).
22	RW	TX_DATA_ECC_CORR_ENA: When 0b1, NTL will correct ECC SBEs when reading Tx Data from CQ_DAT.
23	RW	CONFIG2_Reserved2: Reserved.
24	RW	PARITY_ERROR_SUE_ENA: When 0b1, NTL will drive SUE on all Data transfers to CQ_DAT for a packet that has a parity error on an incoming Data flit.
25	RW	DATA_POISON_SUE_ENA: When 0b1, NTL will drive SUE on all Data transfers to CQ_DAT for a packet that receives LMD = Data Poison.
26	RW	HDR_ARR_ECC_SUE_ENA: When 0b1, NTL will drive SUE on all Data transfers to CQ_DAT for a packet that has an ECC UE/SUE on the header info read from the Rx Header Array.
27	RW	DAT_ARR_ECC_SUE_ENA: When 0b1, NTL will drive SUE on all Data transfers to CQ_DAT for a packet that has an ECC UE/SUE on data read from the Rx Data Array. NTL will only check ECC on reads of the Rx Data Array that require NTL to update the data before sending to CQ_DAT (for example, BE flit or Data flits for Atomic CAS ops).
28	RW	TX_ECC_DATA_POISON_ENA: When 0b1, NTL will send LMD = Data Poison for an outgoing NVLink packet that encounters an ECC UE/SUE on data read from CQ_DAT.
29:31	RW	CONFIG2_Reserved3: Reserved.
32	RW	PRI_STATE_MACHINE_RESET: Reset Priority Register Interface (PRI) state machine to Idle state (Debug use only).
33:63	RW	CONFIG2_Reserved4: Reserved.

Register Name	NTL Miscellaneous Configuration 3 Register
Mnemonic	NPU.STCK2.NTL0.REGS.CONFIG3
Address	00000000050112C1 (SCOM)
Description	The NTL Miscellaneous Configuration 3 Register is used for future control of internal NTL functions. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG3_Reserved1: Reserved.

Register Name	NTL CERR Hold 1 Register
Mnemonic	NPU.STCK2.NTL0.REGS.CERR_HOLD1
Address	00000000050112C2 (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLRREG	NTL_HOLD1_1: ERROR - NTL RX - AN / = 1 in an incoming NVLink packet where Rx Vld = 1 and Rx Hdr Vld = 1.
2	RWX_WCLRREG	NTL_HOLD1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the Address field is valid.
3	RWX_WCLRREG	NTL_HOLD1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the Address field is valid.
4	RWX_WCLRREG	NTL_HOLD1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink Read,Write,Atomic,RMW request packet.
5	RWX_WCLRREG	NTL_HOLD1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLRREG	NTL_HOLD1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid, and not Read nor Write.
7	RWX_WCLRREG	NTL_HOLD1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink ReqRsp with Data packet.
8	RWX_WCLRREG	NTL_HOLD1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	RWX_WCLRREG	NTL_HOLD1_9: ERROR - NTL RX - Compressed Responses not populated in the order CR0,CR1,CR2 in an incoming NVLink response packet.
10	RWX_WCLRREG	NTL_HOLD1_10: ERROR - NTL RX - Compressed Response with an Invalid/Reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLRREG	NTL_HOLD1_11: ERROR - NTL RX - Address(63:49) / = 0 in an incoming NVLink request packet where the Address field is valid.
12	RWX_WCLRREG	NTL_HOLD1_12: ERROR - NTL RX - Address(48:47) / = 0 in an incoming NVLink UT = 0 request packet where the Address field is valid, and not ATR.
13	RWX_WCLRREG	NTL_HOLD1_13: ERROR - NTL RX - DatLen / = 16,32,64,128B in an incoming NVLink Probe packet.
14	RWX_WCLRREG	NTL_HOLD1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink ReqRsp with Data packet.
15	RWX_WCLRREG	NTL_HOLD1_15: ERROR - NTL RX - AtomicSz / = 4B or 8B in an incoming NVLink Atomic packet.
16	RWX_WCLRREG	NTL_HOLD1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink Atomic packet where no BE flit exists.

Bits	SCOM	Field Mnemonic: Description
17	RWX_WCLRREG	NTL_HOLD1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLRREG	NTL_HOLD1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLRREG	NTL_HOLD1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLRREG	NTL_HOLD1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLRREG	NTL_HOLD1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLRREG	NTL_HOLD1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLRREG	NTL_HOLD1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLRREG	NTL_HOLD1_24: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Header Array.
25	RWX_WCLRREG	NTL_HOLD1_25: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Header Array.
26	RWX_WCLRREG	NTL_HOLD1_26: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(128:167) read from the Header Array.
27	RWX_WCLRREG	NTL_HOLD1_27: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Data Array.
28	RWX_WCLRREG	NTL_HOLD1_28: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Data Array.
29	RWX_WCLRREG	NTL_HOLD1_29: ERROR - NTL RX - Parity error on incoming NDL Rx Vld and Hdr_Vld signals.
30	RWX_WCLRREG	NTL_HOLD1_30: ERROR - NTL RX - Parity error on incoming NDL Rx LMD and CRC signals.
31	RWX_WCLRREG	NTL_HOLD1_31: ERROR - NTL RX - Parity error on incoming NDL Rx Header flit signals.
32	RWX_WCLRREG	NTL_HOLD1_32: ERROR - NTL RX - Parity error on incoming NDL Rx AE flit signals.
33	RWX_WCLRREG	NTL_HOLD1_33: ERROR - NTL RX - Parity error on incoming NDL Rx Data flit signals.
34	RWX_WCLRREG	NTL_HOLD1_34: ERROR - NTL RX - An NVLink packet with data received LMD = Data Poison.
35	RWX_WCLRREG	NTL_HOLD1_35: ERROR - NTL RX - New CREQ Header flit from NVLink received when the CREQ Header Array is full.
36	RWX_WCLRREG	NTL_HOLD1_36: ERROR - NTL RX - New CREQ Data flit from NVLink received when the CREQ Data Array is full.
37	RWX_WCLRREG	NTL_HOLD1_37: ERROR - NTL RX - CREQ Data flit was attempted to be read from the CREQ Data Array when it was empty.
38	RWX_WCLRREG	NTL_HOLD1_38: ERROR - NTL RX - New RSP Header flit from NVLink received when the RSP Header Array is full.
39	RWX_WCLRREG	NTL_HOLD1_39: ERROR - NTL RX - New RSP Data flit from NVLink received when the RSP Data Array is full.
40	RWX_WCLRREG	NTL_HOLD1_40: ERROR - NTL RX - RSP Data flit was attempted to be read from the RSP Data Array when it was empty.
41	RWX_WCLRREG	NTL_HOLD1_41: ERROR - NTL RX - New PRB Header flit from NVLink received when the PRB Header Array is full.
42	RWX_WCLRREG	NTL_HOLD1_42: ERROR - NTL RX - New ATR Header flit from NVLink received when the ATR Header Array is full.
43	RWX_WCLRREG	NTL_HOLD1_43: ERROR - NTL RX - A new NVLink Header flit was received when NTL was still expecting Data flits for the previous packet.
44	RWX_WCLRREG	NTL_HOLD1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or Data Array on the same cycle.
45	RWX_WCLRREG	NTL_HOLD1_45: ERROR - NTL RX - A CQ Slice Credit was received when one was already valid (overflow).

Bits	SCOM	Field Mnemonic: Description
46	RWX_WCLRREG	NTL_HOLD1_46: ERROR - NTL RX - A CQ ATR Credit was received when one was already valid (overflow).
47	RWX_WCLRREG	NTL_HOLD1_47: ERROR - NTL RX - A CQ Flush Credit was received when 15 were already valid (overflow).
48	RWX_WCLRREG	NTL_HOLD1_48: ERROR - NTL RX - A CQ Global Credit was received when 3 were already valid (overflow).
49	RWX_WCLRREG	NTL_HOLD1_49: ERROR - NTL RX - A CQ Response Credit was received when one was already valid (overflow).
50	RWX_WCLRREG	NTL_HOLD1_50: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLRREG	NTL_HOLD1_51: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLRREG	NTL_HOLD1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLRREG	NTL_HOLD1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLRREG	NTL_HOLD1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLRREG	NTL_HOLD1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLRREG	NTL_HOLD1_56: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Header Array.
57	RWX_WCLRREG	NTL_HOLD1_57: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Header Array.
58	RWX_WCLRREG	NTL_HOLD1_58: ERROR - NTL RX - ECC Correctable Error (CE) on Data(128:167) read from the Header Array.
59	RWX_WCLRREG	NTL_HOLD1_59: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Data Array.
60	RWX_WCLRREG	NTL_HOLD1_60: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Data Array.
61	RWX_WCLRREG	NTL_HOLD1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLRREG	NTL_HOLD1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLRREG	NTL_HOLD1_63: ERROR - NTL RX - Reserved.

Register Name	NTL CERR Mask 1 Register
Mnemonic	NPU.STCK2.NTL0.REGS.CERR_MASK1
Address	00000000050112C3 (SCOM)
Description	c_err_rpt mask latches read-only reg

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	ROX	NTL_MASK1_1: ERROR - NTL RX - AN / = 1 in an incoming NVLink packet where Rx Vld = 1 and Rx Hdr Vld = 1.
2	ROX	NTL_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the Address field is valid.
3	ROX	NTL_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the Address field is valid.

Bits	SCOM	Field Mnemonic: Description
4	ROX	NTL_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink Read,Write,Atomic,RMW request packet.
5	ROX	NTL_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	ROX	NTL_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid, and not Read nor Write.
7	ROX	NTL_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink ReqRsp with Data packet.
8	ROX	NTL_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	ROX	NTL_MASK1_9: ERROR - NTL RX - Compressed Responses not populated in the order CR0,CR1,CR2 in an incoming NVLink response packet.
10	ROX	NTL_MASK1_10: ERROR - NTL RX - Compressed Response with an Invalid/Reserved TD/IVC combination in an incoming NVLink response packet.
11	ROX	NTL_MASK1_11: ERROR - NTL RX - Address(63:49) / = 0 in an incoming NVLink request packet where the Address field is valid.
12	ROX	NTL_MASK1_12: ERROR - NTL RX - Address(48:47) / = 0 in an incoming NVLink UT = 0 request packet where the Address field is valid, and not ATR.
13	ROX	NTL_MASK1_13: ERROR - NTL RX - DatLen / = 16,32,64,128B in an incoming NVLink Probe packet.
14	ROX	NTL_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink ReqRsp with Data packet.
15	ROX	NTL_MASK1_15: ERROR - NTL RX - AtomicSz / = 4B or 8B in an incoming NVLink Atomic packet.
16	ROX	NTL_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink Atomic packet where no BE flit exists.
17	ROX	NTL_MASK1_17: ERROR - NTL RX - Reserved.
18	ROX	NTL_MASK1_18: ERROR - NTL RX - Reserved.
19	ROX	NTL_MASK1_19: ERROR - NTL RX - Reserved.
20	ROX	NTL_MASK1_20: ERROR - NTL RX - Reserved.
21	ROX	NTL_MASK1_21: ERROR - NTL RX - Reserved.
22	ROX	NTL_MASK1_22: ERROR - NTL RX - Reserved.
23	ROX	NTL_MASK1_23: ERROR - NTL RX - Reserved.
24	ROX	NTL_MASK1_24: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Header Array.
25	ROX	NTL_MASK1_25: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Header Array.
26	ROX	NTL_MASK1_26: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(128:167) read from the Header Array.
27	ROX	NTL_MASK1_27: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Data Array.
28	ROX	NTL_MASK1_28: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Data Array.
29	ROX	NTL_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL Rx Vld and Hdr_Vld signals.
30	ROX	NTL_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL Rx LMD and CRC signals.
31	ROX	NTL_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL Rx Header flit signals.
32	ROX	NTL_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL Rx AE flit signals.
33	ROX	NTL_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL Rx Data flit signals.

Bits	SCOM	Field Mnemonic: Description
34	ROX	NTL_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = Data Poison.
35	ROX	NTL_MASK1_35: ERROR - NTL RX - New CREQ Header flit from NVLink received when the CREQ Header Array is full.
36	ROX	NTL_MASK1_36: ERROR - NTL RX - New CREQ Data flit from NVLink received when the CREQ Data Array is full.
37	ROX	NTL_MASK1_37: ERROR - NTL RX - CREQ Data flit was attempted to be read from the CREQ Data Array when it was empty.
38	ROX	NTL_MASK1_38: ERROR - NTL RX - New RSP Header flit from NVLink received when the RSP Header Array is full.
39	ROX	NTL_MASK1_39: ERROR - NTL RX - New RSP Data flit from NVLink received when the RSP Data Array is full.
40	ROX	NTL_MASK1_40: ERROR - NTL RX - RSP Data flit was attempted to be read from the RSP Data Array when it was empty.
41	ROX	NTL_MASK1_41: ERROR - NTL RX - New PRB Header flit from NVLink received when the PRB Header Array is full.
42	ROX	NTL_MASK1_42: ERROR - NTL RX - New ATR Header flit from NVLink received when the ATR Header Array is full.
43	ROX	NTL_MASK1_43: ERROR - NTL RX - A new NVLink Header flit was received when NTL was still expecting Data flits for the previous packet.
44	ROX	NTL_MASK1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or Data Array on the same cycle.
45	ROX	NTL_MASK1_45: ERROR - NTL RX - A CQ Slice Credit was received when one was already valid (overflow).
46	ROX	NTL_MASK1_46: ERROR - NTL RX - A CQ ATR Credit was received when one was already valid (overflow).
47	ROX	NTL_MASK1_47: ERROR - NTL RX - A CQ Flush Credit was received when 15 were already valid (overflow).
48	ROX	NTL_MASK1_48: ERROR - NTL RX - A CQ Global Credit was received when 3 were already valid (overflow).
49	ROX	NTL_MASK1_49: ERROR - NTL RX - A CQ Response Credit was received when one was already valid (overflow).
50	ROX	NTL_MASK1_50: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	ROX	NTL_MASK1_51: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	ROX	NTL_MASK1_52: ERROR - NTL RX - Reserved.
53	ROX	NTL_MASK1_53: ERROR - NTL RX - Reserved.
54	ROX	NTL_MASK1_54: ERROR - NTL RX - Reserved.
55	ROX	NTL_MASK1_55: ERROR - NTL RX - Reserved.
56	ROX	NTL_MASK1_56: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Header Array.
57	ROX	NTL_MASK1_57: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Header Array.
58	ROX	NTL_MASK1_58: ERROR - NTL RX - ECC Correctable Error (CE) on Data(128:167) read from the Header Array.
59	ROX	NTL_MASK1_59: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Data Array.

Bits	SCOM	Field Mnemonic: Description
60	ROX	NTL_MASK1_60: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Data Array.
61	ROX	NTL_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	ROX	NTL_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	ROX	NTL_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First 1 Register**
Mnemonic	NPU.STCK2.NTL0.REGS.CERR_FIRST1
Address	00000000050112C4 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLEAR	NTL_FIRST1_1: ERROR - NTL RX - AN / = 1 in an incoming NVLink packet where Rx Vld = 1 and Rx Hdr Vld = 1.
2	RWX_WCLEAR	NTL_FIRST1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the Address field is valid.
3	RWX_WCLEAR	NTL_FIRST1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the Address field is valid.
4	RWX_WCLEAR	NTL_FIRST1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink Read,Write,Atomic,RMW request packet.
5	RWX_WCLEAR	NTL_FIRST1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLEAR	NTL_FIRST1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid, and not Read nor Write.
7	RWX_WCLEAR	NTL_FIRST1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink ReqRsp with Data packet.
8	RWX_WCLEAR	NTL_FIRST1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	RWX_WCLEAR	NTL_FIRST1_9: ERROR - NTL RX - Compressed Responses not populated in the order CR0,CR1,CR2 in an incoming NVLink response packet.
10	RWX_WCLEAR	NTL_FIRST1_10: ERROR - NTL RX - Compressed Response with an Invalid/Reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLEAR	NTL_FIRST1_11: ERROR - NTL RX - Address(63:49) / = 0 in an incoming NVLink request packet where the Address field is valid.
12	RWX_WCLEAR	NTL_FIRST1_12: ERROR - NTL RX - Address(48:47) / = 0 in an incoming NVLink UT = 0 request packet where the Address field is valid, and not ATR.
13	RWX_WCLEAR	NTL_FIRST1_13: ERROR - NTL RX - DatLen / = 16,32,64,128B in an incoming NVLink Probe packet.
14	RWX_WCLEAR	NTL_FIRST1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink ReqRsp with Data packet.
15	RWX_WCLEAR	NTL_FIRST1_15: ERROR - NTL RX - AtomicSz / = 4B or 8B in an incoming NVLink Atomic packet.
16	RWX_WCLEAR	NTL_FIRST1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink Atomic packet where no BE flit exists.
17	RWX_WCLEAR	NTL_FIRST1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLEAR	NTL_FIRST1_18: ERROR - NTL RX - Reserved.

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLEAR	NTL_FIRST1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLEAR	NTL_FIRST1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLEAR	NTL_FIRST1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLEAR	NTL_FIRST1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLEAR	NTL_FIRST1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLEAR	NTL_FIRST1_24: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Header Array.
25	RWX_WCLEAR	NTL_FIRST1_25: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Header Array.
26	RWX_WCLEAR	NTL_FIRST1_26: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(128:167) read from the Header Array.
27	RWX_WCLEAR	NTL_FIRST1_27: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Data Array.
28	RWX_WCLEAR	NTL_FIRST1_28: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Data Array.
29	RWX_WCLEAR	NTL_FIRST1_29: ERROR - NTL RX - Parity error on incoming NDL Rx Vld and Hdr_Vld signals.
30	RWX_WCLEAR	NTL_FIRST1_30: ERROR - NTL RX - Parity error on incoming NDL Rx LMD and CRC signals.
31	RWX_WCLEAR	NTL_FIRST1_31: ERROR - NTL RX - Parity error on incoming NDL Rx Header flit signals.
32	RWX_WCLEAR	NTL_FIRST1_32: ERROR - NTL RX - Parity error on incoming NDL Rx AE flit signals.
33	RWX_WCLEAR	NTL_FIRST1_33: ERROR - NTL RX - Parity error on incoming NDL Rx Data flit signals.
34	RWX_WCLEAR	NTL_FIRST1_34: ERROR - NTL RX - An NVLink packet with data received LMD = Data Poison.
35	RWX_WCLEAR	NTL_FIRST1_35: ERROR - NTL RX - New CREQ Header flit from NVLink received when the CREQ Header Array is full.
36	RWX_WCLEAR	NTL_FIRST1_36: ERROR - NTL RX - New CREQ Data flit from NVLink received when the CREQ Data Array is full.
37	RWX_WCLEAR	NTL_FIRST1_37: ERROR - NTL RX - CREQ Data flit was attempted to be read from the CREQ Data Array when it was empty.
38	RWX_WCLEAR	NTL_FIRST1_38: ERROR - NTL RX - New RSP Header flit from NVLink received when the RSP Header Array is full.
39	RWX_WCLEAR	NTL_FIRST1_39: ERROR - NTL RX - New RSP Data flit from NVLink received when the RSP Data Array is full.
40	RWX_WCLEAR	NTL_FIRST1_40: ERROR - NTL RX - RSP Data flit was attempted to be read from the RSP Data Array when it was empty.
41	RWX_WCLEAR	NTL_FIRST1_41: ERROR - NTL RX - New PRB Header flit from NVLink received when the PRB Header Array is full.
42	RWX_WCLEAR	NTL_FIRST1_42: ERROR - NTL RX - New ATR Header flit from NVLink received when the ATR Header Array is full.
43	RWX_WCLEAR	NTL_FIRST1_43: ERROR - NTL RX - A new NVLink Header flit was received when NTL was still expecting Data flits for the previous packet.
44	RWX_WCLEAR	NTL_FIRST1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or Data Array on the same cycle.
45	RWX_WCLEAR	NTL_FIRST1_45: ERROR - NTL RX - A CQ Slice Credit was received when one was already valid (overflow).
46	RWX_WCLEAR	NTL_FIRST1_46: ERROR - NTL RX - A CQ ATR Credit was received when one was already valid (overflow).

Bits	SCOM	Field Mnemonic: Description
47	RWX_WCLEAR	NTL_FIRST1_47: ERROR - NTL RX - A CQ Flush Credit was received when 15 were already valid (overflow).
48	RWX_WCLEAR	NTL_FIRST1_48: ERROR - NTL RX - A CQ Global Credit was received when 3 were already valid (overflow).
49	RWX_WCLEAR	NTL_FIRST1_49: ERROR - NTL RX - A CQ Response Credit was received when one was already valid (overflow).
50	RWX_WCLEAR	NTL_FIRST1_50: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLEAR	NTL_FIRST1_51: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLEAR	NTL_FIRST1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLEAR	NTL_FIRST1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLEAR	NTL_FIRST1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLEAR	NTL_FIRST1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLEAR	NTL_FIRST1_56: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Header Array.
57	RWX_WCLEAR	NTL_FIRST1_57: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Header Array.
58	RWX_WCLEAR	NTL_FIRST1_58: ERROR - NTL RX - ECC Correctable Error (CE) on Data(128:167) read from the Header Array.
59	RWX_WCLEAR	NTL_FIRST1_59: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Data Array.
60	RWX_WCLEAR	NTL_FIRST1_60: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Data Array.
61	RWX_WCLEAR	NTL_FIRST1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLEAR	NTL_FIRST1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLEAR	NTL_FIRST1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First Mask 1 Register**
Mnemonic	NPU.STCK2.NTL0.REGS.CERR_FIRST_MASK1
Address	00000000050112C5 (SCOM)
Description	1 error mask register Mask errors from being captured in the First-1 Error registers and the RAS Error Message registers

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RW	NTL_FIRST_MASK1_1: ERROR - NTL RX - AN / = 1 in an incoming NVLink packet where Rx Vld = 1 and Rx Hdr Vld = 1.
2	RW	NTL_FIRST_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the Address field is valid.
3	RW	NTL_FIRST_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the Address field is valid.
4	RW	NTL_FIRST_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink Read,Write,Atomic,RMW request packet.

Bits	SCOM	Field Mnemonic: Description
5	RW	NTL_FIRST_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RW	NTL_FIRST_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid, and not Read nor Write.
7	RW	NTL_FIRST_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink ReqRsp with Data packet.
8	RW	NTL_FIRST_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	RW	NTL_FIRST_MASK1_9: ERROR - NTL RX - Compressed Responses not populated in the order CR0,CR1,CR2 in an incoming NVLink response packet.
10	RW	NTL_FIRST_MASK1_10: ERROR - NTL RX - Compressed Response with an Invalid/Reserved TD/IVC combination in an incoming NVLink response packet.
11	RW	NTL_FIRST_MASK1_11: ERROR - NTL RX - Address(63:49) / = 0 in an incoming NVLink request packet where the Address field is valid.
12	RW	NTL_FIRST_MASK1_12: ERROR - NTL RX - Address(48:47) / = 0 in an incoming NVLink UT = 0 request packet where the Address field is valid, and not ATR.
13	RW	NTL_FIRST_MASK1_13: ERROR - NTL RX - DatLen / = 16,32,64,128B in an incoming NVLink Probe packet.
14	RW	NTL_FIRST_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink ReqRsp with Data packet.
15	RW	NTL_FIRST_MASK1_15: ERROR - NTL RX - AtomicSz / = 4B or 8B in an incoming NVLink Atomic packet.
16	RW	NTL_FIRST_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink Atomic packet where no BE flit exists.
17	RW	NTL_FIRST_MASK1_17: ERROR - NTL RX - Reserved.
18	RW	NTL_FIRST_MASK1_18: ERROR - NTL RX - Reserved.
19	RW	NTL_FIRST_MASK1_19: ERROR - NTL RX - Reserved.
20	RW	NTL_FIRST_MASK1_20: ERROR - NTL RX - Reserved.
21	RW	NTL_FIRST_MASK1_21: ERROR - NTL RX - Reserved.
22	RW	NTL_FIRST_MASK1_22: ERROR - NTL RX - Reserved.
23	RW	NTL_FIRST_MASK1_23: ERROR - NTL RX - Reserved.
24	RW	NTL_FIRST_MASK1_24: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Header Array.
25	RW	NTL_FIRST_MASK1_25: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Header Array.
26	RW	NTL_FIRST_MASK1_26: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(128:167) read from the Header Array.
27	RW	NTL_FIRST_MASK1_27: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Data Array.
28	RW	NTL_FIRST_MASK1_28: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Data Array.
29	RW	NTL_FIRST_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL Rx Vld and Hdr_Vld signals.
30	RW	NTL_FIRST_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL Rx LMD and CRC signals.
31	RW	NTL_FIRST_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL Rx Header flit signals.
32	RW	NTL_FIRST_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL Rx AE flit signals.
33	RW	NTL_FIRST_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL Rx Data flit signals.

Bits	SCOM	Field Mnemonic: Description
34	RW	NTL_FIRST_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = Data Poison.
35	RW	NTL_FIRST_MASK1_35: ERROR - NTL RX - New CREQ Header flit from NVLink received when the CREQ Header Array is full.
36	RW	NTL_FIRST_MASK1_36: ERROR - NTL RX - New CREQ Data flit from NVLink received when the CREQ Data Array is full.
37	RW	NTL_FIRST_MASK1_37: ERROR - NTL RX - CREQ Data flit was attempted to be read from the CREQ Data Array when it was empty.
38	RW	NTL_FIRST_MASK1_38: ERROR - NTL RX - New RSP Header flit from NVLink received when the RSP Header Array is full.
39	RW	NTL_FIRST_MASK1_39: ERROR - NTL RX - New RSP Data flit from NVLink received when the RSP Data Array is full.
40	RW	NTL_FIRST_MASK1_40: ERROR - NTL RX - RSP Data flit was attempted to be read from the RSP Data Array when it was empty.
41	RW	NTL_FIRST_MASK1_41: ERROR - NTL RX - New PRB Header flit from NVLink received when the PRB Header Array is full.
42	RW	NTL_FIRST_MASK1_42: ERROR - NTL RX - New ATR Header flit from NVLink received when the ATR Header Array is full.
43	RW	NTL_FIRST_MASK1_43: ERROR - NTL RX - A new NVLink Header flit was received when NTL was still expecting Data flits for the previous packet.
44	RW	NTL_FIRST_MASK1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or Data Array on the same cycle.
45	RW	NTL_FIRST_MASK1_45: ERROR - NTL RX - A CQ Slice Credit was received when one was already valid (overflow).
46	RW	NTL_FIRST_MASK1_46: ERROR - NTL RX - A CQ ATR Credit was received when one was already valid (overflow).
47	RW	NTL_FIRST_MASK1_47: ERROR - NTL RX - A CQ Flush Credit was received when 15 were already valid (overflow).
48	RW	NTL_FIRST_MASK1_48: ERROR - NTL RX - A CQ Global Credit was received when 3 were already valid (overflow).
49	RW	NTL_FIRST_MASK1_49: ERROR - NTL RX - A CQ Response Credit was received when one was already valid (overflow).
50	RW	NTL_FIRST_MASK1_50: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RW	NTL_FIRST_MASK1_51: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RW	NTL_FIRST_MASK1_52: ERROR - NTL RX - Reserved.
53	RW	NTL_FIRST_MASK1_53: ERROR - NTL RX - Reserved.
54	RW	NTL_FIRST_MASK1_54: ERROR - NTL RX - Reserved.
55	RW	NTL_FIRST_MASK1_55: ERROR - NTL RX - Reserved.
56	RW	NTL_FIRST_MASK1_56: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Header Array.
57	RW	NTL_FIRST_MASK1_57: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Header Array.
58	RW	NTL_FIRST_MASK1_58: ERROR - NTL RX - ECC Correctable Error (CE) on Data(128:167) read from the Header Array.
59	RW	NTL_FIRST_MASK1_59: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Data Array.

Bits	SCOM	Field Mnemonic: Description
60	RW	NTL_FIRST_MASK1_60: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Data Array.
61	RW	NTL_FIRST_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RW	NTL_FIRST_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RW	NTL_FIRST_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR Hold 2 Register**
Mnemonic	NPU.STCK2.NTL0.REGS.CERR_HOLD2
Address	00000000050112C6 (SCOM)
Description	2 latches register c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD2_0: ERROR - NTL TX - Parity error on incoming NDL Tx Credit signals.
1	RWX_WCLRREG	NTL_HOLD2_1: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(0:63) read from CQ_DAT.
2	RWX_WCLRREG	NTL_HOLD2_2: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(64:127) read from CQ_DAT.
3	RWX_WCLRREG	NTL_HOLD2_3: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(0:63) read from CQ_DAT.
4	RWX_WCLRREG	NTL_HOLD2_4: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(64:127) read from CQ_DAT.
5	RWX_WCLRREG	NTL_HOLD2_5: ERROR - NTL TX - Read or Atomic request with a length that is not a power of 2.
6	RWX_WCLRREG	NTL_HOLD2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLRREG	NTL_HOLD2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLRREG	NTL_HOLD2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLRREG	NTL_HOLD2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLRREG	NTL_HOLD2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLRREG	NTL_HOLD2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLRREG	NTL_HOLD2_12: ERROR - NTL TX - More than 1 entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLRREG	NTL_HOLD2_13: ERROR - NTL TX - More than 1 entry in the CREQ Sticky CAM was hit at the same time.
14	RWX_WCLRREG	NTL_HOLD2_14: ERROR - NTL TX - More than 1 entry in the DGD Sticky CAM was hit at the same time.
15	RWX_WCLRREG	NTL_HOLD2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLRREG	NTL_HOLD2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLRREG	NTL_HOLD2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLRREG	NTL_HOLD2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLRREG	NTL_HOLD2_19: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
20	RWX_WCLRREG	NTL_HOLD2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLRREG	NTL_HOLD2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLRREG	NTL_HOLD2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLRREG	NTL_HOLD2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLRREG	NTL_HOLD2_24: ERROR - NTL TX - ECC Correctable Error (CE) on Data(0:63) read from CQ_DAT.
25	RWX_WCLRREG	NTL_HOLD2_25: ERROR - NTL TX - ECC Correctable Error (CE) on Data(64:127) read from CQ_DAT.
26	RWX_WCLRREG	NTL_HOLD2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLRREG	NTL_HOLD2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLRREG	NTL_HOLD2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLRREG	NTL_HOLD2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLRREG	NTL_HOLD2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLRREG	NTL_HOLD2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLRREG	NTL_HOLD2_32: ERROR - NTL REGS - CREQ Header Credits received from the GPU are greater than max value.
33	RWX_WCLRREG	NTL_HOLD2_33: ERROR - NTL REGS - DGD Header Credits received from the GPU are greater than max value.
34	RWX_WCLRREG	NTL_HOLD2_34: ERROR - NTL REGS - ATSD Header Credits received from the GPU are greater than max value.
35	RWX_WCLRREG	NTL_HOLD2_35: ERROR - NTL REGS - RSP Header Credits received from the GPU are greater than max value.
36	RWX_WCLRREG	NTL_HOLD2_36: ERROR - NTL REGS - CREQ Data Credits received from the GPU are greater than max value.
37	RWX_WCLRREG	NTL_HOLD2_37: ERROR - NTL REGS - RSP Data Credits received from the GPU are greater than max value.
38	RWX_WCLRREG	NTL_HOLD2_38: ERROR - NTL REGS - Replay Buffer Credits received from NDL are greater than 512.
39	RWX_WCLRREG	NTL_HOLD2_39: ERROR - NTL REGS - Async Buffer Credits received from the NDL Wrapper are greater than 64.
40	RWX_WCLRREG	NTL_HOLD2_40: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for different NTLs.
41	RWX_WCLRREG	NTL_HOLD2_41: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for the same NTL.
42	RWX_WCLRREG	NTL_HOLD2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLRREG	NTL_HOLD2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLRREG	NTL_HOLD2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLRREG	NTL_HOLD2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLRREG	NTL_HOLD2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLRREG	NTL_HOLD2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLRREG	NTL_HOLD2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLRREG	NTL_HOLD2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLRREG	NTL_HOLD2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLRREG	NTL_HOLD2_51: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RWX_WCLRREG	NTL_HOLD2_52: ERROR - NTL REGS - PHY timeout error indication received on a Private Register Interface response.
53	RWX_WCLRREG	NTL_HOLD2_53: ERROR - NTL REGS - NDL error error indication received on a Private Register Interface response.
54	RWX_WCLRREG	NTL_HOLD2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a Private Register Interface response.
55	RWX_WCLRREG	NTL_HOLD2_55: ERROR - NTL REGS - Bad address error indication received on a Private Register Interface response.
56	RWX_WCLRREG	NTL_HOLD2_56: ERROR - NTL REGS - Parity error error indication received on a Private Register Interface response.
57	RWX_WCLRREG	NTL_HOLD2_57: ERROR - NTL REGS - Protocol error error indication received on a Private Register Interface response.
58	RWX_WCLRREG	NTL_HOLD2_58: ERROR - NTL REGS - Private Register Interface Ack signal from NDL Wrapper went invalid in the middle of a PRI response.
59	RWX_WCLRREG	NTL_HOLD2_59: ERROR - NTL REGS - Parity error on incoming NDL Priority Register Interface (PRI) response signals.
60	RWX_WCLRREG	NTL_HOLD2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLRREG	NTL_HOLD2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLRREG	NTL_HOLD2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLRREG	NTL_HOLD2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR Mask 2 Register**
Mnemonic	NPU.STCK2.NTL0.REGS.CERR_MASK2
Address	00000000050112C7 (SCOM)
Description	2 latches register c_err_rpt mask latches read-only reg

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL Tx Credit signals.
1	ROX	NTL_MASK2_1: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(0:63) read from CQ_DAT.
2	ROX	NTL_MASK2_2: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(64:127) read from CQ_DAT.
3	ROX	NTL_MASK2_3: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(0:63) read from CQ_DAT.
4	ROX	NTL_MASK2_4: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(64:127) read from CQ_DAT.
5	ROX	NTL_MASK2_5: ERROR - NTL TX - Read or Atomic request with a length that is not a power of 2.
6	ROX	NTL_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	ROX	NTL_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	ROX	NTL_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	ROX	NTL_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	ROX	NTL_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.

Bits	SCOM	Field Mnemonic: Description
11	ROX	NTL_MASK2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.
12	ROX	NTL_MASK2_12: ERROR - NTL TX - More than 1 entry in the 256B Ops CAM was hit at the same time.
13	ROX	NTL_MASK2_13: ERROR - NTL TX - More than 1 entry in the CREQ Sticky CAM was hit at the same time.
14	ROX	NTL_MASK2_14: ERROR - NTL TX - More than 1 entry in the DGD Sticky CAM was hit at the same time.
15	ROX	NTL_MASK2_15: ERROR - NTL TX - Reserved.
16	ROX	NTL_MASK2_16: ERROR - NTL TX - Reserved.
17	ROX	NTL_MASK2_17: ERROR - NTL TX - Reserved.
18	ROX	NTL_MASK2_18: ERROR - NTL TX - Reserved.
19	ROX	NTL_MASK2_19: ERROR - NTL TX - Reserved.
20	ROX	NTL_MASK2_20: ERROR - NTL TX - Reserved.
21	ROX	NTL_MASK2_21: ERROR - NTL TX - Reserved.
22	ROX	NTL_MASK2_22: ERROR - NTL TX - Reserved.
23	ROX	NTL_MASK2_23: ERROR - NTL TX - Reserved.
24	ROX	NTL_MASK2_24: ERROR - NTL TX - ECC Correctable Error (CE) on Data(0:63) read from CQ_DAT.
25	ROX	NTL_MASK2_25: ERROR - NTL TX - ECC Correctable Error (CE) on Data(64:127) read from CQ_DAT.
26	ROX	NTL_MASK2_26: ERROR - NTL TX - Reserved.
27	ROX	NTL_MASK2_27: ERROR - NTL TX - Reserved.
28	ROX	NTL_MASK2_28: ERROR - NTL TX - Reserved.
29	ROX	NTL_MASK2_29: ERROR - NTL TX - Reserved.
30	ROX	NTL_MASK2_30: ERROR - NTL TX - Reserved.
31	ROX	NTL_MASK2_31: ERROR - NTL TX - Reserved.
32	ROX	NTL_MASK2_32: ERROR - NTL REGS - CREQ Header Credits received from the GPU are greater than max value.
33	ROX	NTL_MASK2_33: ERROR - NTL REGS - DGD Header Credits received from the GPU are greater than max value.
34	ROX	NTL_MASK2_34: ERROR - NTL REGS - ATSD Header Credits received from the GPU are greater than max value.
35	ROX	NTL_MASK2_35: ERROR - NTL REGS - RSP Header Credits received from the GPU are greater than max value.
36	ROX	NTL_MASK2_36: ERROR - NTL REGS - CREQ Data Credits received from the GPU are greater than max value.
37	ROX	NTL_MASK2_37: ERROR - NTL REGS - RSP Data Credits received from the GPU are greater than max value.
38	ROX	NTL_MASK2_38: ERROR - NTL REGS - Replay Buffer Credits received from NDL are greater than 512.
39	ROX	NTL_MASK2_39: ERROR - NTL REGS - Async Buffer Credits received from the NDL Wrapper are greater than 64.
40	ROX	NTL_MASK2_40: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for different NTLs.
41	ROX	NTL_MASK2_41: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for the same NTL.
42	ROX	NTL_MASK2_42: ERROR - NTL REGS - Reserved.
43	ROX	NTL_MASK2_43: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
44	ROX	NTL_MASK2_44: ERROR - NTL REGS - Reserved.
45	ROX	NTL_MASK2_45: ERROR - NTL REGS - Reserved.
46	ROX	NTL_MASK2_46: ERROR - NTL REGS - Reserved.
47	ROX	NTL_MASK2_47: ERROR - NTL REGS - Reserved.
48	ROX	NTL_MASK2_48: ERROR - NTL REGS - Reserved.
49	ROX	NTL_MASK2_49: ERROR - NTL REGS - Reserved.
50	ROX	NTL_MASK2_50: ERROR - NTL REGS - Reserved.
51	ROX	NTL_MASK2_51: ERROR - NTL REGS - Reserved.
52	ROX	NTL_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a Private Register Interface response.
53	ROX	NTL_MASK2_53: ERROR - NTL REGS - NDL error error indication received on a Private Register Interface response.
54	ROX	NTL_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a Private Register Interface response.
55	ROX	NTL_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a Private Register Interface response.
56	ROX	NTL_MASK2_56: ERROR - NTL REGS - Parity error error indication received on a Private Register Interface response.
57	ROX	NTL_MASK2_57: ERROR - NTL REGS - Protocol error error indication received on a Private Register Interface response.
58	ROX	NTL_MASK2_58: ERROR - NTL REGS - Private Register Interface Ack signal from NDL Wrapper went invalid in the middle of a PRI response.
59	ROX	NTL_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL Priority Register Interface (PRI) response signals.
60	ROX	NTL_MASK2_60: ERROR - NTL REGS - Reserved.
61	ROX	NTL_MASK2_61: ERROR - NTL REGS - Reserved.
62	ROX	NTL_MASK2_62: ERROR - NTL REGS - Reserved.
63	ROX	NTL_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	NTL CERR First 2 Register
Mnemonic	NPU.STCK2.NTL0.REGS.CERR_FIRST2
Address	00000000050112C8 (SCOM)
Description	2 latches register c_err_rpt first error latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST2_0: ERROR - NTL TX - Parity error on incoming NDL Tx Credit signals.
1	RWX_WCLEAR	NTL_FIRST2_1: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(0:63) read from CQ_DAT.
2	RWX_WCLEAR	NTL_FIRST2_2: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(64:127) read from CQ_DAT.
3	RWX_WCLEAR	NTL_FIRST2_3: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(0:63) read from CQ_DAT.

Bits	SCOM	Field Mnemonic: Description
4	RWX_WCLEAR	NTL_FIRST2_4: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(64:127) read from CQ_DAT.
5	RWX_WCLEAR	NTL_FIRST2_5: ERROR - NTL TX - Read or Atomic request with a length that is not a power of 2.
6	RWX_WCLEAR	NTL_FIRST2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLEAR	NTL_FIRST2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLEAR	NTL_FIRST2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLEAR	NTL_FIRST2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLEAR	NTL_FIRST2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLEAR	NTL_FIRST2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLEAR	NTL_FIRST2_12: ERROR - NTL TX - More than 1 entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLEAR	NTL_FIRST2_13: ERROR - NTL TX - More than 1 entry in the CREQ Sticky CAM was hit at the same time.
14	RWX_WCLEAR	NTL_FIRST2_14: ERROR - NTL TX - More than 1 entry in the DGD Sticky CAM was hit at the same time.
15	RWX_WCLEAR	NTL_FIRST2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLEAR	NTL_FIRST2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLEAR	NTL_FIRST2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLEAR	NTL_FIRST2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLEAR	NTL_FIRST2_19: ERROR - NTL TX - Reserved.
20	RWX_WCLEAR	NTL_FIRST2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLEAR	NTL_FIRST2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLEAR	NTL_FIRST2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLEAR	NTL_FIRST2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLEAR	NTL_FIRST2_24: ERROR - NTL TX - ECC Correctable Error (CE) on Data(0:63) read from CQ_DAT.
25	RWX_WCLEAR	NTL_FIRST2_25: ERROR - NTL TX - ECC Correctable Error (CE) on Data(64:127) read from CQ_DAT.
26	RWX_WCLEAR	NTL_FIRST2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLEAR	NTL_FIRST2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLEAR	NTL_FIRST2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLEAR	NTL_FIRST2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLEAR	NTL_FIRST2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLEAR	NTL_FIRST2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLEAR	NTL_FIRST2_32: ERROR - NTL REGS - CREQ Header Credits received from the GPU are greater than max value.
33	RWX_WCLEAR	NTL_FIRST2_33: ERROR - NTL REGS - DGD Header Credits received from the GPU are greater than max value.
34	RWX_WCLEAR	NTL_FIRST2_34: ERROR - NTL REGS - ATSD Header Credits received from the GPU are greater than max value.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	NTL_FIRST2_35: ERROR - NTL REGS - RSP Header Credits received from the GPU are greater than max value.
36	RWX_WCLEAR	NTL_FIRST2_36: ERROR - NTL REGS - CREQ Data Credits received from the GPU are greater than max value.
37	RWX_WCLEAR	NTL_FIRST2_37: ERROR - NTL REGS - RSP Data Credits received from the GPU are greater than max value.
38	RWX_WCLEAR	NTL_FIRST2_38: ERROR - NTL REGS - Replay Buffer Credits received from NDL are greater than 512.
39	RWX_WCLEAR	NTL_FIRST2_39: ERROR - NTL REGS - Async Buffer Credits received from the NDL Wrapper are greater than 64.
40	RWX_WCLEAR	NTL_FIRST2_40: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for different NTLs.
41	RWX_WCLEAR	NTL_FIRST2_41: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for the same NTL.
42	RWX_WCLEAR	NTL_FIRST2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLEAR	NTL_FIRST2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLEAR	NTL_FIRST2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLEAR	NTL_FIRST2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLEAR	NTL_FIRST2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLEAR	NTL_FIRST2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLEAR	NTL_FIRST2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLEAR	NTL_FIRST2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLEAR	NTL_FIRST2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLEAR	NTL_FIRST2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLEAR	NTL_FIRST2_52: ERROR - NTL REGS - PHY timeout error indication received on a Private Register Interface response.
53	RWX_WCLEAR	NTL_FIRST2_53: ERROR - NTL REGS - NDL error error indication received on a Private Register Interface response.
54	RWX_WCLEAR	NTL_FIRST2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a Private Register Interface response.
55	RWX_WCLEAR	NTL_FIRST2_55: ERROR - NTL REGS - Bad address error indication received on a Private Register Interface response.
56	RWX_WCLEAR	NTL_FIRST2_56: ERROR - NTL REGS - Parity error error indication received on a Private Register Interface response.
57	RWX_WCLEAR	NTL_FIRST2_57: ERROR - NTL REGS - Protocol error error indication received on a Private Register Interface response.
58	RWX_WCLEAR	NTL_FIRST2_58: ERROR - NTL REGS - Private Register Interface Ack signal from NDL Wrapper went invalid in the middle of a PRI response.
59	RWX_WCLEAR	NTL_FIRST2_59: ERROR - NTL REGS - Parity error on incoming NDL Priority Register Interface (PRI) response signals.
60	RWX_WCLEAR	NTL_FIRST2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLEAR	NTL_FIRST2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLEAR	NTL_FIRST2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLEAR	NTL_FIRST2_63: ERROR - NTL REGS - Reserved.

Register Name	NTL CERR First Mask 2 Register
Mnemonic	NPU.STCK2.NTL0.REGS.CERR_FIRST_MASK2
Address	00000000050112C9 (SCOM)
Description	2 error mask register Mask errors from being captured in the First-2 Error registers and the RAS Error Message registers

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL Tx Credit signals.
1	RW	NTL_FIRST_MASK2_1: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(0:63) read from CQ_DAT.
2	RW	NTL_FIRST_MASK2_2: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(64:127) read from CQ_DAT.
3	RW	NTL_FIRST_MASK2_3: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(0:63) read from CQ_DAT.
4	RW	NTL_FIRST_MASK2_4: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(64:127) read from CQ_DAT.
5	RW	NTL_FIRST_MASK2_5: ERROR - NTL TX - Read or Atomic request with a length that is not a power of 2.
6	RW	NTL_FIRST_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RW	NTL_FIRST_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RW	NTL_FIRST_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RW	NTL_FIRST_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RW	NTL_FIRST_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RW	NTL_FIRST_MASK2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.
12	RW	NTL_FIRST_MASK2_12: ERROR - NTL TX - More than 1 entry in the 256B Ops CAM was hit at the same time.
13	RW	NTL_FIRST_MASK2_13: ERROR - NTL TX - More than 1 entry in the CREQ Sticky CAM was hit at the same time.
14	RW	NTL_FIRST_MASK2_14: ERROR - NTL TX - More than 1 entry in the DGD Sticky CAM was hit at the same time.
15	RW	NTL_FIRST_MASK2_15: ERROR - NTL TX - Reserved.
16	RW	NTL_FIRST_MASK2_16: ERROR - NTL TX - Reserved.
17	RW	NTL_FIRST_MASK2_17: ERROR - NTL TX - Reserved.
18	RW	NTL_FIRST_MASK2_18: ERROR - NTL TX - Reserved.
19	RW	NTL_FIRST_MASK2_19: ERROR - NTL TX - Reserved.
20	RW	NTL_FIRST_MASK2_20: ERROR - NTL TX - Reserved.
21	RW	NTL_FIRST_MASK2_21: ERROR - NTL TX - Reserved.
22	RW	NTL_FIRST_MASK2_22: ERROR - NTL TX - Reserved.
23	RW	NTL_FIRST_MASK2_23: ERROR - NTL TX - Reserved.
24	RW	NTL_FIRST_MASK2_24: ERROR - NTL TX - ECC Correctable Error (CE) on Data(0:63) read from CQ_DAT.

Bits	SCOM	Field Mnemonic: Description
25	RW	NTL_FIRST_MASK2_25: ERROR - NTL TX - ECC Correctable Error (CE) on Data(64:127) read from CQ_DAT.
26	RW	NTL_FIRST_MASK2_26: ERROR - NTL TX - Reserved.
27	RW	NTL_FIRST_MASK2_27: ERROR - NTL TX - Reserved.
28	RW	NTL_FIRST_MASK2_28: ERROR - NTL TX - Reserved.
29	RW	NTL_FIRST_MASK2_29: ERROR - NTL TX - Reserved.
30	RW	NTL_FIRST_MASK2_30: ERROR - NTL TX - Reserved.
31	RW	NTL_FIRST_MASK2_31: ERROR - NTL TX - Reserved.
32	RW	NTL_FIRST_MASK2_32: ERROR - NTL REGS - CREQ Header Credits received from the GPU are greater than max value.
33	RW	NTL_FIRST_MASK2_33: ERROR - NTL REGS - DGD Header Credits received from the GPU are greater than max value.
34	RW	NTL_FIRST_MASK2_34: ERROR - NTL REGS - ATSD Header Credits received from the GPU are greater than max value.
35	RW	NTL_FIRST_MASK2_35: ERROR - NTL REGS - RSP Header Credits received from the GPU are greater than max value.
36	RW	NTL_FIRST_MASK2_36: ERROR - NTL REGS - CREQ Data Credits received from the GPU are greater than max value.
37	RW	NTL_FIRST_MASK2_37: ERROR - NTL REGS - RSP Data Credits received from the GPU are greater than max value.
38	RW	NTL_FIRST_MASK2_38: ERROR - NTL REGS - Replay Buffer Credits received from NDL are greater than 512.
39	RW	NTL_FIRST_MASK2_39: ERROR - NTL REGS - Async Buffer Credits received from the NDL Wrapper are greater than 64.
40	RW	NTL_FIRST_MASK2_40: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for different NTLs.
41	RW	NTL_FIRST_MASK2_41: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for the same NTL.
42	RW	NTL_FIRST_MASK2_42: ERROR - NTL REGS - Reserved.
43	RW	NTL_FIRST_MASK2_43: ERROR - NTL REGS - Reserved.
44	RW	NTL_FIRST_MASK2_44: ERROR - NTL REGS - Reserved.
45	RW	NTL_FIRST_MASK2_45: ERROR - NTL REGS - Reserved.
46	RW	NTL_FIRST_MASK2_46: ERROR - NTL REGS - Reserved.
47	RW	NTL_FIRST_MASK2_47: ERROR - NTL REGS - Reserved.
48	RW	NTL_FIRST_MASK2_48: ERROR - NTL REGS - Reserved.
49	RW	NTL_FIRST_MASK2_49: ERROR - NTL REGS - Reserved.
50	RW	NTL_FIRST_MASK2_50: ERROR - NTL REGS - Reserved.
51	RW	NTL_FIRST_MASK2_51: ERROR - NTL REGS - Reserved.
52	RW	NTL_FIRST_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a Private Register Interface response.
53	RW	NTL_FIRST_MASK2_53: ERROR - NTL REGS - NDL error error indication received on a Private Register Interface response.
54	RW	NTL_FIRST_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a Private Register Interface response.

Bits	SCOM	Field Mnemonic: Description
55	RW	NTL_FIRST_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a Private Register Interface response.
56	RW	NTL_FIRST_MASK2_56: ERROR - NTL REGS - Parity error error indication received on a Private Register Interface response.
57	RW	NTL_FIRST_MASK2_57: ERROR - NTL REGS - Protocol error error indication received on a Private Register Interface response.
58	RW	NTL_FIRST_MASK2_58: ERROR - NTL REGS - Private Register Interface Ack signal from NDL Wrapper went invalid in the middle of a PRI response.
59	RW	NTL_FIRST_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL Priority Register Interface (PRI) response signals.
60	RW	NTL_FIRST_MASK2_60: ERROR - NTL REGS - Reserved.
61	RW	NTL_FIRST_MASK2_61: ERROR - NTL REGS - Reserved.
62	RW	NTL_FIRST_MASK2_62: ERROR - NTL REGS - Reserved.
63	RW	NTL_FIRST_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL Scratch 2 Register**
Mnemonic	NPU.STCK2.NTL0.REGS.SCRATCH2
Address	00000000050112CA (SCOM)
Description	The NTL Scratch 2 Register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH2: Scratch register.

Register Name	**NTL Scratch 3 Register**
Mnemonic	NPU.STCK2.NTL0.REGS.SCRATCH3
Address	00000000050112CB (SCOM)
Description	The NTL Scratch 3 Register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH3: Scratch register.

Register Name	**NTL Debug0 Configuration Register**
Mnemonic	NPU.STCK2.NTL0.REGS.DEBUG0_CONFIG
Address	00000000050112CC (SCOM)
Description	The NTL Debug Trace 0 Configuration Register is used to configure what debug information is sent on the Debug Trace 0 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of Debug Trace 0. 0x00 = Debug Trace 0 byte 0 inputs. 0x01 = Debug Trace 0 byte 1 inputs. 0x02 = Debug Trace 0 byte 2 inputs. 0x03 = Debug Trace 0 byte 3 inputs. 0x04 = Debug Trace 0 byte 4 inputs. 0x05 = Debug Trace 0 byte 5 inputs. 0x06 = Debug Trace 0 byte 6 inputs. 0x07 = Debug Trace 0 byte 7 inputs. 0x08 = Debug Trace 0 byte 8 inputs. 0x09 = Debug Trace 0 byte 9 inputs. 0x0A = Debug Trace 0 byte 10 inputs. 0x0B = RX Debug Group 0. 0x0C = RX Debug Group 1. 0x0D = RX Debug Group 2. 0x0E = RX Debug Group 3. 0x0F = RX Debug Group 4. 0x10 = RX Debug Group 5. 0x11 = RX Debug Group 6. 0x12 = RX Debug Group 7. 0x13 = RX Debug Group 8. 0x14 = TX Debug Group 0. 0x15 = TX Debug Group 1. 0x16 = TX Debug Group 2. 0x17 = TX Debug Group 3. 0x18 = TX Debug Group 4. 0x19 = TX Debug Group 5. 0x1A = TX Debug Group 6. 0x1B = REGS Debug Group 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of Debug Trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of Debug Trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of Debug Trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of Debug Trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of Debug Trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of Debug Trace 0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of Debug Trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of Debug Trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of Debug Trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of Debug Trace 0.
55:62	RW	DEBUG0_CONFIG_Reserved1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for Debug Trace latches.

Register Name	**NTL Debug1 Configuration Register**
Mnemonic	NPU.STCK2.NTL0.REGS.DEBUG1_CONFIG
Address	00000000050112CD (SCOM)
Description	The NTL Debug Trace 1 Configuration Register is used to configure what debug information is sent on the Debug Trace 1 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of Debug Trace 1. 0x00 = Debug Trace 1 byte 0 inputs. 0x01 = Debug Trace 1 byte 1 inputs. 0x02 = Debug Trace 1 byte 2 inputs. 0x03 = Debug Trace 1 byte 3 inputs. 0x04 = Debug Trace 1 byte 4 inputs. 0x05 = Debug Trace 1 byte 5 inputs. 0x06 = Debug Trace 1 byte 6 inputs. 0x07 = Debug Trace 1 byte 7 inputs. 0x08 = Debug Trace 1 byte 8 inputs. 0x09 = Debug Trace 1 byte 9 inputs. 0x0A = Debug Trace 1 byte 10 inputs. 0x0B = RX Debug Group 0. 0x0C = RX Debug Group 1. 0x0D = RX Debug Group 2. 0x0E = RX Debug Group 3. 0x0F = RX Debug Group 4. 0x10 = RX Debug Group 5. 0x11 = RX Debug Group 6. 0x12 = RX Debug Group 7. 0x13 = RX Debug Group 8. 0x14 = TX Debug Group 0. 0x15 = TX Debug Group 1. 0x16 = TX Debug Group 2. 0x17 = TX Debug Group 3. 0x18 = TX Debug Group 4. 0x19 = TX Debug Group 5. 0x1A = TX Debug Group 6. 0x1B = REGS Debug Group 0.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of Debug Trace 1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of Debug Trace 1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of Debug Trace 1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of Debug Trace 1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of Debug Trace 1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of Debug Trace 1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of Debug Trace 1.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of Debug Trace 1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of Debug Trace 1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of Debug Trace 1.
55:62	RW	DEBUG1_CONFIG_Reserved1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for Debug Trace latches.

Register Name	**NTL Performance Configuration Register**
Mnemonic	NPU.STCK2.NTL0.REGS.PERF_CONFIG
Address	00000000050112CE (SCOM)
Description	The NTL Performance Configuration Register is used to configure what information is counted by the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: PMULet Enable (clocks enable).

Bits	SCOM	Field Mnemonic: Description
1	RW	PERF_CONFIG_RESETMODE: 0/1 = reset-on-read/reset-on-write.
2	RW	PERF_CONFIG_FREEZEMODE: 0/1 = freerun-mode/freeze-on-any-max.
3	RW	PERF_CONFIG_DISABLE_PMISC: 0/1 = enable-pmisc/disable-pmisc control of counters.
4	RW	PERF_CONFIG_PMISC_MODE: 0/1 = global pmu pmisc no reset/global pmu pmisc reset-on-enable.
5:7	RW	PERF_CONFIG_CASCADE: PMULet cascade config.
8:9	RW	PERF_CONFIG_PRESCALE_C0: prescale config for counter 0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: prescale config for counter 1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: prescale config for counter 2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: prescale config for counter 3.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select: 0x00 = Disable. 0x01 = Cycles. 0x02 = Latency events. 0x03 = Latency cycles. 0x04 = Latency aborts. 0x20 = REGS - NDL PRI request. 0x21 = REGS - NDL PRI Write request. 0x22 = REGS - NDL PRI Read request. 0x23 = REGS - PHY PRI request. 0x24 = REGS - PHY PRI Write request. 0x25 = REGS - PHY PRI Read request. 0x40 = TX - any flit sent. 0x41 = TX - Header flit sent. 0x42 = TX - AE flit sent. 0x43 = TX - BE flit sent. 0x44 = TX - Data flit sent. 0x45 = TX - Flow Control packet. 0x46 = TX - Write.NC. 0x47 = TX - Write.NC 128B. 0x48 = TX - Write.NC 32-96B. 0x49 = TX - Write.NC 1-16B. 0x4A = TX - Write.NC with BE flit. 0x4B = TX - Read. 0x4C = TX - Upgrade. 0x4D = TX - Atomic. 0x4E = TX - Downgrade. 0x4F = TX - ATSD. 0x50 = TX - Request Response no-data. 0x51 = TX - Request Response with-data. 0x52 = TX - Probe Response no-data. 0x53 = TX - Probe Response with-data. 0x54 = TX - ATR Response. 0x55 = TX - TransDone Response no-data. 0x56 = TX - TransDone Response with-data. 0x57 = TX - TransDone Response with-data 128B. 0x58 = TX - TransDone Response with-data 32-96B. 0x59 = TX - TransDone Response with-data 1-16B. 0x5A = TX - TransDone Response with-data with BE flit. 0x5B = TX - Not enough CREQ Header Credits. 0x5C = TX - Not enough DGD Header Credits. 0x5D = TX - Not enough ATSD Header Credits. 0x5E = TX - Not enough RSP Header Credits. 0x5F = TX - Not enough CREQ Data Credits. 0x60 = TX - Not enough RSP Data Credits.

Bits	SCOM	Field Mnemonic: Description
		0x61 = TX - Not enough Replay Buffer Credits. 0x62 = TX - Not enough Async Buffer Credits. 0x80 = RX - CREQ Header Array full. 0x81 = RX - PRB Header Array full. 0x82 = RX - ATR Header Array full. 0x83 = RX - RSP Header Array full. 0x84 = RX - CREQ Data Array full. 0x85 = RX - RSP Data Array full. 0x86 = RX - any flit received. 0x87 = RX - Header flit received. 0x88 = RX - AE flit received. 0x89 = RX - BE flit received. 0x8A = RX - Data flit received. 0x8B = RX - NOP Flow Control flit received. 0x8C = RX - Write.NC (UT = 0). 0x8D = RX - Write.NC (UT = 1). 0x8E = RX - Write.NC (UT = 0) 128B. 0x8F = RX - Write.NC (UT = 1) 128B. 0x90 = RX - Write.NC (UT = 0) 256B. 0x91 = RX - Write.NC (UT = 1) 256B. 0x92 = RX - Write.NC (UT = 0) 32-96B. 0x93 = RX - Write.NC (UT = 1) 32-96B. 0x94 = RX - Write.NC (UT = 0) 1-16B. 0x95 = RX - Write.NC (UT = 1) 1-16B. 0x96 = RX - Write.NC (UT = 0) w/ BE flit. 0x97 = RX - Write.NC (UT = 1) w/ BE flit. 0x98 = RX - Write.NC (UT = 0) to MMIO Space. 0x99 = RX - Write.NC (UT = 0) to MMIO Space and split into mult requests. 0x9A = RX - Write.NC (UT = 1) and split into mult requests. 0x9B = RX - Read.NC (UT = 0). 0x9C = RX - Read.NC (UT = 1). 0x9D = RX - Read.NC (UT = 0) 128B. 0x9E = RX - Read.NC (UT = 1) 128B. 0x9F = RX - Read.NC (UT = 0) 256B. 0xA0 = RX - Read.NC (UT = 1) 256B. 0xA1 = RX - Read.NC (UT = 0) 32-96B. 0xA2 = RX - Read.NC (UT = 1) 32-96B. 0xA3 = RX - Read.NC (UT = 0) 1-16B. 0xA4 = RX - Read.NC (UT = 1) 1-16B. 0xA5 = RX - Flush. 0xA6 = RX - RMW. 0xA7 = RX - Atomic.NR. 0xA8 = RX - Atomic.RR. 0xA9 = RX - Probe.I.MO. 0xAA = RX - Probe.I.N. 0xAB = RX - Probe.X.MO. 0xAC = RX - ATR. 0xAD = RX - ReqRsp.ND. 0xAE = RX - ReqRsp.D. 0xAF = RX - DGDRsp. 0xB0 = RX - ATSDRsp. 0xB1 = RX - TransDone.ND. 0xB2 = RX - TransDone.D. 0xB3 = RX - TransDone.D w/ BE flit. 0xB4 = RX - CREQ non-Flush waiting for CQ Credit. 0xB5 = RX - CREQ Flush waiting for CQ Credit. 0xB6 = RX - CREQ waiting for Global Credit. 0xB7 = RX - CREQ 256B operation waiting for 256B Ops CAM entry. 0xB8 = RX - PRB waiting for CQ Credit. 0xB9 = RX - PRB waiting for Global Credit.

Bits	SCOM	Field Mnemonic: Description
		0xBA = RX - ATR waiting for CQ Credit. 0xBB = RX - ATR waiting for Global Credit.
24:31	RW	PERF_CONFIG_EVENT1: Event 1 select (see Event 0 select for encodes).
32:39	RW	PERF_CONFIG_EVENT2: Event 2 select (see Event 0 select for encodes).
40:47	RW	PERF_CONFIG_EVENT3: Event 3 select (see Event 0 select for encodes).
48:50	RW	PERF_CONFIG_LATENCY: Latency select: 0 = Disable. 1 = Read.NC to Response. 2 = Write.RR to Response. 3 = Atomic.RR to Response. 4 = RMW to Response. 5 = Flush to Response. 6 = Probe to Response. 7 = ATR to Response.
51:63	RW	PERF_CONFIG_Reserved: Reserved.

Register Name	**NTL Performance Count Register**
Mnemonic	NPU.STCK2.NTL0.REGS.PERF_COUNT
Address	00000000050112CF (SCOM)
Description	The NTL Performance Count Register holds the performance counts from the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	IDIAL_PERF_COUNT0: Performance Counter 0.
16:31	RWX_WCLRREG	IDIAL_PERF_COUNT1: Performance Counter 1.
32:47	RWX_WCLRREG	IDIAL_PERF_COUNT2: Performance Counter 2.
48:63	RWX_WCLRREG	IDIAL_PERF_COUNT3: Performance Counter 3.

Register Name	**NTL CREQ Header Array Pointer Register**
Mnemonic	NPU.STCK2.NTL0.REGS.CREQ_HA_PTR
Address	00000000050112D0 (SCOM)
Description	The NTL CREQ Header Array Pointer Register is used to change the start and/or end entry in the NTL Header Array for holding CREQ header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	CREQ_HA_PTR_Reserved1: Reserved.
5:11	RW	CREQ_HA_PTR_START: Starting Header Array location for CREQ headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	CREQ_HA_PTR_Reserved2: Reserved.
17:23	RW	CREQ_HA_PTR_END: Ending Header Array location for CREQ headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL PRB Header Array Pointer Register
Mnemonic	NPU.STCK2.NTL0.REGS.PRB_HA_PTR
Address	00000000050112D1 (SCOM)
Description	The NTL PRB Header Array Pointer Register is used to change the start and/or end entry in the NTL Header Array for holding PRB header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	PRB_HA_PTR_Reserved1: Reserved.
5:11	RW	PRB_HA_PTR_START: Starting Header Array location for PRB headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	PRB_HA_PTR_Reserved2: Reserved.
17:23	RW	PRB_HA_PTR_END: Ending Header Array location for PRB headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL ATR Header Array Pointer Register
Mnemonic	NPU.STCK2.NTL0.REGS.ATR_HA_PTR
Address	00000000050112D2 (SCOM)
Description	The NTL ATR Header Array Pointer Register is used to change the start and/or end entry in the NTL Header Array for holding ATR header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	ATR_HA_PTR_Reserved1: Reserved.
5:11	RW	ATR_HA_PTR_START: Starting Header Array location for ATR headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	ATR_HA_PTR_Reserved2: Reserved.
17:23	RW	ATR_HA_PTR_END: Ending Header Array location for ATR headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Header Array Pointer Register
Mnemonic	NPU.STCK2.NTL0.REGS.RSP_HA_PTR
Address	00000000050112D3 (SCOM)
Description	The NTL RSP Header Array Pointer Register is used to change the start and/or end entry in the NTL Header Array for holding RSP header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	RSP_HA_PTR_Reserved1: Reserved.
5:11	RW	RSP_HA_PTR_START: Starting Header Array location for RSP headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.

Bits	SCOM	Field Mnemonic: Description
12:16	RW	RSP_HA_PTR_Reserved2: Reserved.
17:23	RW	RSP_HA_PTR_END: Ending Header Array location for RSP headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL CREQ Data Array Pointer Register
Mnemonic	NPU.STCK2.NTL0.REGS.CREQ_DA_PTR
Address	00000000050112D4 (SCOM)
Description	The NTL CREQ Data Array Pointer Register is used to change the start and/or end entry in the NTL Data Array for holding CREQ data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	CREQ_DA_PTR_Reserved1: Reserved.
3:11	RW	CREQ_DA_PTR_START: Starting Data Array location for CREQ data flits received from the GPU. The Data Array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	CREQ_DA_PTR_Reserved2: Reserved.
15:23	RW	CREQ_DA_PTR_END: Ending Data Array location for CREQ data flits received from the GPU. The Data Array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Data Array Pointer Register
Mnemonic	NPU.STCK2.NTL0.REGS.RSP_DA_PTR
Address	00000000050112D5 (SCOM)
Description	The NTL RSP Data Array Pointer Register is used to change the start and/or end entry in the NTL Data Array for holding RSP data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	RSP_DA_PTR_Reserved1: Reserved.
3:11	RW	RSP_DA_PTR_START: Starting Data Array location for RSP data flits received from the GPU. The Data Array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	RSP_DA_PTR_Reserved2: Reserved.
15:23	RW	RSP_DA_PTR_END: Ending Data Array location for RSP data flits received from the GPU. The Data Array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL Private Register Interface (PRI) Configuration Register
Mnemonic	NPU.STCK2.NTL0.REGS.PRI_CONFIG
Address	00000000050112D6 (SCOM)
Description	The NTL PRI Configuration Register is used to set up the Private Register Interface settings for this NTL. This register must be configured before any PRI requests are attempted to NDL or PHY registers.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PRI_CONFIG_NDL: NDL indication sent in the PRI Read/Write access: 00 = NDL 0. 01 = NDL 1. 10 = NDL 2. 11 = Disable (this will disable NTL from decoding the NDL register space).
2:3	RW	PRI_CONFIG_PHY: Indicates if this NTL should decode a PHY register space: 00 = Decode PHY0 register space (one and only one NTL that is connected to PHY 0 must be set to this value). 01 = Decode PHY1 register space (one and only one NTL that is connected to PHY 1 must be set to this value). 1- = Do not decode any PHY register space.
4:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	NTL Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK2.NTL0.REGS.CONFIG1
Address	00000000050112D8 (SCOM)
Description	The NVLink transaction layer (NTL) Miscellaneous Configuration 1 Register is used to control NVLink packet formatting by the POWER9 processor. It also controls resetting of the POWER9 NTL.

Bits	SCOM	Field Mnemonic: Description
0	RW	COMPRESSED_RSP_ENA: When 0b1, NTL will attempt to compress responses that it sends to the GPU whenever possible.
1:3	RW	CONFIG1_Reserved1: Reserved.
4	RW	CREQ_AE_ALWAYS: When 0b1, NTL will always send an AE flit when it sends a CREQ packet to the GPU.
5	RW	DGD_AE_ALWAYS: When 0b1, NTL will always send an AE flit when it sends a Downgrade packet to the GPU.
6	RW	RSP_AE_ALWAYS: When 0b1, NTL will always send an AE flit when it sends a Response packet to the GPU.
7	RW	CONFIG1_Reserved2: Reserved.
8:9	RW	NTL_RESET: This field indicates the NTL Reset mode: 00 - Reset disabled. 11 - Reset (Fence) both NTL and the processor bus for this Brick. 10 - Reset (Fence) only the processor bus for this Brick, NTL will be operational. 01 - Reserved. The only legal sequence is 00->11->10->00. This field should not be changed unless bits 0:1 in the CQ Fence Status register equals the value in this field.
10:63	RW	CONFIG1_Reserved3: Reserved.

Register Name	NTL Scratch 1 Register
Mnemonic	NPU.STCK2.NTL0.REGS.SCRATCH1
Address	00000000050112DA (SCOM)
Description	The NTL Scratch 1 Register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH1: Scratch register.

Register Name	NTL Low Power Configuration Register
Mnemonic	NPU.STCK2.NTL0.REGS.LOW_PWR
Address	00000000050112DC (SCOM)
Description	The NTL Low Power Configuration Register is used to enable the NPU to request that the NVLink interconnect be placed into low-power mode. The register also defines the conditions under which the NPU turns its low-power request on or off.

Bits	SCOM	Field Mnemonic: Description
0	RW	LP_MODE_ENABLE: When 0b1, this NTL is allowed to activate the Low Power Requested signal to NDL when the Low Power Count > = Low Power Count Threshold.
1	RW	LP_ONLY_MODE: When 0b1, this NTL will activate the Low Power Requested signal to NDL continuously. This can be used for lab stress/debug.
2:7	RW	LP_TIMER_TICK_CONFIG: Rate for the Low Power timer tick (2^n cycles).
8:19	RW	LP_MIN_CRED_THRESH: Whenever the NDL Replay Buffer Credits < this threshold, the Low Power Requested signal to NDL will be de-activated. This value must be greater than 0 and less than the Max Credit Threshold.
20:31	RW	LP_MAX_CRED_THRESH: Whenever the NDL Replay Buffer Credits > = this threshold and the Low Power timer tick is active, then the Low Power Count will be incremented by 1. This value must be greater than the Min Credit Threshold.
32:43	RW	LP_CNT_THRESH: Whenever the Low Power Count > = this threshold, this NTL will activate the Low Power Requested signal to NDL until the NDL Replay Buffer Credits < Low Power Min Credit Threshold. This value must be greater than 0.
44:63	RO	Constant = 0b00000000000000000000

Register Name	NTL Miscellaneous Configuration 2 Register
Mnemonic	NPU.STCK2.NTL1.REGS.CONFIG2
Address	00000000050112E0 (SCOM)
Description	The NTL Miscellaneous Configuration 2 Register is used to control internal NTL function. It contains mode bits, chicken switches, and thresholds.

Bits	SCOM	Field Mnemonic: Description
0	RW	BRICK_ENABLE: When 0b1, this NVLink brick is enabled. This configuration bit will be used as a general clock gate for latches in the NTL design.
1	RW	RSP_CTL_CRED_SINGLE_ENA: When 0b1, NTL will only give CQ_CTL 1 RSP credit at a time, instead of the normal 2.
2	RW	CREQ_BE_128: When 0b1, NTL will always send 128 bytes of data when it needs to send a Byte Enable (BE) flit to the GPU for a CREQ packet. When 0b0, NTL will send the least number of data flits required.

Bits	SCOM	Field Mnemonic: Description
3	RW	DGD_BE_128: When 0b1, NTL will always send 128 bytes of data when it needs to send a Byte Enable (BE) flit to the GPU for a Downgrade packet (BE and data flits are sent in the TransDone packet for the Downgrade). When 0b0, NTL will send the least number of data flits required.
4	RW	WR_SPLIT_UT0_ENA: When 0b1, NTL will split up Write requests with UT = 0 from the GPU that map to MMIO space into legal processor bus sizes/alignments. When 0b0, NTL will pass all Write requests with UT = 0 as is to CQ.
5	RW	WR_SPLIT_UT1_ENA: When 0b1, NTL will split up Write requests with UT = 1 from the GPU into legal processor bus sizes/alignments. This will include both DMA Writes and MMIO Writes since there is no way for NTL to distinguish between them. When 0b0, NTL will pass all Write requests with UT = 1 as is to CQ.
6	RW	BRICK_DEBUG_MODE: When 0b1, NTL will ignore all incoming NVLink packets from the GPU and will throw away all NVLink requests/responses from CQ destined for the GPU. This mode is used for debug purposes only when the NPU is not connected over NVLink to a GPU.
7	RW	P9_TO_P9_MODE: When 0b1, NTL will set UT = 1 for all incoming Read, Write, and Atomic NVLink packets before sending to CQ. This mode is used for debug purposes only when the NPU is connected to another/same NPU over NVLink.
8:9	RW	CONFIG2_Reserved1: Reserved.
10:15	RW	CAM256_MAX_CNT: This field specifies the number of entries in the CAM that holds information to send Responses for 256 byte operations that require a Response. (max value = 48).
16	RW	NDL_RX_PARITY_ENA: When 0b1, NTL will check parity on the incoming NDL RX signals.
17	RW	NDL_TX_PARITY_ENA: When 0b1, NTL will check parity on the incoming NDL TX (that is, TX Credits) signals.
18	RW	NDL_PRI_PARITY_ENA: When 0b1, NTL will check parity on the incoming NDL Priority Register Interface signals.
19	RW	RCV_CREDIT_OVERFLOW_ENA: When 0b1, NTL will check for overflows on any Received Credits from the GPU, NDL, and NDL Wrapper.
20	RW	HDR_ARR_ECC_CORR_ENA: When 0b1, NTL will correct ECC SBEs when reading the Rx Header Array.
21	RW	DAT_ARR_ECC_CORR_ENA: When 0b1, NTL will correct ECC SBEs when reading the Rx Data Array. NTL will only correct ECC on reads of the Rx Data Array that require NTL to update the data before sending to CQ_DAT (for example, BE flit or Data flits for Atomic CAS ops).
22	RW	TX_DATA_ECC_CORR_ENA: When 0b1, NTL will correct ECC SBEs when reading Tx Data from CQ_DAT.
23	RW	CONFIG2_Reserved2: Reserved.
24	RW	PARITY_ERROR_SUE_ENA: When 0b1, NTL will drive SUE on all Data transfers to CQ_DAT for a packet that has a parity error on an incoming Data flit.
25	RW	DATA_POISON_SUE_ENA: When 0b1, NTL will drive SUE on all Data transfers to CQ_DAT for a packet that receives LMD = Data Poison.
26	RW	HDR_ARR_ECC_SUE_ENA: When 0b1, NTL will drive SUE on all Data transfers to CQ_DAT for a packet that has an ECC UE/SUE on the header info read from the Rx Header Array.
27	RW	DAT_ARR_ECC_SUE_ENA: When 0b1, NTL will drive SUE on all Data transfers to CQ_DAT for a packet that has an ECC UE/SUE on data read from the Rx Data Array. NTL will only check ECC on reads of the Rx Data Array that require NTL to update the data before sending to CQ_DAT (for example, BE flit or Data flits for Atomic CAS ops).
28	RW	TX_ECC_DATA_POISON_ENA: When 0b1, NTL will send LMD = Data Poison for an outgoing NVLink packet that encounters an ECC UE/SUE on data read from CQ_DAT.
29:31	RW	CONFIG2_Reserved3: Reserved.
32	RW	PRI_STATE_MACHINE_RESET: Reset Priority Register Interface (PRI) state machine to Idle state (Debug use only).
33:63	RW	CONFIG2_Reserved4: Reserved.

Register Name	NTL Miscellaneous Configuration 3 Register
Mnemonic	NPU.STCK2.NTL1.REGS.CONFIG3
Address	00000000050112E1 (SCOM)
Description	The NTL Miscellaneous Configuration 3 Register is used for future control of internal NTL functions. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG3_Reserved1: Reserved.

Register Name	NTL CERR Hold 1 Register
Mnemonic	NPU.STCK2.NTL1.REGS.CERR_HOLD1
Address	00000000050112E2 (SCOM)
Description	c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLRREG	NTL_HOLD1_1: ERROR - NTL RX - AN / = 1 in an incoming NVLink packet where Rx Vld = 1 and Rx Hdr Vld = 1.
2	RWX_WCLRREG	NTL_HOLD1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the Address field is valid.
3	RWX_WCLRREG	NTL_HOLD1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the Address field is valid.
4	RWX_WCLRREG	NTL_HOLD1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink Read,Write,Atomic,RMW request packet.
5	RWX_WCLRREG	NTL_HOLD1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLRREG	NTL_HOLD1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid, and not Read nor Write.
7	RWX_WCLRREG	NTL_HOLD1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink ReqRsp with Data packet.
8	RWX_WCLRREG	NTL_HOLD1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	RWX_WCLRREG	NTL_HOLD1_9: ERROR - NTL RX - Compressed Responses not populated in the order CR0,CR1,CR2 in an incoming NVLink response packet.
10	RWX_WCLRREG	NTL_HOLD1_10: ERROR - NTL RX - Compressed Response with an Invalid/Reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLRREG	NTL_HOLD1_11: ERROR - NTL RX - Address(63:49) / = 0 in an incoming NVLink request packet where the Address field is valid.
12	RWX_WCLRREG	NTL_HOLD1_12: ERROR - NTL RX - Address(48:47) / = 0 in an incoming NVLink UT = 0 request packet where the Address field is valid, and not ATR.
13	RWX_WCLRREG	NTL_HOLD1_13: ERROR - NTL RX - DatLen / = 16,32,64,128B in an incoming NVLink Probe packet.
14	RWX_WCLRREG	NTL_HOLD1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink ReqRsp with Data packet.
15	RWX_WCLRREG	NTL_HOLD1_15: ERROR - NTL RX - AtomicSz / = 4B or 8B in an incoming NVLink Atomic packet.
16	RWX_WCLRREG	NTL_HOLD1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink Atomic packet where no BE flit exists.

Bits	SCOM	Field Mnemonic: Description
17	RWX_WCLRREG	NTL_HOLD1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLRREG	NTL_HOLD1_18: ERROR - NTL RX - Reserved.
19	RWX_WCLRREG	NTL_HOLD1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLRREG	NTL_HOLD1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLRREG	NTL_HOLD1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLRREG	NTL_HOLD1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLRREG	NTL_HOLD1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLRREG	NTL_HOLD1_24: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Header Array.
25	RWX_WCLRREG	NTL_HOLD1_25: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Header Array.
26	RWX_WCLRREG	NTL_HOLD1_26: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(128:167) read from the Header Array.
27	RWX_WCLRREG	NTL_HOLD1_27: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Data Array.
28	RWX_WCLRREG	NTL_HOLD1_28: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Data Array.
29	RWX_WCLRREG	NTL_HOLD1_29: ERROR - NTL RX - Parity error on incoming NDL Rx Vld and Hdr_Vld signals.
30	RWX_WCLRREG	NTL_HOLD1_30: ERROR - NTL RX - Parity error on incoming NDL Rx LMD and CRC signals.
31	RWX_WCLRREG	NTL_HOLD1_31: ERROR - NTL RX - Parity error on incoming NDL Rx Header flit signals.
32	RWX_WCLRREG	NTL_HOLD1_32: ERROR - NTL RX - Parity error on incoming NDL Rx AE flit signals.
33	RWX_WCLRREG	NTL_HOLD1_33: ERROR - NTL RX - Parity error on incoming NDL Rx Data flit signals.
34	RWX_WCLRREG	NTL_HOLD1_34: ERROR - NTL RX - An NVLink packet with data received LMD = Data Poison.
35	RWX_WCLRREG	NTL_HOLD1_35: ERROR - NTL RX - New CREQ Header flit from NVLink received when the CREQ Header Array is full.
36	RWX_WCLRREG	NTL_HOLD1_36: ERROR - NTL RX - New CREQ Data flit from NVLink received when the CREQ Data Array is full.
37	RWX_WCLRREG	NTL_HOLD1_37: ERROR - NTL RX - CREQ Data flit was attempted to be read from the CREQ Data Array when it was empty.
38	RWX_WCLRREG	NTL_HOLD1_38: ERROR - NTL RX - New RSP Header flit from NVLink received when the RSP Header Array is full.
39	RWX_WCLRREG	NTL_HOLD1_39: ERROR - NTL RX - New RSP Data flit from NVLink received when the RSP Data Array is full.
40	RWX_WCLRREG	NTL_HOLD1_40: ERROR - NTL RX - RSP Data flit was attempted to be read from the RSP Data Array when it was empty.
41	RWX_WCLRREG	NTL_HOLD1_41: ERROR - NTL RX - New PRB Header flit from NVLink received when the PRB Header Array is full.
42	RWX_WCLRREG	NTL_HOLD1_42: ERROR - NTL RX - New ATR Header flit from NVLink received when the ATR Header Array is full.
43	RWX_WCLRREG	NTL_HOLD1_43: ERROR - NTL RX - A new NVLink Header flit was received when NTL was still expecting Data flits for the previous packet.
44	RWX_WCLRREG	NTL_HOLD1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or Data Array on the same cycle.
45	RWX_WCLRREG	NTL_HOLD1_45: ERROR - NTL RX - A CQ Slice Credit was received when one was already valid (overflow).

Bits	SCOM	Field Mnemonic: Description
46	RWX_WCLRREG	NTL_HOLD1_46: ERROR - NTL RX - A CQ ATR Credit was received when one was already valid (overflow).
47	RWX_WCLRREG	NTL_HOLD1_47: ERROR - NTL RX - A CQ Flush Credit was received when 15 were already valid (overflow).
48	RWX_WCLRREG	NTL_HOLD1_48: ERROR - NTL RX - A CQ Global Credit was received when 3 were already valid (overflow).
49	RWX_WCLRREG	NTL_HOLD1_49: ERROR - NTL RX - A CQ Response Credit was received when one was already valid (overflow).
50	RWX_WCLRREG	NTL_HOLD1_50: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLRREG	NTL_HOLD1_51: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLRREG	NTL_HOLD1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLRREG	NTL_HOLD1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLRREG	NTL_HOLD1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLRREG	NTL_HOLD1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLRREG	NTL_HOLD1_56: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Header Array.
57	RWX_WCLRREG	NTL_HOLD1_57: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Header Array.
58	RWX_WCLRREG	NTL_HOLD1_58: ERROR - NTL RX - ECC Correctable Error (CE) on Data(128:167) read from the Header Array.
59	RWX_WCLRREG	NTL_HOLD1_59: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Data Array.
60	RWX_WCLRREG	NTL_HOLD1_60: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Data Array.
61	RWX_WCLRREG	NTL_HOLD1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLRREG	NTL_HOLD1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLRREG	NTL_HOLD1_63: ERROR - NTL RX - Reserved.

Register Name	NTL CERR Mask 1 Register
Mnemonic	NPU.STCK2.NTL1.REGS.CERR_MASK1
Address	00000000050112E3 (SCOM)
Description	c_err_rpt mask latches read-only reg

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	ROX	NTL_MASK1_1: ERROR - NTL RX - AN / = 1 in an incoming NVLink packet where Rx Vld = 1 and Rx Hdr Vld = 1.
2	ROX	NTL_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the Address field is valid.
3	ROX	NTL_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the Address field is valid.

Bits	SCOM	Field Mnemonic: Description
4	ROX	NTL_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink Read,Write,Atomic,RMW request packet.
5	ROX	NTL_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	ROX	NTL_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid, and not Read nor Write.
7	ROX	NTL_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink ReqRsp with Data packet.
8	ROX	NTL_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	ROX	NTL_MASK1_9: ERROR - NTL RX - Compressed Responses not populated in the order CR0,CR1,CR2 in an incoming NVLink response packet.
10	ROX	NTL_MASK1_10: ERROR - NTL RX - Compressed Response with an Invalid/Reserved TD/IVC combination in an incoming NVLink response packet.
11	ROX	NTL_MASK1_11: ERROR - NTL RX - Address(63:49) / = 0 in an incoming NVLink request packet where the Address field is valid.
12	ROX	NTL_MASK1_12: ERROR - NTL RX - Address(48:47) / = 0 in an incoming NVLink UT = 0 request packet where the Address field is valid, and not ATR.
13	ROX	NTL_MASK1_13: ERROR - NTL RX - DatLen / = 16,32,64,128B in an incoming NVLink Probe packet.
14	ROX	NTL_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink ReqRsp with Data packet.
15	ROX	NTL_MASK1_15: ERROR - NTL RX - AtomicSz / = 4B or 8B in an incoming NVLink Atomic packet.
16	ROX	NTL_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink Atomic packet where no BE flit exists.
17	ROX	NTL_MASK1_17: ERROR - NTL RX - Reserved.
18	ROX	NTL_MASK1_18: ERROR - NTL RX - Reserved.
19	ROX	NTL_MASK1_19: ERROR - NTL RX - Reserved.
20	ROX	NTL_MASK1_20: ERROR - NTL RX - Reserved.
21	ROX	NTL_MASK1_21: ERROR - NTL RX - Reserved.
22	ROX	NTL_MASK1_22: ERROR - NTL RX - Reserved.
23	ROX	NTL_MASK1_23: ERROR - NTL RX - Reserved.
24	ROX	NTL_MASK1_24: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Header Array.
25	ROX	NTL_MASK1_25: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Header Array.
26	ROX	NTL_MASK1_26: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(128:167) read from the Header Array.
27	ROX	NTL_MASK1_27: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Data Array.
28	ROX	NTL_MASK1_28: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Data Array.
29	ROX	NTL_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL Rx Vld and Hdr_Vld signals.
30	ROX	NTL_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL Rx LMD and CRC signals.
31	ROX	NTL_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL Rx Header flit signals.
32	ROX	NTL_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL Rx AE flit signals.
33	ROX	NTL_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL Rx Data flit signals.

Bits	SCOM	Field Mnemonic: Description
34	ROX	NTL_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = Data Poison.
35	ROX	NTL_MASK1_35: ERROR - NTL RX - New CREQ Header flit from NVLink received when the CREQ Header Array is full.
36	ROX	NTL_MASK1_36: ERROR - NTL RX - New CREQ Data flit from NVLink received when the CREQ Data Array is full.
37	ROX	NTL_MASK1_37: ERROR - NTL RX - CREQ Data flit was attempted to be read from the CREQ Data Array when it was empty.
38	ROX	NTL_MASK1_38: ERROR - NTL RX - New RSP Header flit from NVLink received when the RSP Header Array is full.
39	ROX	NTL_MASK1_39: ERROR - NTL RX - New RSP Data flit from NVLink received when the RSP Data Array is full.
40	ROX	NTL_MASK1_40: ERROR - NTL RX - RSP Data flit was attempted to be read from the RSP Data Array when it was empty.
41	ROX	NTL_MASK1_41: ERROR - NTL RX - New PRB Header flit from NVLink received when the PRB Header Array is full.
42	ROX	NTL_MASK1_42: ERROR - NTL RX - New ATR Header flit from NVLink received when the ATR Header Array is full.
43	ROX	NTL_MASK1_43: ERROR - NTL RX - A new NVLink Header flit was received when NTL was still expecting Data flits for the previous packet.
44	ROX	NTL_MASK1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or Data Array on the same cycle.
45	ROX	NTL_MASK1_45: ERROR - NTL RX - A CQ Slice Credit was received when one was already valid (overflow).
46	ROX	NTL_MASK1_46: ERROR - NTL RX - A CQ ATR Credit was received when one was already valid (overflow).
47	ROX	NTL_MASK1_47: ERROR - NTL RX - A CQ Flush Credit was received when 15 were already valid (overflow).
48	ROX	NTL_MASK1_48: ERROR - NTL RX - A CQ Global Credit was received when 3 were already valid (overflow).
49	ROX	NTL_MASK1_49: ERROR - NTL RX - A CQ Response Credit was received when one was already valid (overflow).
50	ROX	NTL_MASK1_50: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	ROX	NTL_MASK1_51: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	ROX	NTL_MASK1_52: ERROR - NTL RX - Reserved.
53	ROX	NTL_MASK1_53: ERROR - NTL RX - Reserved.
54	ROX	NTL_MASK1_54: ERROR - NTL RX - Reserved.
55	ROX	NTL_MASK1_55: ERROR - NTL RX - Reserved.
56	ROX	NTL_MASK1_56: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Header Array.
57	ROX	NTL_MASK1_57: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Header Array.
58	ROX	NTL_MASK1_58: ERROR - NTL RX - ECC Correctable Error (CE) on Data(128:167) read from the Header Array.
59	ROX	NTL_MASK1_59: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Data Array.

Bits	SCOM	Field Mnemonic: Description
60	ROX	NTL_MASK1_60: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Data Array.
61	ROX	NTL_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	ROX	NTL_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	ROX	NTL_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First 1 Register**
Mnemonic	NPU.STCK2.NTL1.REGS.CERR_FIRST1
Address	00000000050112E4 (SCOM)
Description	c_err_rpt first error latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RWX_WCLEAR	NTL_FIRST1_1: ERROR - NTL RX - AN / = 1 in an incoming NVLink packet where Rx Vld = 1 and Rx Hdr Vld = 1.
2	RWX_WCLEAR	NTL_FIRST1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the Address field is valid.
3	RWX_WCLEAR	NTL_FIRST1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the Address field is valid.
4	RWX_WCLEAR	NTL_FIRST1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink Read,Write,Atomic,RMW request packet.
5	RWX_WCLEAR	NTL_FIRST1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RWX_WCLEAR	NTL_FIRST1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid, and not Read nor Write.
7	RWX_WCLEAR	NTL_FIRST1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink ReqRsp with Data packet.
8	RWX_WCLEAR	NTL_FIRST1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	RWX_WCLEAR	NTL_FIRST1_9: ERROR - NTL RX - Compressed Responses not populated in the order CR0,CR1,CR2 in an incoming NVLink response packet.
10	RWX_WCLEAR	NTL_FIRST1_10: ERROR - NTL RX - Compressed Response with an Invalid/Reserved TD/IVC combination in an incoming NVLink response packet.
11	RWX_WCLEAR	NTL_FIRST1_11: ERROR - NTL RX - Address(63:49) / = 0 in an incoming NVLink request packet where the Address field is valid.
12	RWX_WCLEAR	NTL_FIRST1_12: ERROR - NTL RX - Address(48:47) / = 0 in an incoming NVLink UT = 0 request packet where the Address field is valid, and not ATR.
13	RWX_WCLEAR	NTL_FIRST1_13: ERROR - NTL RX - DatLen / = 16,32,64,128B in an incoming NVLink Probe packet.
14	RWX_WCLEAR	NTL_FIRST1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink ReqRsp with Data packet.
15	RWX_WCLEAR	NTL_FIRST1_15: ERROR - NTL RX - AtomicSz / = 4B or 8B in an incoming NVLink Atomic packet.
16	RWX_WCLEAR	NTL_FIRST1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink Atomic packet where no BE flit exists.
17	RWX_WCLEAR	NTL_FIRST1_17: ERROR - NTL RX - Reserved.
18	RWX_WCLEAR	NTL_FIRST1_18: ERROR - NTL RX - Reserved.

Bits	SCOM	Field Mnemonic: Description
19	RWX_WCLEAR	NTL_FIRST1_19: ERROR - NTL RX - Reserved.
20	RWX_WCLEAR	NTL_FIRST1_20: ERROR - NTL RX - Reserved.
21	RWX_WCLEAR	NTL_FIRST1_21: ERROR - NTL RX - Reserved.
22	RWX_WCLEAR	NTL_FIRST1_22: ERROR - NTL RX - Reserved.
23	RWX_WCLEAR	NTL_FIRST1_23: ERROR - NTL RX - Reserved.
24	RWX_WCLEAR	NTL_FIRST1_24: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Header Array.
25	RWX_WCLEAR	NTL_FIRST1_25: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Header Array.
26	RWX_WCLEAR	NTL_FIRST1_26: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(128:167) read from the Header Array.
27	RWX_WCLEAR	NTL_FIRST1_27: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Data Array.
28	RWX_WCLEAR	NTL_FIRST1_28: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Data Array.
29	RWX_WCLEAR	NTL_FIRST1_29: ERROR - NTL RX - Parity error on incoming NDL Rx Vld and Hdr_Vld signals.
30	RWX_WCLEAR	NTL_FIRST1_30: ERROR - NTL RX - Parity error on incoming NDL Rx LMD and CRC signals.
31	RWX_WCLEAR	NTL_FIRST1_31: ERROR - NTL RX - Parity error on incoming NDL Rx Header flit signals.
32	RWX_WCLEAR	NTL_FIRST1_32: ERROR - NTL RX - Parity error on incoming NDL Rx AE flit signals.
33	RWX_WCLEAR	NTL_FIRST1_33: ERROR - NTL RX - Parity error on incoming NDL Rx Data flit signals.
34	RWX_WCLEAR	NTL_FIRST1_34: ERROR - NTL RX - An NVLink packet with data received LMD = Data Poison.
35	RWX_WCLEAR	NTL_FIRST1_35: ERROR - NTL RX - New CREQ Header flit from NVLink received when the CREQ Header Array is full.
36	RWX_WCLEAR	NTL_FIRST1_36: ERROR - NTL RX - New CREQ Data flit from NVLink received when the CREQ Data Array is full.
37	RWX_WCLEAR	NTL_FIRST1_37: ERROR - NTL RX - CREQ Data flit was attempted to be read from the CREQ Data Array when it was empty.
38	RWX_WCLEAR	NTL_FIRST1_38: ERROR - NTL RX - New RSP Header flit from NVLink received when the RSP Header Array is full.
39	RWX_WCLEAR	NTL_FIRST1_39: ERROR - NTL RX - New RSP Data flit from NVLink received when the RSP Data Array is full.
40	RWX_WCLEAR	NTL_FIRST1_40: ERROR - NTL RX - RSP Data flit was attempted to be read from the RSP Data Array when it was empty.
41	RWX_WCLEAR	NTL_FIRST1_41: ERROR - NTL RX - New PRB Header flit from NVLink received when the PRB Header Array is full.
42	RWX_WCLEAR	NTL_FIRST1_42: ERROR - NTL RX - New ATR Header flit from NVLink received when the ATR Header Array is full.
43	RWX_WCLEAR	NTL_FIRST1_43: ERROR - NTL RX - A new NVLink Header flit was received when NTL was still expecting Data flits for the previous packet.
44	RWX_WCLEAR	NTL_FIRST1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or Data Array on the same cycle.
45	RWX_WCLEAR	NTL_FIRST1_45: ERROR - NTL RX - A CQ Slice Credit was received when one was already valid (overflow).
46	RWX_WCLEAR	NTL_FIRST1_46: ERROR - NTL RX - A CQ ATR Credit was received when one was already valid (overflow).

Bits	SCOM	Field Mnemonic: Description
47	RWX_WCLEAR	NTL_FIRST1_47: ERROR - NTL RX - A CQ Flush Credit was received when 15 were already valid (overflow).
48	RWX_WCLEAR	NTL_FIRST1_48: ERROR - NTL RX - A CQ Global Credit was received when 3 were already valid (overflow).
49	RWX_WCLEAR	NTL_FIRST1_49: ERROR - NTL RX - A CQ Response Credit was received when one was already valid (overflow).
50	RWX_WCLEAR	NTL_FIRST1_50: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RWX_WCLEAR	NTL_FIRST1_51: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RWX_WCLEAR	NTL_FIRST1_52: ERROR - NTL RX - Reserved.
53	RWX_WCLEAR	NTL_FIRST1_53: ERROR - NTL RX - Reserved.
54	RWX_WCLEAR	NTL_FIRST1_54: ERROR - NTL RX - Reserved.
55	RWX_WCLEAR	NTL_FIRST1_55: ERROR - NTL RX - Reserved.
56	RWX_WCLEAR	NTL_FIRST1_56: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Header Array.
57	RWX_WCLEAR	NTL_FIRST1_57: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Header Array.
58	RWX_WCLEAR	NTL_FIRST1_58: ERROR - NTL RX - ECC Correctable Error (CE) on Data(128:167) read from the Header Array.
59	RWX_WCLEAR	NTL_FIRST1_59: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Data Array.
60	RWX_WCLEAR	NTL_FIRST1_60: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Data Array.
61	RWX_WCLEAR	NTL_FIRST1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RWX_WCLEAR	NTL_FIRST1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RWX_WCLEAR	NTL_FIRST1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR First Mask 1 Register**
Mnemonic	NPU.STCK2.NTL1.REGS.CERR_FIRST_MASK1
Address	00000000050112E5 (SCOM)
Description	1 error mask register Mask errors from being captured in the First-1 Error registers and the RAS Error Message registers

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK1_0: ERROR - NTL RX - Unsupported command or ExCmd field encode received in an incoming NVLink packet.
1	RW	NTL_FIRST_MASK1_1: ERROR - NTL RX - AN / = 1 in an incoming NVLink packet where Rx Vld = 1 and Rx Hdr Vld = 1.
2	RW	NTL_FIRST_MASK1_2: ERROR - NTL RX - DatLen = 64B and Addr(6:5) = 11 in an incoming NVLink request packet where the Address field is valid.
3	RW	NTL_FIRST_MASK1_3: ERROR - NTL RX - DatLen = 96B and Addr(6) = 1 in an incoming NVLink request packet where the Address field is valid.
4	RW	NTL_FIRST_MASK1_4: ERROR - NTL RX - AddrType = 01 or 10 in an incoming NVLink Read,Write,Atomic,RMW request packet.

Bits	SCOM	Field Mnemonic: Description
5	RW	NTL_FIRST_MASK1_5: ERROR - NTL RX - DatLen = Reserved encode in an incoming NVLink request/response packet where the DatLen field is valid.
6	RW	NTL_FIRST_MASK1_6: ERROR - NTL RX - DatLen = 256B in an incoming NVLink request packet where the DatLen field is valid, and not Read nor Write.
7	RW	NTL_FIRST_MASK1_7: ERROR - NTL RX - BE flit exists in an incoming NVLink ReqRsp with Data packet.
8	RW	NTL_FIRST_MASK1_8: ERROR - NTL RX - DatLen = 96B or 128B in an incoming NVLink Atomic CAS packet.
9	RW	NTL_FIRST_MASK1_9: ERROR - NTL RX - Compressed Responses not populated in the order CR0,CR1,CR2 in an incoming NVLink response packet.
10	RW	NTL_FIRST_MASK1_10: ERROR - NTL RX - Compressed Response with an Invalid/Reserved TD/IVC combination in an incoming NVLink response packet.
11	RW	NTL_FIRST_MASK1_11: ERROR - NTL RX - Address(63:49) / = 0 in an incoming NVLink request packet where the Address field is valid.
12	RW	NTL_FIRST_MASK1_12: ERROR - NTL RX - Address(48:47) / = 0 in an incoming NVLink UT = 0 request packet where the Address field is valid, and not ATR.
13	RW	NTL_FIRST_MASK1_13: ERROR - NTL RX - DatLen / = 16,32,64,128B in an incoming NVLink Probe packet.
14	RW	NTL_FIRST_MASK1_14: ERROR - NTL RX - DatLen = 96B or 256B in an incoming NVLink ReqRsp with Data packet.
15	RW	NTL_FIRST_MASK1_15: ERROR - NTL RX - AtomicSz / = 4B or 8B in an incoming NVLink Atomic packet.
16	RW	NTL_FIRST_MASK1_16: ERROR - NTL RX - DatLen and AtomicSz not both 4B or 8B in an incoming NVLink Atomic packet where no BE flit exists.
17	RW	NTL_FIRST_MASK1_17: ERROR - NTL RX - Reserved.
18	RW	NTL_FIRST_MASK1_18: ERROR - NTL RX - Reserved.
19	RW	NTL_FIRST_MASK1_19: ERROR - NTL RX - Reserved.
20	RW	NTL_FIRST_MASK1_20: ERROR - NTL RX - Reserved.
21	RW	NTL_FIRST_MASK1_21: ERROR - NTL RX - Reserved.
22	RW	NTL_FIRST_MASK1_22: ERROR - NTL RX - Reserved.
23	RW	NTL_FIRST_MASK1_23: ERROR - NTL RX - Reserved.
24	RW	NTL_FIRST_MASK1_24: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Header Array.
25	RW	NTL_FIRST_MASK1_25: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Header Array.
26	RW	NTL_FIRST_MASK1_26: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(128:167) read from the Header Array.
27	RW	NTL_FIRST_MASK1_27: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(0:63) read from the Data Array.
28	RW	NTL_FIRST_MASK1_28: ERROR - NTL RX - ECC Uncorrectable Error (UE) on Data(64:127) read from the Data Array.
29	RW	NTL_FIRST_MASK1_29: ERROR - NTL RX - Parity error on incoming NDL Rx Vld and Hdr_Vld signals.
30	RW	NTL_FIRST_MASK1_30: ERROR - NTL RX - Parity error on incoming NDL Rx LMD and CRC signals.
31	RW	NTL_FIRST_MASK1_31: ERROR - NTL RX - Parity error on incoming NDL Rx Header flit signals.
32	RW	NTL_FIRST_MASK1_32: ERROR - NTL RX - Parity error on incoming NDL Rx AE flit signals.
33	RW	NTL_FIRST_MASK1_33: ERROR - NTL RX - Parity error on incoming NDL Rx Data flit signals.

Bits	SCOM	Field Mnemonic: Description
34	RW	NTL_FIRST_MASK1_34: ERROR - NTL RX - An NVLink packet with data received LMD = Data Poison.
35	RW	NTL_FIRST_MASK1_35: ERROR - NTL RX - New CREQ Header flit from NVLink received when the CREQ Header Array is full.
36	RW	NTL_FIRST_MASK1_36: ERROR - NTL RX - New CREQ Data flit from NVLink received when the CREQ Data Array is full.
37	RW	NTL_FIRST_MASK1_37: ERROR - NTL RX - CREQ Data flit was attempted to be read from the CREQ Data Array when it was empty.
38	RW	NTL_FIRST_MASK1_38: ERROR - NTL RX - New RSP Header flit from NVLink received when the RSP Header Array is full.
39	RW	NTL_FIRST_MASK1_39: ERROR - NTL RX - New RSP Data flit from NVLink received when the RSP Data Array is full.
40	RW	NTL_FIRST_MASK1_40: ERROR - NTL RX - RSP Data flit was attempted to be read from the RSP Data Array when it was empty.
41	RW	NTL_FIRST_MASK1_41: ERROR - NTL RX - New PRB Header flit from NVLink received when the PRB Header Array is full.
42	RW	NTL_FIRST_MASK1_42: ERROR - NTL RX - New ATR Header flit from NVLink received when the ATR Header Array is full.
43	RW	NTL_FIRST_MASK1_43: ERROR - NTL RX - A new NVLink Header flit was received when NTL was still expecting Data flits for the previous packet.
44	RW	NTL_FIRST_MASK1_44: ERROR - NTL RX - More than one VC tried to write the Header and/or Data Array on the same cycle.
45	RW	NTL_FIRST_MASK1_45: ERROR - NTL RX - A CQ Slice Credit was received when one was already valid (overflow).
46	RW	NTL_FIRST_MASK1_46: ERROR - NTL RX - A CQ ATR Credit was received when one was already valid (overflow).
47	RW	NTL_FIRST_MASK1_47: ERROR - NTL RX - A CQ Flush Credit was received when 15 were already valid (overflow).
48	RW	NTL_FIRST_MASK1_48: ERROR - NTL RX - A CQ Global Credit was received when 3 were already valid (overflow).
49	RW	NTL_FIRST_MASK1_49: ERROR - NTL RX - A CQ Response Credit was received when one was already valid (overflow).
50	RW	NTL_FIRST_MASK1_50: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink CREQ packet without data.
51	RW	NTL_FIRST_MASK1_51: ERROR - NTL RX - A Send SUE on data transfers to CQ_DAT latch was set for a NVLink RSP packet without data.
52	RW	NTL_FIRST_MASK1_52: ERROR - NTL RX - Reserved.
53	RW	NTL_FIRST_MASK1_53: ERROR - NTL RX - Reserved.
54	RW	NTL_FIRST_MASK1_54: ERROR - NTL RX - Reserved.
55	RW	NTL_FIRST_MASK1_55: ERROR - NTL RX - Reserved.
56	RW	NTL_FIRST_MASK1_56: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Header Array.
57	RW	NTL_FIRST_MASK1_57: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Header Array.
58	RW	NTL_FIRST_MASK1_58: ERROR - NTL RX - ECC Correctable Error (CE) on Data(128:167) read from the Header Array.
59	RW	NTL_FIRST_MASK1_59: ERROR - NTL RX - ECC Correctable Error (CE) on Data(0:63) read from the Data Array.

Bits	SCOM	Field Mnemonic: Description
60	RW	NTL_FIRST_MASK1_60: ERROR - NTL RX - ECC Correctable Error (CE) on Data(64:127) read from the Data Array.
61	RW	NTL_FIRST_MASK1_61: ERROR - NTL RX - CRC error occurred on an incoming NVLink packet.
62	RW	NTL_FIRST_MASK1_62: ERROR - NTL RX - LMD = Stomp occurred on an incoming NVLink packet.
63	RW	NTL_FIRST_MASK1_63: ERROR - NTL RX - Reserved.

Register Name	**NTL CERR Hold 2 Register**
Mnemonic	NPU.STCK2.NTL1.REGS.CERR_HOLD2
Address	00000000050112E6 (SCOM)
Description	2 latches register c_err_rpt hold latches read-write-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	NTL_HOLD2_0: ERROR - NTL TX - Parity error on incoming NDL Tx Credit signals.
1	RWX_WCLRREG	NTL_HOLD2_1: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(0:63) read from CQ_DAT.
2	RWX_WCLRREG	NTL_HOLD2_2: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(64:127) read from CQ_DAT.
3	RWX_WCLRREG	NTL_HOLD2_3: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(0:63) read from CQ_DAT.
4	RWX_WCLRREG	NTL_HOLD2_4: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(64:127) read from CQ_DAT.
5	RWX_WCLRREG	NTL_HOLD2_5: ERROR - NTL TX - Read or Atomic request with a length that is not a power of 2.
6	RWX_WCLRREG	NTL_HOLD2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLRREG	NTL_HOLD2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLRREG	NTL_HOLD2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLRREG	NTL_HOLD2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLRREG	NTL_HOLD2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLRREG	NTL_HOLD2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLRREG	NTL_HOLD2_12: ERROR - NTL TX - More than 1 entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLRREG	NTL_HOLD2_13: ERROR - NTL TX - More than 1 entry in the CREQ Sticky CAM was hit at the same time.
14	RWX_WCLRREG	NTL_HOLD2_14: ERROR - NTL TX - More than 1 entry in the DGD Sticky CAM was hit at the same time.
15	RWX_WCLRREG	NTL_HOLD2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLRREG	NTL_HOLD2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLRREG	NTL_HOLD2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLRREG	NTL_HOLD2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLRREG	NTL_HOLD2_19: ERROR - NTL TX - Reserved.

Bits	SCOM	Field Mnemonic: Description
20	RWX_WCLRREG	NTL_HOLD2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLRREG	NTL_HOLD2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLRREG	NTL_HOLD2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLRREG	NTL_HOLD2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLRREG	NTL_HOLD2_24: ERROR - NTL TX - ECC Correctable Error (CE) on Data(0:63) read from CQ_DAT.
25	RWX_WCLRREG	NTL_HOLD2_25: ERROR - NTL TX - ECC Correctable Error (CE) on Data(64:127) read from CQ_DAT.
26	RWX_WCLRREG	NTL_HOLD2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLRREG	NTL_HOLD2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLRREG	NTL_HOLD2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLRREG	NTL_HOLD2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLRREG	NTL_HOLD2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLRREG	NTL_HOLD2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLRREG	NTL_HOLD2_32: ERROR - NTL REGS - CREQ Header Credits received from the GPU are greater than max value.
33	RWX_WCLRREG	NTL_HOLD2_33: ERROR - NTL REGS - DGD Header Credits received from the GPU are greater than max value.
34	RWX_WCLRREG	NTL_HOLD2_34: ERROR - NTL REGS - ATSD Header Credits received from the GPU are greater than max value.
35	RWX_WCLRREG	NTL_HOLD2_35: ERROR - NTL REGS - RSP Header Credits received from the GPU are greater than max value.
36	RWX_WCLRREG	NTL_HOLD2_36: ERROR - NTL REGS - CREQ Data Credits received from the GPU are greater than max value.
37	RWX_WCLRREG	NTL_HOLD2_37: ERROR - NTL REGS - RSP Data Credits received from the GPU are greater than max value.
38	RWX_WCLRREG	NTL_HOLD2_38: ERROR - NTL REGS - Replay Buffer Credits received from NDL are greater than 512.
39	RWX_WCLRREG	NTL_HOLD2_39: ERROR - NTL REGS - Async Buffer Credits received from the NDL Wrapper are greater than 64.
40	RWX_WCLRREG	NTL_HOLD2_40: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for different NTLs.
41	RWX_WCLRREG	NTL_HOLD2_41: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for the same NTL.
42	RWX_WCLRREG	NTL_HOLD2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLRREG	NTL_HOLD2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLRREG	NTL_HOLD2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLRREG	NTL_HOLD2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLRREG	NTL_HOLD2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLRREG	NTL_HOLD2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLRREG	NTL_HOLD2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLRREG	NTL_HOLD2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLRREG	NTL_HOLD2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLRREG	NTL_HOLD2_51: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RWX_WCLRREG	NTL_HOLD2_52: ERROR - NTL REGS - PHY timeout error indication received on a Private Register Interface response.
53	RWX_WCLRREG	NTL_HOLD2_53: ERROR - NTL REGS - NDL error error indication received on a Private Register Interface response.
54	RWX_WCLRREG	NTL_HOLD2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a Private Register Interface response.
55	RWX_WCLRREG	NTL_HOLD2_55: ERROR - NTL REGS - Bad address error indication received on a Private Register Interface response.
56	RWX_WCLRREG	NTL_HOLD2_56: ERROR - NTL REGS - Parity error error indication received on a Private Register Interface response.
57	RWX_WCLRREG	NTL_HOLD2_57: ERROR - NTL REGS - Protocol error error indication received on a Private Register Interface response.
58	RWX_WCLRREG	NTL_HOLD2_58: ERROR - NTL REGS - Private Register Interface Ack signal from NDL Wrapper went invalid in the middle of a PRI response.
59	RWX_WCLRREG	NTL_HOLD2_59: ERROR - NTL REGS - Parity error on incoming NDL Priority Register Interface (PRI) response signals.
60	RWX_WCLRREG	NTL_HOLD2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLRREG	NTL_HOLD2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLRREG	NTL_HOLD2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLRREG	NTL_HOLD2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL CERR Mask 2 Register**
Mnemonic	NPU.STCK2.NTL1.REGS.CERR_MASK2
Address	00000000050112E7 (SCOM)
Description	2 latches register c_err_rpt mask latches read-only reg

Bits	SCOM	Field Mnemonic: Description
0	ROX	NTL_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL Tx Credit signals.
1	ROX	NTL_MASK2_1: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(0:63) read from CQ_DAT.
2	ROX	NTL_MASK2_2: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(64:127) read from CQ_DAT.
3	ROX	NTL_MASK2_3: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(0:63) read from CQ_DAT.
4	ROX	NTL_MASK2_4: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(64:127) read from CQ_DAT.
5	ROX	NTL_MASK2_5: ERROR - NTL TX - Read or Atomic request with a length that is not a power of 2.
6	ROX	NTL_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	ROX	NTL_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	ROX	NTL_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	ROX	NTL_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	ROX	NTL_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.

Bits	SCOM	Field Mnemonic: Description
11	ROX	NTL_MASK2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.
12	ROX	NTL_MASK2_12: ERROR - NTL TX - More than 1 entry in the 256B Ops CAM was hit at the same time.
13	ROX	NTL_MASK2_13: ERROR - NTL TX - More than 1 entry in the CREQ Sticky CAM was hit at the same time.
14	ROX	NTL_MASK2_14: ERROR - NTL TX - More than 1 entry in the DGD Sticky CAM was hit at the same time.
15	ROX	NTL_MASK2_15: ERROR - NTL TX - Reserved.
16	ROX	NTL_MASK2_16: ERROR - NTL TX - Reserved.
17	ROX	NTL_MASK2_17: ERROR - NTL TX - Reserved.
18	ROX	NTL_MASK2_18: ERROR - NTL TX - Reserved.
19	ROX	NTL_MASK2_19: ERROR - NTL TX - Reserved.
20	ROX	NTL_MASK2_20: ERROR - NTL TX - Reserved.
21	ROX	NTL_MASK2_21: ERROR - NTL TX - Reserved.
22	ROX	NTL_MASK2_22: ERROR - NTL TX - Reserved.
23	ROX	NTL_MASK2_23: ERROR - NTL TX - Reserved.
24	ROX	NTL_MASK2_24: ERROR - NTL TX - ECC Correctable Error (CE) on Data(0:63) read from CQ_DAT.
25	ROX	NTL_MASK2_25: ERROR - NTL TX - ECC Correctable Error (CE) on Data(64:127) read from CQ_DAT.
26	ROX	NTL_MASK2_26: ERROR - NTL TX - Reserved.
27	ROX	NTL_MASK2_27: ERROR - NTL TX - Reserved.
28	ROX	NTL_MASK2_28: ERROR - NTL TX - Reserved.
29	ROX	NTL_MASK2_29: ERROR - NTL TX - Reserved.
30	ROX	NTL_MASK2_30: ERROR - NTL TX - Reserved.
31	ROX	NTL_MASK2_31: ERROR - NTL TX - Reserved.
32	ROX	NTL_MASK2_32: ERROR - NTL REGS - CREQ Header Credits received from the GPU are greater than max value.
33	ROX	NTL_MASK2_33: ERROR - NTL REGS - DGD Header Credits received from the GPU are greater than max value.
34	ROX	NTL_MASK2_34: ERROR - NTL REGS - ATSD Header Credits received from the GPU are greater than max value.
35	ROX	NTL_MASK2_35: ERROR - NTL REGS - RSP Header Credits received from the GPU are greater than max value.
36	ROX	NTL_MASK2_36: ERROR - NTL REGS - CREQ Data Credits received from the GPU are greater than max value.
37	ROX	NTL_MASK2_37: ERROR - NTL REGS - RSP Data Credits received from the GPU are greater than max value.
38	ROX	NTL_MASK2_38: ERROR - NTL REGS - Replay Buffer Credits received from NDL are greater than 512.
39	ROX	NTL_MASK2_39: ERROR - NTL REGS - Async Buffer Credits received from the NDL Wrapper are greater than 64.
40	ROX	NTL_MASK2_40: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for different NTLs.
41	ROX	NTL_MASK2_41: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for the same NTL.
42	ROX	NTL_MASK2_42: ERROR - NTL REGS - Reserved.
43	ROX	NTL_MASK2_43: ERROR - NTL REGS - Reserved.

Bits	SCOM	Field Mnemonic: Description
44	ROX	NTL_MASK2_44: ERROR - NTL REGS - Reserved.
45	ROX	NTL_MASK2_45: ERROR - NTL REGS - Reserved.
46	ROX	NTL_MASK2_46: ERROR - NTL REGS - Reserved.
47	ROX	NTL_MASK2_47: ERROR - NTL REGS - Reserved.
48	ROX	NTL_MASK2_48: ERROR - NTL REGS - Reserved.
49	ROX	NTL_MASK2_49: ERROR - NTL REGS - Reserved.
50	ROX	NTL_MASK2_50: ERROR - NTL REGS - Reserved.
51	ROX	NTL_MASK2_51: ERROR - NTL REGS - Reserved.
52	ROX	NTL_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a Private Register Interface response.
53	ROX	NTL_MASK2_53: ERROR - NTL REGS - NDL error error indication received on a Private Register Interface response.
54	ROX	NTL_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a Private Register Interface response.
55	ROX	NTL_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a Private Register Interface response.
56	ROX	NTL_MASK2_56: ERROR - NTL REGS - Parity error error indication received on a Private Register Interface response.
57	ROX	NTL_MASK2_57: ERROR - NTL REGS - Protocol error error indication received on a Private Register Interface response.
58	ROX	NTL_MASK2_58: ERROR - NTL REGS - Private Register Interface Ack signal from NDL Wrapper went invalid in the middle of a PRI response.
59	ROX	NTL_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL Priority Register Interface (PRI) response signals.
60	ROX	NTL_MASK2_60: ERROR - NTL REGS - Reserved.
61	ROX	NTL_MASK2_61: ERROR - NTL REGS - Reserved.
62	ROX	NTL_MASK2_62: ERROR - NTL REGS - Reserved.
63	ROX	NTL_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	NTL CERR First 2 Register
Mnemonic	NPU.STCK2.NTL1.REGS.CERR_FIRST2
Address	00000000050112E8 (SCOM)
Description	2 latches register c_err_rpt first error latches read-write-1-clear reg

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	NTL_FIRST2_0: ERROR - NTL TX - Parity error on incoming NDL Tx Credit signals.
1	RWX_WCLEAR	NTL_FIRST2_1: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(0:63) read from CQ_DAT.
2	RWX_WCLEAR	NTL_FIRST2_2: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(64:127) read from CQ_DAT.
3	RWX_WCLEAR	NTL_FIRST2_3: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(0:63) read from CQ_DAT.

Bits	SCOM	Field Mnemonic: Description
4	RWX_WCLEAR	NTL_FIRST2_4: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(64:127) read from CQ_DAT.
5	RWX_WCLEAR	NTL_FIRST2_5: ERROR - NTL TX - Read or Atomic request with a length that is not a power of 2.
6	RWX_WCLEAR	NTL_FIRST2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RWX_WCLEAR	NTL_FIRST2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RWX_WCLEAR	NTL_FIRST2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RWX_WCLEAR	NTL_FIRST2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RWX_WCLEAR	NTL_FIRST2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RWX_WCLEAR	NTL_FIRST2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.
12	RWX_WCLEAR	NTL_FIRST2_12: ERROR - NTL TX - More than 1 entry in the 256B Ops CAM was hit at the same time.
13	RWX_WCLEAR	NTL_FIRST2_13: ERROR - NTL TX - More than 1 entry in the CREQ Sticky CAM was hit at the same time.
14	RWX_WCLEAR	NTL_FIRST2_14: ERROR - NTL TX - More than 1 entry in the DGD Sticky CAM was hit at the same time.
15	RWX_WCLEAR	NTL_FIRST2_15: ERROR - NTL TX - Reserved.
16	RWX_WCLEAR	NTL_FIRST2_16: ERROR - NTL TX - Reserved.
17	RWX_WCLEAR	NTL_FIRST2_17: ERROR - NTL TX - Reserved.
18	RWX_WCLEAR	NTL_FIRST2_18: ERROR - NTL TX - Reserved.
19	RWX_WCLEAR	NTL_FIRST2_19: ERROR - NTL TX - Reserved.
20	RWX_WCLEAR	NTL_FIRST2_20: ERROR - NTL TX - Reserved.
21	RWX_WCLEAR	NTL_FIRST2_21: ERROR - NTL TX - Reserved.
22	RWX_WCLEAR	NTL_FIRST2_22: ERROR - NTL TX - Reserved.
23	RWX_WCLEAR	NTL_FIRST2_23: ERROR - NTL TX - Reserved.
24	RWX_WCLEAR	NTL_FIRST2_24: ERROR - NTL TX - ECC Correctable Error (CE) on Data(0:63) read from CQ_DAT.
25	RWX_WCLEAR	NTL_FIRST2_25: ERROR - NTL TX - ECC Correctable Error (CE) on Data(64:127) read from CQ_DAT.
26	RWX_WCLEAR	NTL_FIRST2_26: ERROR - NTL TX - Reserved.
27	RWX_WCLEAR	NTL_FIRST2_27: ERROR - NTL TX - Reserved.
28	RWX_WCLEAR	NTL_FIRST2_28: ERROR - NTL TX - Reserved.
29	RWX_WCLEAR	NTL_FIRST2_29: ERROR - NTL TX - Reserved.
30	RWX_WCLEAR	NTL_FIRST2_30: ERROR - NTL TX - Reserved.
31	RWX_WCLEAR	NTL_FIRST2_31: ERROR - NTL TX - Reserved.
32	RWX_WCLEAR	NTL_FIRST2_32: ERROR - NTL REGS - CREQ Header Credits received from the GPU are greater than max value.
33	RWX_WCLEAR	NTL_FIRST2_33: ERROR - NTL REGS - DGD Header Credits received from the GPU are greater than max value.
34	RWX_WCLEAR	NTL_FIRST2_34: ERROR - NTL REGS - ATSD Header Credits received from the GPU are greater than max value.

Bits	SCOM	Field Mnemonic: Description
35	RWX_WCLEAR	NTL_FIRST2_35: ERROR - NTL REGS - RSP Header Credits received from the GPU are greater than max value.
36	RWX_WCLEAR	NTL_FIRST2_36: ERROR - NTL REGS - CREQ Data Credits received from the GPU are greater than max value.
37	RWX_WCLEAR	NTL_FIRST2_37: ERROR - NTL REGS - RSP Data Credits received from the GPU are greater than max value.
38	RWX_WCLEAR	NTL_FIRST2_38: ERROR - NTL REGS - Replay Buffer Credits received from NDL are greater than 512.
39	RWX_WCLEAR	NTL_FIRST2_39: ERROR - NTL REGS - Async Buffer Credits received from the NDL Wrapper are greater than 64.
40	RWX_WCLEAR	NTL_FIRST2_40: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for different NTLs.
41	RWX_WCLEAR	NTL_FIRST2_41: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for the same NTL.
42	RWX_WCLEAR	NTL_FIRST2_42: ERROR - NTL REGS - Reserved.
43	RWX_WCLEAR	NTL_FIRST2_43: ERROR - NTL REGS - Reserved.
44	RWX_WCLEAR	NTL_FIRST2_44: ERROR - NTL REGS - Reserved.
45	RWX_WCLEAR	NTL_FIRST2_45: ERROR - NTL REGS - Reserved.
46	RWX_WCLEAR	NTL_FIRST2_46: ERROR - NTL REGS - Reserved.
47	RWX_WCLEAR	NTL_FIRST2_47: ERROR - NTL REGS - Reserved.
48	RWX_WCLEAR	NTL_FIRST2_48: ERROR - NTL REGS - Reserved.
49	RWX_WCLEAR	NTL_FIRST2_49: ERROR - NTL REGS - Reserved.
50	RWX_WCLEAR	NTL_FIRST2_50: ERROR - NTL REGS - Reserved.
51	RWX_WCLEAR	NTL_FIRST2_51: ERROR - NTL REGS - Reserved.
52	RWX_WCLEAR	NTL_FIRST2_52: ERROR - NTL REGS - PHY timeout error indication received on a Private Register Interface response.
53	RWX_WCLEAR	NTL_FIRST2_53: ERROR - NTL REGS - NDL error error indication received on a Private Register Interface response.
54	RWX_WCLEAR	NTL_FIRST2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a Private Register Interface response.
55	RWX_WCLEAR	NTL_FIRST2_55: ERROR - NTL REGS - Bad address error indication received on a Private Register Interface response.
56	RWX_WCLEAR	NTL_FIRST2_56: ERROR - NTL REGS - Parity error error indication received on a Private Register Interface response.
57	RWX_WCLEAR	NTL_FIRST2_57: ERROR - NTL REGS - Protocol error error indication received on a Private Register Interface response.
58	RWX_WCLEAR	NTL_FIRST2_58: ERROR - NTL REGS - Private Register Interface Ack signal from NDL Wrapper went invalid in the middle of a PRI response.
59	RWX_WCLEAR	NTL_FIRST2_59: ERROR - NTL REGS - Parity error on incoming NDL Priority Register Interface (PRI) response signals.
60	RWX_WCLEAR	NTL_FIRST2_60: ERROR - NTL REGS - Reserved.
61	RWX_WCLEAR	NTL_FIRST2_61: ERROR - NTL REGS - Reserved.
62	RWX_WCLEAR	NTL_FIRST2_62: ERROR - NTL REGS - Reserved.
63	RWX_WCLEAR	NTL_FIRST2_63: ERROR - NTL REGS - Reserved.

Register Name	NTL CERR First Mask 2 Register
Mnemonic	NPU.STCK2.NTL1.REGS.CERR_FIRST_MASK2
Address	00000000050112E9 (SCOM)
Description	2 error mask register Mask errors from being captured in the First-2 Error registers and the RAS Error Message registers

Bits	SCOM	Field Mnemonic: Description
0	RW	NTL_FIRST_MASK2_0: ERROR - NTL TX - Parity error on incoming NDL Tx Credit signals.
1	RW	NTL_FIRST_MASK2_1: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(0:63) read from CQ_DAT.
2	RW	NTL_FIRST_MASK2_2: ERROR - NTL TX - ECC Uncorrectable Error (UE) on Data(64:127) read from CQ_DAT.
3	RW	NTL_FIRST_MASK2_3: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(0:63) read from CQ_DAT.
4	RW	NTL_FIRST_MASK2_4: ERROR - NTL TX - ECC Special Uncorrectable Error (SUE) on Data(64:127) read from CQ_DAT.
5	RW	NTL_FIRST_MASK2_5: ERROR - NTL TX - Read or Atomic request with a length that is not a power of 2.
6	RW	NTL_FIRST_MASK2_6: ERROR - NTL TX - New CREQ request received from CQ when one already existed (overflow).
7	RW	NTL_FIRST_MASK2_7: ERROR - NTL TX - New DGD request received from CQ when one already existed (overflow).
8	RW	NTL_FIRST_MASK2_8: ERROR - NTL TX - New ATSD request received from CQ when one already existed (overflow).
9	RW	NTL_FIRST_MASK2_9: ERROR - NTL TX - New RSP request received from CQ when two already existed (overflow).
10	RW	NTL_FIRST_MASK2_10: ERROR - NTL TX - A data beat was received from CQ_DAT when one was not expected.
11	RW	NTL_FIRST_MASK2_11: ERROR - NTL TX - More than 1 type of flit was attempted to be sent to NDL at the same time.
12	RW	NTL_FIRST_MASK2_12: ERROR - NTL TX - More than 1 entry in the 256B Ops CAM was hit at the same time.
13	RW	NTL_FIRST_MASK2_13: ERROR - NTL TX - More than 1 entry in the CREQ Sticky CAM was hit at the same time.
14	RW	NTL_FIRST_MASK2_14: ERROR - NTL TX - More than 1 entry in the DGD Sticky CAM was hit at the same time.
15	RW	NTL_FIRST_MASK2_15: ERROR - NTL TX - Reserved.
16	RW	NTL_FIRST_MASK2_16: ERROR - NTL TX - Reserved.
17	RW	NTL_FIRST_MASK2_17: ERROR - NTL TX - Reserved.
18	RW	NTL_FIRST_MASK2_18: ERROR - NTL TX - Reserved.
19	RW	NTL_FIRST_MASK2_19: ERROR - NTL TX - Reserved.
20	RW	NTL_FIRST_MASK2_20: ERROR - NTL TX - Reserved.
21	RW	NTL_FIRST_MASK2_21: ERROR - NTL TX - Reserved.
22	RW	NTL_FIRST_MASK2_22: ERROR - NTL TX - Reserved.
23	RW	NTL_FIRST_MASK2_23: ERROR - NTL TX - Reserved.
24	RW	NTL_FIRST_MASK2_24: ERROR - NTL TX - ECC Correctable Error (CE) on Data(0:63) read from CQ_DAT.

Bits	SCOM	Field Mnemonic: Description
25	RW	NTL_FIRST_MASK2_25: ERROR - NTL TX - ECC Correctable Error (CE) on Data(64:127) read from CQ_DAT.
26	RW	NTL_FIRST_MASK2_26: ERROR - NTL TX - Reserved.
27	RW	NTL_FIRST_MASK2_27: ERROR - NTL TX - Reserved.
28	RW	NTL_FIRST_MASK2_28: ERROR - NTL TX - Reserved.
29	RW	NTL_FIRST_MASK2_29: ERROR - NTL TX - Reserved.
30	RW	NTL_FIRST_MASK2_30: ERROR - NTL TX - Reserved.
31	RW	NTL_FIRST_MASK2_31: ERROR - NTL TX - Reserved.
32	RW	NTL_FIRST_MASK2_32: ERROR - NTL REGS - CREQ Header Credits received from the GPU are greater than max value.
33	RW	NTL_FIRST_MASK2_33: ERROR - NTL REGS - DGD Header Credits received from the GPU are greater than max value.
34	RW	NTL_FIRST_MASK2_34: ERROR - NTL REGS - ATSD Header Credits received from the GPU are greater than max value.
35	RW	NTL_FIRST_MASK2_35: ERROR - NTL REGS - RSP Header Credits received from the GPU are greater than max value.
36	RW	NTL_FIRST_MASK2_36: ERROR - NTL REGS - CREQ Data Credits received from the GPU are greater than max value.
37	RW	NTL_FIRST_MASK2_37: ERROR - NTL REGS - RSP Data Credits received from the GPU are greater than max value.
38	RW	NTL_FIRST_MASK2_38: ERROR - NTL REGS - Replay Buffer Credits received from NDL are greater than 512.
39	RW	NTL_FIRST_MASK2_39: ERROR - NTL REGS - Async Buffer Credits received from the NDL Wrapper are greater than 64.
40	RW	NTL_FIRST_MASK2_40: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for different NTLs.
41	RW	NTL_FIRST_MASK2_41: ERROR - NTL REGS - Multiple Private Register Interface requests active at the same time for the same NTL.
42	RW	NTL_FIRST_MASK2_42: ERROR - NTL REGS - Reserved.
43	RW	NTL_FIRST_MASK2_43: ERROR - NTL REGS - Reserved.
44	RW	NTL_FIRST_MASK2_44: ERROR - NTL REGS - Reserved.
45	RW	NTL_FIRST_MASK2_45: ERROR - NTL REGS - Reserved.
46	RW	NTL_FIRST_MASK2_46: ERROR - NTL REGS - Reserved.
47	RW	NTL_FIRST_MASK2_47: ERROR - NTL REGS - Reserved.
48	RW	NTL_FIRST_MASK2_48: ERROR - NTL REGS - Reserved.
49	RW	NTL_FIRST_MASK2_49: ERROR - NTL REGS - Reserved.
50	RW	NTL_FIRST_MASK2_50: ERROR - NTL REGS - Reserved.
51	RW	NTL_FIRST_MASK2_51: ERROR - NTL REGS - Reserved.
52	RW	NTL_FIRST_MASK2_52: ERROR - NTL REGS - PHY timeout error indication received on a Private Register Interface response.
53	RW	NTL_FIRST_MASK2_53: ERROR - NTL REGS - NDL error error indication received on a Private Register Interface response.
54	RW	NTL_FIRST_MASK2_54: ERROR - NTL REGS - Access to NDL while in reset error indication received on a Private Register Interface response.

Bits	SCOM	Field Mnemonic: Description
55	RW	NTL_FIRST_MASK2_55: ERROR - NTL REGS - Bad address error indication received on a Private Register Interface response.
56	RW	NTL_FIRST_MASK2_56: ERROR - NTL REGS - Parity error error indication received on a Private Register Interface response.
57	RW	NTL_FIRST_MASK2_57: ERROR - NTL REGS - Protocol error error indication received on a Private Register Interface response.
58	RW	NTL_FIRST_MASK2_58: ERROR - NTL REGS - Private Register Interface Ack signal from NDL Wrapper went invalid in the middle of a PRI response.
59	RW	NTL_FIRST_MASK2_59: ERROR - NTL REGS - Parity error on incoming NDL Priority Register Interface (PRI) response signals.
60	RW	NTL_FIRST_MASK2_60: ERROR - NTL REGS - Reserved.
61	RW	NTL_FIRST_MASK2_61: ERROR - NTL REGS - Reserved.
62	RW	NTL_FIRST_MASK2_62: ERROR - NTL REGS - Reserved.
63	RW	NTL_FIRST_MASK2_63: ERROR - NTL REGS - Reserved.

Register Name	**NTL Scratch 2 Register**
Mnemonic	NPU.STCK2.NTL1.REGS.SCRATCH2
Address	00000000050112EA (SCOM)
Description	The NTL Scratch 2 Register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH2: Scratch register.

Register Name	**NTL Scratch 3 Register**
Mnemonic	NPU.STCK2.NTL1.REGS.SCRATCH3
Address	00000000050112EB (SCOM)
Description	The NTL Scratch 3 Register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH3: Scratch register.

Register Name	**NTL Debug0 Configuration Register**
Mnemonic	NPU.STCK2.NTL1.REGS.DEBUG0_CONFIG
Address	00000000050112EC (SCOM)
Description	The NTL Debug Trace 0 Configuration Register is used to configure what debug information is sent on the Debug Trace 0 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of Debug Trace 0. 0x00 = Debug Trace 0 byte 0 inputs. 0x01 = Debug Trace 0 byte 1 inputs. 0x02 = Debug Trace 0 byte 2 inputs. 0x03 = Debug Trace 0 byte 3 inputs. 0x04 = Debug Trace 0 byte 4 inputs. 0x05 = Debug Trace 0 byte 5 inputs. 0x06 = Debug Trace 0 byte 6 inputs. 0x07 = Debug Trace 0 byte 7 inputs. 0x08 = Debug Trace 0 byte 8 inputs. 0x09 = Debug Trace 0 byte 9 inputs. 0x0A = Debug Trace 0 byte 10 inputs. 0x0B = RX Debug Group 0. 0x0C = RX Debug Group 1. 0x0D = RX Debug Group 2. 0x0E = RX Debug Group 3. 0x0F = RX Debug Group 4. 0x10 = RX Debug Group 5. 0x11 = RX Debug Group 6. 0x12 = RX Debug Group 7. 0x13 = RX Debug Group 8. 0x14 = TX Debug Group 0. 0x15 = TX Debug Group 1. 0x16 = TX Debug Group 2. 0x17 = TX Debug Group 3. 0x18 = TX Debug Group 4. 0x19 = TX Debug Group 5. 0x1A = TX Debug Group 6. 0x1B = REGS Debug Group 0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of Debug Trace 0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of Debug Trace 0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of Debug Trace 0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of Debug Trace 0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of Debug Trace 0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of Debug Trace 0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of Debug Trace 0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of Debug Trace 0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of Debug Trace 0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of Debug Trace 0.
55:62	RW	DEBUG0_CONFIG_Reserved1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock gates for Debug Trace latches.

Register Name	**NTL Debug1 Configuration Register**
Mnemonic	NPU.STCK2.NTL1.REGS.DEBUG1_CONFIG
Address	00000000050112ED (SCOM)
Description	The NTL Debug Trace 1 Configuration Register is used to configure what debug information is sent on the Debug Trace 1 bus outputs of NTL.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of Debug Trace 1. 0x00 = Debug Trace 1 byte 0 inputs. 0x01 = Debug Trace 1 byte 1 inputs. 0x02 = Debug Trace 1 byte 2 inputs. 0x03 = Debug Trace 1 byte 3 inputs. 0x04 = Debug Trace 1 byte 4 inputs. 0x05 = Debug Trace 1 byte 5 inputs. 0x06 = Debug Trace 1 byte 6 inputs. 0x07 = Debug Trace 1 byte 7 inputs. 0x08 = Debug Trace 1 byte 8 inputs. 0x09 = Debug Trace 1 byte 9 inputs. 0x0A = Debug Trace 1 byte 10 inputs. 0x0B = RX Debug Group 0. 0x0C = RX Debug Group 1. 0x0D = RX Debug Group 2. 0x0E = RX Debug Group 3. 0x0F = RX Debug Group 4. 0x10 = RX Debug Group 5. 0x11 = RX Debug Group 6. 0x12 = RX Debug Group 7. 0x13 = RX Debug Group 8. 0x14 = TX Debug Group 0. 0x15 = TX Debug Group 1. 0x16 = TX Debug Group 2. 0x17 = TX Debug Group 3. 0x18 = TX Debug Group 4. 0x19 = TX Debug Group 5. 0x1A = TX Debug Group 6. 0x1B = REGS Debug Group 0.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of Debug Trace 1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of Debug Trace 1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of Debug Trace 1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of Debug Trace 1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of Debug Trace 1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of Debug Trace 1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of Debug Trace 1.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of Debug Trace 1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of Debug Trace 1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of Debug Trace 1.
55:62	RW	DEBUG1_CONFIG_Reserved1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock gates for Debug Trace latches.

Register Name	**NTL Performance Configuration Register**
Mnemonic	NPU.STCK2.NTL1.REGS.PERF_CONFIG
Address	00000000050112EE (SCOM)
Description	The NTL Performance Configuration Register is used to configure what information is counted by the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: PMULet Enable (clocks enable).

Bits	SCOM	Field Mnemonic: Description
1	RW	PERF_CONFIG_RESETMODE: 0/1 = reset-on-read/reset-on-write.
2	RW	PERF_CONFIG_FREEZEMODE: 0/1 = freerun-mode/freeze-on-any-max.
3	RW	PERF_CONFIG_DISABLE_PMISC: 0/1 = enable-pmisc/disable-pmisc control of counters.
4	RW	PERF_CONFIG_PMISC_MODE: 0/1 = global pmu pmisc no reset/global pmu pmisc reset-on-enable.
5:7	RW	PERF_CONFIG_CASCADE: PMULet cascade config.
8:9	RW	PERF_CONFIG_PRESCALE_C0: prescale config for counter 0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: prescale config for counter 1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: prescale config for counter 2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: prescale config for counter 3.
16:23	RW	PERF_CONFIG_EVENT0: Event 0 select: 0x00 = Disable. 0x01 = Cycles. 0x02 = Latency events. 0x03 = Latency cycles. 0x04 = Latency aborts. 0x20 = REGS - NDL PRI request. 0x21 = REGS - NDL PRI Write request. 0x22 = REGS - NDL PRI Read request. 0x23 = REGS - PHY PRI request. 0x24 = REGS - PHY PRI Write request. 0x25 = REGS - PHY PRI Read request. 0x40 = TX - any flit sent. 0x41 = TX - Header flit sent. 0x42 = TX - AE flit sent. 0x43 = TX - BE flit sent. 0x44 = TX - Data flit sent. 0x45 = TX - Flow Control packet. 0x46 = TX - Write.NC. 0x47 = TX - Write.NC 128B. 0x48 = TX - Write.NC 32-96B. 0x49 = TX - Write.NC 1-16B. 0x4A = TX - Write.NC with BE flit. 0x4B = TX - Read. 0x4C = TX - Upgrade. 0x4D = TX - Atomic. 0x4E = TX - Downgrade. 0x4F = TX - ATSD. 0x50 = TX - Request Response no-data. 0x51 = TX - Request Response with-data. 0x52 = TX - Probe Response no-data. 0x53 = TX - Probe Response with-data. 0x54 = TX - ATR Response. 0x55 = TX - TransDone Response no-data. 0x56 = TX - TransDone Response with-data. 0x57 = TX - TransDone Response with-data 128B. 0x58 = TX - TransDone Response with-data 32-96B. 0x59 = TX - TransDone Response with-data 1-16B. 0x5A = TX - TransDone Response with-data with BE flit. 0x5B = TX - Not enough CREQ Header Credits. 0x5C = TX - Not enough DGD Header Credits. 0x5D = TX - Not enough ATSD Header Credits. 0x5E = TX - Not enough RSP Header Credits. 0x5F = TX - Not enough CREQ Data Credits. 0x60 = TX - Not enough RSP Data Credits.

Bits	SCOM	Field Mnemonic: Description
		0x61 = TX - Not enough Replay Buffer Credits. 0x62 = TX - Not enough Async Buffer Credits. 0x80 = RX - CREQ Header Array full. 0x81 = RX - PRB Header Array full. 0x82 = RX - ATR Header Array full. 0x83 = RX - RSP Header Array full. 0x84 = RX - CREQ Data Array full. 0x85 = RX - RSP Data Array full. 0x86 = RX - any flit received. 0x87 = RX - Header flit received. 0x88 = RX - AE flit received. 0x89 = RX - BE flit received. 0x8A = RX - Data flit received. 0x8B = RX - NOP Flow Control flit received. 0x8C = RX - Write.NC (UT = 0). 0x8D = RX - Write.NC (UT = 1). 0x8E = RX - Write.NC (UT = 0) 128B. 0x8F = RX - Write.NC (UT = 1) 128B. 0x90 = RX - Write.NC (UT = 0) 256B. 0x91 = RX - Write.NC (UT = 1) 256B. 0x92 = RX - Write.NC (UT = 0) 32-96B. 0x93 = RX - Write.NC (UT = 1) 32-96B. 0x94 = RX - Write.NC (UT = 0) 1-16B. 0x95 = RX - Write.NC (UT = 1) 1-16B. 0x96 = RX - Write.NC (UT = 0) w/ BE flit. 0x97 = RX - Write.NC (UT = 1) w/ BE flit. 0x98 = RX - Write.NC (UT = 0) to MMIO Space. 0x99 = RX - Write.NC (UT = 0) to MMIO Space and split into mult requests. 0x9A = RX - Write.NC (UT = 1) and split into mult requests. 0x9B = RX - Read.NC (UT = 0). 0x9C = RX - Read.NC (UT = 1). 0x9D = RX - Read.NC (UT = 0) 128B. 0x9E = RX - Read.NC (UT = 1) 128B. 0x9F = RX - Read.NC (UT = 0) 256B. 0xA0 = RX - Read.NC (UT = 1) 256B. 0xA1 = RX - Read.NC (UT = 0) 32-96B. 0xA2 = RX - Read.NC (UT = 1) 32-96B. 0xA3 = RX - Read.NC (UT = 0) 1-16B. 0xA4 = RX - Read.NC (UT = 1) 1-16B. 0xA5 = RX - Flush. 0xA6 = RX - RMW. 0xA7 = RX - Atomic.NR. 0xA8 = RX - Atomic.RR. 0xA9 = RX - Probe.I.MO. 0xAA = RX - Probe.I.N. 0xAB = RX - Probe.X.MO. 0xAC = RX - ATR. 0xAD = RX - ReqRsp.ND. 0xAE = RX - ReqRsp.D. 0xAF = RX - DGDRsp. 0xB0 = RX - ATSDRsp. 0xB1 = RX - TransDone.ND. 0xB2 = RX - TransDone.D. 0xB3 = RX - TransDone.D w/ BE flit. 0xB4 = RX - CREQ non-Flush waiting for CQ Credit. 0xB5 = RX - CREQ Flush waiting for CQ Credit. 0xB6 = RX - CREQ waiting for Global Credit. 0xB7 = RX - CREQ 256B operation waiting for 256B Ops CAM entry. 0xB8 = RX - PRB waiting for CQ Credit. 0xB9 = RX - PRB waiting for Global Credit.

Bits	SCOM	Field Mnemonic: Description
		0xBA = RX - ATR waiting for CQ Credit. 0xBB = RX - ATR waiting for Global Credit.
24:31	RW	PERF_CONFIG_EVENT1: Event 1 select (see Event 0 select for encodes).
32:39	RW	PERF_CONFIG_EVENT2: Event 2 select (see Event 0 select for encodes).
40:47	RW	PERF_CONFIG_EVENT3: Event 3 select (see Event 0 select for encodes).
48:50	RW	PERF_CONFIG_LATENCY: Latency select: 0 = Disable. 1 = Read.NC to Response. 2 = Write.RR to Response. 3 = Atomic.RR to Response. 4 = RMW to Response. 5 = Flush to Response. 6 = Probe to Response. 7 = ATR to Response.
51:63	RW	PERF_CONFIG_Reserved: Reserved.

Register Name	NTL Performance Count Register
Mnemonic	NPU.STCK2.NTL1.REGS.PERF_COUNT
Address	00000000050112EF (SCOM)
Description	The NTL Performance Count Register holds the performance counts from the NTL PMULet.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	IDIAL_PERF_COUNT0: Performance Counter 0.
16:31	RWX_WCLRREG	IDIAL_PERF_COUNT1: Performance Counter 1.
32:47	RWX_WCLRREG	IDIAL_PERF_COUNT2: Performance Counter 2.
48:63	RWX_WCLRREG	IDIAL_PERF_COUNT3: Performance Counter 3.

Register Name	NTL CREQ Header Array Pointer Register
Mnemonic	NPU.STCK2.NTL1.REGS.CREQ_HA_PTR
Address	00000000050112F0 (SCOM)
Description	The NTL CREQ Header Array Pointer Register is used to change the start and/or end entry in the NTL Header Array for holding CREQ header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	CREQ_HA_PTR_Reserved1: Reserved.
5:11	RW	CREQ_HA_PTR_START: Starting header array location for CREQ headers received from the GPU. The header array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	CREQ_HA_PTR_Reserved2: Reserved.
17:23	RW	CREQ_HA_PTR_END: Ending Header Array location for CREQ headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL PRB Header Array Pointer Register
Mnemonic	NPU.STCK2.NTL1.REGS.PRB_HA_PTR
Address	00000000050112F1 (SCOM)
Description	The NTL PRB Header Array Pointer Register is used to change the start and/or end entry in the NTL Header Array for holding PRB header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	PRB_HA_PTR_Reserved1: Reserved.
5:11	RW	PRB_HA_PTR_START: Starting Header Array location for PRB headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	PRB_HA_PTR_Reserved2: Reserved.
17:23	RW	PRB_HA_PTR_END: Ending Header Array location for PRB headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL ATR Header Array Pointer Register
Mnemonic	NPU.STCK2.NTL1.REGS.ATR_HA_PTR
Address	00000000050112F2 (SCOM)
Description	The NTL ATR Header Array Pointer Register is used to change the start and/or end entry in the NTL Header Array for holding ATR header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	ATR_HA_PTR_Reserved1: Reserved.
5:11	RW	ATR_HA_PTR_START: Starting Header Array location for ATR headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
12:16	RW	ATR_HA_PTR_Reserved2: Reserved.
17:23	RW	ATR_HA_PTR_END: Ending Header Array location for ATR headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Header Array Pointer Register
Mnemonic	NPU.STCK2.NTL1.REGS.RSP_HA_PTR
Address	00000000050112F3 (SCOM)
Description	The NTL RSP Header Array Pointer Register is used to change the start and/or end entry in the NTL Header Array for holding RSP header information.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	RSP_HA_PTR_Reserved1: Reserved.
5:11	RW	RSP_HA_PTR_START: Starting Header Array location for RSP headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.

Bits	SCOM	Field Mnemonic: Description
12:16	RW	RSP_HA_PTR_Reserved2: Reserved.
17:23	RW	RSP_HA_PTR_END: Ending Header Array location for RSP headers received from the GPU. The Header Array is 128 entries and is divided into four sections to hold CREQ, PRB, ATR, and RSP headers. These four sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL CREQ Data Array Pointer Register
Mnemonic	NPU.STCK2.NTL1.REGS.CREQ_DA_PTR
Address	00000000050112F4 (SCOM)
Description	The NTL CREQ Data Array Pointer Register is used to change the start and/or end entry in the NTL Data Array for holding CREQ data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	CREQ_DA_PTR_Reserved1: Reserved.
3:11	RW	CREQ_DA_PTR_START: Starting Data Array location for CREQ data flits received from the GPU. The Data Array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	CREQ_DA_PTR_Reserved2: Reserved.
15:23	RW	CREQ_DA_PTR_END: Ending Data Array location for CREQ data flits received from the GPU. The Data Array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL RSP Data Array Pointer Register
Mnemonic	NPU.STCK2.NTL1.REGS.RSP_DA_PTR
Address	00000000050112F5 (SCOM)
Description	The NTL RSP Data Array Pointer Register is used to change the start and/or end entry in the NTL Data Array for holding RSP data flits.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	RSP_DA_PTR_Reserved1: Reserved.
3:11	RW	RSP_DA_PTR_START: Starting Data Array location for RSP data flits received from the GPU. The Data Array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
12:14	RW	RSP_DA_PTR_Reserved2: Reserved.
15:23	RW	RSP_DA_PTR_END: Ending Data Array location for RSP data flits received from the GPU. The Data Array is 512 entries and is divided into two sections to hold CREQ and RSP data flits. These two sections cannot overlap.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NTL Private Register Interface (PRI) Configuration Register
Mnemonic	NPU.STCK2.NTL1.REGS.PRI_CONFIG
Address	00000000050112F6 (SCOM)
Description	The NTL PRI Configuration Register is used to set up the Private Register Interface settings for this NTL. This register must be configured before any PRI requests are attempted to NDL or PHY registers.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PRI_CONFIG_NDL: NDL indication sent in the PRI Read/Write access: 00 = NDL 0. 01 = NDL 1. 10 = NDL 2. 11 = Disable (this will disable NTL from decoding the NDL register space).
2:3	RW	PRI_CONFIG_PHY: Indicates if this NTL should decode a PHY register space: 00 = Decode PHY0 register space (one and only one NTL that is connected to PHY 0 must be set to this value). 01 = Decode PHY1 register space (one and only one NTL that is connected to PHY 1 must be set to this value). 1- = Do not decode any PHY register space.
4:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	NTL Miscellaneous Configuration 1 Register
Mnemonic	NPU.STCK2.NTL1.REGS.CONFIG1
Address	00000000050112F8 (SCOM)
Description	The NVLink transaction layer (NTL) Miscellaneous Configuration 1 Register is used to control NVLink packet formatting by the POWER9 processor. It also controls resetting of the POWER9 NTL.

Bits	SCOM	Field Mnemonic: Description
0	RW	COMPRESSED_RSP_ENA: When 0b1, NTL will attempt to compress responses that it sends to the GPU whenever possible.
1:3	RW	CONFIG1_Reserved1: Reserved.
4	RW	CREQ_AE_ALWAYS: When 0b1, NTL will always send an AE flit when it sends a CREQ packet to the GPU.
5	RW	DGD_AE_ALWAYS: When 0b1, NTL will always send an AE flit when it sends a Downgrade packet to the GPU.
6	RW	RSP_AE_ALWAYS: When 0b1, NTL will always send an AE flit when it sends a Response packet to the GPU.
7	RW	CONFIG1_Reserved2: Reserved.
8:9	RW	NTL_RESET: This field indicates the NTL Reset mode: 00 - Reset disabled. 11 - Reset (Fence) both NTL and the processor bus for this Brick. 10 - Reset (Fence) only the processor bus for this Brick, NTL will be operational. 01 - Reserved. The only legal sequence is 00->11->10->00. This field should not be changed unless bits 0:1 in the CQ Fence Status register equals the value in this field.
10:63	RW	CONFIG1_Reserved3: Reserved.

Register Name	NTL Scratch 1 Register
Mnemonic	NPU.STCK2.NTL1.REGS.SCRATCH1
Address	00000000050112FA (SCOM)
Description	The NTL Scratch 1 Register is provided in case a new control function is required in the future. It has no control function at this time.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IDIAL_SCRATCH1: Scratch register.

Register Name	NTL Low Power Configuration Register
Mnemonic	NPU.STCK2.NTL1.REGS.LOW_PWR
Address	00000000050112FC (SCOM)
Description	The NTL Low Power Configuration Register is used to enable the NPU to request that the NVLink interconnect be placed into low-power mode. The register also defines the conditions under which the NPU turns its low-power request on or off.

Bits	SCOM	Field Mnemonic: Description
0	RW	LP_MODE_ENABLE: When 0b1, this NTL is allowed to activate the Low Power Requested signal to NDL when the Low Power Count > = Low Power Count Threshold.
1	RW	LP_ONLY_MODE: When 0b1, this NTL will activate the Low Power Requested signal to NDL continuously. This can be used for lab stress/debug.
2:7	RW	LP_TIMER_TICK_CONFIG: Rate for the Low Power timer tick (2^n cycles).
8:19	RW	LP_MIN_CRED_THRESH: Whenever the NDL Replay Buffer Credits < this threshold, the Low Power Requested signal to NDL will be de-activated. This value must be greater than 0 and less than the Max Credit Threshold.
20:31	RW	LP_MAX_CRED_THRESH: Whenever the NDL Replay Buffer Credits > = this threshold and the Low Power timer tick is active, then the Low Power Count will be incremented by 1. This value must be greater than the Min Credit Threshold.
32:43	RW	LP_CNT_THRESH: Whenever the Low Power Count > = this threshold, this NTL will activate the Low Power Requested signal to NDL until the NDL Replay Buffer Credits < Low Power Min Credit Threshold. This value must be greater than 0.
44:63	RO	Constant = 0b00000000000000000000

Register Name	NPU ATS PMU Control Register
Mnemonic	NPU.ATS.REG.NPU_AT_PMU_CTRL
Address	0000000005011300 (SCOM)
Description	The PMU Count Control Register contains configuration information for the PMULet counters in ATS. Note ATS also counts events from MISC macro.

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CONFIG_ENABLE: 0b1 - PMULet enabled.
1	RW	PERF_CONFIG_RESETMODE: PMULet resetmode.
2	RW	PERF_CONFIG_FREEZEMODE: PMULet freezemode.
3	RW	PERF_CONFIG_DISABLE_PMISC: PMULet disable_pmisc.
4	RW	PERF_CONFIG_PMISC_MODE: PMULet pmisc_mode.

Bits	SCOM	Field Mnemonic: Description
5:7	RW	PERF_CONFIG_CASCADE: PMULet cascade.
8:9	RW	PERF_CONFIG_PRESCALE_C0: PMULet prescale_c0.
10:11	RW	PERF_CONFIG_PRESCALE_C1: PMULet prescale_c1.
12:13	RW	PERF_CONFIG_PRESCALE_C2: PMULet prescale_c2.
14:15	RW	PERF_CONFIG_PRESCALE_C3: PMULet prescale_c3.
16:17	RW	PERF_CONFIG_OPERATION_C0: PMULet operation_c0.
18:19	RW	PERF_CONFIG_OPERATION_C1: PMULet operation_c1.
20:21	RW	PERF_CONFIG_OPERATION_C2: PMULet operation_c2.
22:23	RW	PERF_CONFIG_OPERATION_C3: PMULet operation_c3.
24:26	RW	PERF_CONFIG_EVENTS: Choose 1 of 8 groups of events to route to PMULet for counting.
27:31	RW	CFG_PMU_PE_MATCH0: bit 0 - 0b1 Enable event gate by PE, match 0. bits 1 to 4 - PE ID.
32:36	RW	CFG_PMU_PE_MATCH1: bit 0 - 0b1 Enable event gate by PE, match 1. bits 1 to 4 - PE ID. Used for group 3 where the same event is counted for two PE IDs.
37:41	RW	PERF_CONFIG_SPARE: Reserved.
42:63	RO	Constant = 0b00000000000000000000

Register Name	NPU ATS PMU Count Register
Mnemonic	NPU.ATS.REG.NPU_AT_PMU_CNT
Address	0000000005011301 (SCOM)
Description	The NPU ATS PMULet Count Register contains the PMULet counters in ATS (4 x 16b). Note ATS also counts events from MISC macro

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PMU_CNT0: PMULet Counter 0.
16:31	ROX	PMU_CNT1: PMULet Counter 1.
32:47	ROX	PMU_CNT2: PMULet Counter 2.
48:63	ROX	PMU_CNT3: PMULet Counter 3.

Register Name	NPU ATS Error Inject Register
Mnemonic	NPU.ATS.REG.NPU_AT_ECC
Address	0000000005011302 (SCOM)
Description	The NPU ATS Error Inject Register is used to inject errors into the arrays in ATS.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INJECT_MODE: 0b10 - Inject Once. 0b01 - Inject continuously.
2:3	RW	INJECT_TYPE: 0b01 - Inject CE (inverts b41). 0b10 - Inject UE (inverts b23 and b53).
4	RW	INJECT_ENABLE: 0b1 - Error inject enabled.

Bits	SCOM	Field Mnemonic: Description
5:8	RW	ARRAY_SELECT: 0b1xxx - TCE Cache Directory (parity protected). 0bx1xx - TCE Data Array (parity protected). 0bxx1x - XLT_EA Array (ecc protected). 0bxxx1 - TDR_mem Array (ecc protected). Note >1 array may be injected simultaneously.
9:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	NPU ATS Debug/Trace Control Register
Mnemonic	NPU.ATS.REG.NPU_ATS_DEBUG
Address	0000000005011303 (SCOM)
Description	The NPU ATS Debug/Trace Control Register is used to control what information is placed on the debug bus by ATS.

Bits	SCOM	Field Mnemonic: Description
0	RW	DEBUG_ENABLE: Debug bus 0 and 1 enable clocks.
1:3	RW	DEBUG_0_SELECT: Debug bus 0 select. 0b001 = arb_reg_trace(0 to 51) and td(52 to 87). 0b010 = xpl_reg_trace(0 to 87). 0b011 = rrc_debug_vec(0 to 87). 0b100 = mlc_reg_trace_bus_0(0 to 87). 0b101 = mlc_reg_trace_bus_1(0 to 87). else = debug0_in_q(0 to 87).
4:6	RW	DEBUG_1_SELECT: Debug bus 1 select. 0b001 = arb_reg_trace(0 to 51) and td(52 to 87). 0b010 = xpl_reg_trace(0 to 87). 0b011 = rrc_debug_vec(0 to 87). 0b100 = mlc_reg_trace_bus_0(0 to 87). 0b101 = mlc_reg_trace_bus_1(0 to 87). else = debug1_in_q(0 to 87).
7:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	NPU ATS Chicken Switch Register
Mnemonic	NPU.ATS.REG.ATS_CKSW
Address	0000000005011304 (SCOM)
Description	The NPU ATS Chicken Switch Register is used to disable logic functions.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ATS_CKSW_SPARE: 0b1 - Disable logic function. Spare / not used.

Register Name	NPU ATS Hold Register
Mnemonic	NPU.ATS.REG.ATS_HOLD
Address	0000000005011305 (SCOM)
Description	The NPU ATS Error Report Register (c_err_rpt) indicates which address translation error conditions have occurred and been captured by a c_err_rpt macro. These errors are routed to MISC for FIR, interrupt, freeze and fence logic (maskable by SCAN-only latches).

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	TVT_ENTRY_INVALID_ESR: 0b1 - An address translation request attempted to use a TVE that was not valid (TCE Table Size = 0b00000). Classification: ER-single.
1	RWX_WCLRREG	TVT_ADDR_RANGE_ERR_ESR: 0b1 - A DMA address failed the range check specified in the TVE. Translate mode: 1) TVT configured to use > max EA (49b) or 2) non-used EA bits are not zero. No-translate mode: EA out of range. Classification: ER-single.
2	RWX_WCLRREG	TCE_PAGE_ACCESS_ERR_ESR: 0b1: An address translation request attempted to access a page in a way that is not allowed by the access permissions in the referenced TCE. For example, attempting to write to a read-only page. Error occurred during TCE Cache lookup. Classification: ER-single.
3	RWX_WCLRREG	TCE_CACHE_MULT_HIT_ERR_ESR: 0b1: An address translation request hit multiple entries in the TCE cache. Classification: ER-single.
4	RWX_WCLRREG	MLC_ACCESS_ERR_ESR: 0b1 - An address translation request attempted to access a page in a way that. is not allowed by the access permissions in the referenced TCE. For example, attempting to write to a read-only page. Error occurred during cache miss table-walk. Classification: ER-single.
5	RWX_WCLRREG	TCE_REQ_TO_ERR_ESR: 0b1 - A TCE table-walk fetch request timed out. Classification: Fatal.
6	RWX_WCLRREG	TCD_PERR_ESR: 0b1 - A parity error was detected on the TCE cache directory array. Classification: Informational.
7	RWX_WCLRREG	TDR_PERR_ESR: 0b1 - A parity error was detected on the TCE cache data array. Classification: Informational.
8	RWX_WCLRREG	AT_EA_UE_ESR: 0b1 - An uncorrectable error was detected on the TCE effective address array (XLT_EA) Classification: Fatal.
9	RWX_WCLRREG	AT_EA_CE_ESR: 0b1 - A correctable error was detected on the TCE effective address array (XLT_EA) Classification: Informational.
10	RWX_WCLRREG	AT_TDRMEM_UE_ESR: 0b1 - Uncorrectable ECC error from TDR_mem array (MLC table-walk state machine also hangs). Classification: Fatal.
11	RWX_WCLRREG	AT_TDRMEM_CE_ESR: 0b1 - Correctable ECC error from TDR_mem array. Classification: Informational.
12	RWX_WCLRREG	RSPOUT_UE_ESR: 0b1 - Uncorrectable ECC error from CQ CTL DMA Read data to TDR_mem array during table-walk. Classification: Fatal.
13	RWX_WCLRREG	RSPOUT_CE_ESR: 0b1 - Correctable ECC error from CQ CTL DMA Read data to TDR_mem array during table_walk. Classification: Informational.
14	RWX_WCLRREG	TVT_PERR_ESR: 0b1 - A parity error has been detected on the registers that make up the TVT (checked every cycle). Classification: Fatal.
15	RWX_WCLRREG	IODA_ADDR_PERR_ESR: 0b1 - A parity error has been detected on the IODA Address Register (checked every cycle). Classification: Fatal.
16	RWX_WCLRREG	ATS_CTRLR_PERR_ESR: 0b1 - A parity error has been detected on the ATS Control Register (checked every cycle). Classification: Fatal.
17	RWX_WCLRREG	ATS_TOR_PERR_ESR: 0b1 - A parity error has been detected on the ATS Timeout Control Register (checked every cycle). Classification: Fatal.
18	RWX_WCLRREG	INVAL_IODA_TBL_SEL_ESR: 0b1 - An invalid table select encode was used in the IODA Address Register (checked on IODA Table Data register read/write). Classification: Informational.
19	RWX_WCLRREG	ESR_RSVD_19: Reserved.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	NPU ATS Mask Register
Mnemonic	NPU.ATS.REG.ATS_MASK
Address	0000000005011306 (SCOM)
Description	The NPU ATS Error Mask Register (c_err_rpt) enables masking of address translation error conditions before routing to MISC for FIR, interrupt, freeze and fence logic. See NPU ATS Error Report Register for a description of error bits. writable via SCAN-only latches.

Bits	SCOM	Field Mnemonic: Description
0:19	RO	IDIAL_ATS_MASK: 0b0 = no mask, 0b1 = mask.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NPU ATS Control Register
Mnemonic	NPU.ATS.REG.ATS_CTRL
Address	0000000005011320 (SCOM)
Description	The NPU ATS Control Register is used to control logic behavior.

Bits	SCOM	Field Mnemonic: Description
0	RW	ATS_ARB_STOP: 0b1 - The NPU ATS rerun logic is stopped. Must also assert ats_arb_stall. TCE table-walks and TCE Kills complete normally.
1	RW	ATS_ARB_STALL: 0b1 - The NPU ATS arbiter blocks all new TCE translate requests from CQ CTL. TCE table walks, translate requests waiting for TCE table walks and TCE Kills complete normally.
2	RW	ATS_TCE_CACHE_DISABLE: 0b1 - The NPU ATS TCE cache will be disabled. All translate requests require table-walk.
3	RW	ATS_TCE_CACHE_1W: 0b1 - The NPU ATS TCE cache will be 1w associative (vs. default 4w associative).
4	RW	ATS_CONFIG_BRAZOS: 0b1 - The NPU ATS uses Brazos mode when expanding GPU Real Address to POWER9 Real Address (vs. default Coral mode). Affects only TVE no-translate mode operations.
5:9	RW	CONFIG_SYNC_WAIT: Number of clock cycles from CTL sync request to CTL sync valid (masks round-trip staging latency ATS->CTL->ATS).
10:63	RW	ATS_CTRL_SPARE: spare config bits.

Register Name	NPU ATS IODA Table Address Register
Mnemonic	NPU.ATS.REG.IODA_ADDR
Address	0000000005011321 (SCOM)
Description	The NPU ATS IODA Table Address register sets the address for accessing one of the architected IODA tables in the NPU. A DMA Quiesce is required before accessing any c8t array (see idial table_select).

Bits	SCOM	Field Mnemonic: Description
0	RW	AUTO_INCREMENT: 0b1 = Automatically increment the Table Address field after the IODA Table Data Register is accessed.
1:10	RO	Constant = 0b0000000000

Bits	SCOM	Field Mnemonic: Description
11:15	RW	TABLE_SELECT: This encoding selects the table to access. 0b01001 - TCE Validation Table (TVT, 16 entries, must be quiesced). 0b01010 - TCE Cache Directory (TCD, 1k entries, must be quiesced). 0b01011 - TCE Cache Data (TDR, 1k entries, must be quiesced). 0b01100 - TCE Tree Walk Data (TDRmem, 24 entries (of 32 entry array), must be quiesced). 0b10000 - AT Effective Address (XLT_EA, 96 entries (of 128 entry array), must be quiesced). others - return random data on reads, ignore writes.
16:53	RO	Constant = 0b00000000000000000000000000000000000000000000
54:63	RWX	TABLE_ADDRESS: This value defines the address for read and write accesses to the selected IODA table. If the Auto Increment bit is set, this value increments after every read or write. of the IODA Table Data Register 0, and advances through the entire 10b range, then wraps to zero. Note, if a table address space is < 10b (TVT, XLT_EA and TDRmem) the least significant address bits are used. Note, the TCD and TDR are implemented using 4x256 entry arrays: (54:55) = array number. (56:63) = hash number.

Register Name	**NPU ATS IODA Table Data 0 Register**
Mnemonic	NPU.ATS.REG.IODA_DAT0
Address	0000000005011322 (SCOM)
Description	The NPU ATS IODA Table Data Register contains the data for writing to or reading from an IODA table in the NPU. A read of this register generates a read of the table and address contained in the IODA Table Address Register. The read data is returned with the read operation. Read data of all 0b1 indicates error (invalid Table Address, invalid offset into Table Address read data parity error, read data ecc ue or sue). A write to this register generates a write to the table and address contained in the IODA Table Address Register. Reads or writes to this register increment the IODA Table Address Register Table Address if the Auto Increment bit is set. c8t arrays may only read/write when ATS is quiesced.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	TABLE_DATA: Data to write or read result data.

Register Name	NPU ATS DMA Synchronization Register
Mnemonic	NPU.ATS.REG.DMA_SYNC
Address	0000000005011323 (SCOM)
Description	This register is used to indicate that all DMA reads or writes that are in progress when the register is written have completed. In this case, in progress means CTL has requested a TCE address translation, and the ATS arbiter has selected the request and begun processing. A sync is typically used during purge cache operations to ensure all old DMA operations have finished using old pages in memory. Firmware must ensure all accesses to an old page have ceased before reallocating a page to another process or thread. Note there is no distinction between read and write sync (all operations must complete for both types of request). Note a DMA sync is also initiated (by hardware) before sending an interrupt request, or by a DMA Quiesce request (by software). This may delay a Firmware sync complete if the requests collide, but will not reset a sync that has completed. A DMA sync may not be cancelled.

Bits	SCOM	Field Mnemonic: Description
0	RWX	START_READ_SYNC: 0b0 - no effect. 0b1 = Starts the DMA Read Synchronization Process.
1	ROX	READ_SYNC_COMPLETE: 0b0 - DMA Read operations that were active when the Start Sync bit. was written to 0b1 are still pending. 0b1 - All DMA read operations that were active when the Start Sync bit. was written have completed.
2	RWX	START_WRITE_SYNC: 0b0 - no effect. 0b1 = Starts the DMA Write Synchronization Process.
3	ROX	WRITE_SYNC_COMPLETE: 0b0 - DMA Write operations that were active when the Start Sync bit. was written to 0b1 are still pending. 0b1 - All DMA write operations that were active when the Start Sync bit. was written have completed.
4:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	NPU ATS TCE Kill Register
Mnemonic	NPU.ATS.REG.TCE_KILL
Address	0000000005011324 (SCOM)
Description	The TCE Kill Register provides a mechanism to support Firmware Managed TCE Coherency. Software has the ability to invalidate any potential TCE system address that may be cached in the NPU. Invalidates to non-cached entries have no affect. Writing this register has a side effect of generating an invalidate/kill to the TCE Cache.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INVALIDATE_ALL: 0b1 - TCE Kill entire cache Note: Bits 0 and 2 cannot both be set!.
1	RO	Constant = 0b0
2	RWX	INVALIDATE_ONE: 0b1 - TCE Kill the Effective address specified in this register Note: Bits 0 and 2 cannot both be set!.
3	RO	Constant = 0b0
4:7	RW	INVALIDATE_PE_NUMBER: PE number of the cache entry or entries to invalidate. Required for invalidate_operation '001' and not required for invalidate_operation '1xx'.
8:14	RO	Constant = 0b0000000

Bits	SCOM	Field Mnemonic: Description
15:51	RW	INVALIDATE_ADDRESS: NV-Link address for the specified PE number for which the corresponding direct TCE is to be invalidated. I/O page aligned. Register bits 15:51 aligns with NV-Link address 51:15. Since this field is I/O page aligned, some of the low order bits of this field will need to be '0' for the I/O page sizes larger than 4 KB. Required for invalidate_operation '001' and not required for invalidate_operation '1xx'.
52:63	RO	Constant = 0b000000000000

Register Name	**NPU ATS Quiesce DMA Register**
Mnemonic	NPU.ATS.REG.NPU_Q_DMA_R
Address	0000000005011325 (SCOM)
Description	The NPU ATS Quiesce DMA Register is used to temporarily block the internal NPU logic from processing new DMA reads or writes from the NV-Link transaction layer interface. This is accomplished via the following sequence: 1) ATS arbiter blocks new TCE translate requests from CTL 2) Wait for all TCE translate requests that are in progress to complete This includes ATS pipeline latency, TCE cache miss table-walk and reruns) 3) Reset bit 6 to 0b0 (all TCE translation requests complete) 4) Wait for CTL to complete all DMA commands 5) Reset bit 4 to 0b0 (all DMAs complete) The quiesce may be cancelled before completion by writing bit 0 to 0b0. ATS is DMA quiesced when bit 1 = 0b1 and bit 4 = 0b0

Bits	SCOM	Field Mnemonic: Description
0	RWX	QUIESCE_DMA: 0b0: UT = 1 commands from the NV-Link interface are processed normally. 0b1: UT = 1 commands from the NV-Link interface are accepted but not processed (ATS arbiter stops selecting new requests). If bit 1 = 0b1, hardware will reset this bit when the dma quiesce is complete, exiting the quiesce state.
1	RWX	QUIESCE_AUTO_RESET: 0b0 - Only software can reset bit 0 of this register. 0b1 - Software can reset bit 0 or hardware will reset bits 0:1 when bits 4 and 6 of this register are both equal to 0b0.
2:3	RO	Constant = 0b00
4	ROX	DMA_RESPONSE: 0b0 - quiesce request has completed (No UT = 1 DMA commands are outstanding on the Powerbus). 0b1 - quiesce request is in progress (UT = 1 DMA commands are outstanding on the Powerbus). Only valid when bit 0 = 0b1.
5	RO	Constant = 0b0
6	ROX	TCE_RESPONSE: 0b0 - quiesce request has partially completed (No TCE translations are in progress). 0b1 - quiesce request is in progress (TCE translations are in progress). Only valid when bit 0 = 0b1.
7:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000

Register Name	**NPU ATS TCE Response Timeout Control Register**
Mnemonic	NPU.ATS.REG.ATS_TCR
Address	0000000005011326 (SCOM)
Description	The NPU ATS TCE Response Timeout Control Register controls the timeout counters in the ATS internal logic. The timeout applies to each DMA read of a TCE Table Walk.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10:15	RW	TCE_TIMEOUT: TCE Response Timeout Value. Timeout minimum is $2^{((n) \times 32)}$ cycles Timeout maximum is $2^{((n) \times 48)}$ cycles 0b1xxxxx = disables the timeout. 0b010100 = provides timeout of ~14 to 21 ms (default).
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	NPU ATS Error Status Register
Mnemonic	NPU.ATS.REG.NPU_AT_ESR
Address	0000000005011327 (SCOM)
Description	The NPU ATS Error Status Register indicates which address translation error conditions have occurred. Errors are maskable via NPU ATS Error Status Mask Register. Same as c_err_rpt register except that reporting is maskable via SCOM independent of FIR reporting.

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	IDIAL_ATS_ESR: See NPU ATS Error Report Register (c_err_rpt) for details.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NPU ATS Error Status Mask Register
Mnemonic	NPU.ATS.REG.NPU_AT_ESMR
Address	0000000005011328 (SCOM)
Description	The NPU AT Error Status Mask Register gates which address translation related error conditions will be logged in the NPU AT Error Status Register.

Bits	SCOM	Field Mnemonic: Description
0:19	RW	IDIAL_ATS_ESR_MSK: 0b1 = An error will not be logged in the NPU ATS Error Status Register. See NPU ATS Error Report Register (c_err_rpt) for details.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NPU ATS First Error Status Register
Mnemonic	NPU.ATS.REG.NPU_AT_FESR
Address	0000000005011329 (SCOM)
Description	The NPU ATS First Error Status Register indicates which address translation related error conditions occurred first. The register freezes after the first error is detected. The value in this register remains frozen until the entire register is cleared by firmware.

Bits	SCOM	Field Mnemonic: Description
0	RWX	FIRST_ERROR_CAPTURED: 0b1 = Error capture information is valid.
1:2	RWX	FIRST_ERROR_SPARE: Reserved.
3:7	RWX	FIRST_ERROR_DECODE: 5-bit encode of first error source. See NPU ATS Error Report Register (c_err_rpt) for details.
8:63	RWX	FIRST_ERROR_INFO: Debug Information for the selected error. See vhdl for details.

Register Name	NPU ATS First Error Status Mask Register
Mnemonic	NPU.ATS.REG.NPU_AT_FESMR
Address	000000000501132A (SCOM)
Description	The ATS First Error Status Mask Register gates which address translation related error conditions will be logged in the NPU ATS First Error Status Register.

Bits	SCOM	Field Mnemonic: Description
0:19	RW	IDIAL_ATS_FER_MSK: 0b1 = An error will not be logged in the NPU ATS First Error Status Register. See NPU ATS Error Report Register (c_err_rpt) for details.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	XTS Error Hold Register
Mnemonic	NPU.XTS.REG.ERR_HOLD
Address	0000000005011340 (SCOM)
Description	XTS error c_err_rpt status and clear register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	DEBUG0_CONFIG_P_ERR: debug0 configuration register parity error.
1	RWX_WCLEAR	DEBUG1_CONFIG_P_ERR: debug1 configuration register parity error.
2	RWX_WCLEAR	XTS_CONFIG_P_ERR: xts configuration register parity error.
3:7	RWX_WCLEAR	ERR_UNUSED1: Unused.
8	RWX_WCLEAR	SNP_REG_ERR0: PBus Snoop 0 address parity error.
9	RWX_WCLEAR	SNP_REG_ERR1: PBus Snoop 0 ttag parity error.
10	RWX_WCLEAR	SNP_REG_ERR2: PBus Snoop 1 address parity error.
11	RWX_WCLEAR	SNP_REG_ERR3: PBus Snoop 1 ttag parity error.
12	RWX_WCLEAR	SNP_REG_ERR4: PBus Snoop bad operation error.
13	RWX_WCLEAR	SNP_REG_ERR5: PBus Snoop sequence parity error.
14	RWX_WCLEAR	SNP_REG_ERR6: PBus Snoop time out.
15	RWX_WCLEAR	ATR_ERR_SM_STATE: ATR state machine parity error.
16	RWX_WCLEAR	ATSD_ERR_SM_STATE: ATSD state machine parity error.
17	RWX_WCLEAR	ATR_ERR_TIMEOUT: ATR state machine time out.
18	RWX_WCLEAR	ATSD_ERR_TIMEOUT: ATSD state machine time out.
19	RWX_WCLEAR	ATSD_ERR_BAD_TAG: unexpected ATSD response tag.
20	RWX_WCLEAR	MAP_REG_ERR2: ATR BDF table lookup parity error.
21	RWX_WCLEAR	MAP_REG_ERR3: ATR PID table lookup parity error.
22	RWX_WCLEAR	MAP_REG_ERR4: ATSD BDF table lookup parity error.
23	RWX_WCLEAR	ATR_ERR_ARBSTATE: ATR arbiter state not on-hot during selection phase.
24:31	RWX_WCLEAR	ERR_UNUSED2: Unused.
32	RWX_WCLEAR	IFC_REG_CERR0: stack 0 MMU response correctable ECC error.

Bits	SCOM	Field Mnemonic: Description
33	RWX_WCLEAR	IFC_REG_CERR1: stack 1 MMU response correctable ECC error.
34	RWX_WCLEAR	IFC_REG_CERR2: stack 2 MMU response correctable ECC error.
35	RWX_WCLEAR	MAP_REG_CERR0: AMR SRAM correctable ECC error.
36	RWX_WCLEAR	MAP_REG_CERR1: SEIDR SRAM correctable ECC error.
37:47	RWX_WCLEAR	ERR_UNUSED3: Unused.
48	RWX_WCLEAR	IFC_REG_ERR0: stack 0 MMU response uncorrectable ECC error.
49	RWX_WCLEAR	IFC_REG_ERR1: stack 0 MMU response special uncorrectable ECC error.
50	RWX_WCLEAR	IFC_REG_ERR2: stack 0 MMU response bad tag.
51	RWX_WCLEAR	IFC_REG_ERR3: stack 1 MMU response uncorrectable ECC error.
52	RWX_WCLEAR	IFC_REG_ERR4: stack 1 MMU response special uncorrectable ECC error.
53	RWX_WCLEAR	IFC_REG_ERR5: stack 1 MMU response bad tag.
54	RWX_WCLEAR	IFC_REG_ERR6: stack 2 MMU response uncorrectable ECC error.
55	RWX_WCLEAR	IFC_REG_ERR7: stack 2 MMU response special uncorrectable ECC error.
56	RWX_WCLEAR	IFC_REG_ERR8: stack 2 MMU response bad tag.
57	RWX_WCLEAR	MAP_REG_ERR0: AMR SRAM uncorrectable ECC error.
58	RWX_WCLEAR	MAP_REG_ERR1: SEIDR SRAM uncorrectable ECC error.
59:62	RWX_WCLEAR	ERR_UNUSED4: Unused.
63	RWX_WCLEAR	ATR_MISS_IRQ: atr miss interrupt.

Register Name	**XTS CERR Error Injection Test Register**
Mnemonic	NPU.XTS.REG.TEST_CERR
Address	0000000005011341 (SCOM)
Description	XTS c_err_rpt error injection test register

Bits	SCOM	Field Mnemonic: Description
0	ROX	ATR_ERR_INJ_PEND: Indicates that an ATR SRAM error injection has been started, but the error has not been injected yet. The error will be injected when the next ATR response is assembled by the XTS.
1	ROX	MAP_ERR_INJ_PEND: Indicates that an MAP SRAM error injection has been started, but the error has not been injected yet. The error will be injected the next time the SEIDR or AMR SRAM is written via MMIO or SCOM.
2:55	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
56:57	WO	TEST_CERR_REGSEL: Selects c_err_rpt to inject an error 00b = none. 01b = fir. 10b = ATR SRAM. 11b = SEIDR/AMR SRAM.
58:63	WO	TEST_CERR_BITSEL: Selects the FIR bit to inject the error 0 = The MSB 1 = The second MSB, ..., 63: The LSB); select CE (0) or UE (1) for SRAM injection.

Register Name	XTS Error Mask Register
Mnemonic	NPU.XTS.REG.ERR_MASK
Address	0000000005011342 (SCOM)
Description	XTS error c_err_rpt mask register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	ERR_MASK_BITS: XTS error c_err_rpt mask bits.

Register Name	XTS Error First Register
Mnemonic	NPU.XTS.REG.ERR_FIRST
Address	0000000005011343 (SCOM)
Description	XTS error first register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLEAR	ERR_FIRST_BITS: XTS error first bits.

Register Name	XTS Configuration Register
Mnemonic	NPU.XTS.REG.XTS_CONFIG
Address	0000000005011344 (SCOM)
Description	XTS Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	XTS_CONFIG_BRAZOS: Enables brazos style physical address compression.
1	RW	XTS_CONFIG_MMIOSD: Enables MMIO controlled translation shoot downs.
2	RW	XTS_CONFIG_BIG_RSP: Enables ATR response sizes matching exactly the request.
3	RW	XTS_CONFIG_CHOP1G: Split 1G page into 16 2M pages.
4	RW	XTS_CONFIG_DIS_NCNP: Disable NCNP flag on inhibited/guarded pages.
5	RW	XTS_CONFIG_OVR_PM: Override PM bit in ATR with PR bit in PID table.
6	RW	XTS_CONFIG_TRY_ATR_RO: Retry RW checkouts as RO on protection fault.
7	RW	XTS_CONFIG_SPLURGE: Use all 8 NMMU channels for prefetches if available.
8	RW	XTS_CONFIG_LIM_PS: Limit valid page sizes to 64K/2M/1G; if 1G splitting is enabled, only 64K/2MB ATR responses will be sent.
9	RW	XTS_CONFIG_PREF2DMD: Convert NMMU prefetch requests to demand types, forcing table walk on NMMU cache miss.
10	RW	XTS_CONFIG_PREFEVOD: Walks even addresses, then odd addresses for prefetches, or vice versa.
11	RW	XTS_CONFIG_EAINJ: When set to 1, injects 3 random bits into EA[12:14] for CO requests.
12	RW	XTS_CONFIG_SPL_ONLY: If set and splurge active, preferred slot no longer wins for prefetches.
13:15	RW	XTS_CONFIG_UNUSED1: XTS configuration unused/reserved bits for future use.
16:23	RW	XTS_CONFIG_TLBIE_DEC_RATE: TLBI temperature dec pulse every n+1 cycles.
24:31	RW	XTS_CONFIG_TLBIE_INC_RATE: TLBI temperature inc pulse every n+1 cycles.
32:39	RW	XTS_CONFIG_TLBIE_CNT_THRESH: throttle if global TLBI temperature counter exceeds this threshold.

Bits	SCOM	Field Mnemonic: Description
40	RW	XTS_CONFIG_UNUSED2: XTS configuration unused/Reserved bits for future use.
41:43	RW	XTS_CONFIG_PREF_TIMEOUT: Delay after which an ATR state machine no longer issues prefetches.
44:47	RW	XTS_CONFIG_PREF_DEPTH: Maximum number of prefetches returned in addition to demand for single ATR request.
48:51	RW	XTS_CONFIG_PREF_THRSH0: Number of concurrent ATR prefetches when no request is queued in front of ATR state machines.
52:55	RW	XTS_CONFIG_PREF_THRSH1: Number of concurrent ATR prefetches when one request is queued in front of ATR state machines.
56:59	RW	XTS_CONFIG_PREF_THRSH2: Number of concurrent ATR prefetches when two requests are queued in front of ATR state machines.
60:63	RW	XTS_CONFIG_PREF_THRSH3: Number of concurrent ATR prefetches when three requests are queued in front of ATR state machines.

Register Name	**XTS Configuration 2 Register**
Mnemonic	NPU.XTS.REG.XTS_CONFIG2
Address	0000000005011345 (SCOM)
Description	XTS Config2 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	XTS_CONFIG2_PERF_ENABLE: PMULet Enable (clocks enable).
1	RW	XTS_CONFIG2_PERF_RESETMODE: 0 = reset-on-read. 1= reset-on-write.
2	RW	XTS_CONFIG2_PERF_FREEZEMODE: 0 = freeze-on-any-max. 1 = freerun-mode.
3	RW	XTS_CONFIG2_PERF_DISABLE_PMISC: 0 = enable-pmisc 1 = disable-pmisc control of counters.
4	RW	XTS_CONFIG2_PERF_PMISC_MODE: 0 = Global pmu pmisc no reset. 1 = Global pmu miscellaneous reset-on-enable.
5:7	RW	XTS_CONFIG2_PERF_CASCADE: pmulet cascade configuration.
8:9	RW	XTS_CONFIG2_PERF_PRESCALE_C0: Prescale configuration for counter 0.
10:11	RW	XTS_CONFIG2_PERF_PRESCALE_C1: Prescale configuration for counter 1.
12:13	RW	XTS_CONFIG2_PERF_PRESCALE_C2: Prescale configuration for counter 2.
14:15	RW	XTS_CONFIG2_PERF_PRESCALE_C3: Prescale configuration for counter 3.
16:23	RW	XTS_CONFIG2_PERF_EVENT0: Event 0 select.
24:31	RW	XTS_CONFIG2_PERF_EVENT1: Event 1 select.
32:39	RW	XTS_CONFIG2_PERF_EVENT2: Event 2 select.
40:47	RW	XTS_CONFIG2_PERF_EVENT3: Event 3 select.
48:55	RW	XTS_CONFIG2_UNUSED: XTS config2 unused/reserved bits for future use.
56:59	RW	XTS_CONFIG2_ATSD_TIMEOUT: Time out select for ATSD.
60:63	RW	XTS_CONFIG2_ATR_TIMEOUT: Time out select for ATR (NMMU response time-out).

Register Name	XTS Debug0 Configuration Register
Mnemonic	NPU.XTS.REG.DEBUG0_CONFIG
Address	0000000005011346 (SCOM)
Description	XTS Debug0 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG0_CONFIG_POD0: Multiplexer control for byte 0 of trace-0.
5:9	RW	DEBUG0_CONFIG_POD1: Multiplexer control for byte 1 of trace-0.
10:14	RW	DEBUG0_CONFIG_POD2: Multiplexer control for byte 2 of trace-0.
15:19	RW	DEBUG0_CONFIG_POD3: Multiplexer control for byte 3 of trace-0.
20:24	RW	DEBUG0_CONFIG_POD4: Multiplexer control for byte 4 of trace-0.
25:29	RW	DEBUG0_CONFIG_POD5: Multiplexer control for byte 5 of trace-0.
30:34	RW	DEBUG0_CONFIG_POD6: Multiplexer control for byte 6 of trace-0.
35:39	RW	DEBUG0_CONFIG_POD7: Multiplexer control for byte 7 of trace-0.
40:44	RW	DEBUG0_CONFIG_POD8: Multiplexer control for byte 8 of trace-0.
45:49	RW	DEBUG0_CONFIG_POD9: Multiplexer control for byte 9 of trace-0.
50:54	RW	DEBUG0_CONFIG_POD10: Multiplexer control for byte 10 of trace-0.
55:62	RW	DEBUG0_CONFIG_Reserved1: Reserved.
63	RW	DEBUG0_CONFIG_ACT: Enable clock-gates for debug trace latches.

Register Name	XTS Debug1 Configuration Register
Mnemonic	NPU.XTS.REG.DEBUG1_CONFIG
Address	0000000005011347 (SCOM)
Description	XTS Debug1 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:4	RW	DEBUG1_CONFIG_POD0: Multiplexer control for byte 0 of trace-1.
5:9	RW	DEBUG1_CONFIG_POD1: Multiplexer control for byte 1 of trace-1.
10:14	RW	DEBUG1_CONFIG_POD2: Multiplexer control for byte 2 of trace-1.
15:19	RW	DEBUG1_CONFIG_POD3: Multiplexer control for byte 3 of trace-1.
20:24	RW	DEBUG1_CONFIG_POD4: Multiplexer control for byte 4 of trace-1.
25:29	RW	DEBUG1_CONFIG_POD5: Multiplexer control for byte 5 of trace-1.
30:34	RW	DEBUG1_CONFIG_POD6: Multiplexer control for byte 6 of trace-1.
35:39	RW	DEBUG1_CONFIG_POD7: Multiplexer control for byte 7 of trace-1.
40:44	RW	DEBUG1_CONFIG_POD8: Multiplexer control for byte 8 of trace-1.
45:49	RW	DEBUG1_CONFIG_POD9: Multiplexer control for byte 9 of trace-1.
50:54	RW	DEBUG1_CONFIG_POD10: Multiplexer control for byte 10 of trace-1.
55:62	RW	DEBUG1_CONFIG_Reserved1: Reserved.
63	RW	DEBUG1_CONFIG_ACT: Enable clock-gates for debug trace latches.

Register Name	NPU XTS PMULet Count Register
Mnemonic	NPU.XTS.REG.XTS_PMU_CNT
Address	0000000005011348 (SCOM)
Description	The NPU XTS PMULet Count Register contains the PMULet counters in XTS (4 x 16b)

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	XTS_PMU_CNT0: PMULet Counter 0.
16:31	ROX	XTS_PMU_CNT1: PMULet Counter 1.
32:47	ROX	XTS_PMU_CNT2: PMULet Counter 2.
48:63	ROX	XTS_PMU_CNT3: PMULet Counter 3.

Register Name	XTS ATRMiss Register
Mnemonic	NPU.XTS.REG.XTS_ATRMISS
Address	000000000501134A (SCOM)
Description	XTS ATRMiss Register

Bits	SCOM	Field Mnemonic: Description
0:14	RO	Constant = 0b000000000000000
15:51	RWX	XTS_ATRMISS_ADDR: Holds captured effective address.
52:53	RO	Constant = 0b00
54	RW	XTS_ATRMISS_FLAG_OTHER: Enable IRQ and capture for misses caused by other issues, that is,, prefetch page size mismatch.
55	RW	XTS_ATRMISS_FLAG_PREF: Enable IRQ and capture for misses caused by prefetch NMMU requests.
56	RW	XTS_ATRMISS_FLAG_DMD: Enable IRQ and capture for misses caused by demand NMMU requests.
57	RW	XTS_ATRMISS_FLAG_MAP: Enable IRQ and capture for misses caused by BDF/PASID map look-up.
58	RW	XTS_ATRMISS_FLAG_FENCE: Enable IRQ and capture for misses caused by fencing.
59	RW	XTS_ATRMISS_RETIRE: If set, launch IRQ after ATR response sent to GPU, otherwise launch IRQ immediately on miss.
60	RW	XTS_ATRMISS_IRQENA: If set, triggers interrupt on qualifying ATR miss (IRQ is independent from capture).
61	RWX	XTS_ATRMISS_SECOND: Set to one by second ATR miss capture.
62	RWX	XTS_ATRMISS_TRIGGERED: Capture only if this bit is clear, set to one by HW on first ATR miss capture.
63	RW	XTS_ATRMISS_ENA: Enable ATR attribute capture on miss.

Register Name	XTS ATRMiss Clear Register
Mnemonic	NPU.XTS.REG.XTS_ATRMISSCLR
Address	000000000501134B (SCOM)
Description	XTS ATRMissClear Register

Bits	SCOM	Field Mnemonic: Description
0:14	RO	Constant = 0b000000000000000
15:51	ROX	XTS_ATRMISS_ADDR: Holds captured effective address.
52:53	RO	Constant = 0b00
54	ROX	XTS_ATRMISS_FLAG_OTHER: Enable IRQ and capture for misses caused by other issues, that is,, prefetch page size mismatch.
55	ROX	XTS_ATRMISS_FLAG_PREF: Enable IRQ and capture for misses caused by prefetch NMMU requests.
56	ROX	XTS_ATRMISS_FLAG_DMD: Enable IRQ and capture for misses caused by demand NMMU requests.
57	ROX	XTS_ATRMISS_FLAG_MAP: Enable IRQ and capture for misses caused by BDF/PASID map look-up.
58	ROX	XTS_ATRMISS_FLAG_FENCE: Enable IRQ and capture for misses caused by fencing.
59	ROX	XTS_ATRMISS_RETIRE: If set, launch IRQ after ATR response sent to GPU, otherwise launch IRQ immediately on miss.

Bits	SCOM	Field Mnemonic: Description
60	ROX	XTS_ATRMISS_IRQENA: if set, triggers interrupt on qualifying ATR miss (IRQ is independent from capture).
61	ROX	XTS_ATRMISS_SECOND: set to one by second ATR miss capture.
62	ROX	XTS_ATRMISS_TRIGGERED: capture only if this bit is clear, set to one by HW on first ATR miss capture.
63	ROX	XTS_ATRMISS_ENA: Enable ATR attr capture on miss.

Register Name	**XTS ATRMiss 2 Register**
Mnemonic	NPU.XTS.REG.XTS_ATRMISS2
Address	000000000501134C (SCOM)
Description	XTS ATRMiss Register 2

Bits	SCOM	Field Mnemonic: Description
0:26	RO	Constant = 0b00000000000000000000000000
27	RWX	XTS_ATRMISS_GPA: Holds captured GPU flag.
28:43	RWX	XTS_ATRMISS_BDF: Holds captured BDF.
44:63	RWX	XTS_ATRMISS_PASID: Holds capture PASID.

Register Name	**XTS MMIO ATSD0 LPARID Register**
Mnemonic	NPU.XTS.ATSD.XTS_ATSD_HYP0
Address	0000000005011360 (SCOM)
Description	XTS MMIO ATSD0 LPARID register

Bits	SCOM	Field Mnemonic: Description
0:51	RO	Constant = 0b000000000000000000000000000000000000000000000000000000
52:63	RW	XTS_ATSD_HYP0_LPARID: LPARID value for MMIO ATSD control entry 0.

Register Name	**XTS MMIO ATSD1 LPARID Register**
Mnemonic	NPU.XTS.ATSD.XTS_ATSD_HYP1
Address	0000000005011361 (SCOM)
Description	XTS MMIO ATSD1 LPARID register

Bits	SCOM	Field Mnemonic: Description
0:51	RO	Constant = 0b000000000000000000000000000000000000000000000000000000
52:63	RW	XTS_ATSD_HYP1_LPARID: LPARID value for MMIO ATSD control entry 1.

Register Name	**XTS MMIO ATSD2 LPARID Register**
Mnemonic	NPU.XTS.ATSD.XTS_ATSD_HYP2
Address	0000000005011362 (SCOM)
Description	XTS MMIO ATSD2 LPARID register

Bits	SCOM	Field Mnemonic: Description
0:51	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
52:63	RW	XTS_ATSD_HYP2_LPARID: LPARID value for MMIO ATSD control entry 2.

Register Name	XTS MMIO ATSD3 LPARID Register
Mnemonic	NPU.XTS.ATSD.XTS_ATSD_HYP3
Address	0000000005011363 (SCOM)
Description	XTS MMIO ATSD3 LPARID register

Bits	SCOM	Field Mnemonic: Description
0:51	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
52:63	RW	XTS_ATSD_HYP3_LPARID: LPARID value for MMIO ATSD control entry 3.

Register Name	XTS MMIO ATSD4 LPARID Register
Mnemonic	NPU.XTS.ATSD.XTS_ATSD_HYP4
Address	0000000005011364 (SCOM)
Description	XTS MMIO ATSD4 LPARID register

Bits	SCOM	Field Mnemonic: Description
0:51	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
52:63	RW	XTS_ATSD_HYP4_LPARID: LPARID value for MMIO ATSD control entry 4.

Register Name	XTS MMIO ATSD5 LPARID Register
Mnemonic	NPU.XTS.ATSD.XTS_ATSD_HYP5
Address	0000000005011365 (SCOM)
Description	XTS MMIO ATSD5 LPARID register

Bits	SCOM	Field Mnemonic: Description
0:51	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
52:63	RW	XTS_ATSD_HYP5_LPARID: LPARID value for MMIO ATSD control entry 5.

Register Name	XTS MMIO ATSD6 LPARID Register
Mnemonic	NPU.XTS.ATSD.XTS_ATSD_HYP6
Address	0000000005011366 (SCOM)
Description	XTS MMIO ATSD6 LPARID register

Bits	SCOM	Field Mnemonic: Description
0:51	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
52:63	RW	XTS_ATSD_HYP6_LPARID: LPARID value for MMIO ATSD control entry 6.

Register Name	XTS MMIO ATSD7 LPARID Register
Mnemonic	NPU.XTS.ATSD.XTS_ATSD_HYP7
Address	0000000005011367 (SCOM)
Description	XTS MMIO ATSD7 LPARID register

Bits	SCOM	Field Mnemonic: Description
0:51	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
52:63	RW	XTS_ATSD_HYP7_LPARID: LPARID value for MMIO ATSD control entry 7.

Register Name	Debug Configuration Register
Mnemonic	NPU.MISC.REGS.DEBUG_CONFIG
Address	0000000005011380 (SCOM)
Description	Debug Configuration Register Selects which of 3 internal / 1 miscellaneous macro debug buses to route the to the 2 external debug buses. The debug bus is 11 bytes wide, with each byte selected independently using 2 bit control. 0b00 = NPU internal debug bus 0 0b01 = NPU internal debug bus 1 0b10 = NPU internal debug bus 2 0b11 = MISC macro debug bus

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MISC_DEBUG_CONFIG_BUS0BYTE0: 2b select for external bus 0, byte 0.
2:3	RW	MISC_DEBUG_CONFIG_BUS0BYTE1: 2b select for external bus 0, byte 1.
4:5	RW	MISC_DEBUG_CONFIG_BUS0BYTE2: 2b select for external bus 0, byte 2.
6:7	RW	MISC_DEBUG_CONFIG_BUS0BYTE3: 2b select for external bus 0, byte 3.
8:9	RW	MISC_DEBUG_CONFIG_BUS0BYTE4: 2b select for external bus 0, byte 4.
10:11	RW	MISC_DEBUG_CONFIG_BUS0BYTE5: 2b select for external bus 0, byte 5.
12:13	RW	MISC_DEBUG_CONFIG_BUS0BYTE6: 2b select for external bus 0, byte 6.
14:15	RW	MISC_DEBUG_CONFIG_BUS0BYTE7: 2b select for external bus 0, byte 7.
16:17	RW	MISC_DEBUG_CONFIG_BUS0BYTE8: 2b select for external bus 0, byte 8.
18:19	RW	MISC_DEBUG_CONFIG_BUS0BYTE9: 2b select for external bus 0, byte 9.
20:21	RW	MISC_DEBUG_CONFIG_BUS0BYTE10: 2b select for external bus 0, byte 10.
22:23	RW	MISC_DEBUG_CONFIG_BUS1BYTE0: 2b select for external bus 1, byte 0.
24:25	RW	MISC_DEBUG_CONFIG_BUS1BYTE1: 2b select for external bus 1, byte 1.
26:27	RW	MISC_DEBUG_CONFIG_BUS1BYTE2: 2b select for external bus 1, byte 2.
28:29	RW	MISC_DEBUG_CONFIG_BUS1BYTE3: 2b select for external bus 1, byte 3.
30:31	RW	MISC_DEBUG_CONFIG_BUS1BYTE4: 2b select for external bus 1, byte 4.
32:33	RW	MISC_DEBUG_CONFIG_BUS1BYTE5: 2b select for external bus 1, byte 5.
34:35	RW	MISC_DEBUG_CONFIG_BUS1BYTE6: 2b select for external bus 1, byte 6.
36:37	RW	MISC_DEBUG_CONFIG_BUS1BYTE7: 2b select for external bus 1, byte 7.
38:39	RW	MISC_DEBUG_CONFIG_BUS1BYTE8: 2b select for external bus 1, byte 8.
40:41	RW	MISC_DEBUG_CONFIG_BUS1BYTE9: 2b select for external bus 1, byte 9.

Bits	SCOM	Field Mnemonic: Description
42:43	RW	MISC_DEBUG_CONFIG_BUS1BYTE10: 2b select for external bus 1, byte 10.
44:62	RW	Reserved: Reserved.
63	RW	ACT_DEBUG: Clock activate MISC macro debug logic.

Register Name	Relaxed Ordering Configuration Register
Mnemonic	NPU.MISC.REGS.RLX_CONFIG
Address	0000000005011381 (SCOM)
Description	Relaxed Ordering brick to cluster mapping and sync control

Bits	SCOM	Field Mnemonic: Description
0:2	RW	CONFIG_BRK0_CLUSTER: Cluster # (0-5) that brick 0 belongs to. Do not change unless the brick is quiesced.
3:5	RW	CONFIG_BRK1_CLUSTER: Cluster # (0-5) that brick 1 belongs to. Do not change unless the brick is quiesced.
6:8	RW	CONFIG_BRK2_CLUSTER: Cluster # (0-5) that brick 2 belongs to. Do not change unless the brick is quiesced.
9:11	RW	CONFIG_BRK3_CLUSTER: Cluster # (0-5) that brick 3 belongs to. Do not change unless the brick is quiesced.
12:14	RW	CONFIG_BRK4_CLUSTER: Cluster # (0-5) that brick 4 belongs to. Do not change unless the brick is quiesced.
15:17	RW	CONFIG_BRK5_CLUSTER: Cluster # (0-5) that brick 5 belongs to. Do not change unless the brick is quiesced.
18:19	RW	RLX_Reserved1: Reserved.
20:25	RW	CONFIG_SYNC_BRK: Mask of bricks to sync.
26:31	ROX	IDIAL_RLX_ISSYNC: Mask of bricks which are synced.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	LCO Configuration Register
Mnemonic	NPU.MISC.REGS.LCO_CONFIG
Address	0000000005011382 (SCOM)
Description	Lateral-castout target selection configuration

Bits	SCOM	Field Mnemonic: Description
0:11	RW	CONFIG_LCO_V_TARG: LCO valid-targets vector.
12:15	RW	CONFIG_LCO_E_TARG_MIN: LCO minimum number of eligible targets.
16:19	RW	CONFIG_LCO_RAND_EVENT: LCO Random event rate.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Optical I/O Configuration for Bricks 0 Register
Mnemonic	NPU.MISC.REGS.OPTICAL_IO_CONFIG
Address	0000000005011383 (SCOM)
Description	Optical I/O used for A-Link or NVLink, bricks 0 - 2

Bits	SCOM	Field Mnemonic: Description
0:2	RW	NDLMUX_BRK0TO2: 0 = A-Link 1 = NVLink for Bricks 0-2.
3:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000

Register Name	Miscellaneous Hold Register
Mnemonic	NPU.MISC.REGS.MISC_HOLD
Address	0000000005011384 (SCOM)
Description	c_err_rpt hold latches read-with-clear register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	IDIAL_NDL0_STALL: Interrupt Request NDL Brick0 Stall.
1	RWX_WCLRREG	IDIAL_NDL0_NOSTALL: Interrupt Request NDL Brick0 No-Stall.
2	RWX_WCLRREG	IDIAL_NDL1_STALL: Interrupt Request NDL Brick1 Stall.
3	RWX_WCLRREG	IDIAL_NDL1_NOSTALL: Interrupt Request NDL Brick1 No-Stall.
4	RWX_WCLRREG	IDIAL_NDL2_STALL: Interrupt Request NDL Brick2 Stall.
5	RWX_WCLRREG	IDIAL_NDL2_NOSTALL: Interrupt Request NDL Brick2 No-Stall.
6	RWX_WCLRREG	IDIAL_NDL3_STALL: Interrupt Request NDL Brick3 Stall.
7	RWX_WCLRREG	IDIAL_NDL3_NOSTALL: Interrupt Request NDL Brick3 No-Stall.
8	RWX_WCLRREG	IDIAL_NDL4_STALL: Interrupt Request NDL Brick4 Stall.
9	RWX_WCLRREG	IDIAL_NDL4_NOSTALL: Interrupt Request NDL Brick4 No-Stall.
10	RWX_WCLRREG	IDIAL_NDL5_STALL: Interrupt Request NDL Brick5 Stall.
11	RWX_WCLRREG	IDIAL_NDL5_NOSTALL: Interrupt Request NDL Brick5 No-Stall.
12	RWX_WCLRREG	IDIAL_MISC_RING_ERRP: NPU Register Ring error (ie noack).
13	RWX_WCLRREG	IDIAL_MISC_IBAR_ERRP: Parity error from interrupt base real address register.

Bits	SCOM	Field Mnemonic: Description
14	RWX_WCLRREG	IDIAL_MISC_SCOMDAA_ERRP: Parity error on Indirect SCOM Address register.
15	RWX_WCLRREG	IDIAL_MISC_CNTL_ERRP: Parity error on MISC Control register.
16	RWX_WCLRREG	IDIAL_MM_LOCAL_XSTOP: NMMU signaled Local Checkstop.
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	Miscellaneous Mask Register
Mnemonic	NPU.MISC.REGS.MISC_MASK
Address	0000000005011385 (SCOM)
Description	c_err_rpt mask latches read-only register

Bits	SCOM	Field Mnemonic: Description
0:16	ROX	IDIAL_MISC_MASK: c_err_rpt mask latches read-only register.
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	Miscellaneous Configuration Register
Mnemonic	NPU.MISC.REGS.MISC_CONFIG
Address	0000000005011386 (SCOM)
Description	Configures MISC

Bits	SCOM	Field Mnemonic: Description
0:4	RW	CONFIG_SYNC_WAIT: Number of clock cycles from sync request to sync valid. (masks round-trip staging latency MISC/ATS/CTL). Must be > = ATS config_sync_wait + 8.
5	RW	PERF_CONFIG_ENABLE: 0b1 Enables performance monitor events.
6	RW	PERF_CONFIG_PE_MASK: 0b1 Enables the selection of performance monitor events by PE ID.
7:10	RW	PERF_CONFIG_PE_MATCH: PE ID to select for performance monitor events (when enabled).
11	RW	IPI_PS: Inter-processor interrupt page size 0b0 = 4 kB. 0b1 = 64 kB.
12	RW	IPI_OS: Inter-processor interrupt operating system 0b0 = AIX. 0b1 = Linux.
13:63	RW	CONFIG_MISC_RSVD: Reserved.

Register Name	Inhibit Configuration Register
Mnemonic	NPU.MISC.REGS.INHIBIT_CONFIG
Address	0000000005011387 (SCOM)
Description	Configures Inhibits for MISC

Bits	SCOM	Field Mnemonic: Description
0:3	RW	CONFIG_INHIBIT_LFREQ: Base LFSR frequency 0: 0..11 = 1/2^(n+1). 12 = 1/2^14. 13 = 1/2^16. 14 = 1/2^18. 15 = 1/2^20.
4	RW	CONFIG_INHIBIT_IFREQ: 0/1 = don't invert/invert base frequency.
5:7	RW	CONFIG_INHIBIT_DEST: Destination of the inhibit. 0 = No destination. 1 = Restore on lco sent. 2 = Restore on lco cr_long. 3 = Restore on lco sent/cr_long. 4 = Gen-id inc head. 5 = Gen-id inc tail. 6 = Gen-id inc head/tail. 7 = All of the above.
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	NPU Freeze 0 Configuration Register
Mnemonic	NPU.MISC.REGS.FREEZE_0_CONFIG
Address	0000000005011388 (SCOM)
Description	on-error Enable for FIR Register 0 NPU Freeze-on-error Enable 0. 0b1 = enable

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG_FREEZE_0: Enable for FIR Register 0.

Register Name	NPU Freeze 1 Configuration Register
Mnemonic	NPU.MISC.REGS.FREEZE_1_CONFIG
Address	0000000005011389 (SCOM)
Description	On-error enable for FIR Register 1 NPU freeze-on-error enable 0. 0b1 = enable.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG_FREEZE_1: Enable for FIR Register 1.

Register Name	NPU Fence 0 Configuration Register
Mnemonic	NPU.MISC.REGS.FENCE_0_CONFIG
Address	000000000501138A (SCOM)
Description	On-error Enable for FIR Register 0 NPU Fence-on-error Enable. 0b1 = enable.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG_FENCE_0: Enable for FIR Register 0.

Register Name	NPU Fence 1 Configuration Register
Mnemonic	NPU.MISC.REGS.FENCE_1_CONFIG
Address	000000000501138B (SCOM)
Description	On-error Enable for FIR Register 1 NPU Fence-on-error Enable. 0b1 = enable.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG_FENCE_1: Enable for FIR Register 1.

Register Name	NPU Interrupt 0 Configuration Register
Mnemonic	NPU.MISC.REGS.INT_0_CONFIG
Address	000000000501138C (SCOM)
Description	On-error Enable for FIR Register 0 NPU Interrupt-on-error Enable. 0b1 = Enable.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG_INT_0: Enable for FIR Register 0.

Register Name	NPU Interrupt 1 Configuration Register
Mnemonic	NPU.MISC.REGS.INT_1_CONFIG
Address	000000000501138D (SCOM)
Description	on-error Enable for FIR Register 1 NPU Interrupt-on-error Enable. 0b1 = Enable.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CONFIG_INT_1: Enable for FIR Register 1.

Register Name	NPU Indirect SCOM Address Register
Mnemonic	NPU.MISC.REGS.DA_ADDR
Address	000000000501138E (SCOM)
Description	NPU Indirect SCOM Address register For usage, see NPU Indirect SCOM Data register

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MISC_DA_ADDR: Indirect SCOM Address.
24:25	RW	MISC_DA_LEN: Indirect SCOM Length. 0b00 = 1B 0b01 = 2B 0b10 = 4B 0b11 = 8B.
26:63	RW	MISC_DA_RSVD: Reserved.

Register Name	NPU Indirect SCOM Data Register
Mnemonic	NPU.MISC.REGS.DA_DATA
Address	000000000501138F (SCOM)
Description	NPU Indirect SCOM data register. A SCOM read/write of this register performs an indirect SCOM NPU ring read/write of the register at the address stored in the NPU indirect SCOM address register.

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	NPU Version Register
Mnemonic	NPU.MISC.REGS.NPU_VERSION
Address	0000000005011390 (SCOM)
Description	NPU Version Register Scan-only latches with default initialization value x000000A200000001

Bits	SCOM	Field Mnemonic: Description
0:23	RO	NPU_VERSION_RSVD0: Reserved.
24:31	RO	NPU_VERSION_MAJOR: Major Revision ID. Indicates that the NPU implements version 2 of the NVLink specification.
32:47	RO	NPU_VERSION_RSVD1: Reserved.
48:63	RO	NPU_VERSION_MINOR: EC version of the NPU.

Register Name	NPU Error Scope Control Configuration Register
Mnemonic	NPU.MISC.REGS.ERR_SCOPE_CTL_CONFIG
Address	0000000005011391 (SCOM)
Description	NPU Scope for CQ CTL/SM Errors. See FIR register for error details.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CONFIG_ERR_SCOPE_CTL: 0b0 = brick(s) scope. 0b1 = NPU scope.
16:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	NPU Ring Address Error Register
Mnemonic	NPU.MISC.REGS.ERR_INFO_NPU_RING_ADDR
Address	0000000005011392 (SCOM)
Description	NPU Ring ACK error information from the MISC master (SCOM direct or indirect)

Bits	SCOM	Field Mnemonic: Description
0:23	RWX	MISC_NPU_RING_ERR_ADDR: NPU ring address.
24:25	RWX	MISC_NPU_RING_ERR_LENR: NPU ring length.
26	RWX	MISC_NPU_RING_ERR_RNW: NPU ring read/not-write.

Bits	SCOM	Field Mnemonic: Description
27	RWX	MISC_NPU_RING_ERR_DA_OP: NPU ring indirect SCOM.
28:63	RO	Constant = 0b00000000000000000000000000000000000000000

Register Name	NPU Interrupt Base Address Register
Mnemonic	NPU.MISC.REGS.INT_BAR
Address	0000000005011393 (SCOM)
Description	NPU Interrupt Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:38	RW	CONFIG_INT_BAR: Powerbus address(13 to 51). Bits used depend on the configuration. 4 kB AIX (13 to 45). 4 kB Linux (13 to 46). 64 kB AIX (13 to 41). 64 kB Linux (13 to 42). (47 to 51) never used.
39:63	RO	Constant = 0b00000000000000000000000000

Register Name	NPU Error Brick Group Configuration Register
Mnemonic	NPU.MISC.REGS.ERROR_BRICK_GROUP_CONFIG
Address	0000000005011394 (SCOM)
Description	NPU Error Brick Group for Freeze and Fence

Bits	SCOM	Field Mnemonic: Description
0:5	RW	CONFIG_ERR_GROUP_BRK0: Error brick group for brick 0.
6:11	RW	CONFIG_ERR_GROUP_BRK1: Error brick group for brick 1.
12:17	RW	CONFIG_ERR_GROUP_BRK2: Error brick group for brick 2.
18:23	RW	CONFIG_ERR_GROUP_BRK3: Error brick group for brick 3.
24:29	RW	CONFIG_ERR_GROUP_BRK4: Error brick group for brick 4.
30:35	RW	CONFIG_ERR_GROUP_BRK5: Error brick group for brick 5.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	NPU Freeze State Register
Mnemonic	NPU.MISC.REGS.FREEZE_STATE
Address	0000000005011395 (SCOM)
Description	NPU freeze state per BDF-to-PE map. Read returns freeze state. Write 0b1 to set freeze. Write 0b0 to clear freeze. May also be set by hardware error.

Bits	SCOM	Field Mnemonic: Description
0	RWX	FREEZE_BDF2PE_00: brick0, entry 0.

Bits	SCOM	Field Mnemonic: Description
1	RWX	FREEZE_BDF2PE_01: brick0, entry 1.
2	RWX	FREEZE_BDF2PE_02: brick0, entry 2.
3	RWX	FREEZE_BDF2PE_10: brick1, entry 0.
4	RWX	FREEZE_BDF2PE_11: brick1, entry 1.
5	RWX	FREEZE_BDF2PE_12: brick1, entry 2.
6	RWX	FREEZE_BDF2PE_20: brick2, entry 0.
7	RWX	FREEZE_BDF2PE_21: brick2, entry 1.
8	RWX	FREEZE_BDF2PE_22: brick2, entry 2.
9	RWX	FREEZE_BDF2PE_30: brick3, entry 0.
10	RWX	FREEZE_BDF2PE_31: brick3, entry 1.
11	RWX	FREEZE_BDF2PE_32: brick3, entry 2.
12	RWX	FREEZE_BDF2PE_40: brick4, entry 0.
13	RWX	FREEZE_BDF2PE_41: brick4, entry 1.
14	RWX	FREEZE_BDF2PE_42: brick4, entry 2.
15	RWX	FREEZE_BDF2PE_50: brick5, entry 0.
16	RWX	FREEZE_BDF2PE_51: brick5, entry 1.
17	RWX	FREEZE_BDF2PE_52: brick5, entry 2.
18:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	**NPU Fence State Register**
Mnemonic	NPU.MISC.REGS.FENCE_STATE
Address	0000000005011396 (SCOM)
Description	NPU fence state per brick. Read returns fence state. Write 1 to set fence. Write 0 to clear fence. May also be set by hardware error.

Bits	SCOM	Field Mnemonic: Description
0	RWX	FENCE_BRK0: brick 0.
1	RWX	FENCE_BRK1: brick 1.
2	RWX	FENCE_BRK2: brick 2.
3	RWX	FENCE_BRK3: brick 3.
4	RWX	FENCE_BRK4: brick 4.
5	RWX	FENCE_BRK5: brick 5.
6:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	**NPU Interrupt Request Register**
Mnemonic	NPU.MISC.REGS.INT_REQ
Address	0000000005011397 (SCOM)
Description	NPU interrupt request per source. Read returns interrupt request. Write 1 to set interrupt request. Write 0 to all bits to clear all interrupt requests.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WOR	INTERRUPT_00: NDL stall, brick 0.
1	RWX_WOR	INTERRUPT_01: NDL nostall, brick 0.
2	RWX_WOR	INTERRUPT_02: NDL stall, brick 1.
3	RWX_WOR	INTERRUPT_03: NDL nostall, brick 1.
4	RWX_WOR	INTERRUPT_04: NDL stall, brick 2.
5	RWX_WOR	INTERRUPT_05: NDL nostall, brick 2.
6	RWX_WOR	INTERRUPT_06: NDL stall, brick 3.
7	RWX_WOR	INTERRUPT_07: NDL nostall, brick 3.
8	RWX_WOR	INTERRUPT_08: NDL stall, brick 4.
9	RWX_WOR	INTERRUPT_09: NDL nostall, brick 4.
10	RWX_WOR	INTERRUPT_10: NDL stall, brick 5.
11	RWX_WOR	INTERRUPT_11: NDL nostall, brick 5.
12	RWX_WOR	INTERRUPT_12: NTL brick 0.
13	RWX_WOR	INTERRUPT_13: NTL brick 1.
14	RWX_WOR	INTERRUPT_14: NTL brick 2.
15	RWX_WOR	INTERRUPT_15: NTL brick 3.
16	RWX_WOR	INTERRUPT_16: NTL brick 4.
17	RWX_WOR	INTERRUPT_17: NTL brick 5.
18	RWX_WOR	INTERRUPT_18: TCE translation.
19	RWX_WOR	INTERRUPT_19: ATS translation.
20	RWX_WOR	INTERRUPT_20: CTL or DAT.
21	RWX_WOR	INTERRUPT_21: MISC.
22	RWX_WOR	INTERRUPT_22: NMMU local checkstop.
23:63	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	**Brick 0 BDF2PE Configuration 0 Register**
Mnemonic	NPU.MISC.REGS.BDF2PE_00_CONFIG
Address	00000000050113A0 (SCOM)
Description	to-PE map 0 Configured BDF-to-PE mapping #0 for brick 0 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_00_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_00_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_00_PE: PE (Partitionable Endpoint) associated with this BDF.

Bits	SCOM	Field Mnemonic: Description
8:23	RW	CONFIG_BDF2PE_00_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 0 BDF2PE Configuration 1 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_01_CONFIG
Address	00000000050113A1 (SCOM)
Description	to-PE map 1 Configured BDF-to-PE mapping #1 for brick 0 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_01_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_01_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_01_PE: PE (Partitionable endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_01_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 0 BDF2PE Configuration 2 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_02_CONFIG
Address	00000000050113A2 (SCOM)
Description	to-PE map 2 Configured BDF-to-PE mapping #2 for brick 0 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_02_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_02_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_02_PE: PE (Partitionable endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_02_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 1 BDF2PE Configuration 0 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_10_CONFIG
Address	00000000050113A3 (SCOM)
Description	to-PE map 0 Configured BDF-to-PE mapping #0 for brick 1 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_10_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_10_Reserved: Reserved.

Bits	SCOM	Field Mnemonic: Description
4:7	RW	CONFIG_BDF2PE_10_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_10_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 1 BDF2PE Configuration 1 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_11_CONFIG
Address	00000000050113A4 (SCOM)
Description	to-PE map 1 Configured BDF-to-PE mapping #1 for brick 1 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_11_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_11_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_11_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_11_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 1 BDF2PE Configuration 2 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_12_CONFIG
Address	00000000050113A5 (SCOM)
Description	to-PE map 2 Configured BDF-to-PE mapping #2 for brick 1. Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_12_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_12_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_12_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_12_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 2 BDF2PE Configuration 0 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_20_CONFIG
Address	00000000050113A6 (SCOM)
Description	to-PE map 0 Configured BDF-to-PE mapping #0 for brick 2. Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_20_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.

Bits	SCOM	Field Mnemonic: Description
1:3	RW	CONFIG_BDF2PE_20_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_20_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_20_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 2 BDF2PE Configuration 1 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_21_CONFIG
Address	00000000050113A7 (SCOM)
Description	to-PE map 1 Configured BDF-to-PE mapping #1 for brick 2 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_21_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_21_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_21_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_21_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 2 BDF2PE Configuration 2 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_22_CONFIG
Address	00000000050113A8 (SCOM)
Description	to-PE map 2 Configured BDF-to-PE mapping #2 for brick 2 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_22_ENABLE: 0/1 = This BDF-to-PE mapping is disabled/enabled.
1:3	RW	CONFIG_BDF2PE_22_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_22_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_22_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 3 BDF2PE Configuration 0 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_30_CONFIG
Address	00000000050113A9 (SCOM)
Description	to-PE map 0 Configured BDF-to-PE mapping #0 for brick 3 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_30_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_30_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_30_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_30_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 3 BDF2PE Configuration 1 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_31_CONFIG
Address	00000000050113AA (SCOM)
Description	to-PE map 1 Configured BDF-to-PE mapping #1 for brick 3 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_31_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_31_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_31_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_31_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 3 BDF2PE Configuration 2 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_32_CONFIG
Address	00000000050113AB (SCOM)
Description	to-PE map 2 Configured BDF-to-PE mapping #2 for brick 3 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_32_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_32_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_32_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_32_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 4 BDF2PE Configuration 0 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_40_CONFIG
Address	00000000050113AC (SCOM)
Description	to-PE map 0 Configured BDF-to-PE mapping #0 for brick 4 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_40_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_40_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_40_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_40_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 4 BDF2PE Configuration 1 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_41_CONFIG
Address	00000000050113AD (SCOM)
Description	to-PE map 1 Configured BDF-to-PE mapping #1 for brick 4 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_41_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_41_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_41_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_41_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Brick 4 BDF2PE Configuration 2 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_42_CONFIG
Address	00000000050113AE (SCOM)
Description	to-PE map 2 Configured BDF-to-PE mapping #2 for brick 4 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_42_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_42_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_42_PE: PE (Partitionable Endpoint) associated with this BDF.

Bits	SCOM	Field Mnemonic: Description
8:23	RW	CONFIG_BDF2PE_42_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 5 BDF2PE Configuration 0 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_50_CONFIG
Address	00000000050113AF (SCOM)
Description	to-PE map 0 Configured BDF-to-PE mapping #0 for brick 5 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_50_ENABLE 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_50_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_50_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_50_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 5 BDF2PE Configuration 1 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_51_CONFIG
Address	00000000050113B0 (SCOM)
Description	to-PE map 1 Configured BDF-to-PE mapping #1 for brick 5 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_51_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_51_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_51_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_51_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Brick 5 BDF2PE Configuration 2 Register
Mnemonic	NPU.MISC.REGS.BDF2PE_52_CONFIG
Address	00000000050113B1 (SCOM)
Description	to-PE map 2 Configured BDF-to-PE mapping #2 for brick 5 Note: Across all six bricks of an NPU, each BDF may map to at most 1 PE

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_BDF2PE_52_ENABLE: 0 = This BDF-to-PE mapping is disabled. 1 = This BDF-to-PE mapping is enabled.
1:3	RW	CONFIG_BDF2PE_52_Reserved: Reserved.
4:7	RW	CONFIG_BDF2PE_52_PE: PE (Partitionable Endpoint) associated with this BDF.
8:23	RW	CONFIG_BDF2PE_52_BDF: BDF (Bus-Device-Function) mapped to this PE.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 0 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE0
Address	00000000050113C0 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE0: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 1 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE1
Address	00000000050113C1 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE1: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 2 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE2
Address	00000000050113C2 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE2: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 3 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE3
Address	00000000050113C3 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE3: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 4 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE4
Address	00000000050113C4 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE4: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 5 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE5
Address	00000000050113C5 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE5: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 6 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE6
Address	00000000050113C6 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE6: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 7 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE7
Address	00000000050113C7 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE7: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 8 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE8
Address	00000000050113C8 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE8: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 9 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE9
Address	00000000050113C9 (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE9: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 10 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE10
Address	00000000050113CA (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE10: 0 = This PE is running. 1 = This PE is frozen.

Bits	SCOM	Field Mnemonic: Description
1:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 11 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE11
Address	00000000050113CB (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE11: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 12 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE12
Address	00000000050113CC (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE12: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 13 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE13
Address	00000000050113CD (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE13: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 14 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE14
Address	00000000050113CE (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE14: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Data for PE 15 Register
Mnemonic	NPU.MISC.REGS.PESTB_DATA_PE15
Address	00000000050113CF (SCOM)
Description	Records which PEs are running/frozen

Bits	SCOM	Field Mnemonic: Description
0	RWX	DMA_STOPPED_STATE_PE15: 0 = This PE is running. 1 = This PE is frozen.
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PESTB Address for PE 0 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE0
Address	00000000050113D0 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE0: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 1 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE1
Address	00000000050113D1 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE1: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 2 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE2
Address	00000000050113D2 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE2: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 3 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE3
Address	00000000050113D3 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE3: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 4 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE4
Address	00000000050113D4 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE4: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 5 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE5
Address	00000000050113D5 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE5: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 6 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE6
Address	00000000050113D6 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE6: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 7 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE7
Address	00000000050113D7 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE7: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 8 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE8
Address	00000000050113D8 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE8: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 9 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE9
Address	00000000050113D9 (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE9: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 10 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE10
Address	00000000050113DA (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE10: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 11 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE11
Address	00000000050113DB (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE11: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 12 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE12
Address	00000000050113DC (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE12: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 13 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE13
Address	00000000050113DD (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE13: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 14 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE14
Address	00000000050113DE (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE14: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PESTB Address for PE 15 Register
Mnemonic	NPU.MISC.REGS.PESTB_ADDR_PE15
Address	00000000050113DF (SCOM)
Description	Records which NVLink Address caused PE freeze state. Only valid for TCE address translation TVT error, TVT address truncation error and page access error (ATS macro error bits 0,1,2,3,4), otherwise zero.

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	DMA_STOPPED_STATE_ADDR_PE15: PESTB(0 to 36) = Coherent Bus(15 to 51) = NVLink Address(48 to 12).
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	System Interrupt Log for PE 0 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE0
Address	00000000050113E0 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE0_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE0_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE0_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE0_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE0_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 1 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE1
Address	00000000050113E1 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE1_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE1_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE1_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE1_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE1_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 2 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE2
Address	00000000050113E2 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE2_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE2_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE2_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.

Bits	SCOM	Field Mnemonic: Description
36:55	RWX	INT_LOG_ERR_PE2_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE2_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 3 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE3
Address	00000000050113E3 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE3_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE3_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE3_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE3_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE3_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 4 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE4
Address	00000000050113E4 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE4_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE4_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE4_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE4_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE4_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 5 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE5
Address	00000000050113E5 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE5_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE5_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE5_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE5_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE5_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 6 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE6
Address	00000000050113E6 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE6_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE6_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE6_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE6_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE6_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 7 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE7
Address	00000000050113E7 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE7_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE7_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE7_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE7_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE7_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 8 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE8
Address	00000000050113E8 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE8_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE8_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE8_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE8_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE8_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 9 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE9
Address	00000000050113E9 (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE9_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE9_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE9_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE9_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE9_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 10 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE10
Address	00000000050113EA (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE10_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE10_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE10_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.

Bits	SCOM	Field Mnemonic: Description
36:55	RWX	INT_LOG_ERR_PE10_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE10_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 11 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE11
Address	00000000050113EB (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE11_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE11_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE11_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE11_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE11_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 12 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE12
Address	00000000050113EC (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE12_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE12_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE12_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE12_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE12_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 13 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE13
Address	00000000050113ED (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE13_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE13_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE13_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE13_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE13_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 14 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE14
Address	00000000050113EE (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE14_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE14_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE14_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE14_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE14_RSVD0: Reserved.

Register Name	System Interrupt Log for PE 15 Register
Mnemonic	NPU.MISC.REGS.INT_LOG_PE15
Address	00000000050113EF (SCOM)
Description	Records which error caused a System Interrupt for each PE

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_LOG_ERR_PE15_VLD: Contents valid (freeze on 1st capture).
1:23	RWX	INT_LOG_ERR_PE15_LVL: Interrupt requester (see Interrupt Level).
24:35	RWX	INT_LOG_ERR_PE15_CQ: Interrupt requester, additional detail. CQ events: CTL0 brk0/1, CTL1 brk2/3, CTL2 brk4/5, DAT0 brk0/1, DAT1 brk2/3, DAT2 brk4/5.
36:55	RWX	INT_LOG_ERR_PE15_DETAIL: Error detail for requester (see FIR 0/1 register). If >1 simultaneous interrupt requester to same PE, capture priority is Interrupt Level 0 (highest) to Level 22. If redundant interrupt request to different PE, capture details for new PE. (for example, ATS interrupt to PE A in progress, then ATS interrupt to PE B).
56:63	RWX	INT_LOG_ERR_PE15_RSVD0: Reserved.

Register Name	NPU FIR 0 Register
Mnemonic	NPU.MISC.FIR_REG_0
Address	0000000005011400 (SCOM) 0000000005011401 (SCOM1) 0000000005011402 (SCOM2)
Description	Local FIR register for the NPU (1 of 2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	NTL_ARRAY_CE: NTL array CE.
1	RWX	WOX_AND	WOX_OR	NTL_ARRAY_HDR_UE: NTL header array UE.
2	RWX	WOX_AND	WOX_OR	NTL_ARRAY_DATA_UE: NTL data array UE.
3	RWX	WOX_AND	WOX_OR	NTL_NVL_FLIT_PERR: NTL NVLInk Control/Header/AE Parity error.
4	RWX	WOX_AND	WOX_OR	NTL_NVL_DATA_PERR: NTL NVLink Data Parity error.
5	RWX	WOX_AND	WOX_OR	NTL_NVL_PKT_MALFOR: NTL NVLink Malformed Packet (illegal command encode, etc.).
6	RWX	WOX_AND	WOX_OR	NTL_NVL_PKT_UNSUPPORTED: NTL NVLink Unsupported Packet (receiving DGD, receiving Atomic with unsupported DatLen, etc).
7	RWX	WOX_AND	WOX_OR	NTL_NVL_CONFIG_ERR: NTL NVLink Config errors (Credits received > max configured).
8	RWX	WOX_AND	WOX_OR	NTL_NVL_CRC_ERR: NTL NVLink CRC errors or LMD = Stomp.
9	RWX	WOX_AND	WOX_OR	NTL_PRI_ERR: NTL PRI errors (errors returned by NDL Wrapper on PRI interface).
10	RWX	WOX_AND	WOX_OR	NTL_LOGIC_ERR: NTL logic error (overflow, underflow, etc).
11	RWX	WOX_AND	WOX_OR	NTL_LMD_POISON: NTL LMD = Data Poison.
12	RWX	WOX_AND	WOX_OR	NTL_ARRAY_DATA_SUE: NTL data array SUE.
13	RWX	WOX_AND	WOX_OR	CTL_ARRAY_CE: CQ CTL/SM ASBE Array single-bit correctable error.
14	RWX	WOX_AND	WOX_OR	CTL_PBUS_RECOV_ERR: CQ CTL/SM PBR processor bus recoverable (ex: abort_trm CResp).
15	RWX	WOX_AND	WOX_OR	CTL_REG_RING_ERR: CQ CTL/SM REG Register ring error (ie noack).
16	RWX	WOX_AND	WOX_OR	CTL_MMIO_ST_DATA_UE: CQ CTL/SM DUE Data Uncorrectable error for MMIO store data.
17	RWX	WOX_AND	WOX_OR	CTL_PEF: CQ CTL/SM PE-Frozen.
18	RWX	WOX_AND	WOX_OR	CTL_NVL_CFG_ERR: CQ CTL/SM NCF NVLink configuration error (ex: Probe missed its GPUBAR).
19	RWX	WOX_AND	WOX_OR	CTL_NVL_FATAL_ERR: CQ CTL/SM NVF NVLink fatal (ex: rcv data resp to write req).
20	RWX	WOX_AND	WOX_OR	Reserved_1: CQ CTL/SM Rsv1 Reserved.
21	RWX	WOX_AND	WOX_OR	CTL_ARRAY_UE: CQ CTL/SM AUE Array uncorrectable error.
22	RWX	WOX_AND	WOX_OR	CTL_PBUS_PERR: CQ CTL/SM PBP processor bus parity error.
23	RWX	WOX_AND	WOX_OR	CTL_PBUS_FATAL_ERR: CQ CTL/SM PBF processor bus Fatal (ex: addr_error CResp).
24	RWX	WOX_AND	WOX_OR	CTL_PBUS_CONFIG_ERR: CQ CTL/SM PBC processor bus configuration error (ex: group > 3).
25	RWX	WOX_AND	WOX_OR	CTL_FWD_PROGRESS_ERR: CQ CTL/SM FWD Forward-Progress (internal timer or rpt_hang.data).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
26	RWX	WOX_AND	WOX_OR	CTL_LOGIC_ERR: CQ CTL/SM NLG NPU Logic error (ex: invalid state, missed table lookup, etc.).
27	RWX	WOX_AND	WOX_OR	CTL_PEST_DIS: CQ CTL/SM UT = 1 to frozen PE.
28	RWX	WOX_AND	WOX_OR	CTL_RSVD_15: CQ CTL/SM Reserved, macro bit 15.
29	RWX	WOX_AND	WOX_OR	DAT_DATA_BE_UE: CQ DAT ECC UE on data/BE arrays. Relevant word is marked with SUE.
30	RWX	WOX_AND	WOX_OR	DAT_DATA_BE_CE: CQ DAT ECC CE on data/BE arrays.
31	RWX	WOX_AND	WOX_OR	DAT_DATA_BE_PERR: CQ DAT parity error on data/BE latches. Relevant word is marked with SUE.
32	RWX	WOX_AND	WOX_OR	DAT_CREG_PERR: CQ DAT parity errors on configuration registers.
33	RWX	WOX_AND	WOX_OR	DAT_RTAG_PERR: CQ DAT parity errors on received processor bus RTAG.
34	RWX	WOX_AND	WOX_OR	DAT_STATE_PERR: CQ DAT parity errors on internal state latches.
35	RWX	WOX_AND	WOX_OR	DAT_LOGIC_ERR: CQ DAT logic error (invalid state bit patterns, credit overflow, etc.).
36	RWX	WOX_AND	WOX_OR	DAT_DATA_BE_SUE: CQ_DAT ECC SUE on data/BE arrays that can be due to poisoned data from GPU.
37	RWX	WOX_AND	WOX_OR	DAT_PBRX_SUE: CQ_DAT ECC SUE on PB receive data (CANNOT be due to poisoned data from GPU).
38	RWX	WOX_AND	WOX_OR	DAT_RSVD_9: CQ DAT Reserved, macro bit 9.
39	RWX	WOX_AND	WOX_OR	DAT_RSVD_10: CQ DAT Reserved, macro bit 10.
40	RWX	WOX_AND	WOX_OR	XTS_INT: XTS internal logic error.
41	RWX	WOX_AND	WOX_OR	XTS_SRAM_CE: XTS correctable errors in XTS internal SRAM.
42	RWX	WOX_AND	WOX_OR	XTS_SRAM_UE: XTS uncorrectable errors in XTS internal SRAM.
43	RWX	WOX_AND	WOX_OR	XTS_PROTOCOL_CE: XTS correctable error on incoming stack transactions.
44	RWX	WOX_AND	WOX_OR	XTS_PROTOCOL_UE: XTS uncorrectable/protocol errors on incoming stack transaction.
45	RWX	WOX_AND	WOX_OR	XTS_PBUS_PROTOCOL: XTS protocol errors on incoming PBUS transaction.
46	RWX	WOX_AND	WOX_OR	XTS_RSVD_6: XTS Translate Request Fail.
47	RWX	WOX_AND	WOX_OR	XTS_RSVD_7: XTS Reserved, macro bit 7.
48	RWX	WOX_AND	WOX_OR	XTS_RSVD_8: XTS Reserved, macro bit 8.
49	RWX	WOX_AND	WOX_OR	XTS_RSVD_9: XTS Reserved, macro bit 9.
50	RWX	WOX_AND	WOX_OR	XTS_RSVD_10: XTS Reserved, macro bit 10.
51	RWX	WOX_AND	WOX_OR	XTS_RSVD_11: XTS Reserved, macro bit 11.
52	RWX	WOX_AND	WOX_OR	XTS_RSVD_12: XTS Reserved, macro bit 12.
53	RWX	WOX_AND	WOX_OR	XTS_RSVD_13: XTS Reserved, macro bit 13.
54	RWX	WOX_AND	WOX_OR	XTS_RSVD_14: XTS Reserved, macro bit 14.
55	RWX	WOX_AND	WOX_OR	XTS_RSVD_15: XTS Reserved, macro bit 15.
56	RWX	WOX_AND	WOX_OR	XTS_RSVD_16: XTS Reserved, macro bit 16.
57	RWX	WOX_AND	WOX_OR	XTS_RSVD_17: XTS Reserved, macro bit 17.
58	RWX	WOX_AND	WOX_OR	XTS_RSVD_18: XTS Reserved, macro bit 18.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
59	RWX	WOX_AND	WOX_OR	XTS_RSVD_19: XTS Reserved, macro bit 19.
60	RWX	WOX_AND	WOX_OR	SCOMSAT00_ERR: MISC Pervasive SCOM satellite signaled internal FSM error (ring 0, sat 0).
61	RWX	WOX_AND	WOX_OR	SCOMSAT01_ERR: MISC Pervasive SCOM satellite signaled internal FSM error (ring 0, sat 1).
62	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERR2_0: Local FIR Parity Error RAS duplicate (ring 1, sat 0).
63	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERR_0: Local FIR Parity Error of ACTION/MASK registers (ring 1, sat 0).

Register Name	**NPU FIR Mask 0 Register**
Mnemonic	NPU.MISC.FIR_MASK_REG_0
Address	0000000005011403 (SCOM) 0000000005011404 (SCOM1) 0000000005011405 (SCOM2)
Description	Mask Select for the FIR bits

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RW	WO_AND	WO_OR	FIR_MASK_0: Mask select for corresponding bit in FIR. (Action0, Action1, Mask) = Action Select. (0,0,0) = Checkstop Error. (0,1,0) = Recoverable Error. (1,0,0) = Not Used. (1,1,0) = Local Core Checkstop / GX freeze. (x,x,1) = Masked.

Register Name	**NPU FIR 0 Action 0 Register**
Mnemonic	NPU.MISC.FIR_ACTION0_REG_0
Address	0000000005011406 (SCOM)
Description	Action Select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FIR_ACTION0_0: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action Select. (0,0,0) = Checkstop Error. (0,1,0) = Recoverable Error. (1,0,0) = Not Used. (1,1,0) = Local Core Checkstop / GX freeze. (x,x,1) = MaskedD.

Register Name	**NPU FIR 0 Action 1 Register**
Mnemonic	NPU.MISC.FIR_ACTION1_REG_0
Address	0000000005011407 (SCOM)
Description	Action Select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FIR_ACTION1_0: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action Select. (0,0,0) = Checkstop Error. (0,1,0) = Recoverable Error. (1,0,0) = Not Used. (1,1,0) = Local Core Checkstop / GX freeze. (x,x,1) = Masked.

Register Name	Pervasive FIR WOF 0 Register
Mnemonic	NPU.MISC.FIR_WOF_REG_0
Address	0000000005011408 (SCOM)
Description	Who is on first register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	FIR_WOF_0: WOF Register locks on first error.

Register Name	NPU FIR 1 Register
Mnemonic	NPU.MISC.FIR_REG_1
Address	0000000005011440 (SCOM) 0000000005011441 (SCOM1) 0000000005011442 (SCOM2)
Description	Local FIR register for the NPU (2 of 2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	NDL_BRK0_STALL: NDL Brick0 stall.
1	RWX	WOX_AND	WOX_OR	NDL_BRK0_NOSTALL: NDL Brick0 nostall.
2	RWX	WOX_AND	WOX_OR	NDL_BRK1_STALL: NDL Brick1 stall.
3	RWX	WOX_AND	WOX_OR	NDL_BRK1_NOSTALL: NDL Brick1 nostall.
4	RWX	WOX_AND	WOX_OR	NDL_BRK2_STALL: NDL Brick2 stall.
5	RWX	WOX_AND	WOX_OR	NDL_BRK2_NOSTALL: NDL Brick2 nostall.
6	RWX	WOX_AND	WOX_OR	NDL_BRK3_STALL: NDL Brick3 stall.
7	RWX	WOX_AND	WOX_OR	NDL_BRK3_NOSTALL: NDL Brick3 nostall.
8	RWX	WOX_AND	WOX_OR	NDL_BRK4_STALL: NDL Brick4 stall.
9	RWX	WOX_AND	WOX_OR	NDL_BRK4_NOSTALL: NDL Brick4 nostall.
10	RWX	WOX_AND	WOX_OR	NDL_BRK5_STALL: NDL Brick5 stall.
11	RWX	WOX_AND	WOX_OR	NDL_BRK5_NOSTALL: NDL Brick5 nostall.
12	RWX	WOX_AND	WOX_OR	MISC_REG_RING_ERR: MISC Register ring error (noack, >1 ack).
13	RWX	WOX_AND	WOX_OR	MISC_INT_RA_PERR: MISC Parity error from interrupt base real address register.
14	RWX	WOX_AND	WOX_OR	MISC_DA_ADDR_PERR: MISC Parity error on Indirect SCOM Address register.
15	RWX	WOX_AND	WOX_OR	MISC_CTRL_PERR: MISC Parity error on MISC Control register.
16	RWX	WOX_AND	WOX_OR	MISC_NMMU_ERR: MISC NMMU signaled Local Checkstop.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
17	RWX	WOX_AND	WOX_OR	ATS_TVT_ENTRY_INVALID: ATS Invalid TVT entry (TCE Table Size = 0b00000).
18	RWX	WOX_AND	WOX_OR	ATS_TVT_ADDR_RANGE_ERR: ATS TVT Address range error (no xlate: EA out of range; xlate: unused EA bits non-zero, TVE uses > max # EA bits).
19	RWX	WOX_AND	WOX_OR	ATS_TCE_PAGE_ACCESS_CA_ERR: ATS TCE Page access error during TCE cache lookup.
20	RWX	WOX_AND	WOX_OR	ATS_TCE_CACHE_MULT_HIT_ERR: ATS Effective Address hit multiple TCE cache entries.
21	RWX	WOX_AND	WOX_OR	ATS_TCE_PAGE_ACCESS_TW_ERR: ATS TCE Page access error during TCE table-walk.
22	RWX	WOX_AND	WOX_OR	ATS_TCE_REQ_TO_ERR: ATS Timeout on TCE tree walk.
23	RWX	WOX_AND	WOX_OR	ATS_TCD_PERR: ATS Parity error on TCE cache directory array.
24	RWX	WOX_AND	WOX_OR	ATS_TDR_PERR: ATS Parity error on TCE cache data array.
25	RWX	WOX_AND	WOX_OR	ATS_AT_EA_UE: ATS ECC UE on Effective Address array.
26	RWX	WOX_AND	WOX_OR	ATS_AT_EA_CE: ATS ECC CE on Effective Address array.
27	RWX	WOX_AND	WOX_OR	ATS_AT_TDRMEM_UE: ATS ECC UE on TDRmem array (table-walk state machine also hangs).
28	RWX	WOX_AND	WOX_OR	ATS_AT_TDRMEM_CE: ATS ECC CE on TDRmem array.
29	RWX	WOX_AND	WOX_OR	ATS_AT_RSPOUT_UE: ATS ECC UE on CQ CTL DMA Read data to TDR_mem array during table-walk.
30	RWX	WOX_AND	WOX_OR	ATS_AT_RSPOUT_CE: ATS ECC CE on CQ CTL DMA Read data to TDR_mem array during table-walk.
31	RWX	WOX_AND	WOX_OR	ATS_TVT_PERR: ATS Parity error on TVT entry.
32	RWX	WOX_AND	WOX_OR	ATS_IODA_ADDR_PERR: ATS Parity error on IODA Address Register.
33	RWX	WOX_AND	WOX_OR	ATS_NPU_CTRL_PERR: ATS Parity error on ATS Control Register.
34	RWX	WOX_AND	WOX_OR	ATS_NPU_TOR_PERR: ATS Parity error on ATS Timeout Control register.
35	RWX	WOX_AND	WOX_OR	ATS_INVAL_IODA_TBL_SEL: ATS Invalid IODA Table Address Register Table Select entry.
36	RWX	WOX_AND	WOX_OR	ATS_RSVD_19: ATS Reserved, macro bit 19.
37	RWX	WOX_AND	WOX_OR	FIR1_RSVD_37: FIR1 Reserved, bit 37.
38	RWX	WOX_AND	WOX_OR	FIR1_RSVD_38: FIR1 Reserved, bit 38.
39	RWX	WOX_AND	WOX_OR	FIR1_RSVD_39: FIR1 Reserved, bit 39.
40	RWX	WOX_AND	WOX_OR	FIR1_RSVD_40: FIR1 Reserved, bit 40.
41	RWX	WOX_AND	WOX_OR	FIR1_RSVD_41: FIR1 Reserved, bit 41.
42	RWX	WOX_AND	WOX_OR	FIR1_RSVD_42: FIR1 Reserved, bit 42.
43	RWX	WOX_AND	WOX_OR	FIR1_RSVD_43: FIR1 Reserved, bit 43.
44	RWX	WOX_AND	WOX_OR	FIR1_RSVD_44: FIR1 Reserved, bit 44.
45	RWX	WOX_AND	WOX_OR	FIR1_RSVD_45: FIR1 Reserved, bit 45.
46	RWX	WOX_AND	WOX_OR	FIR1_RSVD_46: FIR1 Reserved, bit 46.
47	RWX	WOX_AND	WOX_OR	FIR1_RSVD_47: FIR1 Reserved, bit 47.
48	RWX	WOX_AND	WOX_OR	FIR1_RSVD_48: FIR1 Reserved, bit 48.
49	RWX	WOX_AND	WOX_OR	FIR1_RSVD_49: FIR1 Reserved, bit 49.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
50	RWX	WOX_AND	WOX_OR	FIR1_RSVD_50: FIR1 Reserved, bit 50.
51	RWX	WOX_AND	WOX_OR	FIR1_RSVD_51: FIR1 Reserved, bit 51.
52	RWX	WOX_AND	WOX_OR	FIR1_RSVD_52: FIR1 Reserved, bit 52.
53	RWX	WOX_AND	WOX_OR	FIR1_RSVD_53: FIR1 Reserved, bit 53.
54	RWX	WOX_AND	WOX_OR	FIR1_RSVD_54: FIR1 Reserved, bit 54.
55	RWX	WOX_AND	WOX_OR	FIR1_RSVD_55: FIR1 Reserved, bit 55.
56	RWX	WOX_AND	WOX_OR	FIR1_RSVD_56: FIR1 Reserved, bit 56.
57	RWX	WOX_AND	WOX_OR	FIR1_RSVD_57: FIR1 Reserved, bit 57.
58	RWX	WOX_AND	WOX_OR	FIR1_RSVD_58: FIR1 Reserved, bit 58.
59	RWX	WOX_AND	WOX_OR	FIR1_RSVD_59: FIR1 Reserved, bit 59.
60	RWX	WOX_AND	WOX_OR	FIR1_RSVD_60: FIR1 Reserved, bit 60.
61	RWX	WOX_AND	WOX_OR	FIR1_RSVD_61: FIR1 Reserved, bit 61.
62	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERR2_1: Local FIR Parity Error RAS duplicate (ring 1, sat 1).
63	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERR_1: Local FIR Parity Error of ACTION/MASK registers (ring 1, sat 1).

Register Name	**NPU FIR Mask 1 Register**
Mnemonic	NPU.MISC.FIR_MASK_REG_1
Address	0000000005011443 (SCOM) 0000000005011444 (SCOM1) 0000000005011445 (SCOM2)
Description	Mask Select for the FIR bits

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RW	WO_AND	WO_OR	FIR_MASK_1: Mask select for corresponding bit in FIR. (Action0, Action1, Mask) = Action Select. (0,0,0) = Checkstop Error. (0,1,0) = Recoverable Error. (1,0,0) = Not Used. (1,1,0) = Local Core Checkstop / GX freeze. (x,x,1) = MASKED.

Register Name	**NPU FIR Action 0 Register 1**
Mnemonic	NPU.MISC.FIR_ACTION0_REG_1
Address	0000000005011446 (SCOM)
Description	Action Select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FIR_ACTION0_1: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action Select. (0,0,0) = Checkstop Error. (0,1,0) = Recoverable Error. (1,0,0) = Not Used. (1,1,0) = Local Core Checkstop / GX freeze. (x,x,1) = MASKED.

Register Name	**NPU FIR 1 Action 1 Register**
Mnemonic	NPU.MISC.FIR_ACTION1_REG_1
Address	0000000005011447 (SCOM)
Description	Action Select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FIR_ACTION1_1: MSB of action select for corresponding bit in FIR. (Action0, Action1, Mask) = Action Select. (0,0,0) = Checkstop Error. (0,1,0) = Recoverable Error. (1,0,0) = Not Used. (1,1,0) = Local Core Checkstop / GX freeze. (x,x,1) = MASKED.

Register Name	**Pervasive FIR WOF 1 Register**
Mnemonic	NPU.MISC.FIR_WOF_REG_1
Address	0000000005011448 (SCOM)
Description	Who is on first register indicates which error occurred first

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	FIR_WOF_1: WOF Register locks on first error.

Register Name	**Power Bus PB West FIR Register**
Mnemonic	PB.COM.PB_WEST_FIR_REG
Address	0000000005011800 (SCOM) 0000000005011801 (SCOM1) 0000000005011802 (SCOM2)
Description	Processor bus PB west nest domain FIR register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ00_PBH_HW1_ERROR: pbieq00_pbh_hw1_error.
1	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ00_PBH_HW2_ERROR: pbieq00_pbh_hw2_error.
2	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ00_PBH_PROTOCOL_ERROR: pbieq00_pbh_protocol_error.
3	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ00_PBH_OVERFLOW_ERROR: pbieq00_pbh_overflow_error.
4	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ01_PBH_HW1_ERROR: pbieq01_pbh_hw1_error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ01_PBH_HW2_ERROR: pbieq01_pbh_hw2_error.
6	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ01_PBH_PROTOCOL_ERROR: pbieq01_pbh_protocol_error.
7	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ01_PBH_OVERFLOW_ERROR: pbieq01_pbh_overflow_error.
8	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ02_PBH_HW1_ERROR: pbieq02_pbh_hw1_error.
9	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ02_PBH_HW2_ERROR: pbieq02_pbh_hw2_error.
10	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ02_PBH_PROTOCOL_ERROR: pbieq02_pbh_protocol_error.
11	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ02_PBH_OVERFLOW_ERROR: pbieq02_pbh_overflow_error.
12	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ03_PBH_HW1_ERROR: pbieq03_pbh_hw1_error.
13	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ03_PBH_HW2_ERROR: pbieq03_pbh_hw2_error.
14	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ03_PBH_PROTOCOL_ERROR: pbieq03_pbh_protocol_error.
15	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ03_PBH_OVERFLOW_ERROR: pbieq03_pbh_overflow_error.
16	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_16: fir_spare_16.
17	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_17: fir_spare_17.
18	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_18: fir_spare_18.
19	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_19: fir_spare_19.
20	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_20: fir_spare_20.
21	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_21: fir_spare_21.
22	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_22: fir_spare_22.
23	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_23: fir_spare_23.
24	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_24: fir_spare_24.
25	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_25: fir_spare_25.
26	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_26: fir_spare_26.
27	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_27: fir_spare_27.
28	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_28: fir_spare_28.
29	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_29: fir_spare_29.
30	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_30: fir_spare_30.
31	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_31: fir_spare_31.
32	RWX	WOX_AND	WOX_OR	FIR_SCOM_WEST_ERR: PBEH west FIR_SCOM_err.
33	RWX	WOX_AND	WOX_OR	FIR_SCOM_WEST_ERR_DUP: PBEH west FIR_SCOM_err duplicate.
34:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus PB West FIR Mask Register
Mnemonic	PB.COM.PB_WEST_FIR_MASK_REG
Address	0000000005011803 (SCOM) 0000000005011804 (SCOM1) 0000000005011805 (SCOM2)
Description	Processor bus PB west nest domain FIR MASK register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ00_PBH_HW1_ERROR_MASK: pbieq00_pbh_hw1_error_mask.
1	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ00_PBH_HW2_ERROR_MASK: pbieq00_pbh_hw2_error_mask.
2	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ00_PBH_PROTOCOL_ERROR_MASK: pbieq00_pbh_protocol_error_mask.
3	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ00_PBH_OVERFLOW_ERROR_MASK: pbieq00_pbh_overflow_error_mask.
4	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ01_PBH_HW1_ERROR_MASK: pbieq01_pbh_hw1_error_mask.
5	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ01_PBH_HW2_ERROR_MASK: pbieq01_pbh_hw2_error_mask.
6	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ01_PBH_PROTOCOL_ERROR_MASK: pbieq01_pbh_protocol_error_mask.
7	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ01_PBH_OVERFLOW_ERROR_MASK: pbieq01_pbh_overflow_error_mask.
8	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ02_PBH_HW1_ERROR_MASK: pbieq02_pbh_hw1_error_mask.
9	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ02_PBH_HW2_ERROR_MASK: pbieq02_pbh_hw2_error_mask.
10	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ02_PBH_PROTOCOL_ERROR_MASK: pbieq02_pbh_protocol_error_mask.
11	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ02_PBH_OVERFLOW_ERROR_MASK: pbieq02_pbh_overflow_error_mask.
12	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ03_PBH_HW1_ERROR_MASK: pbieq03_pbh_hw1_error_mask.
13	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ03_PBH_HW2_ERROR_MASK: pbieq03_pbh_hw2_error_mask.
14	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ03_PBH_PROTOCOL_ERROR_MASK: pbieq03_pbh_protocol_error_mask.
15	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEQ03_PBH_OVERFLOW_ERROR_MASK: pbieq03_pbh_overflow_error_mask.
16	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_16_MASK: fir_spare_16_mask.
17	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_17_MASK: fir_spare_17_mask.
18	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_18_MASK: fir_spare_18_mask.
19	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_19_MASK: fir_spare_19_mask.
20	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_20_MASK: fir_spare_20_mask.
21	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_21_MASK: fir_spare_21_mask.
22	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_22_MASK: fir_spare_22_mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
23	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_23_MASK: fir_spare_23_mask.
24	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_24_MASK: fir_spare_24_mask.
25	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_25_MASK: fir_spare_25_mask.
26	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_26_MASK: fir_spare_26_mask.
27	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_27_MASK: fir_spare_27_mask.
28	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_28_MASK: fir_spare_28_mask.
29	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_29_MASK: fir_spare_29_mask.
30	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_30_MASK: fir_spare_30_mask.
31	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_31_MASK: fir_spare_31_mask.
32	RWX	WOX_AND	WOX_OR	FIR_SCOM_WEST_ERR_MASK: PBEH WEST FIR_SCOM_err_mask.
33	RWX	WOX_AND	WOX_OR	FIR_SCOM_WEST_ERR_MASK_DUP: PBEH WEST FIR_SCOM_err_mask_dup.
34:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus PB West FIR Action 0 Register
Mnemonic	PB.COM.PB_WEST_FIR_ACTION0_REG
Address	0000000005011806 (SCOM)
Description	Processor bus PB west nest domain FIR Action 0 Register

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PB_WEST_FIR_ACTION0: Processor bus PBEH WEST nest domain FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Recoverable Interrupt to Processor. (1,1) = Invalid.
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus PB West FIR Action 1 Register
Mnemonic	PB.COM.PB_WEST_FIR_ACTION1_REG
Address	0000000005011807 (SCOM)
Description	Processor bus PB west nest domain FIR Action 1 Register

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PB_WEST_FIR_ACTION1: Processor bus PB WEST nest domain FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Recoverable Interrupt to Processor. (1,1) = Invalid.
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus PB West Mode Configuration Register
Mnemonic	PB.COM.PB_WEST_MODE
Address	000000000501180A (SCOM)
Description	Power Bus west mode configuration register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1:3	RO	Constant = 0b000
4	RWX	PB_CFG_CHIP_IS_SYSTEM: Configures whether there are other POWER9s in the system.
5:7	RW	Reserved.
8	RWX	PB_CFG_HNG_CHK_DISABLE: Hang Check Disable.
9	RWX	PB_DBG_CLR_MAX_HANG_STAGE: Resets the maximum hang state level (pb_hang_level).
10:11	RW	Reserved.
12:15	RWX	PB_CFG_SW_AB_WAIT: Adds delay to tc_pb_switch_ab input from TPC during hot plug sequence.
16:22	RWX	PB_CFG_SP_HW_MARK: configures the maximum system pumps an IO unit may issue.
23:29	RWX	PB_CFG_GP_HW_MARK: configures the maximum group pumps this chip may issue.
30:35	RWX	PB_CFG_LCL_HW_MARK: configures the maximum local pumps this chip may issue.
36:41	RWX	Reserved.
42:56	RW	Reserved.
57	RWX	PB_CFG_REQ_GATHER_ENABLE: Enable data OW gathering on all chiplet/link requests. {default = on}.
58	RW	PB_CFG_SWITCH_CD_PULSE: Controls switch_cd pulse width. Uses pb_cfg_sw_ab_wait to extend pulse. Default = long pulse. Requires pb_cfg_sw_ab_wait > cnt_5 for 6 cycle pulse.
59	RWX	PB_CFG_SWITCH_OPTION_AB: SCOM access to determine what signal drives pb_cfg_switch_cd. on = tc_pb_switch_ab, off = tc_pb_switch_cd.
60:62	RW	Reserved.
63	RWX	Reserved.

Register Name	Power Bus PB West HP Mode Next Register
Mnemonic	PB.COM.PB_WEST_HP_MODE_NEXT
Address	000000000501180B (SCOM)
Description	Power Bus West High-Performance Mode Next Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_NEXT: Processor bus master.
1	RWX	PB_CFG_TM_MASTER_NEXT: Configure chip as the processor bus TM master.
2	RWX	PB_CFG_CHG_RATE_GP_MASTER_NEXT: Sets the group pump change rate master. This master gathers all general-purpose chg_rate.reqs and issues a chg_rate.gnt.
3	RWX	PB_CFG_CHG_RATE_SP_MASTER_NEXT: Sets the system pump change rate master. This master gathers all special-purpose chg_rate.reqs and issues a chg_rate.gnt.
4	RWX	PB_CFG_LINK_A0_EN_NEXT: Link A0 enabled.
5	RWX	PB_CFG_LINK_A1_EN_NEXT: Link A1 enabled.
6	RWX	PB_CFG_LINK_A2_EN_NEXT: Link A2 enabled.

Bits	SCOM	Field Mnemonic: Description
7	RWX	PB_CFG_LINK_A3_EN_NEXT: Link A3 enabled.
8	RWX	PB_CFG_LINK_NA0_ADDR_DIS_NEXT: Link A0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NA1_ADDR_DIS_NEXT: Link A1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NA2_ADDR_DIS_NEXT: Link A2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NA3_ADDR_DIS_NEXT: Link A3 address broadcast disabled.
12:15	RWX	PB_CFG_LINK_A0_GROUPID_NEXT: Group ID of chip connected to A0 link.
16:19	RWX	PB_CFG_LINK_A1_GROUPID_NEXT: Group ID of chip connected to A1 link.
20:23	RWX	PB_CFG_LINK_A2_GROUPID_NEXT: Group ID of chip connected to A2 link.
24:27	RWX	PB_CFG_LINK_A3_GROUPID_NEXT: Group ID of chip connected to A3 link.
28	RWX	PB_CFG_A_AGGREGATE_NEXT: Processor bus A links are configured as parallel buses to the same chip.
29	RWX	PB_CFG_HOP_MODE_NEXT: Sets SMP hop mode. 0 = 1-hop or 2-hop SMP topology. 1 = 3-hop SMP topology.
30	RWX	PB_CFG_SMP_OPTICS_MODE_NEXT: Sets SMP optics mode. 0 = Optic Links are configured as X-bus SMP protocol. 1 = Optic Links are configured as A-bus SMP protocol.
31	RWX	PB_CFG_CAPI_MODE_NEXT: Indicates a CAPI 2.0 link is attached in the SMP system.
32:33	RWX	PB_CFG_OPT0_MODE_NEXT: Optical Link 0 configuration.
34:35	RWX	PB_CFG_OPT1_MODE_NEXT: Optical Link 1 configuration.
36:37	RWX	PB_CFG_OPT2_MODE_NEXT: Optical Link 2 configuration.
38:39	RWX	PB_CFG_OPT3_MODE_NEXT: Optical Link 3 configuration.
40:46	RWX	PB_CFG_XLATE_ADDR_TO_ID_WEST_NEXT: Configures the translation of the address to topology ID XOR mask.
47:48	RW	Reserved.
49	RWX	Reserved.
50	RWX	PB_CFG_A_GATHER_ENABLE_NEXT: Enable data OW gathering on A links.
51	RW	Reserved.
52	RWX	PB_CFG_PHYP_IS_GROUP_NEXT: Configures the PHYP boundary. 0 = phyp_is_system 1 = phyp_is_group
53	RWX	PB_CFG_ADDR_BAR_MODE_NEXT: Address BAR Mode. The SMP is limited to two or four sockets. When 1, pb_cfg_pump_mode must also be set to 1.
54	RWX	PB_CFG_PUMP_MODE_NEXT: Configures the physical broadcast. 0 = Chip_is_node (default). 1 = Chip_is_group.
55	RWX	PB_CFG_DCACHE_CAPP_MODE_NEXT: Dcache CAPP mode. 0 = off (default). 1 = on.
56:63	RWX	PB_CFG_A_CMD_RATE_WEST_NEXT: Configures the paced command rate to not overrun the A link.

Register Name	Power Bus PB West HP Mode Current Register
Mnemonic	PB.COM.PB_WEST_HP_MODE_CURR
Address	000000000501180C (SCOM)
Description	Power Bus West High-Performance Mode Current Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_CURR: Processor bus master.
1	RWX	PB_CFG_TM_MASTER_CURR: Configure chip as PB TM master.
2	RWX	PB_CFG_CHG_RATE_GP_MASTER_CURR: Sets the group pump change rate master. This master gathers all general-purpose chg_rate.reqs and issues a chg_rate.gnt.
3	RWX	PB_CFG_CHG_RATE_SP_MASTER_CURR: Sets the system pump change rate master. This master gathers all special-purpose chg_rate.reqs and issues a chg_rate.gnt.
4	RWX	PB_CFG_LINK_A0_EN_CURR: Link A0 enabled.
5	RWX	PB_CFG_LINK_A1_EN_CURR: Link A1 enabled.
6	RWX	PB_CFG_LINK_A2_EN_CURR: Link A2 enabled.
7	RWX	PB_CFG_LINK_A3_EN_CURR: Link A3 enabled.
8	RWX	PB_CFG_LINK_NA0_ADDR_DIS_CURR: Link A0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NA1_ADDR_DIS_CURR: Link A1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NA2_ADDR_DIS_CURR: Link A2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NA3_ADDR_DIS_CURR: Link A3 address broadcast disabled.
12:15	RWX	PB_CFG_LINK_A0_GROUPID_CURR: Group ID of chip connected to A0 link.
16:19	RWX	PB_CFG_LINK_A1_GROUPID_CURR: Group ID of chip connected to A1 link.
20:23	RWX	PB_CFG_LINK_A2_GROUPID_CURR: Group ID of chip connected to A2 link.
24:27	RWX	PB_CFG_LINK_A3_GROUPID_CURR: Group ID of chip connected to A3 link.
28	RWX	PB_CFG_A_AGGREGATE_CURR: Processor bus A links are configured as parallel buses to same chip.
29	RWX	PB_CFG_HOP_MODE_CURR: Sets SMP hop mode. 0 = 1-hop or 2-hop SMP topology. 1 = 3-hop SMP topology.
30	RWX	PB_CFG_SMP_OPTICS_MODE_CURR: Sets SMP optics mode. 0 = Optic links are configured as X-bus SMP protocol. 1 = Optic links are configured as A-bus SMP protocol.
31	RWX	PB_CFG_CAPI_MODE_CURR: Indicates a CAPI 2.0 link is attached in the SMP system.
32:33	RWX	PB_CFG_OPT0_MODE_CURR: Optical link 0 configuration.
34:35	RWX	PB_CFG_OPT1_MODE_CURR: Optical link 1 configuration.
36:37	RWX	PB_CFG_OPT2_MODE_CURR: Optical link 2 configuration.
38:39	RWX	PB_CFG_OPT3_MODE_CURR: Optical link 3 configuration.
40:46	RWX	PB_CFG_XLATE_ADDR_TO_ID_WEST_CURR: Configures the translation of the address to topology ID XOR mask.
47:48	RW	Reserved.
49	RWX	Reserved.
50	RWX	PB_CFG_A_GATHER_ENABLE_CURR: Enable data OW gathering on A links.
51	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RWX	PB_CFG_PHYP_IS_GROUP_CURR: Configures the PHYP boundary. 0 = phyp_is_system. 1 = phyp_is_group.
53	RWX	PB_CFG_ADDR_BAR_MODE_CURR: Address BAR Mode. The SMP is limited to two or four sockets. When 1, pb_cfg_pump_mode must also be set to 1.
54	RWX	PB_CFG_PUMP_MODE_CURR: Configures the physical broadcast. 0 = Chip_is_node (default). 1 = Chip_is_group.
55	RWX	PB_CFG_DCACHE_CAPP_MODE_CURR: Dcache CAPP mode. 0 = off (default). 1 = on.
56:63	RWX	PB_CFG_A_CMD_RATE_WEST_CURR: configures the paced command rate to not overrun the A link.

Register Name	Power Bus PB West HPA Mode Next Register
Mnemonic	PB.COM.PB_WEST_HPA_MODE_NEXT
Address	000000000501180D (SCOM)
Description	Power Bus West HPA Mode Next Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved.
1	RWX	Reserved.
2	RWX	Reserved.
3	RWX	Reserved.
4	RWX	Reserved.
5	RWX	Reserved.
6	RWX	Reserved.
7	RWX	Reserved.
8	RWX	Reserved.
9	RWX	Reserved.
10	RWX	Reserved.
11	RWX	Reserved.
12:15	RW	Reserved.
16:19	RWX	Reserved.
20:23	RWX	Reserved.
24:27	RWX	Reserved.
28:31	RWX	Reserved.
32:35	RWX	Reserved.
36:39	RWX	Reserved.
40:43	RWX	Reserved.
44:47	RWX	Reserved.
48:51	RWX	Reserved.
52:55	RWX	Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RWX	Reserved.
60:63	RWX	Reserved.

Register Name	Power Bus PB West HPA Mode Current Register
Mnemonic	PB.COM.PB_WEST_HPA_MODE_CURR
Address	000000000501180E (SCOM)
Description	Power Bus West HPA Mode Current Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved.
1	RWX	Reserved.
2	RWX	Reserved.
3	RWX	Reserved.
4	RWX	Reserved.
5	RWX	Reserved.
6	RWX	Reserved.
7	RWX	Reserved.
8	RWX	Reserved.
9	RWX	Reserved.
10	RWX	Reserved.
11	RWX	Reserved.
12:15	RW	Reserved.
16:19	RWX	Reserved.
20:23	RWX	Reserved.
24:27	RWX	Reserved.
28:31	RWX	Reserved.
32:35	RWX	Reserved.
36:39	RWX	Reserved.
40:43	RWX	Reserved.
44:47	RWX	Reserved.
48:51	RWX	Reserved.
52:55	RWX	Reserved.
56:59	RWX	Reserved.
60:63	RWX	Reserved.

Register Name	Power Bus PB West HPX Mode Next Register
Mnemonic	PB.COM.PB_WEST_HPX_MODE_NEXT
Address	000000000501180F (SCOM)
Description	Power Bus West HPX Mode Next Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_NEXT: Link X0 enabled.
1	RWX	PB_CFG_LINK_X1_EN_NEXT: Link X1 enabled.
2	RWX	PB_CFG_LINK_X2_EN_NEXT: Link X2 enabled.
3	RWX	PB_CFG_LINK_X3_EN_NEXT: Link X3 enabled.
4	RWX	PB_CFG_LINK_X4_EN_NEXT: Link X4 enabled.
5	RWX	PB_CFG_LINK_X5_EN_NEXT: Link X5 enabled.
6	RWX	PB_CFG_LINK_X6_EN_NEXT: Link X6 enabled.
7	RW	Reserved.
8	RWX	PB_CFG_LINK_NX0_ADDR_DIS_NEXT: Link X0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NX1_ADDR_DIS_NEXT: Link X1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NX2_ADDR_DIS_NEXT: Link X2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NX3_ADDR_DIS_NEXT: Link X3 address broadcast disabled.
12	RWX	PB_CFG_LINK_NX4_ADDR_DIS_NEXT: Link X4 address broadcast disabled.
13	RWX	PB_CFG_LINK_NX5_ADDR_DIS_NEXT: Link X5 address broadcast disabled.
14	RWX	PB_CFG_LINK_NX6_ADDR_DIS_NEXT: Link X6 address broadcast disabled.
15	RW	Reserved.
16:18	RWX	PB_CFG_LINK_X0_CHIPID_NEXT: Chip ID of chip connected to X0 link.
19:21	RWX	PB_CFG_LINK_X1_CHIPID_NEXT: Chip ID of chip connected to X1 link.
22:24	RWX	PB_CFG_LINK_X2_CHIPID_NEXT: Chip ID of chip connected to X2 link.
25:27	RWX	PB_CFG_LINK_X3_CHIPID_NEXT: Chip ID of chip connected to X3 link.
28:30	RWX	PB_CFG_LINK_X4_CHIPID_NEXT: Chip ID of chip connected to X4 link.
31:33	RWX	PB_CFG_LINK_X5_CHIPID_NEXT: Chip ID of chip connected to X5 link.
34:36	RWX	PB_CFG_LINK_X6_CHIPID_NEXT: Chip ID of chip connected to X6 link.
37	RWX	PB_CFG_X_AGGREGATE_NEXT: Processor bus X links are configured as parallel buses to the same chip.
38:47	RW	Reserved.
48	RW	PB_CFG_X_FP_DISABLED_NEXT: Processor bus X link RTAG fastpath disable.
49	RWX	PB_CFG_X_INDIRECT_EN_NEXT: Processor bus X links are configured for indirect data routing.
50	RWX	PB_CFG_X_GATHER_ENABLE_NEXT: Enable data OW gathering on X links.
51:55	RW	Reserved.
56:63	RWX	PB_CFG_X_CMD_RATE_WEST_NEXT: Configures the paced command rate to not overrun the X link.

Register Name	Power Bus PB West HPX Mode Current Register
Mnemonic	PB.COM.PB_WEST_HPX_MODE_CURR
Address	0000000005011810 (SCOM)
Description	Power Bus West HPX Mode Current Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_CURR: Link X0 enabled.
1	RWX	PB_CFG_LINK_X1_EN_CURR: Link X1 enabled.
2	RWX	PB_CFG_LINK_X2_EN_CURR: Link X2 enabled.
3	RWX	PB_CFG_LINK_X3_EN_CURR: Link X3 enabled.
4	RWX	PB_CFG_LINK_X4_EN_CURR: Link X4 enabled.
5	RWX	PB_CFG_LINK_X5_EN_CURR: Link X5 enabled.
6	RWX	PB_CFG_LINK_X6_EN_CURR: Link X6 enabled.
7	RW	Reserved.
8	RWX	PB_CFG_LINK_NX0_ADDR_DIS_CURR: Link X0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NX1_ADDR_DIS_CURR: Link X1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NX2_ADDR_DIS_CURR: Link X2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NX3_ADDR_DIS_CURR: Link X3 address broadcast disabled.
12	RWX	PB_CFG_LINK_NX4_ADDR_DIS_CURR: Link X4 address broadcast disabled.
13	RWX	PB_CFG_LINK_NX5_ADDR_DIS_CURR: Link X5 address broadcast disabled.
14	RWX	PB_CFG_LINK_NX6_ADDR_DIS_CURR: Link X6 address broadcast disabled.
15	RW	Reserved.
16:18	RWX	PB_CFG_LINK_X0_CHIPID_CURR: Chip ID of chip connected to X0 link.
19:21	RWX	PB_CFG_LINK_X1_CHIPID_CURR: Chip ID of chip connected to X1 link.
22:24	RWX	PB_CFG_LINK_X2_CHIPID_CURR: Chip ID of chip connected to X2 link.
25:27	RWX	PB_CFG_LINK_X3_CHIPID_CURR: Chip ID of chip connected to X3 link.
28:30	RWX	PB_CFG_LINK_X4_CHIPID_CURR: Chip ID of chip connected to X4 link.
31:33	RWX	PB_CFG_LINK_X5_CHIPID_CURR: Chip ID of chip connected to X5 link.
34:36	RWX	PB_CFG_LINK_X6_CHIPID_CURR: Chip ID of chip connected to X6 link.
37	RWX	PB_CFG_X_AGGREGATE_CURR: Processor bus X links are configured as parallel buses to same chip.
38:47	RW	Reserved.
48	RW	PB_CFG_X_FP_DISABLED_CURR: Processor bus X link RTAG fastpath disable.
49	RWX	PB_CFG_X_INDIRECT_EN_CURR: Processor bus X links are configured for indirect data routing.
50	RWX	PB_CFG_X_GATHER_ENABLE_CURR: Enable data OW gathering on X links.
51:55	RW	Reserved.
56:63	RWX	PB_CFG_X_CMD_RATE_WEST_CURR: configures the paced command rate to not overrun the X link.

Register Name	Power Bus PB West Serial Configuration Load Register
Mnemonic	PB.COM.PB_WEST_SCONFIG_LOAD
Address	0000000005011811 (SCOM)
Description	Power Bus West Serial Configuration Load Register

Bits	SCOM	Field Mnemonic: Description
0	WOX	PB_CFG_WEST_SCONFIG_LOAD: Load Serial Mode Registers.
1	RWX	PB_CFG_WEST_SCONFIG_SLOW: Set Load of Serial Mode Registers to 16:1 slow clock.
2:7	WOX	PB_CFG_WEST_SCONFIG_SHIFT_COUNT: Configures length of Serial Mode Register.
8:11	RWX	PB_CFG_WEST_SCONFIG_SELECT: Select Serial Mode register: 0000 = pbh_pbiex_eh. 0001 = pbh_pbiex_ex. 0010 = pbh_dat_ex_req_pmac. 0011 = pbh_dat_em_req_pmac. 0100 = pbh_dat_arb_ex_pmac. 0101 = pbh_dat_arb_em_pmac.
12:63	RWX	PB_CFG_WEST_SCONFIG_SHIFT_DATA: Serial Mode Register Data.

Register Name	Power Bus PB West Spare Configuration Register
Mnemonic	PB.COM.PB_WEST_SPARE
Address	0000000005011812 (SCOM)
Description	Power Bus West Spare Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus PB West FW Scratch 0 Register
Mnemonic	PB.COM.PB_WEST_FW_SCRATCH0
Address	0000000005011813 (SCOM) 0000000005011814 (SCOM1) 0000000005011815 (SCOM2)
Description	Power Bus PB West FW Scratch 0 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RWX	WOX_AND	WOX_OR	Reserved.

Register Name	Power Bus PB West FW Scratch 1 Register
Mnemonic	PB.COM.PB_WEST_FW_SCRATCH1
Address	0000000005011816 (SCOM) 0000000005011817 (SCOM1) 0000000005011818 (SCOM2)
Description	Power bus West FW Scratch 1 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RWX	WOX_AND	WOX_OR	Reserved.

Register Name	Power Bus PB CENT FIR Register
Mnemonic	PB.COM.PB_CENT_FIR_REG
Address	0000000005011C00 (SCOM) 0000000005011C01 (SCOM1) 0000000005011C02 (SCOM2)
Description	Processor bus CENT nest domain FIR register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_CENT_PROTOCOL_ERROR: protocol_error.
1	RWX	WOX_AND	WOX_OR	PB_CENT_OVERFLOW_ERROR: overflow_error.
2	RWX	WOX_AND	WOX_OR	PB_CENT_HW_PARITY_ERROR: hw_parity_error.
3	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_3: fir_spare_3.
4	RWX	WOX_AND	WOX_OR	PB_CENT_COHERENCY_ERROR: coherency_error.
5	RWX	WOX_AND	WOX_OR	PB_CENT_CRESP_ADDR_ERROR: cresp_addr_error.
6	RWX	WOX_AND	WOX_OR	PB_CENT_CRESP_ERROR: cresp_error.
7	RWX	WOX_AND	WOX_OR	PB_CENT_HANG_RECOVERY_LIMIT_ERROR: hang_recovery_limit_error.
8	RWX	WOX_AND	WOX_OR	PB_CENT_DATA_ROUTE_ERROR: data_route_error.
9	RWX	WOX_AND	WOX_OR	PB_CENT_HANG_RECOVERY_GTE_LEVEL1: hang_recovery_gte_level1.
10	RWX	WOX_AND	WOX_OR	PB_CENT_FORCE_MP_IPL: force_mp_ipl.
11	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_11: fir_spare_11.
12	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_12: fir_spare_12.
13	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_13: fir_spare_13.
14	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_14: fir_spare_14.
15	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_15: fir_spare_15.
16	RWX	WOX_AND	WOX_OR	FIR_SCOM_CENT_ERR: PBEH CENT FIR_SCOM_err.
17	RWX	WOX_AND	WOX_OR	FIR_SCOM_CENT_ERR_DUP: PBEH CENT FIR_SCOM_err duplicate.
18:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	Power Bus PB CENT FIR Mask Register
Mnemonic	PB.COM.PB_CENT_FIR_MASK_REG
Address	0000000005011C03 (SCOM) 0000000005011C04 (SCOM1) 0000000005011C05 (SCOM2)
Description	Processor bus PB CENT nest domain FIR MASK register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_CENT_PROTOCOL_ERROR_MASK: protocol_error_mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
1	RWX	WOX_AND	WOX_OR	PB_CENT_OVERFLOW_ERROR_MASK: overflow_error_mask.
2	RWX	WOX_AND	WOX_OR	PB_CENT_HW_PARITY_ERROR_MASK: hw_parity_error_mask.
3	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_3_MASK: fir_spare_3_mask.
4	RWX	WOX_AND	WOX_OR	PB_CENT_COHERENCY_ERROR_MASK: coherency_error_mask.
5	RWX	WOX_AND	WOX_OR	PB_CENT_CRESP_ADDR_ERROR_MASK: cresp_addr_error_mask.
6	RWX	WOX_AND	WOX_OR	PB_CENT_CRESP_ERROR_MASK: cresp_error_mask.
7	RWX	WOX_AND	WOX_OR	PB_CENT_HANG_RECOVERY_LIMIT_ERROR_MASK: hang_recovery_limit_error_mask.
8	RWX	WOX_AND	WOX_OR	PB_CENT_DATA_ROUTE_ERROR_MASK: data_route_error_mask.
9	RWX	WOX_AND	WOX_OR	PB_CENT_HANG_RECOVERY_GTE_LEVEL1_MASK: hang_recovery_gte_level1_mask.
10	RWX	WOX_AND	WOX_OR	PB_CENT_FORCE_MP_IPL_MASK: force_mp_ipl_mask.
11	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_11_MASK: fir_spare_11_mask.
12	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_12_MASK: fir_spare_12_mask.
13	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_13_MASK: fir_spare_13_mask.
14	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_14_MASK: fir_spare_14_mask.
15	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_15_MASK: fir_spare_15_mask.
16	RWX	WOX_AND	WOX_OR	FIR_SCOM_CENT_ERR_MASK: PBEH CENT FIR_SCOM_err_mask.
17	RWX	WOX_AND	WOX_OR	FIR_SCOM_CENT_ERR_MASK_DUP: PBEH CENT FIR_SCOM_err_mask_dup.
18:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	**Power Bus PB CENT FIR Action 0 Register**
Mnemonic	PB.COM.PB_CENT_FIR_ACTION0_REG
Address	0000000005011C06 (SCOM)
Description	Processor bus PB CENT nest domain FIR Action 0 Register

Bits	SCOM	Field Mnemonic: Description
0:17	RW	PB_CENT_FIR_ACTION0: Processor bus PBEH CENT nest domain FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Recoverable Interrupt to Processor. (1,1) = Invalid.
18:59	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	**Power Bus PB CENT FIR Action 1 Register**
Mnemonic	PB.COM.PB_CENT_FIR_ACTION1_REG
Address	0000000005011C07 (SCOM)
Description	Processor bus PB CENT nest domain FIR Action 1 Register

Bits	SCOM	Field Mnemonic: Description
0:17	RW	PB_CENT_FIR_ACTION1: Processor bus PB CENT nest domain FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Recoverable Interrupt to Processor. (1,1) = Invalid.
18:59	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Power Bus PB CENT Mode Register
Mnemonic	PB.COM.PB_CENT_MODE
Address	0000000005011C0A (SCOM)
Description	00 pb_cent_pbixxx_init 01:03 pb_cent_dbg_max_hang_stage_reached 04 pb_cfg_cent_chip_is_system 05:07 spare 08 pb_cfg_cent_hng_chk_disable 09 pb_cfg_cent_dbg_clr_max_hang_stage 10:11 spare 12:15 pb_cfg_cent_sw_ab_wait(0:3) 16:22 pb_cfg_cent_sp_hw_mark(0:6) 23:29 pb_cfg_cent_gp_hw_mark(0:6) 30:35 pb_cfg_cent_lcl_hw_mark(0:5) 36:41 pb_cfg_cent_cpu_ratio_override(0:5) 42:56 spare 57 pb_cfg_cent_req_gather_enable 58 spare 59 pb_cfg_cent_switch_option_ab 60:62 spare 63 pb_cfg_cent_reset_error_capture

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1:3	ROX	Reserved.
4	RWX	PB_CFG_CHIP_IS_SYSTEM: Configures whether there are other POWER9s in the system.
5:7	RW	Reserved.
8	RWX	PB_CFG_HNG_CHK_DISABLE: Hang Check Disable.
9	RWX	PB_DBG_CLR_MAX_HANG_STAGE: Resets the maximum hang state level (pb_hang_level).
10:11	RW	Reserved.
12:15	RWX	PB_CFG_SW_AB_WAIT: Adds delay to tc_pb_switch_ab input from TPC during hot plug sequence.
16:22	RWX	PB_CFG_SP_HW_MARK: Configures the maximum system pumps an IO unit may issue.
23:29	RWX	PB_CFG_GP_HW_MARK: Configures the maximum group pumps this chip may issue.
30:35	RWX	PB_CFG_LCL_HW_MARK: Configures the maximum local pumps this chip may issue.
36:41	RWX	PB_CFG_CPU_RATIO_OVERRIDE: Overrides PBIEQ RCMD/cr rates. 000000 = Full Speed 000001 = 2nd highest 00001x = 3rd highest 0001xx = 4th highest 001xxx = 5th highest 01xxxx = 6th highest 1xxxxx = Slowest speed.
42:56	RW	Reserved.
57	RWX	PB_CFG_REQ_GATHER_ENABLE: Enable data OW gathering on all chiplet/link requests. {default = on}.
58	RW	PB_CFG_SWITCH_CD_PULSE: Controls switch_cd pulse width. Uses pb_cfg_sw_ab_wait to extend pulse. Default = long pulse. Requires pb_cfg_sw_ab_wait > cnt_5 for 6 cycle pulse.
59	RWX	PB_CFG_SWITCH_OPTION_AB: SCOM access to determine what signal drives pb_cfg_switch_cd. on = tc_pb_switch_ab, off = tc_pb_switch_cd.
60:62	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
63	RWX	PB_CFG_RESET_ERROR_CAPTURE: Reset CRESP error capture latches.

Register Name	Power Bus PB CENT HP Mode Next Register
Mnemonic	PB.COM.PB_CENT_HP_MODE_NEXT
Address	0000000005011C0B (SCOM)
Description	00 pb_cfg_cent_master_chip 01 pb_cfg_cent_tm_master 02 pb_cfg_cent_chg_rate_gp_master 03 pb_cfg_cent_chg_rate_sp_master 04 pb_cfg_cent_link_a0_en 05 pb_cfg_cent_link_a1_en 06 pb_cfg_cent_link_a2_en 07 pb_cfg_cent_link_a3_en 08 pb_cfg_cent_na0_addr_dis 09 pb_cfg_cent_na1_addr_dis 10 pb_cfg_cent_na2_addr_dis 11 pb_cfg_cent_na3_addr_dis 12:15 pb_cfg_cent_link_a0_groupid 16:19 pb_cfg_cent_link_a1_groupid 20:23 pb_cfg_cent_link_a2_groupid 24:27 pb_cfg_cent_link_a3_groupid 28 pb_cfg_cent_a_aggregate 29 pb_cfg_cent_hop_mode 30 pb_cfg_cent_smp_optics_mode 31 pb_cfg_cent_capi_mode 32:33 pb_cfg_cent_opt0_mode 34:35 pb_cfg_cent_opt1_mode 36:37 pb_cfg_cent_opt2_mode 38:39 pb_cfg_cent_opt3_mode 40:46 pb_cfg_cent_xlate_addr_to_id 47:48 spare 49 pb_cfg_cent_a_indirect_en 50 pb_cfg_cent_a_gather_enable 51 spare 52 pb_cfg_cent_phyp_is_group 53 pb_cfg_cent_addr_bar_mode 54 pb_cfg_cent_pump_mode 55 pb_cfg_cent_dcache_capp_mode 56:63 pb_cfg_cent_a_cmd_rate

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_NEXT: Processor bus master.
1	RWX	PB_CFG_TM_MASTER_NEXT: Configure Chip as PB TM Master.
2	RWX	PB_CFG_CHG_RATE_GP_MASTER_NEXT: Sets the group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt.
3	RWX	PB_CFG_CHG_RATE_SP_MASTER_NEXT: Sets the system pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt.
4	RWX	PB_CFG_LINK_A0_EN_NEXT: Link A0 enabled.
5	RWX	PB_CFG_LINK_A1_EN_NEXT: Link A1 enabled.
6	RWX	PB_CFG_LINK_A2_EN_NEXT: Link A2 enabled.
7	RWX	PB_CFG_LINK_A3_EN_NEXT: Link A3 enabled.
8	RWX	PB_CFG_LINK_NA0_ADDR_DIS_NEXT: Link A0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NA1_ADDR_DIS_NEXT: Link A1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NA2_ADDR_DIS_NEXT: Link A2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NA3_ADDR_DIS_NEXT: Link A3 address broadcast disabled.
12:15	RWX	PB_CFG_LINK_A0_GROUPID_NEXT: Group ID of chip connected to A0 link.
16:19	RWX	PB_CFG_LINK_A1_GROUPID_NEXT: Group ID of chip connected to A1 link.
20:23	RWX	PB_CFG_LINK_A2_GROUPID_NEXT: Group ID of chip connected to A2 link.
24:27	RWX	PB_CFG_LINK_A3_GROUPID_NEXT: Group ID of chip connected to A3 link.
28	RWX	PB_CFG_A_AGGREGATE_NEXT: Processor bus A links are configured as parallel buses to same chip.
29	RWX	PB_CFG_HOP_MODE_NEXT: Sets SMP hop mode. 0 = 1-hop or 2-hop SMP topology. 1 = 3-hop SMP topology.
30	RWX	PB_CFG_SMP_OPTICS_MODE_NEXT: Sets SMP optics mode. 0 = Optic Links are configured as X-bus SMP protocol. 1 = Optic Links are configured as A-bus SMP protocol.
31	RWX	PB_CFG_CAPI_MODE_NEXT: Indicates a CAPI 2.0 link is attached in the SMP system.
32:33	RWX	PB_CFG_OPT0_MODE_NEXT: Optical Link 0 configuration.

Bits	SCOM	Field Mnemonic: Description
34:35	RWX	PB_CFG_OPT1_MODE_NEXT: Optical Link 1 configuration.
36:37	RWX	PB_CFG_OPT2_MODE_NEXT: Optical Link 2 configuration.
38:39	RWX	PB_CFG_OPT3_MODE_NEXT: Optical Link 3 configuration.
40:46	RWX	PB_CFG_XLATE_ADDR_TO_ID_CENT_NEXT: Configures the translation of the address to topology ID XOR mask.
47:48	RW	Reserved.
49	RWX	Reserved.
50	RWX	PB_CFG_A_GATHER_ENABLE_NEXT: Enable data OW gathering on A links.
51	RW	Reserved.
52	RWX	PB_CFG_PHYP_IS_GROUP_NEXT: Configures phyp boundary. 0 = phyp_is_system. 1 = phyp_is_group.
53	RWX	PB_CFG_ADDR_BAR_MODE_NEXT: Address BAR Mode. The SMP is limited to 2 or 4 sockets. When 1, pb_cfg_pump_mode must also be set to 1.
54	RWX	PB_CFG_PUMP_MODE_NEXT: Configures the physical broadcast. 0 = Chip_is_node (Default). 1 = Chip_is_group.
55	RWX	PB_CFG_DCACHE_CAPP_MODE_NEXT: Dcache CAPP mode. 0 = off (Default). 1 = on.
56:63	RWX	PB_CFG_A_CMD_RATE_CENT_NEXT: configures the paced command rate to not overrun the A link.

Register Name	Power Bus PB CENT HP Mode Current Register
Mnemonic	PB.COM.PB_CENT_HP_MODE_CURR
Address	0000000005011C0C (SCOM)
Description	00 pb_cfg_cent_master_chip 01 pb_cfg_cent_tm_master 02 pb_cfg_cent_chg_rate_gp_master 03 pb_cfg_cent_chg_rate_sp_master 04 pb_cfg_cent_link_a0_en 05 pb_cfg_cent_link_a1_en 06 pb_cfg_cent_link_a2_en 07 pb_cfg_cent_link_a3_en 08 pb_cfg_cent_na0_addr_dis 09 pb_cfg_cent_na1_addr_dis 10 pb_cfg_cent_na2_addr_dis 11 pb_cfg_cent_na3_addr_dis 12:15 pb_cfg_cent_link_a0_groupid 16:19 pb_cfg_cent_link_a1_groupid 20:23 pb_cfg_cent_link_a2_groupid 24:27 pb_cfg_cent_link_a3_groupid 28 pb_cfg_cent_a_aggregate 29 pb_cfg_cent_hop_mode 30 pb_cfg_cent_smp_optics_mode 31 pb_cfg_cent_capi_mode 32:33 pb_cfg_cent_opt0_mode 34:35 pb_cfg_cent_opt1_mode 36:37 pb_cfg_cent_opt2_mode 38:39 pb_cfg_cent_opt3_mode 40:46 pb_cfg_cent_xlate_addr_to_id 47:48 spare 49 pb_cfg_cent_a_indirect_en 50 pb_cfg_cent_a_gather_enable 51 spare 52 pb_cfg_cent_phyp_is_group 53 pb_cfg_cent_addr_bar_mode 54 pb_cfg_cent_pump_mode 55 pb_cfg_cent_dcache_capp_mode 56:63 pb_cfg_cent_a_cmd_rate

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_CURR: Processor bus master.
1	RWX	PB_CFG_TM_MASTER_CURR: configure Chip as PB TM Master.
2	RWX	PB_CFG_CHG_RATE_GP_MASTER_CURR: Sets the Group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt.
3	RWX	PB_CFG_CHG_RATE_SP_MASTER_CURR: Sets the System pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt.
4	RWX	PB_CFG_LINK_A0_EN_CURR: Link A0 enabled.
5	RWX	PB_CFG_LINK_A1_EN_CURR: Link A1 enabled.
6	RWX	PB_CFG_LINK_A2_EN_CURR: Link A2 enabled.
7	RWX	PB_CFG_LINK_A3_EN_CURR: Link A3 enabled.

Bits	SCOM	Field Mnemonic: Description
8	RWX	PB_CFG_LINK_NA0_ADDR_DIS_CURR: Link A0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NA1_ADDR_DIS_CURR: Link A1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NA2_ADDR_DIS_CURR: Link A2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NA3_ADDR_DIS_CURR: Link A3 address broadcast disabled.
12:15	RWX	PB_CFG_LINK_A0_GROUPID_CURR: Group ID of chip connected to A0 link.
16:19	RWX	PB_CFG_LINK_A1_GROUPID_CURR: Group ID of chip connected to A1 link.
20:23	RWX	PB_CFG_LINK_A2_GROUPID_CURR: Group ID of chip connected to A2 link.
24:27	RWX	PB_CFG_LINK_A3_GROUPID_CURR: Group ID of chip connected to A3 link.
28	RWX	PB_CFG_A_AGGREGATE_CURR: Processor bus A links are configured as parallel buses to same chip.
29	RWX	PB_CFG_HOP_MODE_CURR: Sets SMP hop mode. 0 = 1-hop or 2-hop SMP topology. 1 = 3-hop SMP topology.
30	RWX	PB_CFG_SMP_OPTICS_MODE_CURR: Sets SMP optics mode. 0 = Optic Links are configured as X-bus SMP protocol. 1 = Optic Links are configured as A-bus SMP protocol.
31	RWX	PB_CFG_CAPI_MODE_CURR: Indicates a CAPI 2.0 link is attached in the SMP system.
32:33	RWX	PB_CFG_OPT0_MODE_CURR: Optical Link 0 configuration.
34:35	RWX	PB_CFG_OPT1_MODE_CURR: Optical Link 1 configuration.
36:37	RWX	PB_CFG_OPT2_MODE_CURR: Optical Link 2 configuration.
38:39	RWX	PB_CFG_OPT3_MODE_CURR: Optical Link 3 configuration.
40:46	RWX	PB_CFG_XLATE_ADDR_TO_ID_CENT_CURR: configures the translation of address to topology ID XOR mask.
47:48	RW	Reserved.
49	RWX	Reserved.
50	RWX	PB_CFG_A_GATHER_ENABLE_CURR: Enable data OW gathering on A links.
51	RW	Reserved.
52	RWX	PB_CFG_PHYP_IS_GROUP_CURR: configures phyp boundary. 0 = phyp_is_system, 1 = phyp_is_group.
53	RWX	PB_CFG_ADDR_BAR_MODE_CURR: Address BAR Mode. The SMP is limited to 2 or 4 sockets. When 1, pb_cfg_pump_mode must also be set to 1.
54	RWX	PB_CFG_PUMP_MODE_CURR: configures the physical broadcast. 0 = Chip_is_node (Default). 1 = Chip_is_group.
55	RWX	PB_CFG_DCACHE_CAPP_MODE_CURR: Dcache CAPP mode. 0 = off (Default). 1 = on.
56:63	RWX	PB_CFG_A_CMD_RATE_CENT_CURR: configures the paced command rate to not overrun the A link.

Register Name	Power Bus PB CENT HPA Mode Next Register
Mnemonic	PB.COM.PB_CENT_HPA_MODE_NEXT
Address	0000000005011C0D (SCOM)
Description	00 pb_cfg_cent_link_x0toa0_en 01 pb_cfg_cent_link_x0toa1_en 02 pb_cfg_cent_link_x0toa2_en 03 pb_cfg_cent_link_x0toa3_en 04 pb_cfg_cent_link_x1toa0_en 05 pb_cfg_cent_link_x1toa1_en 06 pb_cfg_cent_link_x1toa2_en 07 pb_cfg_cent_link_x1toa3_en 08 pb_cfg_cent_link_x2toa0_en 09 pb_cfg_cent_link_x2toa1_en 10 pb_cfg_cent_link_x2toa2_en 11 pb_cfg_cent_link_x2toa3_en 12:15 spare 16:19 pb_cfg_cent_link_x0toa0_groupid 20:23 pb_cfg_cent_link_x0toa1_groupid 24:27 pb_cfg_cent_link_x0toa2_groupid 28:31 pb_cfg_cent_link_x0toa3_groupid 32:35 pb_cfg_cent_link_x1toa0_groupid 36:39 pb_cfg_cent_link_x1toa1_groupid 40:43 pb_cfg_cent_link_x1toa2_groupid 44:47 pb_cfg_cent_link_x1toa3_groupid 48:51 pb_cfg_cent_link_x2toa0_groupid 52:55 pb_cfg_cent_link_x2toa1_groupid 56:59 pb_cfg_cent_link_x2toa2_groupid 60:63 pb_cfg_cent_link_x2toa3_groupid

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved.
1	RWX	Reserved.
2	RWX	Reserved.
3	RWX	Reserved.
4	RWX	Reserved.
5	RWX	Reserved.
6	RWX	Reserved.
7	RWX	Reserved.
8	RWX	Reserved.
9	RWX	Reserved.
10	RWX	Reserved.
11	RWX	Reserved.
12:15	RW	Reserved.
16:19	RWX	Reserved.
20:23	RWX	Reserved.
24:27	RWX	Reserved.
28:31	RWX	Reserved.
32:35	RWX	Reserved.
36:39	RWX	Reserved.
40:43	RWX	Reserved.
44:47	RWX	Reserved.
48:51	RWX	Reserved.
52:55	RWX	Reserved.
56:59	RWX	Reserved.
60:63	RWX	Reserved.

Register Name	**Power Bus PB CENT HPA Mode Current Register**
Mnemonic	PB.COM.PB_CENT_HPA_MODE_CURR
Address	0000000005011C0E (SCOM)
Description	00 pb_cfg_cent_link_x0toa0_en 01 pb_cfg_cent_link_x0toa1_en 02 pb_cfg_cent_link_x0toa2_en 03 pb_cfg_cent_link_x0toa3_en 04 pb_cfg_cent_link_x1toa0_en 05 pb_cfg_cent_link_x1toa1_en 06 pb_cfg_cent_link_x1toa2_en 07 pb_cfg_cent_link_x1toa3_en 08 pb_cfg_cent_link_x2toa0_en 09 pb_cfg_cent_link_x2toa1_en 10 pb_cfg_cent_link_x2toa2_en 11 pb_cfg_cent_link_x2toa3_en 12:15 spare 16:19 pb_cfg_cent_link_x0toa0_groupid 20:23 pb_cfg_cent_link_x0toa1_groupid 24:27 pb_cfg_cent_link_x0toa2_groupid 28:31 pb_cfg_cent_link_x0toa3_groupid 32:35 pb_cfg_cent_link_x1toa0_groupid 36:39 pb_cfg_cent_link_x1toa1_groupid 40:43 pb_cfg_cent_link_x1toa2_groupid 44:47 pb_cfg_cent_link_x1toa3_groupid 48:51 pb_cfg_cent_link_x2toa0_groupid 52:55 pb_cfg_cent_link_x2toa1_groupid 56:59 pb_cfg_cent_link_x2toa2_groupid 60:63 pb_cfg_cent_link_x2toa3_groupid

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved.
1	RWX	Reserved.
2	RWX	Reserved.
3	RWX	Reserved.
4	RWX	Reserved.
5	RWX	Reserved.
6	RWX	Reserved.
7	RWX	Reserved.
8	RWX	Reserved.
9	RWX	Reserved.
10	RWX	Reserved.
11	RWX	Reserved.
12:15	RW	Reserved.
16:19	RWX	Reserved.
20:23	RWX	Reserved.
24:27	RWX	Reserved.
28:31	RWX	Reserved.
32:35	RWX	Reserved.
36:39	RWX	Reserved.
40:43	RWX	Reserved.
44:47	RWX	Reserved.
48:51	RWX	Reserved.
52:55	RWX	Reserved.
56:59	RWX	Reserved.
60:63	RWX	Reserved.

Register Name	Power Bus PB CENT HPX Mode Next Register
Mnemonic	PB.COM.PB_CENT_HPX_MODE_NEXT
Address	0000000005011C0F (SCOM)
Description	00 pb_cfg_cent_link_x0_en 01 pb_cfg_cent_link_x1_en 02 pb_cfg_cent_link_x2_en 03 pb_cfg_cent_link_x3_en 04 pb_cfg_cent_link_x4_en 05 pb_cfg_cent_link_x5_en 06 pb_cfg_cent_link_x6_en 07 spare 08 pb_cfg_cent_nx0_addr_dis 09 pb_cfg_cent_nx1_addr_dis 10 pb_cfg_cent_nx2_addr_dis 11 pb_cfg_cent_nx3_addr_dis 12 pb_cfg_cent_nx4_addr_dis 13 pb_cfg_cent_nx5_addr_dis 14 pb_cfg_cent_nx6_addr_dis 15 spare 16:18 pb_cfg_cent_link_x0_id(0:2) 19:21 pb_cfg_cent_link_x1_id(0:2) 22:24 pb_cfg_cent_link_x2_id(0:2) 25:27 pb_cfg_cent_link_x3_id(0:2) 28:30 pb_cfg_cent_link_x4_id(0:2) 31:33 pb_cfg_cent_link_x5_id(0:2) 34:36 pb_cfg_cent_link_x6_id(0:2) 37 pb_cfg_cent_x_aggregate 38:48 spare 49 pb_cfg_cent_x_indirect_en 50 pb_cfg_cent_x_gather_enable 51:55 spare 56:63 pb_cfg_cent_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_NEXT: Link X0 enabled.
1	RWX	PB_CFG_LINK_X1_EN_NEXT: Link X1 enabled.
2	RWX	PB_CFG_LINK_X2_EN_NEXT: Link X2 enabled.
3	RWX	PB_CFG_LINK_X3_EN_NEXT: Link X3 enabled.
4	RWX	PB_CFG_LINK_X4_EN_NEXT: Link X4 enabled.
5	RWX	PB_CFG_LINK_X5_EN_NEXT: Link X5 enabled.
6	RWX	PB_CFG_LINK_X6_EN_NEXT: Link X6 enabled.
7	RW	Reserved.
8	RWX	PB_CFG_LINK_NX0_ADDR_DIS_NEXT: Link X0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NX1_ADDR_DIS_NEXT: Link X1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NX2_ADDR_DIS_NEXT: Link X2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NX3_ADDR_DIS_NEXT: Link X3 address broadcast disabled.
12	RWX	PB_CFG_LINK_NX4_ADDR_DIS_NEXT: Link X4 address broadcast disabled.
13	RWX	PB_CFG_LINK_NX5_ADDR_DIS_NEXT: Link X5 address broadcast disabled.
14	RWX	PB_CFG_LINK_NX6_ADDR_DIS_NEXT: Link X6 address broadcast disabled.
15	RW	Reserved.
16:18	RWX	PB_CFG_LINK_X0_CHIPID_NEXT: Chip ID of chip connected to X0 link.
19:21	RWX	PB_CFG_LINK_X1_CHIPID_NEXT: Chip ID of chip connected to X1 link.
22:24	RWX	PB_CFG_LINK_X2_CHIPID_NEXT: Chip ID of chip connected to X2 link.
25:27	RWX	PB_CFG_LINK_X3_CHIPID_NEXT: Chip ID of chip connected to X3 link.
28:30	RWX	PB_CFG_LINK_X4_CHIPID_NEXT: Chip ID of chip connected to X4 link.
31:33	RWX	PB_CFG_LINK_X5_CHIPID_NEXT: Chip ID of chip connected to X5 link.
34:36	RWX	PB_CFG_LINK_X6_CHIPID_NEXT: Chip ID of chip connected to X6 link.
37	RWX	PB_CFG_X_AGGREGATE_NEXT: Processor bus X links are configured as parallel buses to same chip.
38:47	RW	Reserved.
48	RW	PB_CFG_X_FP_DISABLED_NEXT: Processor bus X link RTAG fastpath disable.
49	RWX	PB_CFG_X_INDIRECT_EN_NEXT: Processor bus X links are configured for indirect data routing.
50	RWX	PB_CFG_X_GATHER_ENABLE_NEXT: Enable data OW gathering on X links.
51:55	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
56:63	RWX	PB_CFG_X_CMD_RATE_CENT_NEXT: configures the paced command rate to not overrun the X link.

Register Name	Power Bus PB CENT HPX Mode Current Register
Mnemonic	PB.COM.PB_CENT_HPX_MODE_CURR
Address	0000000005011C10 (SCOM)
Description	00 pb_cfg_cent_link_x0_en 01 pb_cfg_cent_link_x1_en 02 pb_cfg_cent_link_x2_en 03 pb_cfg_cent_link_x3_en 04 pb_cfg_cent_link_x4_en 05 pb_cfg_cent_link_x5_en 06 pb_cfg_cent_link_x6_en 07 spare 08 pb_cfg_cent_nx0_addr_dis 09 pb_cfg_cent_nx1_addr_dis 10 pb_cfg_cent_nx2_addr_dis 11 pb_cfg_cent_nx3_addr_dis 12 pb_cfg_cent_nx4_addr_dis 13 pb_cfg_cent_nx5_addr_dis 14 pb_cfg_cent_nx6_addr_dis 15 spare 16:18 pb_cfg_cent_link_x0_id(0:2) 19:21 pb_cfg_cent_link_x1_id(0:2) 22:24 pb_cfg_cent_link_x2_id(0:2) 25:27 pb_cfg_cent_link_x3_id(0:2) 28:30 pb_cfg_cent_link_x4_id(0:2) 31:33 pb_cfg_cent_link_x5_id(0:2) 34:36 pb_cfg_cent_link_x6_id(0:2) 37 pb_cfg_cent_x_aggregate 38:48 spare 49 pb_cfg_cent_x_indirect_en 50 pb_cfg_cent_x_gather_enable 51:55 spare 56:63 pb_cfg_cent_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_CURR: Link X0 enabled.
1	RWX	PB_CFG_LINK_X1_EN_CURR: Link X1 enabled.
2	RWX	PB_CFG_LINK_X2_EN_CURR: Link X2 enabled.
3	RWX	PB_CFG_LINK_X3_EN_CURR: Link X3 enabled.
4	RWX	PB_CFG_LINK_X4_EN_CURR: Link X4 enabled.
5	RWX	PB_CFG_LINK_X5_EN_CURR: Link X5 enabled.
6	RWX	PB_CFG_LINK_X6_EN_CURR: Link X6 enabled.
7	RW	Reserved.
8	RWX	PB_CFG_LINK_NX0_ADDR_DIS_CURR: Link X0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NX1_ADDR_DIS_CURR: Link X1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NX2_ADDR_DIS_CURR: Link X2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NX3_ADDR_DIS_CURR: Link X3 address broadcast disabled.
12	RWX	PB_CFG_LINK_NX4_ADDR_DIS_CURR: Link X4 address broadcast disabled.
13	RWX	PB_CFG_LINK_NX5_ADDR_DIS_CURR: Link X5 address broadcast disabled.
14	RWX	PB_CFG_LINK_NX6_ADDR_DIS_CURR: Link X6 address broadcast disabled.
15	RW	Reserved.
16:18	RWX	PB_CFG_LINK_X0_CHIPID_CURR: Chip ID of chip connected to X0 link.
19:21	RWX	PB_CFG_LINK_X1_CHIPID_CURR: Chip ID of chip connected to X1 link.
22:24	RWX	PB_CFG_LINK_X2_CHIPID_CURR: Chip ID of chip connected to X2 link.
25:27	RWX	PB_CFG_LINK_X3_CHIPID_CURR: Chip ID of chip connected to X3 link.
28:30	RWX	PB_CFG_LINK_X4_CHIPID_CURR: Chip ID of chip connected to X4 link.
31:33	RWX	PB_CFG_LINK_X5_CHIPID_CURR: Chip ID of chip connected to X5 link.
34:36	RWX	PB_CFG_LINK_X6_CHIPID_CURR: Chip ID of chip connected to X6 link.
37	RWX	PB_CFG_X_AGGREGATE_CURR: Processor bus X links are configured as parallel buses to same chip.
38:47	RW	Reserved.
48	RW	PB_CFG_X_FP_DISABLED_CURR: Processor bus X link RTAG fastpath disable.

Bits	SCOM	Field Mnemonic: Description
49	RWX	PB_CFG_X_INDIRECT_EN_CURR: Processor bus X links are configured for indirect data routing.
50	RWX	PB_CFG_X_GATHER_ENABLE_CURR: Enable data OW gathering on X links.
51:55	RW	Reserved.
56:63	RWX	PB_CFG_X_CMD_RATE_CENT_CURR: configures the paced command rate to not overrun the X link.

Register Name	Power Bus PB CENT Serial Configuration Load Register
Mnemonic	PB.COM.PB_CENT_SCONFIG_LOAD
Address	0000000005011C11 (SCOM)
Description	00 = pb_cfg_sconfig_load 01 = pb_cfg_sconfig_slow 02:07 = pb_cfg_sconfig_shift_count 08:11 = pb_cfg_sconfig_select 12:63 = pb_cfg_sconfig_shift_data

Bits	SCOM	Field Mnemonic: Description
0	WOX	PB_CFG_CENT_SCONFIG_LOAD: Load Serial Mode Registers.
1	RWX	PB_CFG_CENT_SCONFIG_SLOW: Set Load of Serial Mode Registers to 16:1 slow clock.
2:7	WOX	PB_CFG_CENT_SCONFIG_SHIFT_COUNT: Configures length of Serial Mode Register.
8:11	RWX	PB_CFG_CENT_SCONFIG_SELECT: Select Serial Mode register 0000 = pbh_pbien 0001 = pbh_pbies 0010 = pbh_dat_ex_req_pmac 0011 = pbh_dat_arb_enes_pmac 01xx = pbh_cmd_snooper_pmac,
12:63	RWX	PB_CFG_CENT_SCONFIG_SHIFT_DATA: Serial Mode Register Data.

Register Name	Power Bus PB CENT Trace Configuration Register
Mnemonic	PB.COM.PB_CENT_TRACE
Address	0000000005011C12 (SCOM)
Description	00:01 pb_cfg_trace_selsn0(0:1) 02:03 pb_cfg_trace_selsn1(0:1) 04:05 pb_cfg_trace_selsn2(0:1) 06:07 pb_cfg_trace_selsn3(0:1) 08:09 pb_cfg_trace_selcr0(0:1) 10:11 pb_cfg_trace_selcr1(0:1) 12:13 pb_cfg_trace_selcr2(0:1) 14:15 pb_cfg_trace_selcr3(0:1) 16:17 pb_cfg_trace_pbien_dbg_0(0:1) 18:19 pb_cfg_trace_pbien_dbg_1(0:1) 20:21 pb_cfg_trace_pbies_dbg_0(0:1) 22:23 pb_cfg_trace_pbies_dbg_1(0:1) 24:25 pb_cfg_trace_pbiot_dbg_0(0:1) 26:27 pb_cfg_trace_pbiot_dbg_1(0:1) 28 pb_cfg_trace_pbiot_dbg 29:31 pb_cfg_trace_selrt(0:2) 32 Enable perftrace mode and enable the perftrace trigger function to send a trigger to EH, EN and ES. (trigger can be ignored at the trace arrays) 33 1 = perftrace trigger has fired. Resets to 0 when the PMU counter is reset. Can also be written to 1 to induce a trigger. 34:35 Perftrace counter select. PMU_group0_counter# will be compared against the pb_cfg_perftrace_counter_match field to generate a perftrace trigger. 36:51 Perftrace counter match. When the selected counter matches these bits, a perftrace trigger is generated. 52 Enable_perftrace_prescale - wide-angle view - perfcounts are prescaled by 128 53 perftrace fixed window mode - take a perftrace sample every 255 or 255x128 cycles 54 0 = event_bus(8:11) routed to perftrace counters 0:3. 1 = event_bus(12:15) routed to perftrace counters 0:3 55 0 = event_bus(16:19) routed to perftrace counters 4:7. 1 = event_bus(20:23) routed to perftrace counters 4:7 56:63 spare

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PB_CFG_TRACE_SELSN0: configures PB Trace SN0 inputs; 10 = RCMD0{por} 01 = lcl_pr0+pbien0 00 = none.

Bits	SCOM	Field Mnemonic: Description
2:3	RW	PB_CFG_TRACE_SELSN1: configures PB Trace SN1 inputs 10 = RCMD1{por} 01 = lcl_pr1+pbien1 00 = none.
4:5	RW	PB_CFG_TRACE_SELSN2: configures PB Trace SN2 inputs 10 = RCMD2{por} 01 = lcl_pr2+pbies0 00 = none.
6:7	RW	PB_CFG_TRACE_SELSN3: configures PB Trace SN3 inputs 10 = RCMD3{por} 01 = lcl_pr3+pbies0 11 = lcl_pr3+pbies1/pbiot 00 = none.
8:9	RW	PB_CFG_TRACE_SELCR0: configures PB Trace CR0 inputs 10 = crsp0{por} 01 = pr0/ecr0 00 = none.
10:11	RW	PB_CFG_TRACE_SELCR1: configures PB Trace CR1 inputs; 10 = crsp1{por}, 01 = pr1/ecr1, 00 = none.
12:13	RW	PB_CFG_TRACE_SELCR2: configures PB Trace CR2 inputs 10 = crsp2{por} 01 = pr2/ecr2 00 = none.
14:15	RW	PB_CFG_TRACE_SELCR3: configures PB Trace CR3 inputs 10 = crsp3{por} 01 = pr3/ecr3, 00 = none.
16:17	RW	PB_CFG_TRACE_PBIEN_DBG_0_SEL: configures PB Trace PBIEN DBG0 inputs 00 = doff_x0 01 = doff_x1 10 = don_x0 11 = don_x1.
18:19	RW	PB_CFG_TRACE_PBIEN_DBG_1_SEL: configures PB Trace PBIEN DBG1 inputs 00 = doff_x2 01 = doff_nxcxa0 10 = don_x2 11 = don_nxcxa0.
20:21	RW	PB_CFG_TRACE_PBIES_DBG_0_SEL: configures PB Trace PBIES DBG0 inputs 00 = doff_pe0 01 = doff_pe1 10 = don_pe0 11 = don_pe1.
22:23	RW	PB_CFG_TRACE_PBIES_DBG_1_SEL: configures PB Trace PBIES DBG1 inputs 00 = doff_pe2 01 = doff_cxa1 10 = don_pe2 11 = don_cxa1.
24:25	RW	PB_CFG_TRACE_PBIOT_DBG_0_SEL: configures PB Trace PBIOT DBG0 inputs 00 = doff_o0 01 = doff_o1 10 = don_o0 11 = don_o1.

Bits	SCOM	Field Mnemonic: Description
26:27	RW	PB_CFG_TRACE_PBIOT_DBG_1_SEL: configures PB Trace PBIOT DBG1 inputs 00 = doff_o2 01 = doff_o3vas 10 = don_o2 11 = don_o3vas.
28	RW	PB_CFG_TRACE_PBIOT_SEL: configures PB Trace PBIOT inputs off = dbg0 on = dbg1.
29:31	RW	PB_CFG_TRACE_SELRT: configures PB Trace RTAG inputs.
32	RW	PB_CFG_PERFTRACE_EN: Enable the perftrace trigger function to send a trigger to EN and ES.
33	RW	PB_CFG_PERFTRACE_TRIG: 1 = perftrace trigger has fired. Resets to 0 when the PMU counter is reset. Can also be written to 1 to induce a trigger.
34:35	RW	PB_CFG_PERFTRACE_COUNTER_SEL: Perftrace counter select. PMU_group0_counter# will be compared against the pb_cfg_perftrace_counter_match field to generate a perftrace trigger.
36:51	RW	PB_CFG_PERFTRACE_COUNTER_MATCH: Perftrace counter match. When the selected counter matches these bits, a perftrace trigger is generated.
52	RW	PB_CFG_ENABLE_PERFTRACE_PRESCALE: Enable_perftrace_prescale - wide-angle view - perfcounts are prescaled by 128.
53	RW	PB_CFG_ENABLE_PERFTRACE_FIXED_WIN: perftrace fixed window mode - take a perftrace sample every 255 or 255x128 cycles.
54	RW	PB_CFG_PERFTRACE_GRP1_SEL: 0 = event_bus(8:11) routed to pertrace counters 0:3. 1 = event_bus(12:15) routed to pertrace counters 0:3.
55	RW	PB_CFG_PERFTRACE_GRP2_SEL: 0 = event_bus(16:19) routed to pertrace counters 4:7. 1 = event_bus(20:23) routed to pertrace counters 4:7.
56:63	RW	Reserved.

Register Name	**Power Bus PB CENT CNPME Register**
Mnemonic	PB.COM.PB_CENT_CNPME
Address	0000000005011C13 (SCOM)
Description	00 = pb_cfg_cnpme_en 01 = pb_cfg_cnpme_reset_mode 02 = pb_cfg_cnpme_counter_mode 03 = pb_cfg_cnpme_global_pmisc_dis 04 = pb_cfg_cnpme_global_pmisc_mode 05 = pb_cfg_cnpme_external_freeze 06:07 = pb_cfg_cnpme_op_0 08:09 = pb_cfg_cnpme_op_1 10:11 = pb_cfg_cnpme_op_2 12:13 = pb_cfg_cnpme_op_3 14:15 = pb_cfg_cnpme_op_4 16:17 = pb_cfg_cnpme_op_5 18:19 = pb_cfg_cnpme_op_6 20:21 = pb_cfg_cnpme_op_7 22:23 = pb_cfg_cnpme_op_8 24:25 = pb_cfg_cnpme_op_9 26:27 = pb_cfg_cnpme_op_10 28:29 = pb_cfg_cnpme_op_11 30:31 = pb_cfg_cnpme_op_12 32:33 = pb_cfg_cnpme_op_13 34:35 = pb_cfg_cnpme_op_14 36:37 = pb_cfg_cnpme_op_15 38:40 = pb_cfg_cnpme_cascade_pmulet0 41:43 = pb_cfg_cnpme_cascade_pmulet1 44:46 = pb_cfg_cnpme_cascade_pmulet2 47:49 = pb_cfg_cnpme_cascade_pmulet3 50:60 = pb_cfg_cnpme_mask 61:63 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_CNPME_EN: Enable CNPME Performance Monitor. Default = 0.
1	RWX	PB_CFG_CNPME_RESET_MODE: Performance Monitor Reset Mode 0 = reset_on_rd. 1 = reset_on_wr. Default = 0.

Bits	SCOM	Field Mnemonic: Description
2	RWX	PB_CFG_CNPME_COUNTER_MODE: 0 = freeze on counter maximum. 1 = Free running. default = 0.
3	RWX	PB_CFG_CNPME_GLOBAL_PMISC_DIS: Disable Global PMU PMISC operation. Default = 0.
4	RWX	PB_CFG_CNPME_GLOBAL_PMISC_MODE: Configure Global PMU PMISC operation. 0 = level {L = pause, H = run} 1 = level w/reset 0->1 default = 0.
5	RWX	PB_CFG_CNPME_EXTERNAL_FREEZE: External Freeze Enable. 0 = Disable external freeze. 1 = Enable external freeze. default = 0.
6:7	RWX	PB_CFG_CNPME_0_1_OP: Performance Monitor Bit 0/1 Select. 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
8:9	RWX	PB_CFG_CNPME_2_3_OP: Performance Monitor Bit 2/3 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
10:11	RWX	PB_CFG_CNPME_4_5_OP: Performance Monitor Bit 4/5 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
12:13	RWX	PB_CFG_CNPME_6_7_OP: Performance Monitor Bit 6/7 Select 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles.
14:15	RWX	PB_CFG_CNPME_8_9_OP: Performance Monitor Bit 8/9 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
16:17	RWX	PB_CFG_CNPME_10_11_OP: Performance Monitor Bit 10/11 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
18:19	RWX	PB_CFG_CNPME_12_13_OP: Performance Monitor Bit 12/13 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
20:21	RWX	PB_CFG_CNPME_14_15_OP: Performance Monitor Bit 14/15 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.

Bits	SCOM	Field Mnemonic: Description
22:23	RWX	PB_CFG_CNPME_16_17_OP: Performance Monitor Bit 16/17 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
24:25	RWX	PB_CFG_CNPME_18_19_OP: Performance Monitor Bit 18/19 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
26:27	RWX	PB_CFG_CNPME_20_21_OP: Performance Monitor Bit 20/21 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
28:29	RWX	PB_CFG_CNPME_22_23_OP: Performance Monitor Bit 22/23 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
30:31	RWX	PB_CFG_CNPME_24_25_OP: Performance Monitor Bit 24/25 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
32:33	RWX	PB_CFG_CNPME_26_27_OP: Performance Monitor Bit 26/27 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
34:35	RWX	PB_CFG_CNPME_28_29_OP: Performance Monitor Bit 28/29 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
36:37	RWX	PB_CFG_CNPME_30_31_OP: Performance Monitor Bit 30/31 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
38:40	RWX	PB_CFG_CNPME_CASCADE_PMU0: PMU0 cascade counters.
41:43	RWX	PB_CFG_CNPME_CASCADE_PMU1: PMU1 cascade counters.
44:46	RWX	PB_CFG_CNPME_CASCADE_PMU2: PMU0 cascade counters.
47:49	RWX	PB_CFG_CNPME_CASCADE_PMU3: PMU3 cascade counters.
50	RWX	PB_CFG_CNPME_PB_MASK: PB unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
51	RWX	PB_CFG_CNPME_MC2_MCS0_MASK: MC2 MCS0 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
52	RWX	PB_CFG_CNPME_MC2_MCS1_MASK: MC2 MCS1 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
53	RWX	PB_CFG_CNPME_MC3_MCS0_MASK: MC3 MCS0 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.

Bits	SCOM	Field Mnemonic: Description
54	RWX	PB_CFG_CNPME_MC3_MCS1_MASK: MC3 MCS1 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
55	RWX	Reserved.
56	RWX	PB_CFG_CNPME_MCD_MASK: MCD unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
57	RWX	PB_CFG_CNPME_PE0_MASK: PE0 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
58	RWX	PB_CFG_CNPME_PE1_MASK: PE1 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
59	RWX	PB_CFG_CNPME_PE2_MASK: PE2 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
60	RWX	PB_CFG_CNPME_VAS_MASK: VAS unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
61:63	RW	Reserved.

Register Name	Power Bus PB CENT CNPMW Register
Mnemonic	PB.COM.PB_CENT_CNPMW
Address	0000000005011C14 (SCOM)
Description	00 = pb_cfg_cnpmw_en 01 = pb_cfg_cnpmw_reset_mode 02 = pb_cfg_cnpmw_counter_mode 03 = pb_cfg_cnpmw_global_pmisc_dis 04 = pb_cfg_cnpmw_global_pmisc_mode 05 = pb_cfg_cnpmw_external_freeze 06:07 = pb_cfg_cnpmw_op_0 08:09 = pb_cfg_cnpmw_op_1 10:11 = pb_cfg_cnpmw_op_2 12:13 = pb_cfg_cnpmw_op_3 14:15 = pb_cfg_cnpmw_op_4 16:17 = pb_cfg_cnpmw_op_5 18:19 = pb_cfg_cnpmw_op_6 20:21 = pb_cfg_cnpmw_op_7 22:23 = pb_cfg_cnpmw_op_8 24:25 = pb_cfg_cnpmw_op_9 26:27 = pb_cfg_cnpmw_op_10 28:29 = pb_cfg_cnpmw_op_11 30:31 = pb_cfg_cnpmw_op_12 32:33 = pb_cfg_cnpmw_op_13 34:35 = pb_cfg_cnpmw_op_14 36:37 = pb_cfg_cnpmw_op_15 38:40 = pb_cfg_cnpmw_cascade_pmulet0 41:43 = pb_cfg_cnpmw_cascade_pmulet1 44:46 = pb_cfg_cnpmw_cascade_pmulet2 47:49 = pb_cfg_cnpmw_cascade_pmulet3 50:60 = pb_cfg_cnpmw_mask 61:63 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_CNPMW_EN: Enable cnpmw Performance Monitor. default = 0.
1	RWX	PB_CFG_CNPMW_RESET_MODE: Performance Monitor Reset Mode 0 = reset_on_rd. 1 = reset_on_wr. default = 0.
2	RWX	PB_CFG_CNPMW_COUNTER_MODE: 0 = freeze on counter max 1 = Free running. default = 0.
3	RWX	PB_CFG_CNPMW_GLOBAL_PMISC_DIS: Disable Global PMU PMISC operation. default = 0.
4	RWX	PB_CFG_CNPMW_GLOBAL_PMISC_MODE: Configure Global PMU PMISC operation. 0 = level {L = pause, H = run} 1 = level w/reset 0->1 default = 0.
5	RWX	PB_CFG_CNPMW_EXTERNAL_FREEZE: External Freeze Enable. 0 = Disable external freeze. 1 = Enable external freeze. default = 0.

Bits	SCOM	Field Mnemonic: Description
6:7	RWX	PB_CFG_CNPMW_0_1_OP: Performance Monitor Bit 0/1 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
8:9	RWX	PB_CFG_CNPMW_2_3_OP: Performance Monitor Bit 2/3 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
10:11	RWX	PB_CFG_CNPMW_4_5_OP: Performance Monitor Bit 4/5 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
12:13	RWX	PB_CFG_CNPMW_6_7_OP: Performance Monitor Bit 6/7 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
14:15	RWX	PB_CFG_CNPMW_8_9_OP: Performance Monitor Bit 8/9 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
16:17	RWX	PB_CFG_CNPMW_10_11_OP: Performance Monitor Bit 10/11 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
18:19	RWX	PB_CFG_CNPMW_12_13_OP: Performance Monitor Bit 12/13 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
20:21	RWX	PB_CFG_CNPMW_14_15_OP: Performance Monitor Bit 14/15 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
22:23	RWX	PB_CFG_CNPMW_16_17_OP: Performance Monitor Bit 16/17 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
24:25	RWX	PB_CFG_CNPMW_18_19_OP: Performance Monitor Bit 18/19 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
26:27	RWX	PB_CFG_CNPMW_20_21_OP: Performance Monitor Bit 20/21 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.

Bits	SCOM	Field Mnemonic: Description
28:29	RWX	PB_CFG_CNPMW_22_23_OP: Performance Monitor Bit 22/23 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
30:31	RWX	PB_CFG_CNPMW_24_25_OP: Performance Monitor Bit 24/25 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
32:33	RWX	PB_CFG_CNPMW_26_27_OP: Performance Monitor Bit 26/27 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
34:35	RWX	PB_CFG_CNPMW_28_29_OP: Performance Monitor Bit 28/29 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
36:37	RWX	PB_CFG_CNPMW_30_31_OP: Performance Monitor Bit 30/31 Select 00 = sel_a. 01 = sel_b. 10 = add_ab. 11 = cycles.
38:40	RWX	PB_CFG_CNPMW_CASCADE_PMU0: PMU0 cascade counters.
41:43	RWX	PB_CFG_CNPMW_CASCADE_PMU1: PMU1 cascade counters.
44:46	RWX	PB_CFG_CNPMW_CASCADE_PMU2: PMU0 cascade counters.
47:49	RWX	PB_CFG_CNPMW_CASCADE_PMU3: PMU3 cascade counters.
50	RWX	PB_CFG_CNPMW_PB_MASK: PB unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
51	RWX	PB_CFG_CNPMW_MC0_MCS0_MASK: MC0 MCS0 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
52	RWX	PB_CFG_CNPMW_MC0_MCS1_MASK: MC0 MCS1 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
53	RWX	PB_CFG_CNPMW_MC1_MCS0_MASK: MC1 MCS0 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
54	RWX	PB_CFG_CNPMW_MC1_MCS1_MASK: MC1 MCS1 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
55	RWX	Reserved.
56	RWX	PB_CFG_CNPMW_INT_MASK: INT unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
57	RWX	PB_CFG_CNPMW_PE0_MASK: PE0 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
58	RWX	PB_CFG_CNPMW_PE1_MASK: PE1 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
59	RWX	PB_CFG_CNPMW_PE2_MASK: PE2 unit event bus mask. When set, unit event bus inputs are disabled. default = 0.
60	RWX	Reserved.

Bits	SCOM	Field Mnemonic: Description
61:63	RW	Reserved.

Register Name	Power Bus PB CENT PMU Prescaler Register
Mnemonic	PB.COM.PB_CENT_PMU_PRESCALER
Address	0000000005011C15 (SCOM)
Description	00 = pb_cfg_cnpme_prescaler_pmu0_c0 02:03 = pb_cfg_cnpme_prescaler_pmu0_c1 04:05 = pb_cfg_cnpme_prescaler_pmu0_c2 06:07 = pb_cfg_cnpme_prescaler_pmu0_c3 08:09 = pb_cfg_cnpme_prescaler_pmu1_c0 10:11 = pb_cfg_cnpme_prescaler_pmu1_c1 12:13 = pb_cfg_cnpme_prescaler_pmu1_c2 14:15 = pb_cfg_cnpme_prescaler_pmu1_c3 16:17 = pb_cfg_cnpme_prescaler_pmu2_c0 18:19 = pb_cfg_cnpme_prescaler_pmu2_c1 20:21 = pb_cfg_cnpme_prescaler_pmu2_c2 22:23 = pb_cfg_cnpme_prescaler_pmu2_c3 24:25 = pb_cfg_cnpme_prescaler_pmu3_c0 26:27 = pb_cfg_cnpme_prescaler_pmu3_c1 28:29 = pb_cfg_cnpme_prescaler_pmu3_c2 30:31 = pb_cfg_cnpme_prescaler_pmu3_c3 32:32 = pb_cfg_cnpmw_prescaler_pmu0_c0 34:35 = pb_cfg_cnpmw_prescaler_pmu0_c1 36:37 = pb_cfg_cnpmw_prescaler_pmu0_c2 38:39 = pb_cfg_cnpmw_prescaler_pmu0_c3 40:41 = pb_cfg_cnpmw_prescaler_pmu1_c0 42:43 = pb_cfg_cnpmw_prescaler_pmu1_c1 44:45 = pb_cfg_cnpmw_prescaler_pmu1_c2 46:47 = pb_cfg_cnpmw_prescaler_pmu1_c3 48:49 = pb_cfg_cnpmw_prescaler_pmu2_c0 50:51 = pb_cfg_cnpmw_prescaler_pmu2_c1 52:53 = pb_cfg_cnpmw_prescaler_pmu2_c2 54:55 = pb_cfg_cnpmw_prescaler_pmu2_c3 56:57 = pb_cfg_cnpmw_prescaler_pmu3_c0 58:59 = pb_cfg_cnpmw_prescaler_pmu3_c1 60:61 = pb_cfg_cnpmw_prescaler_pmu3_c2 62:63 = pb_cfg_cnpmw_prescaler_pmu3_c3

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	PB_CFG_CNPME_PRESCALER_GRP0_C0: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
2:3	RWX	PB_CFG_CNPME_PRESCALER_GRP0_C1: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
4:5	RWX	PB_CFG_CNPME_PRESCALER_GRP0_C2: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
6:7	RWX	PB_CFG_CNPME_PRESCALER_GRP0_C3: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
8:9	RWX	PB_CFG_CNPME_PRESCALER_GRP1_C0: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
10:11	RWX	PB_CFG_CNPME_PRESCALER_GRP1_C1: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.

Bits	SCOM	Field Mnemonic: Description
12:13	RWX	PB_CFG_CNPME_PRESCALER_GRP1_C2: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
14:15	RWX	PB_CFG_CNPME_PRESCALER_GRP1_C3: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
16:17	RWX	PB_CFG_CNPME_PRESCALER_GRP2_C0: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
18:19	RWX	PB_CFG_CNPME_PRESCALER_GRP2_C1: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
20:21	RWX	PB_CFG_CNPME_PRESCALER_GRP2_C2: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
22:23	RWX	PB_CFG_CNPME_PRESCALER_GRP2_C3: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
24:25	RWX	PB_CFG_CNPME_PRESCALER_GRP3_C0: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
26:27	RWX	PB_CFG_CNPME_PRESCALER_GRP3_C1: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
28:29	RWX	PB_CFG_CNPME_PRESCALER_GRP3_C2: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
30:31	RWX	PB_CFG_CNPME_PRESCALER_GRP3_C3: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
32	RWX	PB_CFG_CNPMW_PRESCALER_GRP0_C0: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.

Bits	SCOM	Field Mnemonic: Description
33	RW	PB_CFG_CNPMW_PRESCALER_GRP0_C0: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
34:35	RWX	PB_CFG_CNPMW_PRESCALER_GRP0_C1: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
36:37	RWX	PB_CFG_CNPMW_PRESCALER_GRP0_C2: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
38:39	RWX	PB_CFG_CNPMW_PRESCALER_GRP0_C3: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
40:41	RWX	PB_CFG_CNPMW_PRESCALER_GRP1_C0: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
42:43	RWX	PB_CFG_CNPMW_PRESCALER_GRP1_C1: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
44:45	RWX	PB_CFG_CNPMW_PRESCALER_GRP1_C2: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
46:47	RWX	PB_CFG_CNPMW_PRESCALER_GRP1_C3: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
48:49	RWX	PB_CFG_CNPMW_PRESCALER_GRP2_C0: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
50:51	RWX	PB_CFG_CNPMW_PRESCALER_GRP2_C1: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
52:53	RWX	PB_CFG_CNPMW_PRESCALER_GRP2_C2: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.

Bits	SCOM	Field Mnemonic: Description
54:55	RWX	PB_CFG_CNPMW_PRESCALER_GRP2_C3: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
56:57	RWX	PB_CFG_CNPMW_PRESCALER_GRP3_C0: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
58:59	RWX	PB_CFG_CNPMW_PRESCALER_GRP3_C1: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
60:61	RWX	PB_CFG_CNPMW_PRESCALER_GRP3_C2: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.
62:63	RWX	PB_CFG_CNPMW_PRESCALER_GRP3_C3: Performance Monitor Prescaler Select 00 = 20 bit. 01 = 16 bit. 10 = 8 bit. 11 = 4 bit.

Register Name	Power Bus PB CENT Event Selection Register
Mnemonic	PB.COM.PB_CENT_EVENT_SEL
Address	0000000005011C16 (SCOM)
Description	00:02 = pb_cfg_event_sel0 03:05 = pb_cfg_event_sel1 06:08 = pb_cfg_event_sel2 09:11 = pb_cfg_event_sel3 12:14 = pb_cfg_event_sel4 15:17 = pb_cfg_event_sel5 18:20 = pb_cfg_event_sel6 21:23 = pb_cfg_event_sel7 24:39 = pb_cfg_cnpme_enable 40:55 = pb_cfg_cnpmw_enable 56 = pb_cfg_pmu_port_sel 57:63 = spare

Bits	SCOM	Field Mnemonic: Description
0:2	RWX	PB_CFG_PMU_SEL0: Performance Monitor Event Bus 0:7 Select.
3:5	RWX	PB_CFG_PMU_SEL1: Performance Monitor Event Bus 8:15 Select.
6:8	RWX	PB_CFG_PMU_SEL2: Performance Monitor Event Bus 16:23 Select.
9:11	RWX	PB_CFG_PMU_SEL3: Performance Monitor Event Bus 24:31 Select.
12:14	RWX	PB_CFG_PMU_SEL4: Performance Monitor Event Bus 32:39 Select.
15:17	RWX	PB_CFG_PMU_SEL5: Performance Monitor Event Bus 40:47 Select.
18:20	RWX	PB_CFG_PMU_SEL6: Performance Monitor Event Bus 48:55 Select.
21:23	RWX	PB_CFG_PMU_SEL7: Performance Monitor Event Bus 56:63 Select.
24:39	RWX	PB_CFG_CNPME_BITWISE_ENABLE: bit-pair enable of PB events asserted on event bus.
40:55	RWX	PB_CFG_CNPMW_BITWISE_ENABLE: bit-pair enable of PB events asserted on event bus.
56	RWX	PB_CFG_PMU_PORT_SEL: Selects PMU RCMD port. 0 = RCMD0&RCMD1 1 = RCMD2&RCMD3.

Bits	SCOM	Field Mnemonic: Description
57:63	RW	Reserved.

Register Name	Power Bus PB CENT Event Compare Register
Mnemonic	PB.COM.PB_CENT_EVENT_COMPA
Address	0000000005011C17 (SCOM)
Description	00:06 = pb_cfg_event_compa_ttype 07:13 = pb_cfg_event_compa_ttype_mask 14:21 = pb_cfg_event_compa_tsize 22:29 = pb_cfg_event_compa_tsize_mask 30:39 = pb_cfg_event_compa_ttag 40:49 = pb_cfg_event_compa_ttag_mask 50:54 = pb_cfg_event_compa_cresp 55:59 = pb_cfg_event_compa_cresp_mask 60 = pb_cfg_event_compa_cresp_polarity 61:63 = pb_cfg_event_compa_scope

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	PB_CFG_EVENT_COMPA_TTYPE: PMU event compare A - Ttype.
7:13	RWX	PB_CFG_EVENT_COMPA_TTYPE_MASK: PMU event compare A - Ttype mask.
14:21	RWX	PB_CFG_EVENT_COMPA_TSIZE: PMU event compare A - tsize.
22:29	RWX	PB_CFG_EVENT_COMPA_TSIZE_MASK: PMU event compare A - tsize mask.
30:39	RWX	PB_CFG_EVENT_COMPA_TTAG: PMU event compare A - ttag.
40:49	RWX	PB_CFG_EVENT_COMPA_TTAG_MASK: PMU event compare A - ttag mask.
50:54	RWX	PB_CFG_EVENT_COMPA_CRESP: PMU event compare A - cresp.
55:59	RWX	PB_CFG_EVENT_COMPA_CRESP_MASK: PMU event compare A - CRESP mask.
60	RWX	PB_CFG_EVENT_COMPA_CRESP_POLARITY: PMU event compare A - CRESP polarity.
61:63	RWX	PB_CFG_EVENT_COMPA_SCOPE: PMU event compare A - scope.

Register Name	Power Bus PB CENT Event Compare B Register
Mnemonic	PB.COM.PB_CENT_EVENT_COMPB
Address	0000000005011C18 (SCOM)
Description	00:06 = pb_cfg_event_compb_ttype 07:13 = pb_cfg_event_compb_ttype_mask 14:21 = pb_cfg_event_compb_tsize 22:29 = pb_cfg_event_compb_tsize_mask 30:39 = pb_cfg_event_compb_ttag 40:49 = pb_cfg_event_compb_ttag_mask 50:54 = pb_cfg_event_compb_cresp 55:59 = pb_cfg_event_compb_cresp_mask 60 = pb_cfg_event_compb_cresp_polarity 61:63 = pb_cfg_event_compb_scope

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	PB_CFG_EVENT_COMPB_TTYPE: PMU event compare B - Ttype.
7:13	RWX	PB_CFG_EVENT_COMPB_TTYPE_MASK: PMU event compare B - Ttype mask.
14:21	RWX	PB_CFG_EVENT_COMPB_TSIZE: PMU event compare B - tsize.
22:29	RWX	PB_CFG_EVENT_COMPB_TSIZE_MASK: PMU event compare B - tsize mask.
30:39	RWX	PB_CFG_EVENT_COMPB_TTAG: PMU event compare B - ttag.
40:49	RWX	PB_CFG_EVENT_COMPB_TTAG_MASK: PMU event compare B - ttag mask.
50:54	RWX	PB_CFG_EVENT_COMPB_CRESP: PMU event compare B - cresp.
55:59	RWX	PB_CFG_EVENT_COMPB_CRESP_MASK: PMU event compare B - CRESP mask.
60	RWX	PB_CFG_EVENT_COMPB_CRESP_POLARITY: PMU event compare B - CRESP polarity.

Bits	SCOM	Field Mnemonic: Description
61:63	RWX	PB_CFG_EVENT_COMPB_SCOPE: PMU event compare B - scope.

Register Name	Power Bus PB CENT Event Compare X Register
Mnemonic	PB.COM.PB_CENT_EVENT_COMPX
Address	0000000005011C19 (SCOM)
Description	00:02 = pb_cfg_event_compa_scope_mask 03:16 = pb_cfg_event_compa_presp 17:30 = pb_cfg_event_compa_presp_mask 32:34 = pb_cfg_event_compb_scope_mask 35:48 = pb_cfg_event_compb_presp 49:62 = pb_cfg_event_compb_presp_mask 63 = spare

Bits	SCOM	Field Mnemonic: Description
0:2	RWX	PB_CFG_EVENT_COMPA_SCOPE_MASK: PMU event compare A - scope mask.
3:16	RWX	PB_CFG_EVENT_COMPA_PRESP: PMU event compare A - presp.
17:30	RWX	PB_CFG_EVENT_COMPA_PRESP_MASK: PMU event compare A - presp mask.
31	RW	Reserved.
32:34	RWX	PB_CFG_EVENT_COMPB_SCOPE_MASK: PMU event compare B - scope mask.
35:48	RWX	PB_CFG_EVENT_COMPB_PRESP: PMU event compare B - presp.
49:62	RWX	PB_CFG_EVENT_COMPB_PRESP_MASK: PMU event compare B - presp mask.
63	RW	Reserved.

Register Name	Power Bus PB CENT PMU0 CNPME Counter Register
Mnemonic	PB.COM.PB_CENT_PMU0_CNPME_COUNTER
Address	0000000005011C1A (SCOM)
Description	00:15 pbh_event_pmu0_cnpme_counter0(0:15) 16:31 pbh_event_pmu0_cnpme_counter1(0:15) 32:47 pbh_event_pmu0_cnpme_counter2(0:15) 48:63 pbh_event_pmu0_cnpme_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	Reserved.
16:31	RWX_WCLRREG	Reserved.
32:47	RWX_WCLRREG	Reserved.
48:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT PMU1 CNPME Counter Register
Mnemonic	PB.COM.PB_CENT_PMU1_CNPME_COUNTER
Address	0000000005011C1B (SCOM)
Description	00:15 pbh_event_pmu1_cnpme_counter0(0:15) 16:31 pbh_event_pmu1_cnpme_counter1(0:15) 32:47 pbh_event_pmu1_cnpme_counter2(0:15) 48:63 pbh_event_pmu1_cnpme_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	Reserved.
16:31	RWX_WCLRREG	Reserved.
32:47	RWX_WCLRREG	Reserved.

Bits	SCOM	Field Mnemonic: Description
48:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT PMU2 CNPME Counter Register
Mnemonic	PB.COM.PB_CENT_PMU2_CNPME_COUNTER
Address	0000000005011C1C (SCOM)
Description	00:15 pbh_event_pmu2_cnpme_counter0(0:15) 16:31 pbh_event_pmu2_cnpme_counter1(0:15) 32:47 pbh_event_pmu2_cnpme_counter2(0:15) 48:63 pbh_event_pmu2_cnpme_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	Reserved.
16:31	RWX_WCLRREG	Reserved.
32:47	RWX_WCLRREG	Reserved.
48:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT PMU3 CNPME Counter Register
Mnemonic	PB.COM.PB_CENT_PMU3_CNPME_COUNTER
Address	0000000005011C1D (SCOM)
Description	00:15 pbh_event_pmu3_cnpme_counter0(0:15) 16:31 pbh_event_pmu3_cnpme_counter1(0:15) 32:47 pbh_event_pmu3_cnpme_counter2(0:15) 48:63 pbh_event_pmu3_cnpme_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	Reserved.
16:31	RWX_WCLRREG	Reserved.
32:47	RWX_WCLRREG	Reserved.
48:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT PMU0 CNPMW Counter Register
Mnemonic	PB.COM.PB_CENT_PMU0_CNPMW_COUNTER
Address	0000000005011C1E (SCOM)
Description	00:15 pbh_event_pmu0_cnpmw_counter0(0:15) 16:31 pbh_event_pmu0_cnpmw_counter1(0:15) 32:47 pbh_event_pmu0_cnpmw_counter2(0:15) 48:63 pbh_event_pmu0_cnpmw_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	Reserved.
16:31	RWX_WCLRREG	Reserved.
32:47	RWX_WCLRREG	Reserved.
48:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT PMU1 CNPMW Counter Register
Mnemonic	PB.COM.PB_CENT_PMU1_CNPMW_COUNTER
Address	0000000005011C1F (SCOM)
Description	00:15 pbh_event_pmu1_cnpmw_counter0(0:15) 16:31 pbh_event_pmu1_cnpmw_counter1(0:15) 32:47 pbh_event_pmu1_cnpmw_counter2(0:15) 48:63 pbh_event_pmu1_cnpmw_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	Reserved.
16:31	RWX_WCLRREG	Reserved.
32:47	RWX_WCLRREG	Reserved.
48:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT PMU2 CNPMW Counter Register
Mnemonic	PB.COM.PB_CENT_PMU2_CNPMW_COUNTER
Address	0000000005011C20 (SCOM)
Description	00:15 pbh_event_pmu2_cnpmw_counter0(0:15) 16:31 pbh_event_pmu2_cnpmw_counter1(0:15) 32:47 pbh_event_pmu2_cnpmw_counter2(0:15) 48:63 pbh_event_pmu2_cnpmw_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	Reserved.
16:31	RWX_WCLRREG	Reserved.
32:47	RWX_WCLRREG	Reserved.
48:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT PMU3 CNPMW Counter Register
Mnemonic	PB.COM.PB_CENT_PMU3_CNPMW_COUNTER
Address	0000000005011C21 (SCOM)
Description	00:15 pbh_event_pmu3_cnpmw_counter0(0:15) 16:31 pbh_event_pmu3_cnpmw_counter1(0:15) 32:47 pbh_event_pmu3_cnpmw_counter2(0:15) 48:63 pbh_event_pmu3_cnpmw_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	Reserved.
16:31	RWX_WCLRREG	Reserved.
32:47	RWX_WCLRREG	Reserved.
48:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT NMPM Counter Register
Mnemonic	PB.COM.PB_CENT_NMPM_COUNTER
Address	0000000005011C22 (SCOM)
Description	00 pb_cfg_apm_en 01:02 pb_cfg_sample_sel(0:1) 03 pb_cfg_pmucnt_en 04:05 pb_cfg_pmucnt_sel(0:1) 06 pb_cfg_nm_hi_comp_lsb 07 pb_cfg_nm_lo_comp_lsb 08:11 pb_cfg_nm_hi_comp(0:3) 12:15 pb_cfg_nm_lo_comp(0:3) 16:39 pb_apm_nm_lo_cnt(0:23) 40:63 pb_apm_nm_hi_cnt(0:23)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_APM_ENABLE: Enable Advanced Power Management Counters.
1:2	RWX	PB_CFG_APM_SAMPLE_SEL: configures APM sample period.
3	RWX	PB_CFG_PMUCNT_EN: Enable Performance Monitor Counters.
4:5	RWX	PB_CFG_PMUCNT_SEL: configures Performance Monitor inputs.
6	RWX	PB_CFG_APM_NM_HI_COMP: configures APM NM high compare.
7	RWX	PB_CFG_APM_NM_LO_COMP: configures APM NM low compare.
8:11	RWX	PB_CFG_APM_NM_HI_COMP: configures APM NM high compare.
12:15	RWX	PB_CFG_APM_NM_LO_COMP: configures APM NM low compare.
16:39	ROX	Reserved.
40:63	ROX	Reserved.

Register Name	Power Bus PB CENT LMPM Counter Register
Mnemonic	PB.COM.PB_CENT_LMPM_COUNTER
Address	0000000005011C23 (SCOM)
Description	Power bus CENT LMPM counter register

Bits	SCOM	Field Mnemonic: Description
0	RW	PB_CFG_APM_DD1_MODE: Configures APM counters for POWER9 mode.
1:2	RWX	PB_CFG_APM_SEL: Configures APM scopes.
3	RW	Reserved.
4	RWX	PB_CFG_PMU_FREEZE_MODE: Configures PMU counters to freeze/reset.
5	RW	Reserved.
6	RWX	PB_CFG_APM_LM_HI_COMP: Configures APM LM high compare.
7	RWX	PB_CFG_APM_LM_LO_COMP: Configures APM LM low compare.
8:11	RWX	PB_CFG_APM_LM_HI_COMP: Configures APM LM high compare.
12:15	RWX	PB_CFG_APM_LM_LO_COMP: Configures APM LM low compare.
16:39	ROX	Reserved.
40:63	ROX	Reserved.

Register Name	Power Bus PB CENT RCMD INTDAT Counter Register
Mnemonic	PB.COM.PB_CENT_RCMD_INTDAT_COUNTER
Address	0000000005011C24 (SCOM)
Description	00:31 pb_apm_RCMD_cnt(0:31) 32:63 pb_apm_intdata_cnt(0:31)

Bits	SCOM	Field Mnemonic: Description
0:31	RWX_WCLRREG	Reserved.
32:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT EXTDAT Counter Register
Mnemonic	PB.COM.PB_CENT_EXTDAT_COUNTER
Address	0000000005011C25 (SCOM)
Description	00:31 pb_apm_extdatasnd_cnt(0:31) 32:63 pb_apm_extdatarcv_cnt(0:31)

Bits	SCOM	Field Mnemonic: Description
0:31	RWX_WCLRREG	Reserved.
32:63	RWX_WCLRREG	Reserved.

Register Name	Power Bus PB CENT GP command RATE DP0 Register
Mnemonic	PB.COM.PB_CENT_GP_CMD_RATE_DP0
Address	0000000005011C26 (SCOM)
Description	00:07 = pb_gp_cmd_rate_dp0_lvl0 08:15 = pb_gp_cmd_rate_dp0_lvl1 16:23 = pb_gp_cmd_rate_dp0_lvl2 24:31 = pb_gp_cmd_rate_dp0_lvl3 32:39 = pb_gp_cmd_rate_dp0_lvl4 40:47 = pb_gp_cmd_rate_dp0_lvl5 48:55 = pb_gp_cmd_rate_dp0_lvl6 56:63 = pb_gp_cmd_rate_dp0_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL0: Configures the command rate for group pump drop priority 0 at level 0.
8:15	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL1: Configures the command rate for group pump drop priority 0 at level 1.
16:23	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL2: Configures the command rate for group pump drop priority 0 at level 2.
24:31	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL3: Configures the command rate for group pump drop priority 0 at level 3.
32:39	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL4: Configures the command rate for group pump drop priority 0 at level 4.
40:47	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL5: Configures the command rate for group pump drop priority 0 at level 5.
48:55	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL6: Configures the command rate for group pump drop priority 0 at level 6.
56:63	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL7: Configures the command rate for group pump drop priority 0 at level 7.

Register Name	Power Bus PB CENT GP command RATE DP1 Register
Mnemonic	PB.COM.PB_CENT_GP_CMD_RATE_DP1
Address	0000000005011C27 (SCOM)
Description	00:07 = pb_gp_cmd_rate_dp1_lvl0 08:15 = pb_gp_cmd_rate_dp1_lvl1 16:23 = pb_gp_cmd_rate_dp1_lvl2 24:31 = pb_gp_cmd_rate_dp1_lvl3 32:39 = pb_gp_cmd_rate_dp1_lvl4 40:47 = pb_gp_cmd_rate_dp1_lvl5 48:55 = pb_gp_cmd_rate_dp1_lvl6 56:63 = pb_gp_cmd_rate_dp1_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL0: Configures the command rate for group pump drop priority 1 at level 0.
8:15	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL1: Configures the command rate for group pump drop priority 1 at level 1.

Bits	SCOM	Field Mnemonic: Description
16:23	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL2: Configures the command rate for group pump drop priority 1 at level 2.
24:31	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL3: Configures the command rate for group pump drop priority 1 at level 3.
32:39	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL4: Configures the command rate for group pump drop priority 1 at level 4.
40:47	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL5: Configures the command rate for group pump drop priority 1 at level 5.
48:55	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL6: Configures the command rate for group pump drop priority 1 at level 6.
56:63	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL7: Configures the command rate for group pump drop priority 1 at level 7.

Register Name	Power Bus PB CENT RGP command RATE DP0 Register
Mnemonic	PB.COM.PB_CENT_RGP_CMD_RATE_DP0
Address	0000000005011C28 (SCOM)
Description	00:07 = pb_rgp_cmd_rate_dp0_lvl0 08:15 = pb_rgp_cmd_rate_dp0_lvl1 16:23 = pb_rgp_cmd_rate_dp0_lvl2 24:31 = pb_rgp_cmd_rate_dp0_lvl3 32:39 = pb_rgp_cmd_rate_dp0_lvl4 40:47 = pb_rgp_cmd_rate_dp0_lvl5 48:55 = pb_rgp_cmd_rate_dp0_lvl6 56:63 = pb_rgp_cmd_rate_dp0_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_RNS_CMD_RATE_DP0_LVL0: Configures the command rate for remote group pump drop priority 0 at level 0.
8:15	RWX	PB_CFG_RNS_CMD_RATE_DP0_LVL1: Configures the command rate for remote group pump drop priority 0 at level 1.
16:23	RWX	PB_CFG_RNS_CMD_RATE_DP0_LVL2: Configures the command rate for remote group pump drop priority 0 at level 2.
24:31	RWX	PB_CFG_RNS_CMD_RATE_DP0_LVL3: Configures the command rate for remote group pump drop priority 0 at level 3.
32:39	RWX	PB_CFG_RNS_CMD_RATE_DP0_LVL4: Configures the command rate for remote group pump drop priority 0 at level 4.
40:47	RWX	PB_CFG_RNS_CMD_RATE_DP0_LVL5: Configures the command rate for remote group pump drop priority 0 at level 5.
48:55	RWX	PB_CFG_RNS_CMD_RATE_DP0_LVL6: Configures the command rate for remote group pump drop priority 0 at level 6.
56:63	RWX	PB_CFG_RNS_CMD_RATE_DP0_LVL7: Configures the command rate for remote group pump drop priority 0 at level 7.

Register Name	Power Bus PB CENT RGP command RATE DP1 Register
Mnemonic	PB.COM.PB_CENT_RGP_CMD_RATE_DP1
Address	0000000005011C29 (SCOM)
Description	00:07 = pb_rgp_cmd_rate_dp1_lvl0 08:15 = pb_rgp_cmd_rate_dp1_lvl1 16:23 = pb_rgp_cmd_rate_dp1_lvl2 24:31 = pb_rgp_cmd_rate_dp1_lvl3 32:39 = pb_rgp_cmd_rate_dp1_lvl4 40:47 = pb_rgp_cmd_rate_dp1_lvl5 48:55 = pb_rgp_cmd_rate_dp1_lvl6 56:63 = pb_rgp_cmd_rate_dp1_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_RNS_CMD_RATE_DP1_LVL0: Configures the command rate for remote group pump drop priority 1 at level 0.
8:15	RWX	PB_CFG_RNS_CMD_RATE_DP1_LVL1: Configures the command rate for remote group pump drop priority 1 at level 1.
16:23	RWX	PB_CFG_RNS_CMD_RATE_DP1_LVL2: Configures the command rate for remote group pump drop priority 1 at level 2.
24:31	RWX	PB_CFG_RNS_CMD_RATE_DP1_LVL3: Configures the command rate for remote group pump drop priority 1 at level 3.
32:39	RWX	PB_CFG_RNS_CMD_RATE_DP1_LVL4: Configures the command rate for remote group pump drop priority 1 at level 4.
40:47	RWX	PB_CFG_RNS_CMD_RATE_DP1_LVL5: Configures the command rate for remote group pump drop priority 1 at level 5.
48:55	RWX	PB_CFG_RNS_CMD_RATE_DP1_LVL6: Configures the command rate for remote group pump drop priority 1 at level 6.
56:63	RWX	PB_CFG_RNS_CMD_RATE_DP1_LVL7: Configures the command rate for remote group pump drop priority 1 at level 7.

Register Name	**Power Bus PB CENT SP command RATE DP0 Register**
Mnemonic	PB.COM.PB_CENT_SP_CMD_RATE_DP0
Address	0000000005011C2A (SCOM)
Description	00:07 = pb_sp_cmd_rate_dp0_lvl0 08:15 = pb_sp_cmd_rate_dp0_lvl1 16:23 = pb_sp_cmd_rate_dp0_lvl2 24:31 = pb_sp_cmd_rate_dp0_lvl3 32:39 = pb_sp_cmd_rate_dp0_lvl4 40:47 = pb_sp_cmd_rate_dp0_lvl5 48:55 = pb_sp_cmd_rate_dp0_lvl6 56:63 = pb_sp_cmd_rate_dp0_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_VG_CMD_RATE_DP0_LVL0: Configures the command rate for system pump drop priority 0 at level 0.
8:15	RWX	PB_CFG_VG_CMD_RATE_DP0_LVL1: Configures the command rate for system pump drop priority 0 at level 1.
16:23	RWX	PB_CFG_VG_CMD_RATE_DP0_LVL2: Configures the command rate for system pump drop priority 0 at level 2.
24:31	RWX	PB_CFG_VG_CMD_RATE_DP0_LVL3: Configures the command rate for system pump drop priority 0 at level 3.
32:39	RWX	PB_CFG_VG_CMD_RATE_DP0_LVL4: Configures the command rate for system pump drop priority 0 at level 4.
40:47	RWX	PB_CFG_VG_CMD_RATE_DP0_LVL5: Configures the command rate for system pump drop priority 0 at level 5.
48:55	RWX	PB_CFG_VG_CMD_RATE_DP0_LVL6: Configures the command rate for system pump drop priority 0 at level 6.
56:63	RWX	PB_CFG_VG_CMD_RATE_DP0_LVL7: Configures the command rate for system pump drop priority 0 at level 7.

Register Name	Power Bus PB CENT SP command RATE DP1 Register
Mnemonic	PB.COM.PB_CENT_SP_CMD_RATE_DP1
Address	0000000005011C2B (SCOM)
Description	00:07 = pb_sp_cmd_rate_dp1_lvl0 08:15 = pb_sp_cmd_rate_dp1_lvl1 16:23 = pb_sp_cmd_rate_dp1_lvl2 24:31 = pb_sp_cmd_rate_dp1_lvl3 32:39 = pb_sp_cmd_rate_dp1_lvl4 40:47 = pb_sp_cmd_rate_dp1_lvl5 48:55 = pb_sp_cmd_rate_dp1_lvl6 56:63 = pb_sp_cmd_rate_dp1_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_VG_CMD_RATE_DP1_LVL0: Configures the command rate for system pump drop priority 1 at level 0.
8:15	RWX	PB_CFG_VG_CMD_RATE_DP1_LVL1: Configures the command rate for system pump drop priority 1 at level 1.
16:23	RWX	PB_CFG_VG_CMD_RATE_DP1_LVL2: Configures the command rate for system pump drop priority 1 at level 2.
24:31	RWX	PB_CFG_VG_CMD_RATE_DP1_LVL3: Configures the command rate for system pump drop priority 1 at level 3.
32:39	RWX	PB_CFG_VG_CMD_RATE_DP1_LVL4: Configures the command rate for system pump drop priority 1 at level 4.
40:47	RWX	PB_CFG_VG_CMD_RATE_DP1_LVL5: Configures the command rate for system pump drop priority 1 at level 5.
48:55	RWX	PB_CFG_VG_CMD_RATE_DP1_LVL6: Configures the command rate for system pump drop priority 1 at level 6.
56:63	RWX	PB_CFG_VG_CMD_RATE_DP1_LVL7: Configures the command rate for system pump drop priority 1 at level 7.

Register Name	Power Bus PB CENT CR Error Register
Mnemonic	PB.COM.PB_CENT_CR_ERROR
Address	0000000005011C2C (SCOM)
Description	00 = pb_cresp_error 01 = pb_cresp_addr_error 02 = pb_cfg_cresp_error_other 03:09 = pb_cfg_cresp_ttype 10:17 = pb_cfg_cresp_tsize 18:39 = pb_cfg_cresp_ttag 40:42 = pb_cfg_cresp_scope 43:47 = pb_cfg_cresp 48:61 = pb_cfg_presp

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3:9	ROX	Reserved.
10:17	ROX	Reserved.
18:39	ROX	Reserved.
40:42	ROX	Reserved.
43:47	ROX	Reserved.
48:61	ROX	Reserved.
62:63	RO	Constant = 0b00

Register Name	Power Bus EH EXTFIR Register
Mnemonic	PB.COM.EXTFIR_REG
Address	0000000005011C2E (SCOM) 0000000005011C2F (SCOM1) 0000000005011C30 (SCOM2)
Description	Processor bus EH EXTFIR register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_X0_FIR_ERR: pb_x0_fir_err.
1	RWX	WOX_AND	WOX_OR	PB_X1_FIR_ERR: pb_x1_fir_err.
2	RWX	WOX_AND	WOX_OR	PB_X2_FIR_ERR: pb_x2_fir_err.
3	RWX	WOX_AND	WOX_OR	PB_X3_FIR_ERR: pb_x3_fir_err.
4	RWX	WOX_AND	WOX_OR	PB_X4_FIR_ERR: pb_x4_fir_err.
5	RWX	WOX_AND	WOX_OR	PB_X5_FIR_ERR: pb_x5_fir_err.
6	RWX	WOX_AND	WOX_OR	PB_X6_FIR_ERR: pb_x6_fir_err.
7	RWX	WOX_AND	WOX_OR	EXTFIR_SCOM_ERROR: Processor bus EXTFIR SCOM error.
8:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Power Bus EXTFIR Mask Register
Mnemonic	PB.COM.EXTFIR_MASK_REG
Address	0000000005011C31 (SCOM) 0000000005011C32 (SCOM1) 0000000005011C33 (SCOM2)
Description	Processor bus EXTFIR mask registers

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	PB_X0_FIR_ERR_MASK: pb_x0_fir_err_mask.
1	RW	WO_AND	WO_OR	PB_X1_FIR_ERR_MASK: pb_x1_fir_err_mask.
2	RW	WO_AND	WO_OR	PB_X2_FIR_ERR_MASK: pb_x2_fir_err_mask.
3	RW	WO_AND	WO_OR	PB_X3_FIR_ERR_MASK: pb_x3_fir_err_mask.
4	RW	WO_AND	WO_OR	PB_X4_FIR_ERR_MASK: pb_x4_fir_err_mask.
5	RW	WO_AND	WO_OR	PB_X5_FIR_ERR_MASK: pb_x5_fir_err_mask.
6	RW	WO_AND	WO_OR	PB_X6_FIR_ERR_MASK: pb_x6_fir_err_mask.
7	RW	WO_AND	WO_OR	EXTFIR_SCOM_ERROR_MASK: Processor bus EXTFIR SCOM error.
8:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Power Bus EXTFIR Action 0 Register
Mnemonic	PB.COM.EXTFIR_ACTION0_REG
Address	0000000005011C34 (SCOM)
Description	Processor bus EXTFIR Action 0 Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	EXTFIR_ACTION0: Processor bus EXTFIR MSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Recoverable Interrupt to Processor. (1,1) = Invalid.
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Power Bus EXTFIR Action 1 Register
Mnemonic	PB.COM.EXTFIR_ACTION1_REG
Address	0000000005011C35 (SCOM)
Description	Processor bus EXTFIR Action 1 Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	EXTFIR_ACTION1: Processor bus EXTFIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Recoverable Interrupt to Processor. (1,1) = Invalid.
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Power Bus PB East FIR Register
Mnemonic	PB.COM.PB_EAST_FIR_REG
Address	0000000005012000 (SCOM) 0000000005012001 (SCOM1) 0000000005012002 (SCOM2)
Description	Processor bus PB EAST nest domain FIR register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ04_PBH_HW1_ERROR: pbieq04_pbh_hw1_error.
1	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ04_PBH_HW2_ERROR: pbieq04_pbh_hw2_error.
2	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ04_PBH_PROTOCOL_ERROR: pbieq04_pbh_protocol_error.
3	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ04_PBH_OVERFLOW_ERROR: pbieq04_pbh_overflow_error.
4	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ05_PBH_HW1_ERROR: pbieq05_pbh_hw1_error.
5	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ05_PBH_HW2_ERROR: pbieq05_pbh_hw2_error.
6	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ05_PBH_PROTOCOL_ERROR: pbieq05_pbh_protocol_error.
7	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ05_PBH_OVERFLOW_ERROR: pbieq05_pbh_overflow_error.
8	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_8: fir_spare_8.
9	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_9: fir_spare_9.
10	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_10: fir_spare_10.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
11	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_11: fir_spare_11.
12	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_12: fir_spare_12.
13	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_13: fir_spare_13.
14	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_14: fir_spare_14.
15	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_15: fir_spare_15.
16	RWX	WOX_AND	WOX_OR	PB_EAST_OVERFLOW_CHECKSTOP: pb_east_overflow_checkstop.
17	RWX	WOX_AND	WOX_OR	PB_EAST_PROTOCOL_CHECKSTOP: pb_east_protocol_checkstop.
18	RWX	WOX_AND	WOX_OR	PB_EAST_ROUTE_CHECKSTOP: pb_east_route_checkstop.
19	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_19: fir_spare_19.
20	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_20: fir_spare_20.
21	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_21: fir_spare_21.
22	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_22: fir_spare_22.
23	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_23: fir_spare_23.
24	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_24: fir_spare_24.
25	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_25: fir_spare_25.
26	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_26: fir_spare_26.
27	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_27: fir_spare_27.
28	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_28: fir_spare_28.
29	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_29: fir_spare_29.
30	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_30: fir_spare_30.
31	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_31: fir_spare_31.
32	RWX	WOX_AND	WOX_OR	FIR_SCOM_EAST_ERR: PBEH EAST FIR_SCOM_err.
33	RWX	WOX_AND	WOX_OR	FIR_SCOM_EAST_ERR_DUP: PBEH EAST FIR_SCOM_err duplicate.
34:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	**Power Bus PB East FIR Mask Register**
Mnemonic	PB.COM.PB_EAST_FIR_MASK_REG
Address	0000000005012003 (SCOM) 0000000005012004 (SCOM1) 0000000005012005 (SCOM2)
Description	Processor bus PB EAST nest domain FIR MASK register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ04_PBH_HW1_ERROR_MASK: pbieq04_pbh_hw1_error_mask.
1	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ04_PBH_HW2_ERROR_MASK: pbieq04_pbh_hw2_error_mask.
2	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ04_PBH_PROTOCOL_ERROR_MASK: pbieq04_pbh_protocol_error_mask.
3	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ04_PBH_OVERFLOW_ERROR_MASK: pbieq04_pbh_overflow_error_mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
4	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ05_PBH_HW1_ERROR_MASK: pbieq05_pbh_hw1_error_mask.
5	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ05_PBH_HW2_ERROR_MASK: pbieq05_pbh_hw2_error_mask.
6	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ05_PBH_PROTOCOL_ERROR_MASK: pbieq05_pbh_protocol_error_mask.
7	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEQ05_PBH_OVERFLOW_ERROR_MASK: pbieq05_pbh_overflow_error_mask.
8	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_8_MASK: fir_spare_8_mask.
9	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_9_MASK: fir_spare_9_mask.
10	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_10_MASK: fir_spare_10_mask.
11	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_11_MASK: fir_spare_11_mask.
12	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_12_MASK: fir_spare_12_mask.
13	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_13_MASK: fir_spare_13_mask.
14	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_14_MASK: fir_spare_14_mask.
15	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_15_MASK: fir_spare_15_mask.
16	RWX	WOX_AND	WOX_OR	PB_EAST_OVERFLOW_CHECKSTOP_MASK: pb_east_overflow_checkstop_mask.
17	RWX	WOX_AND	WOX_OR	PB_EAST_PROTOCOL_CHECKSTOP_MASK: pb_east_protocol_checkstop_mask.
18	RWX	WOX_AND	WOX_OR	PB_EAST_ROUTE_CHECKSTOP_MASK: pb_east_route_checkstop_mask.
19	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_19_MASK: fir_spare_19_mask.
20	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_20_MASK: fir_spare_20_mask.
21	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_21_MASK: fir_spare_21_mask.
22	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_22_MASK: fir_spare_22_mask.
23	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_23_MASK: fir_spare_23_mask.
24	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_24_MASK: fir_spare_24_mask.
25	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_25_MASK: fir_spare_25_mask.
26	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_26_MASK: fir_spare_26_mask.
27	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_27_MASK: fir_spare_27_mask.
28	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_28_MASK: fir_spare_28_mask.
29	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_29_MASK: fir_spare_29_mask.
30	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_30_MASK: fir_spare_30_mask.
31	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_31_MASK: fir_spare_31_mask.
32	RWX	WOX_AND	WOX_OR	FIR_SCOM_EAST_ERR_MASK: PBEH EAST FIR_SCOM_err_mask.
33	RWX	WOX_AND	WOX_OR	FIR_SCOM_EAST_ERR_MASK_DUP: PBEH EAST FIR_SCOM_err_mask_dup.
34:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus PB East FIR Action 0 Register
Mnemonic	PB.COM.PB_EAST_FIR_ACTION0_REG
Address	0000000005012006 (SCOM)
Description	Processor bus PB EAST nest domain FIR Action 0 Register

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PB_EAST_FIR_ACTION0: Processor bus PBEH EAST nest domain FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Recoverable Interrupt to Processor. (1,1) = Invalid.
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus PB East FIR Action 1 Register
Mnemonic	PB.COM.PB_EAST_FIR_ACTION1_REG
Address	0000000005012007 (SCOM)
Description	Processor bus PB EAST nest domain FIR Action 1 Register

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PB_EAST_FIR_ACTION1: Processor bus PB EAST nest domain FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Recoverable Interrupt to Processor. (1,1) = Invalid.
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus PB East Mode Configuration Register
Mnemonic	PB.COM.PB_EAST_MODE
Address	000000000501200A (SCOM)
Description	00 = pb_east_pbixxx_init 01:03 = spare 04 pb_= cfg_east_chip_is_system 05:07 = spare 08 = pb_cfg_east_hng_chk_disable 09 = pb_cfg_east_dbg_clr_max_hang_stage 10:11 = spare 12:15 pb_cfg_east_sw_ab_wait(0:3) 16:22 = pb_cfg_east_sp_hw_mark(0:6) 23:29 = pb_cfg_east_gp_hw_mark(0:6) 30:35 = pb_cfg_east_lcl_hw_mark(0:5) 36:41 = pb_cfg_east_cpu_ratio_override(0:5) 42:56 = spare 57 = pb_cfg_east_req_gather_enable 58 = spare 59 = pb_cfg_east_switch_option_ab 60:62 = spare 63 pb_cfg_east_reset_error_capture

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1:3	RO	Constant = 0b000
4	RWX	PB_CFG_CHIP_IS_SYSTEM: configures whether there are other POWER9s in the system.
5:7	RW	Reserved.
8	RWX	PB_CFG_HNG_CHK_DISABLE: Hang Check Disable.
9	RWX	PB_DBG_CLR_MAX_HANG_STAGE: Resets the maximum hang state level (pb_hang_level).
10:11	RW	Reserved.
12:15	RWX	PB_CFG_SW_AB_WAIT: Adds delay to tc_pb_switch_ab input from TPC during hot plug sequence.
16:22	RWX	PB_CFG_SP_HW_MARK: configures the maximum system pumps an IO unit may issue.
23:29	RWX	PB_CFG_GP_HW_MARK: configures the maximum group pumps this chip may issue.
30:35	RWX	PB_CFG_LCL_HW_MARK: configures the maximum local pumps this chip may issue.
36:41	RWX	Reserved.
42:56	RW	Reserved.
57	RWX	PB_CFG_REQ_GATHER_ENABLE: Enable data OW gathering on all chiplet/link requests. {default = on}.
58	RW	PB_CFG_SWITCH_CD_PULSE: Controls switch_cd pulse width. Uses pb_cfg_sw_ab_wait to extend pulse. Default = long pulse. Requires pb_cfg_sw_ab_wait > cnt_5 for 6 cycle pulse.
59	RWX	PB_CFG_SWITCH_OPTION_AB: SCOM access to determine what signal drives pb_cfg_switch_cd. on = tc_pb_switch_ab, off = tc_pb_switch_cd.
60:62	RW	Reserved.
63	RWX	Reserved.

Register Name	**Power Bus PB East HP Mode Configuration Register**
Mnemonic	PB.COM.PB_EAST_HP_MODE_NEXT
Address	000000000501200B (SCOM)
Description	00 = pb_cfg_east_master_chip 01 = pb_cfg_east_tm_master 02 = pb_cfg_east_chg_rate_gp_master 03 = pb_cfg_east_chg_rate_sp_master 04 = pb_cfg_east_link_a0_en 05 = pb_cfg_east_link_a1_en 06 = pb_cfg_east_link_a2_en 07 = pb_cfg_east_link_a3_en 08 = pb_cfg_east_na0_addr_dis 09 = pb_cfg_east_na1_addr_dis 10 = pb_cfg_east_na2_addr_dis 11 = pb_cfg_east_na3_addr_dis 12:15 = pb_cfg_east_link_a0_groupid 16:19 = pb_cfg_east_link_a1_groupid 20:23 = pb_cfg_east_link_a2_groupid 24:27 = pb_cfg_east_link_a3_groupid 28 = pb_cfg_east_a_aggregate 29 = pb_cfg_east_hop_mode 30 = pb_cfg_east_smp_optics_mode 31 = pb_cfg_east_capi_mode 32:33 = pb_cfg_east_opt0_mode 34:35 = pb_cfg_east_opt1_mode 36:37 = pb_cfg_east_opt2_mode 38:39 = pb_cfg_east_opt3_mode 40:46 = pb_cfg_east_xlate_addr_to_id 47:48 = spare 49 = pb_cfg_east_a_indirect_en 50 = pb_cfg_east_a_gather_enable 51 = spare 52 pb_cfg_east_phyp_is_group 53 = pb_cfg_east_addr_bar_mode 54 = pb_cfg_east_pump_mode 55 = pb_cfg_east_dcache_capp_mode 56:63 = pb_cfg_east_a_cmd_rate

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_NEXT: Processor bus master.
1	RWX	PB_CFG_TM_MASTER_NEXT: configure Chip as PB TM Master.
2	RWX	PB_CFG_CHG_RATE_GP_MASTER_NEXT: Sets the Group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt.
3	RWX	PB_CFG_CHG_RATE_SP_MASTER_NEXT: Sets the System pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt.
4	RWX	PB_CFG_LINK_A0_EN_NEXT: Link A0 enabled.
5	RWX	PB_CFG_LINK_A1_EN_NEXT: Link A1 enabled.
6	RWX	PB_CFG_LINK_A2_EN_NEXT: Link A2 enabled.
7	RWX	PB_CFG_LINK_A3_EN_NEXT: Link A3 enabled.
8	RWX	PB_CFG_LINK_NA0_ADDR_DIS_NEXT: Link A0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NA1_ADDR_DIS_NEXT: Link A1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NA2_ADDR_DIS_NEXT: Link A2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NA3_ADDR_DIS_NEXT: Link A3 address broadcast disabled.
12:15	RWX	PB_CFG_LINK_A0_GROUPID_NEXT: Group ID of chip connected to A0 link.

Bits	SCOM	Field Mnemonic: Description
16:19	RWX	PB_CFG_LINK_A1_GROUPID_NEXT: Group ID of chip connected to A1 link.
20:23	RWX	PB_CFG_LINK_A2_GROUPID_NEXT: Group ID of chip connected to A2 link.
24:27	RWX	PB_CFG_LINK_A3_GROUPID_NEXT: Group ID of chip connected to A3 link.
28	RWX	PB_CFG_A_AGGREGATE_NEXT: Processor bus A links are configured as parallel buses to same chip.
29	RWX	PB_CFG_HOP_MODE_NEXT: Sets SMP hop mode. 0 = 1-hop or 2-hop SMP topology. 1 = 3-hop SMP topology.
30	RWX	PB_CFG_SMP_OPTICS_MODE_NEXT: Sets SMP optics mode. 0 = Optic Links are configured as X-bus SMP protocol. 1 = Optic Links are configured as A-bus SMP protocol.
31	RWX	PB_CFG_CAPI_MODE_NEXT: Indicates a CAPI 2.0 link is attached in the SMP system.
32:33	RWX	PB_CFG_OPT0_MODE_NEXT: Optical Link 0 configuration.
34:35	RWX	PB_CFG_OPT1_MODE_NEXT: Optical Link 1 configuration.
36:37	RWX	PB_CFG_OPT2_MODE_NEXT: Optical Link 2 configuration.
38:39	RWX	PB_CFG_OPT3_MODE_NEXT: Optical Link 3 configuration.
40:46	RWX	PB_CFG_XLATE_ADDR_TO_ID_EAST_NEXT: Configures the translation of address to topology ID XOR mask.
47:48	RW	Reserved.
49	RWX	Reserved.
50	RWX	PB_CFG_A_GATHER_ENABLE_NEXT: Enable data OW gathering on A links.
51	RW	Reserved.
52	RWX	PB_CFG_PHYP_IS_GROUP_NEXT: Configures phyp boundary. 0 = phyp_is_system. 1 = phyp_is_group.
53	RWX	PB_CFG_ADDR_BAR_MODE_NEXT: Address BAR Mode. The SMP is limited to 2 or 4 sockets. When 1, pb_cfg_pump_mode must also be set to 1.
54	RWX	PB_CFG_PUMP_MODE_NEXT: configures the physical broadcast. 0 = Chip_is_node (Default). 1 = Chip_is_group.
55	RWX	PB_CFG_DCACHE_CAPP_MODE_NEXT: Dcache CAPP mode. 0 = off (Default). 1 = on.
56:63	RWX	PB_CFG_A_CMD_RATE_EAST_NEXT: Configures the paced command rate to not overrun the A link.

Register Name	**Power Bus PB East HP Mode Configuration Register**
Mnemonic	PB.COM.PB_EAST_HP_MODE_CURR
Address	000000000501200C (SCOM)
Description	00 = pb_cfg_east_master_chip 01 = pb_cfg_east_tm_master 02 = pb_cfg_east_chg_rate_gp_master 03 = pb_cfg_east_chg_rate_sp_master 04 = pb_cfg_east_link_a0_en 05 = pb_cfg_east_link_a1_en 06 = pb_cfg_east_link_a2_en 07 = pb_cfg_east_link_a3_en 08 = pb_cfg_east_na0_addr_dis 09 = pb_cfg_east_na1_addr_dis 10 = pb_cfg_east_na2_addr_dis 11 = pb_cfg_east_na3_addr_dis 12:15 = pb_cfg_east_link_a0_groupid 16:19 = pb_cfg_east_link_a1_groupid 20:23 = pb_cfg_east_link_a2_groupid 24:27 = pb_cfg_east_link_a3_groupid 28 = pb_cfg_east_a_aggregate 29 = pb_cfg_east_hop_mode 30 = pb_cfg_east_smp_optics_mode 31 = pb_cfg_east_capi_mode 32:33 = pb_cfg_east_opt0_mode 34:35 = pb_cfg_east_opt1_mode 36:37 = pb_cfg_east_opt2_mode 38:39 = pb_cfg_east_opt3_mode 40:46 = pb_cfg_east_xlate_addr_to_id 47:48 = spare 49 pb_cfg_east_a_indirect_en 50 = pb_cfg_east_a_gather_enable 51 = spare 52 = pb_cfg_east_phyp_is_group 53 = pb_cfg_east_addr_bar_mode 54 = pb_cfg_east_pump_mode 55 = pb_cfg_east_dcache_capp_mode 56:63 = pb_cfg_east_a_cmd_rate

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_CURR: Processor bus master.
1	RWX	PB_CFG_TM_MASTER_CURR: configure Chip as PB TM Master.
2	RWX	PB_CFG_CHG_RATE_GP_MASTER_CURR: Sets the Group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt.
3	RWX	PB_CFG_CHG_RATE_SP_MASTER_CURR: Sets the System pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt.
4	RWX	PB_CFG_LINK_A0_EN_CURR: Link A0 enabled.
5	RWX	PB_CFG_LINK_A1_EN_CURR: Link A1 enabled.
6	RWX	PB_CFG_LINK_A2_EN_CURR: Link A2 enabled.
7	RWX	PB_CFG_LINK_A3_EN_CURR: Link A3 enabled.
8	RWX	PB_CFG_LINK_NA0_ADDR_DIS_CURR: Link A0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NA1_ADDR_DIS_CURR: Link A1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NA2_ADDR_DIS_CURR: Link A2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NA3_ADDR_DIS_CURR: Link A3 address broadcast disabled.
12:15	RWX	PB_CFG_LINK_A0_GROUPID_CURR: Group ID of chip connected to A0 link.

Bits	SCOM	Field Mnemonic: Description
16:19	RWX	PB_CFG_LINK_A1_GROUPID_CURR: Group ID of chip connected to A1 link.
20:23	RWX	PB_CFG_LINK_A2_GROUPID_CURR: Group ID of chip connected to A2 link.
24:27	RWX	PB_CFG_LINK_A3_GROUPID_CURR: Group ID of chip connected to A3 link.
28	RWX	PB_CFG_A_AGGREGATE_CURR: Processor bus A links are configured as parallel buses to same chip.
29	RWX	PB_CFG_HOP_MODE_CURR: Sets SMP hop mode. 0 = 1-hop or 2-hop SMP topology. 1 = 3-hop SMP topology.
30	RWX	PB_CFG_SMP_OPTICS_MODE_CURR: Sets SMP optics mode. 0 = Optic Links are configured as X-bus SMP protocol. 1 = Optic Links are configured as A-bus SMP protocol.
31	RWX	PB_CFG_CAPI_MODE_CURR: Indicates a CAPI 2.0 link is attached in the SMP system.
32:33	RWX	PB_CFG_OPT0_MODE_CURR: Optical Link 0 configuration.
34:35	RWX	PB_CFG_OPT1_MODE_CURR: Optical Link 1 configuration.
36:37	RWX	PB_CFG_OPT2_MODE_CURR: Optical Link 2 configuration.
38:39	RWX	PB_CFG_OPT3_MODE_CURR: Optical Link 3 configuration.
40:46	RWX	PB_CFG_XLATE_ADDR_TO_ID_EAST_CURR: Configures the translation of address to topology ID XOR mask.
47:48	RW	Reserved.
49	RWX	Reserved.
50	RWX	PB_CFG_A_GATHER_ENABLE_CURR: Enable data OW gathering on A links.
51	RW	Reserved.
52	RWX	PB_CFG_PHYP_IS_GROUP_CURR: Configures phyp boundary. 0 = phyp_is_system 1 = phyp_is_group.
53	RWX	PB_CFG_ADDR_BAR_MODE_CURR: Address BAR Mode. The SMP is limited to 2 or 4 sockets. When 1, pb_cfg_pump_mode must also be set to 1.
54	RWX	PB_CFG_PUMP_MODE_CURR: configures the physical broadcast. 0 = Chip_is_node (Default). 1 = Chip_is_group.
55	RWX	PB_CFG_DCACHE_CAPP_MODE_CURR: Dcache CAPP mode. 0 = off (Default). 1 = on.
56:63	RWX	PB_CFG_A_CMD_RATE_EAST_CURR: Configures the paced command rate to not overrun the A link.

Register Name	**Power Bus PB East HP Mode Configuration Register**
Mnemonic	PB.COM.PB_EAST_HPA_MODE_NEXT
Address	000000000501200D (SCOM)
Description	00 = pb_cfg_east_link_x0toa0_en 01 = pb_cfg_east_link_x0toa1_en 02 = pb_cfg_east_link_x0toa2_en 03 = pb_cfg_east_link_x0toa3_en 04 = pb_cfg_east_link_x1toa0_en 05 = pb_cfg_east_link_x1toa1_en 06 = pb_cfg_east_link_x1toa2_en 07 = pb_cfg_east_link_x1toa3_en 08 = pb_cfg_east_link_x2toa0_en 09 = pb_cfg_east_link_x2toa1_en 10 = pb_cfg_east_link_x2toa2_en 11 = pb_cfg_east_link_x2toa3_en 12:15 = spare 16:19 = pb_cfg_east_link_x0toa0_groupid 20:23 = pb_cfg_east_link_x0toa1_groupid 24:27 = pb_cfg_east_link_x0toa2_groupid 28:31 = pb_cfg_east_link_x0toa3_groupid 32:35 = pb_cfg_east_link_x1toa0_groupid 36:39 = pb_cfg_east_link_x1toa1_groupid 40:43 = pb_cfg_east_link_x1toa2_groupid 44:47 = pb_cfg_east_link_x1toa3_groupid 48:51 = pb_cfg_east_link_x2toa0_groupid 52:55 = pb_cfg_east_link_x2toa1_groupid 56:59 = pb_cfg_east_link_x2toa2_groupid 60:63 = pb_cfg_east_link_x2toa3_groupid

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved.
1	RWX	Reserved.
2	RWX	Reserved.
3	RWX	Reserved.
4	RWX	Reserved.
5	RWX	Reserved.
6	RWX	Reserved.
7	RWX	Reserved.
8	RWX	Reserved.
9	RWX	Reserved.
10	RWX	Reserved.
11	RWX	Reserved.
12:15	RW	Reserved.
16:19	RWX	Reserved.
20:23	RWX	Reserved.
24:27	RWX	Reserved.
28:31	RWX	Reserved.
32:35	RWX	Reserved.
36:39	RWX	Reserved.

Bits	SCOM	Field Mnemonic: Description
40:43	RWX	Reserved.
44:47	RWX	Reserved.
48:51	RWX	Reserved.
52:55	RWX	Reserved.
56:59	RWX	Reserved.
60:63	RWX	Reserved.

Register Name	**Power Bus PB East HP Mode Configuration Register**
Mnemonic	PB.COM.PB_EAST_HPA_MODE_CURR
Address	000000000501200E (SCOM)
Description	00 = pb_cfg_east_link_x0toa0_en 01 = pb_cfg_east_link_x0toa1_en 02 = pb_cfg_east_link_x0toa2_en 03 = pb_cfg_east_link_x0toa3_en 04 = pb_cfg_east_link_x1toa0_en 05 = pb_cfg_east_link_x1toa1_en 06 = pb_cfg_east_link_x1toa2_en 07 = pb_cfg_east_link_x1toa3_en 08 = pb_cfg_east_link_x2toa0_en 09 = pb_cfg_east_link_x2toa1_en 10 = pb_cfg_east_link_x2toa2_en 11 = pb_cfg_east_link_x2toa3_en 12:15 = spare 16:19 = pb_cfg_east_link_x0toa0_groupid 20:23 = pb_cfg_east_link_x0toa1_groupid 24:27 = pb_cfg_east_link_x0toa2_groupid 28:31 = pb_cfg_east_link_x0toa3_groupid 32:35 = pb_cfg_east_link_x1toa0_groupid 36:39 = pb_cfg_east_link_x1toa1_groupid 40:43 = pb_cfg_east_link_x1toa2_groupid 44:47 = pb_cfg_east_link_x1toa3_groupid 48:51 = pb_cfg_east_link_x2toa0_groupid 52:55 = pb_cfg_east_link_x2toa1_groupid 56:59 = pb_cfg_east_link_x2toa2_groupid 60:63 = pb_cfg_east_link_x2toa3_groupid

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved.
1	RWX	Reserved.
2	RWX	Reserved.
3	RWX	Reserved.
4	RWX	Reserved.
5	RWX	Reserved.
6	RWX	Reserved.
7	RWX	Reserved.
8	RWX	Reserved.
9	RWX	Reserved.
10	RWX	Reserved.

Bits	SCOM	Field Mnemonic: Description
11	RWX	Reserved.
12:15	RW	Reserved.
16:19	RWX	Reserved.
20:23	RWX	Reserved.
24:27	RWX	Reserved.
28:31	RWX	Reserved.
32:35	RWX	Reserved.
36:39	RWX	Reserved.
40:43	RWX	Reserved.
44:47	RWX	Reserved.
48:51	RWX	Reserved.
52:55	RWX	Reserved.
56:59	RWX	Reserved.
60:63	RWX	Reserved.

Register Name	Power Bus PB East HP Mode Configuration Register
Mnemonic	PB.COM.PB_EAST_HPX_MODE_NEXT
Address	000000000501200F (SCOM)
Description	00 = pb_cfg_east_link_x0_en 01 = pb_cfg_east_link_x1_en 02 = pb_cfg_east_link_x2_en 03 = pb_cfg_east_link_x3_en 04 = pb_cfg_east_link_x4_en 05 = pb_cfg_east_link_x5_en 06 = pb_cfg_east_link_x6_en 07 = spare 08 pb_cfg_east_nx0_addr_dis 09 = pb_cfg_east_nx1_addr_dis 10 = pb_cfg_east_nx2_addr_dis 11 = pb_cfg_east_nx3_addr_dis 12 = pb_cfg_east_nx4_addr_dis 13 = pb_cfg_east_nx5_addr_dis 14 = pb_cfg_east_nx6_addr_dis 15 spare = 16:18 pb_cfg_east_link_x0_id(0:2) 19:21 = pb_cfg_east_link_x1_id(0:2) 22:24 = pb_cfg_east_link_x2_id(0:2) 25:27 = pb_cfg_east_link_x3_id(0:2) 28:30 = pb_cfg_east_link_x4_id(0:2) 31:33 = pb_cfg_east_link_x5_id(0:2) 34:36 = pb_cfg_east_link_x6_id(0:2) 37 = pb_cfg_east_x_aggregate 38:48 = spare 49 = pb_cfg_east_x_indirect_en 50 = pb_cfg_east_x_gather_enable 51:55 = spare 56:63 = pb_cfg_east_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_NEXT: Link X0 enabled.

Bits	SCOM	Field Mnemonic: Description
1	RWX	PB_CFG_LINK_X1_EN_NEXT: Link X1 enabled.
2	RWX	PB_CFG_LINK_X2_EN_NEXT: Link X2 enabled.
3	RWX	PB_CFG_LINK_X3_EN_NEXT: Link X3 enabled.
4	RWX	PB_CFG_LINK_X4_EN_NEXT: Link X4 enabled.
5	RWX	PB_CFG_LINK_X5_EN_NEXT: Link X5 enabled.
6	RWX	PB_CFG_LINK_X6_EN_NEXT: Link X6 enabled.
7	RW	Reserved.
8	RWX	PB_CFG_LINK_NX0_ADDR_DIS_NEXT: Link X0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NX1_ADDR_DIS_NEXT: Link X1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NX2_ADDR_DIS_NEXT: Link X2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NX3_ADDR_DIS_NEXT: Link X3 address broadcast disabled.
12	RWX	PB_CFG_LINK_NX4_ADDR_DIS_NEXT: Link X4 address broadcast disabled.
13	RWX	PB_CFG_LINK_NX5_ADDR_DIS_NEXT: Link X5 address broadcast disabled.
14	RWX	PB_CFG_LINK_NX6_ADDR_DIS_NEXT: Link X6 address broadcast disabled.
15	RW	Reserved.
16:18	RWX	PB_CFG_LINK_X0_CHIPID_NEXT: Chip ID of chip connected to X0 link.
19:21	RWX	PB_CFG_LINK_X1_CHIPID_NEXT: Chip ID of chip connected to X1 link.
22:24	RWX	PB_CFG_LINK_X2_CHIPID_NEXT: Chip ID of chip connected to X2 link.
25:27	RWX	PB_CFG_LINK_X3_CHIPID_NEXT: Chip ID of chip connected to X3 link.
28:30	RWX	PB_CFG_LINK_X4_CHIPID_NEXT: Chip ID of chip connected to X4 link.
31:33	RWX	PB_CFG_LINK_X5_CHIPID_NEXT: Chip ID of chip connected to X5 link.
34:36	RWX	PB_CFG_LINK_X6_CHIPID_NEXT: Chip ID of chip connected to X6 link.
37	RWX	PB_CFG_X_AGGREGATE_NEXT: Processor bus X links are configured as parallel buses to same chip.
38:47	RW	Reserved.
48	RW	PB_CFG_X_FP_DISABLED_NEXT: Processor bus X link RTAG fastpath disable.
49	RWX	PB_CFG_X_INDIRECT_EN_NEXT: Processor bus X links are configured for indirect data routing.
50	RWX	PB_CFG_X_GATHER_ENABLE_NEXT: Enable data OW gathering on X links.
51:55	RW	Reserved.
56:63	RWX	PB_CFG_X_CMD_RATE_EAST_NEXT: configures the paced command rate to not overrun the X link.

Register Name	**Power Bus PB East HP Mode Configuration Register**
Mnemonic	PB.COM.PB_EAST_HPX_MODE_CURR
Address	0000000005012010 (SCOM)
Description	00 = pb_cfg_east_link_x0_en 01 = pb_cfg_east_link_x1_en 02 = pb_cfg_east_link_x2_en 03 = pb_cfg_east_link_x3_en 04 = pb_cfg_east_link_x4_en 05 = pb_cfg_east_link_x5_en 06 = pb_cfg_east_link_x6_en 07 = spare 08 = pb_cfg_east_nx0_addr_dis 09 = pb_cfg_east_nx1_addr_dis 10 = pb_cfg_east_nx2_addr_dis 11 = pb_cfg_east_nx3_addr_dis 12 = pb_cfg_east_nx4_addr_dis 13 = pb_cfg_east_nx5_addr_dis 14 = pb_cfg_east_nx6_addr_dis 15 = spare 16:18 = pb_cfg_east_link_x0_id(0:2) 19:21 = pb_cfg_east_link_x1_id(0:2) 22:24 = pb_cfg_east_link_x2_id(0:2) 25:27 = pb_cfg_east_link_x3_id(0:2) 28:30 = pb_cfg_east_link_x4_id(0:2) 31:33 = pb_cfg_east_link_x5_id(0:2) 34:36 = pb_cfg_east_link_x6_id(0:2) 37 = pb_cfg_east_x_aggregate 38:48 = spare 49 = pb_cfg_east_x_indirect_en 50 = pb_cfg_east_x_gather_enable 51:55 = spare 56:63 pb_cfg_east_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_CURR: Link X0 enabled.
1	RWX	PB_CFG_LINK_X1_EN_CURR: Link X1 enabled.
2	RWX	PB_CFG_LINK_X2_EN_CURR: Link X2 enabled.
3	RWX	PB_CFG_LINK_X3_EN_CURR: Link X3 enabled.
4	RWX	PB_CFG_LINK_X4_EN_CURR: Link X4 enabled.
5	RWX	PB_CFG_LINK_X5_EN_CURR: Link X5 enabled.
6	RWX	PB_CFG_LINK_X6_EN_CURR: Link X6 enabled.
7	RW	Reserved.
8	RWX	PB_CFG_LINK_NX0_ADDR_DIS_CURR: Link X0 address broadcast disabled.
9	RWX	PB_CFG_LINK_NX1_ADDR_DIS_CURR: Link X1 address broadcast disabled.
10	RWX	PB_CFG_LINK_NX2_ADDR_DIS_CURR: Link X2 address broadcast disabled.
11	RWX	PB_CFG_LINK_NX3_ADDR_DIS_CURR: Link X3 address broadcast disabled.
12	RWX	PB_CFG_LINK_NX4_ADDR_DIS_CURR: Link X4 address broadcast disabled.
13	RWX	PB_CFG_LINK_NX5_ADDR_DIS_CURR: Link X5 address broadcast disabled.
14	RWX	PB_CFG_LINK_NX6_ADDR_DIS_CURR: Link X6 address broadcast disabled.
15	RW	Reserved.
16:18	RWX	PB_CFG_LINK_X0_CHIPID_CURR: Chip ID of chip connected to X0 link.

Bits	SCOM	Field Mnemonic: Description
19:21	RWX	PB_CFG_LINK_X1_CHIPID_CURR: Chip ID of chip connected to X1 link.
22:24	RWX	PB_CFG_LINK_X2_CHIPID_CURR: Chip ID of chip connected to X2 link.
25:27	RWX	PB_CFG_LINK_X3_CHIPID_CURR: Chip ID of chip connected to X3 link.
28:30	RWX	PB_CFG_LINK_X4_CHIPID_CURR: Chip ID of chip connected to X4 link.
31:33	RWX	PB_CFG_LINK_X5_CHIPID_CURR: Chip ID of chip connected to X5 link.
34:36	RWX	PB_CFG_LINK_X6_CHIPID_CURR: Chip ID of chip connected to X6 link.
37	RWX	PB_CFG_X_AGGREGATE_CURR: Processor bus X links are configured as parallel buses to same chip.
38:47	RW	Reserved.
48	RW	PB_CFG_X_FP_DISABLED_CURR: Processor bus X link RTAG fastpath disable.
49	RWX	PB_CFG_X_INDIRECT_EN_CURR: Processor bus X links are configured for indirect data routing.
50	RWX	PB_CFG_X_GATHER_ENABLE_CURR: Enable data OW gathering on X links.
51:55	RW	Reserved.
56:63	RWX	PB_CFG_X_CMD_RATE_EAST_CURR: Configures the paced command rate to not overrun the X link.

Register Name	Power Bus PB East Serial Configuration Load Register
Mnemonic	PB.COM.PB_EAST_SCONFIG_LOAD
Address	0000000005012011 (SCOM)
Description	00 = pb_cfg_sconfig_load 01 = pb_cfg_sconfig_slow 02:07 = pb_cfg_sconfig_shift_count 08:11 = pb_cfg_sconfig_select 12:63 = pb_cfg_sconfig_shift_data

Bits	SCOM	Field Mnemonic: Description
0	WOX	PB_CFG_EAST_SCONFIG_LOAD: Load Serial Mode Registers.
1	RWX	PB_CFG_EAST_SCONFIG_SLOW: Set Load of Serial Mode Registers to 16:1 slow clock.
2:7	WOX	PB_CFG_EAST_SCONFIG_SHIFT_COUNT: Configures length of Serial Mode Register.
8:11	RWX	PB_CFG_EAST_SCONFIG_SELECT: Select Serial Mode register: 0000 = pbh_pbiex_eh 0001 = pbh_pbiex_ex 0010 = pbh_dat_ex_req_pmac, 0011 = pbh_dat_em_req_pmac, 0100 = pbh_dat_arb_ex_pmac, 0101 = pbh_dat_arb_em_pmac.
12:63	RWX	PB_CFG_EAST_SCONFIG_SHIFT_DATA: Serial Mode Register Data.

Register Name	Power Bus PB East SPARE Configuration Register
Mnemonic	PB.COM.PB_EAST_SPARE
Address	0000000005012012 (SCOM)
Description	00:63 = pb_east_spare

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus PB East FW Scratch 0 Register
Mnemonic	PB.COM.PB_EAST_FW_SCRATCH0
Address	0000000005012013 (SCOM) 0000000005012014 (SCOM1) 0000000005012015 (SCOM2)
Description	00:63 = pb_east_fw_scratch0

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RWX	WOX_AND	WOX_OR	Reserved.

Register Name	Power Bus PB East FW Scratch 1 Register
Mnemonic	PB.COM.PB_EAST_FW_SCRATCH1
Address	0000000005012016 (SCOM) 0000000005012017 (SCOM1) 0000000005012018 (SCOM2)
Description	00:63 = pb_east_fw_scratch1

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RWX	WOX_AND	WOX_OR	Reserved.

Register Name	FBC PPE SCOM LFIR Register
Mnemonic	PB.PB_PPE.PB_PPE_LFIR
Address	0000000005012400 (SCOM) 0000000005012401 (SCOM1) 0000000005012402 (SCOM2)
Description	FBC_PPE_SCOM LFIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_PPE_INTERNAL_ERROR: PPE asserted an internally detected error condition that caused it to halt. This indication is intended to be reported to both Core PPM macros to be forwarded to the OCC complex as an error interrupt.
1	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_PPE_EXTERNAL_ERROR: PPE detected an error condition on an external interface to the Memory Bolt-on that caused it to halt. This indication is intended to be reported to both Core PPM macros to be forwarded to the OCC complex as an error interrupt.
2	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_PPE_PROGRESS_ERROR: PPE detected a lack of forward progress that caused it to halt.
3	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_PPE_BREAKPOINT_ERROR: PPE halted either upon a hardware debug or software-requested breakpoint event.
4	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_PPE_WATCHDOG: PPE asserted a watchdog timeout condition. Will likely be masked, for debug information only.
5	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_PPE_HALTED: PPE asserted a halt condition. Will likely be masked since there are several sources of halt that may be valid.
6	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_PPE_DEBUG_TRIGGER: PPE asserted a debug trigger.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
7	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_SRAM_UE: SRAM Uncorrectable Error. FBC_PPE will get a MCHK. Should be marked as as a recoverable error for Runtime Diagnostics reporting.
8	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_SRAM_CE: SRAM Correctable Error. FBC_PPE received corrected data, but SRAM content is bad until next scrub to that line. (Should be masked in the product; unmasked and marked as a recoverable error in manufacturing test).
9	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_SRAM_SCRUB_ERR: Scrub timer tick occurred when scrub is still pending.
10	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_BCE_ERROR: Block Copy Engine Error: Not applicable to the FBC_PPE.
11	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_SPARE11: Implemented but not used. Inputs tied to 0.
12	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_FIR_PARITY_ERR_DUP: Internal FIR parity error duplicate (same as fir_parity_err).
13	RWX	WOX_AND	WOX_OR	PB_PPE_LFIR_FIR_PARITY_ERR: Internal FIR parity error.
14:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	FBC PPE SCOM LFIR Mask Register
Mnemonic	PB.PB_PPE.PB_PPE_LFIRMASK
Address	0000000005012403 (SCOM) 0000000005012404 (SCOM1) 0000000005012405 (SCOM2)
Description	FBC_PPE_SCOM LFIR Mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:13	RW	WO_AND	WO_OR	PB_PPE_LFIRMASK_FIR_MASK: Mask for PPE asserted error conditions.
14:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	FBC PPE SCOM LFIR Action 0 Register
Mnemonic	PB.PB_PPE.PB_PPE_LFIRACT0
Address	0000000005012406 (SCOM)
Description	FBC_PPE_SCOM LFIR Action0

Bits	SCOM	Field Mnemonic: Description
0:13	RW	PB_PPE_LFIRACT0_FIR_ACTION0: MSB of action select for corresponding bit in FIR.
14:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	FBC_PPE_SCOM LFIR Action 1 Register
Mnemonic	PB.PB_PPE.PB_PPE_LFIRACT1
Address	0000000005012407 (SCOM)
Description	FBC_PPE_SCOM LFIR Action1

Bits	SCOM	Field Mnemonic: Description
0:13	RW	PB_PPE_LFIRACT1_FIR_ACTION1: LSB of action select for corresponding bit in FIR.
14:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	PPE Local SRAM Control Register
Mnemonic	PB.PB_PPE.PPE.ARB.CSCR
Address	000000000501240A (SCOM) 000000000501240B (SCOM1) 000000000501240C (SCOM2)
Description	PPE Local SRAM Control Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	CSCR_SRAM_ACCESS_MODE: SRAM Access Mode.
1	RWX	WOX_CLEAR	WOX_OR	CSCR_SRAM_SCRUB_ENABLE: Enable background scrub (atomic read-write) to periodically check, and if needed correct, the data in the SRAM for bit flips due to alpha particles. This bit is cleared by the hardware when a UE is detected to assist with fault analysis.
2	RW	WO_CLEAR	WO_OR	CSCR_ECC_CORRECT_DIS: Do not correct the data coming out of the array on ECC detected correctable errors. This will cause CEs to report an error back to the PPE in addition to the usual UEs.
3	RW	WO_CLEAR	WO_OR	CSCR_ECC_DETECT_DIS: Do not flag an error back to PPE for ECC miscompares. Data from the SRAM is always treated as good. Note that errors are always detected and reported to the FIR and must be masked there independently from this bit.
4	RW	WO_CLEAR	WO_OR	CSCR_ECC_INJECT_TYPE: Used only when ECC_INJECT_ERR is set. When set to 1, causes an ECC error to be reported on every SRAM read. When 0, causes a single ECC error to be indicated on the next SRAM read to occur, since it also clears ECC_INJECT_ERR when that happens.
5	RWX	WOX_CLEAR	WOX_OR	CSCR_ECC_INJECT_ERR: When set, the hardware will inject or cause a fake uncorrectable error (UE) to be reported to both the PPE and the FIR on all SRAM reads. The SRAM contents are not modified. Type of error to inject is determined by the previous bit. If ECC_INJECT_TYPE = 1, then this bit clears when the first error is injected. Note this bit can also be set by the PPE local register CFMSR.
6:7	RW	WO_CLEAR	WO_OR	CSCR_SPARE_6_7: Implemented but unused.
8:46	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000
47:59	RWX	WOX_CLEAR	WOX_OR	CSCR_SRAM_SCRUB_INDEX: 32KB Scrub Index. This field is auto-incremented by hardware for every scrub operation. Upon a UE detection, this field is over-written with the index of the doubleword containing the error. Note: SRAM_SCRUB_ENABLE should be set to 0 when writing this field to prevent one cycle window from ignoring this write if a scrub update happens to occur concurrently.
60:63	RO	RO	RO	Constant = 0b0000

Register Name	PPE Local SRAM Address Register
Mnemonic	PB.PB_PPE.PPE.ARB.CSAR
Address	000000000501240D (SCOM)
Description	PPE Local SRAM Address Register

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:28	RW	CSAR_SRAM_ADDRESS: Address of an 8B SRAM entry in the 32KB SRAM array.
29:63	RO	Constant = 0b00000000000000000000000000000000000000

Register Name	PPE Local SRAM Data Register
Mnemonic	PB.PB_PPE.PPE.ARB.CSDR
Address	000000000501240E (SCOM)
Description	PPE Local SRAM Data Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CSDR_SRAM_DATA: 8 B SRAM data entry for the address given by the SRAM_ADDRESS. Reads cause this register to be written with data from the Local SRAM. Writes cause the local SRAM to be written with the contents of this register.

Register Name	Power Bus Electrical Link Power Save Configuration Register
Mnemonic	PB.PB_PPE.PB_PSAVE_CFG
Address	000000000501241A (SCOM)
Description	Processor bus Electrical Link PowerSave Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	PSAVE_ENABLE: Enable power-saving mode. Cuts the link width in half during low-utilization periods.
1	WO_1P	X0_ACT: set to 1 to make X0 config reg be written with data from bit 5:39. This bit self-resets to 0.
2	WO_1P	X1_ACT: set to 1 to make X1 config reg be written with data from bit 5:39. This bit self-resets to 0.
3	WO_1P	X2_ACT: set to 1 to make X2 config reg be written with data from bit 5:39. This bit self-resets to 0.
4	RW	PS_SPARE1: ps spare1.
5:7	RW	PSAVE_WSIZE: psave sample window size - size = $2^{(n+8)}$ useable cycles. Generally, ~80% of the cycles are useable in normal mode (the other 20% are occupied by link overhead). When the link is in psave mode, the sample window size is automatically cut in half by the logic, which makes the psave sample window the same length of time as the normal window.
8:15	RW	PSAVE_LUC: psave Low Utilization Count - how many consecutive sample windows need to be below the low utilization threshold to kick the link into psave mode.
16:23	RW	PSAVE_HUC: psave High Utilization Count - how many consecutive sample windows need to be above the high utilization threshold to kick the link into normal mode.
24:26	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
27:31	RW	PSAVE_LUT: psave Low Utilization Threshold - if in normal mode, and utilization during a sample window is below (n+1)/32, (n = 0 to 31, 3.125% steps) increment the low utilization consecutive window counter. If above, reset it. Note: the logic only looks at the 5 most significant bits of interest, and thus is effectively doing a rounddown function when checking the utilization count against the threshold. The n+1 accounts for this behavior.
32:34	RW	Reserved.
35:39	RW	PSAVE_HUT: psave High Utilization Threshold - if in psave mode, and utilization during a sample window is above n/32, (n = 0 to 31, 3.125% steps) increment the high utilization consecutive window counter. If below, reset it. Note: the logic only looks at the 5 most significant bits of interest, and thus is effectively doing a rounddown function when checking the utilization count against the threshold, but the n/32 properly accounts for this behavior.

Register Name	Power Bus Electrical Link Power Save Monitor Register
Mnemonic	PB.PB_PPE.PB_PSAVE_MON_CFG
Address	000000000501241B (SCOM)
Description	Processor bus Electrical Link PowerSave Monitor Register

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 0b000
3:7	RW	X0_LO_MON: x0 low monitor - forms ratio (value+1)/32. If utilization is less than or equal to this ratio during a window, the lut_hist will post a 1 for the window.
8:10	RO	Constant = 0b000
11:15	RW	X0_HI_MON: x0 high monitor - forms ratio value/32. If utilization is greater than or equal to this ratio during a window, the hut_hist will post a 1 for the window.
16:18	RO	Constant = 0b000
19:23	RW	X1_LO_MON: x1 low monitor - forms ratio (value+1)/32. If utilization is less than or equal to this ratio during a window, the lut_hist will post a 1 for the window.
24:26	RO	Constant = 0b000
27:31	RW	X1_HI_MON: x1 high monitor - forms ratio value/32. If utilization is greater than or equal to this ratio during a window, the hut_hist will post a 1 for the window.
32:34	RO	Constant = 0b000
35:39	RW	X2_LO_MON: x2 low monitor - forms ratio (value+1)/32. If utilization is less than or equal to this ratio during a window, the lut_hist will post a 1 for the window.
40:42	RO	Constant = 0b000
43:47	RW	X2_HI_MON: x2 high monitor - forms ratio value/32. If utilization is greater than or equal to this ratio during a window, the hut_hist will post a 1 for the window.

Register Name	Power Bus Electrical Link Power Save X0 Even History Register
Mnemonic	PB.PB_PPE.PB_PSAVE_X0EVN_HIST
Address	000000000501241C (SCOM)
Description	The state of TDM/HUT/LUT in 3bit groupings for the past 16 windows, arranged in 3-bit groupings, oldest window starting at bit 0, most recent window starting at bit 45.

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
3:5	ROX	Reserved.
6:8	ROX	Reserved.
9:11	ROX	Reserved.
12:14	ROX	Reserved.
15:17	ROX	Reserved.
18:20	ROX	Reserved.
21:23	ROX	Reserved.
24:26	ROX	Reserved.
27:29	ROX	Reserved.
30:32	ROX	Reserved.
33:35	ROX	Reserved.
36:38	ROX	Reserved.
39:41	ROX	Reserved.
42:44	ROX	Reserved.
45:47	ROX	Reserved.

Register Name	Power Bus Electrical Link Power Save X0 Odd History Register
Mnemonic	PB.PB_PPE.PB_PSAVE_X0ODD_HIST
Address	000000000501241D (SCOM)
Description	The state of TDM/HUT/LUT in 3bit groupings for the past 16 windows, arranged in 3-bit groupings, oldest window starting at bit 0, most recent window starting at bit 45.

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	Reserved.
3:5	ROX	Reserved.
6:8	ROX	Reserved.
9:11	ROX	Reserved.
12:14	ROX	Reserved.
15:17	ROX	Reserved.
18:20	ROX	Reserved.
21:23	ROX	Reserved.
24:26	ROX	Reserved.
27:29	ROX	Reserved.
30:32	ROX	Reserved.
33:35	ROX	Reserved.
36:38	ROX	Reserved.
39:41	ROX	Reserved.
42:44	ROX	Reserved.
45:47	ROX	Reserved.

Register Name	Power Bus Electrical Link Power Save X1 Even History Register
Mnemonic	PB.PB_PPE.PB_PSAVE_X1EVN_HIST
Address	000000000501241E (SCOM)
Description	The state of TDM/HUT/LUT in 3bit groupings for the past 16 windows, arranged in 3-bit groupings, oldest window starting at bit 0, most recent window starting at bit 45.

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	Reserved.
3:5	ROX	Reserved.
6:8	ROX	Reserved.
9:11	ROX	Reserved.
12:14	ROX	Reserved.
15:17	ROX	Reserved.
18:20	ROX	Reserved.
21:23	ROX	Reserved.
24:26	ROX	Reserved.
27:29	ROX	Reserved.
30:32	ROX	Reserved.
33:35	ROX	Reserved.
36:38	ROX	Reserved.
39:41	ROX	Reserved.
42:44	ROX	Reserved.
45:47	ROX	Reserved.

Register Name	Power Bus Electrical Link Power Save X1 Odd History Register
Mnemonic	PB.PB_PPE.PB_PSAVE_X1ODD_HIST
Address	000000000501241F (SCOM)
Description	The state of TDM/HUT/LUT in 3bit groupings for the past 16 windows, arranged in 3-bit groupings, oldest window starting at bit 0, most recent window starting at bit 45.

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	Reserved.
3:5	ROX	Reserved.
6:8	ROX	Reserved.
9:11	ROX	Reserved.
12:14	ROX	Reserved.
15:17	ROX	Reserved.
18:20	ROX	Reserved.
21:23	ROX	Reserved.
24:26	ROX	Reserved.
27:29	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
30:32	ROX	Reserved.
33:35	ROX	Reserved.
36:38	ROX	Reserved.
39:41	ROX	Reserved.
42:44	ROX	Reserved.
45:47	ROX	Reserved.

Register Name	Power Bus Electrical Link Power Save X2 Even History Register
Mnemonic	PB.PB_PPE.PB_PSAVE_X2EVN_HIST
Address	0000000005012420 (SCOM)
Description	The state of TDM/HUT/LUT in 3bit groupings for the past 16 windows, arranged in 3-bit groupings, oldest window starting at bit 0, most recent window starting at bit 45.

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	Reserved.
3:5	ROX	Reserved.
6:8	ROX	Reserved.
9:11	ROX	Reserved.
12:14	ROX	Reserved.
15:17	ROX	Reserved.
18:20	ROX	Reserved.
21:23	ROX	Reserved.
24:26	ROX	Reserved.
27:29	ROX	Reserved.
30:32	ROX	Reserved.
33:35	ROX	Reserved.
36:38	ROX	Reserved.
39:41	ROX	Reserved.
42:44	ROX	Reserved.
45:47	ROX	Reserved.

Register Name	Power Bus Electrical Link Power Save X2 Odd History Register
Mnemonic	PB.PB_PPE.PB_PSAVE_X2ODD_HIST
Address	0000000005012421 (SCOM)
Description	The state of TDM/HUT/LUT in 3bit groupings for the past 16 windows, arranged in 3-bit groupings, oldest window starting at bit 0, most recent window starting at bit 45.

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	Reserved.
3:5	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
6:8	ROX	Reserved.
9:11	ROX	Reserved.
12:14	ROX	Reserved.
15:17	ROX	Reserved.
18:20	ROX	Reserved.
21:23	ROX	Reserved.
24:26	ROX	Reserved.
27:29	ROX	Reserved.
30:32	ROX	Reserved.
33:35	ROX	Reserved.
36:38	ROX	Reserved.
39:41	ROX	Reserved.
42:44	ROX	Reserved.
45:47	ROX	Reserved.

Register Name	TX and Common Control Status Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_CTRL_STAT_REG
Address	0000000005012800 (SCOM)
Description	TX and Common Control Status Register

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_SCWR_TO_TXRF: OFF: Disable SCOM write to TX RF. ON: Enable SCOM write to TX RF.
1	RW	DISABLE_ECC_COR_GXC_PSI: OFF: Enable ECC Correction GXC PSI. ON: Disable ECC Correction GXC PSI.
2	RW	DISABLE_ECC_COR_TXRF_PSI: OFF: Enable ECC Correction TXRF PSI. ON: Disable ECC Correction TXRF PSI.
3	RW	TX_CRC_MODE: OFF: TX_CRC-16 Mode. ON: TX_CRC-32 Mode.
4	RW	TX_CHIP_PERSONALISATION: OFF: TX Processor Chip. ON: TX FSP-1 Chip.
5	RW	TX_ENABLE_STREAMING_MODE: OFF: TX Disable Streaming Mode. ON: TX Enable Streaming Mode.
6	RW	TX_CHIP_INTERFACEMODE: ON: Processor Chip. ON: FSP-1 Chip.
7	RW	DISABLE_TIMEOUT_AND_RETRY: OFF: Enable Timeout and Retry Function. ON: Disable Timeout and Retry Function.
8	RW	FENCE_IO_INTERFACE: OFF: no fence I/O interface. ON: Fence the I/O interface.
9	RW	FENCE_GX_INTERFACE: OFF: no fence gx interface. ON: Fence the gx interface.
10	RW	GX_ENABLE_OVERWRITE: OFF: no gx_enable_overwrite. ON: gx_enable_overwrite.

Bits	SCOM	Field Mnemonic: Description
11	RW	Reserved.
12:31	RO	Constant = 0b00000000000000000000

Register Name	TX Timeout Retry Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_TO_RT_REG
Address	0000000005012801 (SCOM)
Description	TX Timeout Retry Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	TX_TIMEOUT_VALUE: Defines timout value, for example: 2exp17*(nclk*2) = 104,8576us (@ 5 GHz core frequency).
4:7	RW	TX_RETRY_VALUE: Defines retry value.
8:31	RO	Constant = 0b00000000000000000000000000

Register Name	TX Error Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_ERROR_REG
Address	0000000005012802 (SCOM) 0000000005012804 (SCOM1)
Description	TX Error Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	RWX_WCLEAR	WOX_OR	Reserved.
1	RWX_WCLEAR	WOX_OR	Reserved.
2	RWX_WCLEAR	WOX_OR	Reserved.
3	RWX_WCLEAR	WOX_OR	Reserved.
4	RWX_WCLEAR	WOX_OR	Reserved.
5	RWX_WCLEAR	WOX_OR	Reserved.
6	RWX_WCLEAR	WOX_OR	Reserved.
7	RWX_WCLEAR	WOX_OR	Reserved.
8	RWX_WCLEAR	WOX_OR	Reserved.
9	RWX_WCLEAR	WOX_OR	Reserved.
10	RWX_WCLEAR	WOX_OR	Reserved.

Bits	SCOM	SCOM1	Field Mnemonic: Description
11	RWX_WCLEAR	WOX_OR	Reserved.
12	RWX_WCLEAR	WOX_OR	Reserved.
13	RWX_WCLEAR	WOX_OR	Reserved.
14	RWX_WCLEAR	WOX_OR	Reserved.
15	RWX_WCLEAR	WOX_OR	Reserved.
16	RWX_WCLEAR	WOX_OR	Reserved.
17	RWX_WCLEAR	WOX_OR	Reserved.
18	RWX_WCLEAR	WOX_OR	Reserved.
19	RWX_WCLEAR	WOX_OR	Reserved.
20	RWX_WCLEAR	WOX_OR	Reserved.
21	RWX_WCLEAR	WOX_OR	Reserved.
22	RWX_WCLEAR	WOX_OR	Reserved.
23	RWX_WCLEAR	WOX_OR	Reserved.
24	RWX_WCLEAR	WOX_OR	Reserved.
25	RWX_WCLEAR	WOX_OR	Reserved.
26	RWX_WCLEAR	WOX_OR	Reserved.
27	RWX_WCLEAR	WOX_OR	Reserved.
28:31	RO	RO	Constant = 0b0000

Register Name	TX Mask Error Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_MASK_REG
Address	0000000005012803 (SCOM)
Description	TX Mask Error Register

Bits	SCOM	Field Mnemonic: Description
0	RO	PSITXINS_DATA_PCK_MASK:
1	RO	PSITXINS_TZRTMP_PCK_MASK:
2	RO	PSITXEI_SHIFT_PCK_MASK:

Bits	SCOM	Field Mnemonic: Description
3	RO	PSITXEI_TRANSMIT_PCK_MASK:
4	RO	PSITXINS_PARITY_MASK:
5	RO	PSITXINS_UNDERRUN_MASK:
6	RO	PSITXBFF_DATA_PCK_MASK:
7	RO	PSITXBFF_TDO_PCK_MASK:
8	RO	PSITXBFF_TFC_PCK_MASK:
9	RO	PSITXLC_FSM_PCK_MASK:
10	RO	PSITXLC_DATA_BUFF_PCK_MASK:
11	RO	PSITXLC_TDO_PCK_MASK:
12	RO	PSITXLC_TADDR_PCK_MASK:
13	RO	PSITXLC_TCTRL_PCK_MASK:
14	RO	PSITXLC_UE_RF_MASK:
15	RO	PSITXLC_CE_RF_MASK:
16	RO	PSITXLC_UE_GX_2N_MASK:
17	RO	PSITXLC_CE_GX_2N_MASK:
18	RO	PSITXLC_DATA_GXST2_PCK_2N_MASK:
19	RO	PSITXLC_DATA_GXST3_PCK_2N_MASK:
20	RO	PSIRFACC_TADDR_PCK_MASK:
21	RO	PSIRFACC_TCTRL_PCK_MASK:
22	RO	PSIRFACC_TDL_CMD_CTRL_PCK_MASK:
23	RO	PSIRFACC_TDL_RSP_CTRL_PCK_MASK:
24	RO	PSIRFACC_TFSM_PCK_MASK:
25	RO	PSIRFACC_TDL_FSM_PCK_MASK:
26	RO	PSIRFACC_TXSC_PCK_MASK:
27	RO	PSIRFACC_TDL_RETRY_ERR_MASK:
28:31	RO	Constant = 0b0000

Register Name	**TX Channel FSM Register**
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_CH_FSM_REG
Address	0000000005012805 (SCOM)
Description	TX Channel FSM

Bits	SCOM	Field Mnemonic: Description
0:2	RWX	Reserved.
3:31	RO	Constant = 0b00000000000000000000000000000

Register Name	TX Data Flow FSM Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_DF_FSM_REG
Address	0000000005012806 (SCOM)
Description	TX Data Flow FSM

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	Reserved.
4:31	RO	Constant = 0b00000000000000000000000000000000

Register Name	TX Error Inject Mode Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_ERR_MODE
Address	0000000005012807 (SCOM)
Description	TX Error Inject Mode

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1	RW	Reserved.
2:31	RO	Constant = 0b00000000000000000000000000000000

Register Name	RX Control Status Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_CTRL_STAT_REG
Address	0000000005012808 (SCOM)
Description	RX Control Status Register

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_SCWR_TO_RXRF: OFF: Disable SCOM write to RX RF. ON: Enable SCOM write to RX RF.
1	RW	Reserved.
2	RW	DISABLE_ECC_COR_RXRF_PSI: OFF: Enable ECC Correction RXRF PSI. ON: Disable ECC Correction RXRF PSI.
3	RW	RX_CRC_MODE: OFF: RX_CRC-16 Mode. ON: RX_CRC-32 Mode.
4	RW	ENABLE_SCRD_FR_RXRF: OFF: Disable SCOM read from RX RF. ON: Enable SCOM read from RX RF.
5	RW	RX_ENABLE_STREAMING_MODE: OFF: RX Disable Streaming Mode. ON: RX Enable Streaming Mode.
6	RW	RX_CHIP_INTERFACEMODE: ON: RX Processor Chip. ON: RX FSP-1 Chip.
7	RW	RX_CHIP_PERSONALISATION: OFF: RX Processor Chip. ON: RX FSP-1 Chip.
8:31	RO	Constant = 0b00000000000000000000000000

Register Name	Error Event Counter Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.EECNT_REG
Address	0000000005012809 (SCOM)
Description	Error Event Counter

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	Reserved.
6:31	RO	Constant = 0b00000000000000000000000000

Register Name	RX Error Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_ERROR_REG
Address	000000000501280A (SCOM) 000000000501280C (SCOM1)
Description	RX Error Register

Bits	SCOM	SCOM1	Field Mnemonic: Description
0	RWX_WCLEAR	WOX_OR	Reserved.
1	RWX_WCLEAR	WOX_OR	Reserved.
2	RWX_WCLEAR	WOX_OR	Reserved.
3	RWX_WCLEAR	WOX_OR	Reserved.
4	RWX_WCLEAR	WOX_OR	Reserved.
5	RWX_WCLEAR	WOX_OR	Reserved.
6	RWX_WCLEAR	WOX_OR	Reserved.
7	RWX_WCLEAR	WOX_OR	Reserved.
8	RWX_WCLEAR	WOX_OR	Reserved.
9	RWX_WCLEAR	WOX_OR	Reserved.
10	RWX_WCLEAR	WOX_OR	Reserved.
11	RWX_WCLEAR	WOX_OR	Reserved.
12	RWX_WCLEAR	WOX_OR	Reserved.
13	RWX_WCLEAR	WOX_OR	Reserved.
14	RWX_WCLEAR	WOX_OR	Reserved.

Bits	SCOM	SCOM1	Field Mnemonic: Description
15	RWX_WCLEAR	WOX_OR	Reserved.
16	RWX_WCLEAR	WOX_OR	Reserved.
17	RWX_WCLEAR	WOX_OR	Reserved.
18	RWX_WCLEAR	WOX_OR	Reserved.
19	RWX_WCLEAR	WOX_OR	Reserved.
20	RWX_WCLEAR	WOX_OR	Reserved.
21	RWX_WCLEAR	WOX_OR	Reserved.
22	RWX_WCLEAR	WOX_OR	Reserved.
23	RWX_WCLEAR	WOX_OR	Reserved.
24	RWX_WCLEAR	WOX_OR	Reserved.
25:31	RO	RO	Constant = 0b0000000

Register Name	RX Mask Error Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_MASK_REG
Address	0000000005012808 (SCOM)
Description	RX Mask Error Register

Bits	SCOM	Field Mnemonic: Description
0	RO	PSIRXINS_RFGSHIFT_PCK_MASK:
1	RO	PSIRXINS_RZRTMP_PCK_MASK:
2	RO	PSIRXINS_DATA_PCK_MASK:
3	RO	PSIRXEI_SHIFT_PCK_MASK:
4	RO	PSIRXEI_TRANSMIT_PCK_MASK:
5	RO	PSIRXINS_OVERRUN_MASK:
6	RO	PSIRXBFF_DATA_PCK_MASK:
7	RO	PSIRXBFF_DATAO_PCK_MASK:
8	RO	PSIRXBFF_RFC_PCK_MASK:
9	RO	PSIRXLC_FSM_PCK_MASK:
10	RO	PSIRXLC_DATA_BUFF_PCK_MASK:
11	RO	PSIRXLC_DATA_PCK_MASK:
12	RO	PSIRXLC_RADDR_PCK_MASK:
13	RO	PSIRXLC_RCTRL_PCK_MASK:
14	RO	PSIRXLC_UE_RF_MASK:

Bits	SCOM	Field Mnemonic: Description
15	RO	PSIRXLC_CE_RF_MASK:
16	RO	PSIRXLC_DATA_GXST1_PCK_2N_MASK:
17	RO	PSIRFACC_RADDR_PCK_MASK:
18	RO	PSIRFACC_RCTRL_PCK_MASK:
19	RO	PSIRFACC_RFSM_PCK_MASK:
20	RO	PSIRFACC_RDL_FSM_PCK_MASK:
21	RO	PSIRFACC_RXSC_PCK_MASK:
22	RO	PSIRFACC_RLINK_STATE_LT_02_MASK:
23	RO	PSIRFACC_C_RXDATA_RDY_ERR_MASK:
24	RO	Reserved.
25:31	RO	Constant = 0b0000000

Register Name	RX Channel FSM Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_CH_FSM_REG
Address	000000000501280D (SCOM)
Description	RX Channel FSM

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	Reserved.
2:31	RO	Constant = 0b00000000000000000000000000000000

Register Name	RX Data Flow FSM Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_DF_FSM_REG
Address	000000000501280E (SCOM)
Description	RX Data Flow FSM

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	Reserved.
4:31	RO	Constant = 0b00000000000000000000000000000000

Register Name	RX Error Inject Mode Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_ERR_MODE
Address	000000000501280F (SCOM)
Description	RX Error Inject Mode

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1	RW	Reserved.
2:31	RO	Constant = 0b00000000000000000000000000000000

Register Name	TX Channel Internal Address Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_CH_INTADDR_REG
Address	0000000005012810 (SCOM)
Description	TX Channel Internal Address Register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1	RW	Reserved.
2	RW	Reserved.
3	RW	Reserved.
4	RW	Reserved.
5	RW	Reserved.
6	RW	Reserved.
7	RW	Reserved.
8:31	RO	Constant = 0b00000000000000000000000

Register Name	TX Channel Data Buffer 0 Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_DBFF_REG0
Address	0000000005012811 (SCOM)
Description	TX Channel Data Buffer Register0

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved.

Register Name	TX Channel Data Buffer 1 Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_DBFF_REG1
Address	0000000005012812 (SCOM)
Description	TX Channel Data Buffer Register1

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved.

Register Name	TX Channel Miscellaneous Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.TX_CH_MISC_REG
Address	0000000005012813 (SCOM)
Description	TX Channel Misc Register

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	Reserved.

Bits	SCOM	Field Mnemonic: Description
4:6	RO	Constant = 0b000
7:11	RWX	Reserved.
12	RWX	Reserved.
13	RWX	Reserved.
14	RWX	Reserved.
15	RWX	Reserved.
16	RWX	Reserved.
17	RWX	Reserved.
18:31	RO	Constant = 0b00000000000000

Register Name	RX Channel Internal Address Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_CH_INTADDR_REG
Address	0000000005012818 (SCOM)
Description	RX Channel Internal Address Register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1	RW	Reserved.
2	RW	Reserved.
3	RW	Reserved.
4	RW	Reserved.
5	RW	Reserved.
6	RW	Reserved.
7	RW	Reserved.
8:31	RO	Constant = 0b00000000000000000000000000

Register Name	RX Channel Data Buffer 0 Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_DBFF_REG0
Address	0000000005012819 (SCOM)
Description	RX Channel Data Buffer Register0

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved.

Register Name	RX Channel Data Buffer 1 Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_DBFF_REG1
Address	000000000501281A (SCOM)
Description	RX Channel Data Buffer Register1

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	Reserved.

Register Name	RX Channel Miscellaneous Register
Mnemonic	BRIDGE.PSI.PSI_WRAP.RX_CH_MISC_REG
Address	000000000501281B (SCOM)
Description	RX Channel Misc Register

Bits	SCOM	Field Mnemonic: Description
0:2	RWX	Reserved.
3:6	RWX	Reserved.
7:11	RWX	Reserved.
12	RWX	Reserved.
13	RWX	Reserved.
14	RWX	Reserved.
15	RWX	Reserved.
16	RWX	Reserved.
17:31	RO	Constant = 0b000000000000000

Register Name	PBA Local Fault Isolation Register
Mnemonic	BRIDGE.PBA.PBAFIR
Address	0000000005012840 (SCOM) 0000000005012841 (SCOM1) 0000000005012842 (SCOM2)
Description	PBA Local Fault Isolation Register. Register bits are set for any error condition detected by the PBA. The PBAFIR will freeze upon logging the first error not masked in PBAFIRMASK.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PBAFIR_OCI_APAR_ERR: OCI Address Parity Error Det Address parity error detected by PBA OCI Slave logic for any valid address. OCI Operation is ignored.
1	RWX	WOX_AND	WOX_OR	PBAFIR_PB_RDADRERR_FW: PB CRESP Addr Error Received for Forwarded Read Request. processor bus request by PBA for a forwarded OCI Read Request received a CRESP error response. See PBAERRRPT0 for per-queue information. The Buffer allocated for this request will continue unless PBACFG[chsw_hang_on_adrerror] = 1. addr_error combined response.
2	RWX	WOX_AND	WOX_OR	PBAFIR_PB_RDDATATO_FW: PB Read Data Timeout for Forwarded Request processor bus Read Request for a forwarded OCI Request timed out waiting for data. PBA is reporting a data hang condition to the processor bus. The Buffer allocated for this request is hung and may be reset by following the PBA Slave Reset Sequence. See PBAERRRPT0 for per-queue information.
3	RWX	WOX_AND	WOX_OR	PBAFIR_PB_SUE_FW: PB Read Data SUE Error for Forwarded Request processor bus Read data for a forwarded OCI Request contained SUE Error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
4	RWX	WOX_AND	WOX_OR	PBAFIR_PB_UE_FW: PB Read Data UE Error for Forwarded Request processor bus Read data for a forwarded OCI Request contained UE Error.
5	RWX	WOX_AND	WOX_OR	PBAFIR_PB_CE_FW: PB Read Data CE Error for Forwarded Request processor bus Read data for a forwarded OCI Request contained CE Error.
6	RWX	WOX_AND	WOX_OR	PBAFIR_OCI_SLAVE_INIT: PBA OCI Slave Initialization Error This is asserted when the upper two OCI address bits indicate they target the PBA Slave but the PBA slave is not setup properly. : No buffer allocated in targetted PBASLVCTLn PBASLVCTLn not enabled for master_id Multiple PBASLVCTLn are enabled for a master_id.
7	RWX	WOX_AND	WOX_OR	PBAFIR_OCI_WRPAR_ERR: OCI Write Data Parity Error Detected Data parity error detected by PBA OCI Slave logic. This write and any previous gathered writes are not forwarded.
8	RWX	WOX_AND	WOX_OR	PBAFIR_Reserved_8: Spare -was OCI Re-Request Timeout.
9	RWX	WOX_AND	WOX_OR	PBAFIR_PB_UNEXPCRESP: PB Unexpected CRESP processor bus Combined Response was received unexpectedly with PBA transfer tag. . Response is ignored. See PBAERRRPT0 for per-queue information.
10	RWX	WOX_AND	WOX_OR	PBAFIR_PB_UNEXPDATA: PB Unexpected Data processor bus data received for transaction ID that was not expecting data. Data is ignored. This does not check for duplicate OW_ID. See PBAERRRPT0 for per-queue information.
11	RWX	WOX_AND	WOX_OR	PBAFIR_PB_PARITY_ERR: PB Tag parity Error Detected Powerbus CRESP TTAG, ATAG, or DPX RTAG Parity error detected. FIR set only.
12	RWX	WOX_AND	WOX_OR	PBAFIR_PB_WRADRERR_FW: PB CRESP Addr Error Received for Forwarded Write Request processor bus request by PBA for a forwarded OCI Write Request received a CRESP error response. See PBAERRRPT0 for per-queue information. addr_error combined response.
13	RWX	WOX_AND	WOX_OR	PBAFIR_PB_BADCRESP: PB Invalid CRESP An invalid CRESP was received for a pending request. PBA will retry the request unless PBACFG[chsw_hang_on_invalid_cresp] = 1. See PBAERRRPT1 for per-queue information.
14	RWX	WOX_AND	WOX_OR	PBAFIR_PB_ACKDEAD_FW_RD: PB CRESP ACK Dead response received for Forwarded Read request to a foreign link. The Buffer allocated for this request will continue unless PBACFG[chsw_hang_on_adrerror] = 1. See PBAERRRPT0 for per-queue information.
15	RWX	WOX_AND	WOX_OR	PBAFIR_PB_OPERTO: PB OPERATIONAL Timeout detected when PBACFG[EXIT_ON_HANG] = 1. The processor bus request is terminated so the OCI request can complete. See PBAERRRPT1 for per queue information.
16	RWX	WOX_AND	WOX_OR	PBAFIR_BCUE_SETUP_ERR: BCUE Setup Error Block Copy Unload Engine Setup Errors. See PBAERRRPT1. Unexpected 'Start' received while running Timeout Response for OCI Request.
17	RWX	WOX_AND	WOX_OR	PBAFIR_BCUE_PB_ACK_DEAD: BCUE processor bus Link Dead ack_dead combined response for processor bus Write.
18	RWX	WOX_AND	WOX_OR	PBAFIR_BCUE_PB_ADRERR: PB CRESP Addr Error Received for BCUE Write Request addr_error combined response.
19	RWX	WOX_AND	WOX_OR	PBAFIR_BCUE_OCI_DATERR: BCUE Read Data Parity Error OR MRDERR Asserted Block Copy Unload Engine detected parity error on read data from the OCI.
20	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_SETUP_ERR: BCDE Setup Error Block Copy Download Engine Setup Errors. See PBAERRRPT1 Unexpected 'Start' received while running Timeout Response for OCI Request (OCI Address error).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
21	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_PB_ACK_DEAD: BCDE processor bus Link Dead ack_dead combined response for processor bus Read.
22	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_PB_ADRERR: PB CRESP Addr Error Received for BCDE Read Request addr_error combined response.
23	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_RDDATATO_ERR: PB Read Data Timeout for BCDE Request processor bus Read Request for a BCDE Request timed out waiting for data. Timer is based on the hang pulse.
24	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_SUE_ERR: PB Read Data SUE Error for BCDE Request processor bus Read data for a BCDE Request contained SUE Error.
25	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_UE_ERR: PB Read Data UE Error for BCDE Request processor bus Read data for a BCDE Request contained UE Error.
26	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_CE: PB Read Data CE Error for BCDE Request processor bus Read data for a BCDE Request contained CE Error.
27	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_OCI_DATERR: BCDE Write Data error indicated by OCI Slave Block Copy Download Engine received WRDERR indication from OCI Slave.
28	RWX	WOX_AND	WOX_OR	PBAFIR_INTERNAL_ERR: Internal Logic Error. See PBAERRRPT2 for more detailed information.
29	RWX	WOX_AND	WOX_OR	PBAFIR_ILLEGAL_CACHE_OP: Byte count is less than full cache line: Write operation did not start gathering on a cache line boundary OR the write address was not contiguous before writing the full cache line.
30	RWX	WOX_AND	WOX_OR	PBAFIR_OCI_BAD_REG_ADDR: Illegal access to OCI Register. Invalid address, read to write-only, write to read-only.
31	RWX	WOX_AND	WOX_OR	PBAFIR_AXPUSH_WRERR: Push Write Error. Push queue did not get OCI ADDRACK for push write request. Either the address is invalid or the targeted detected and address parity error. See PBAERRRPT2 for per queue information.
32	RWX	WOX_AND	WOX_OR	PBAFIR_AXRCV_DLO_ERR: PBAXRCV Low data before High Data. See PBAXRCVSTAT[rcv_capture] for more information.
33	RWX	WOX_AND	WOX_OR	PBAFIR_AXRCV_DLO_TO: PBAXRCV Low data timeout. See PBAXRCVSTAT[rcv_capture] for more information.
34	RWX	WOX_AND	WOX_OR	PBAFIR_AXRCV_RSVDATA_TO: PBAXRCV Reservation data timeout. Reservation acquired but phase1 data never seen. This could happen if PBAXSND is unable to get access to the processor bus. See PBAXRCVSTAT[rcv_capture] for more information.
35	RWX	WOX_AND	WOX_OR	PBAFIR_AXFLOW_ERR: Illegal PBAX Flow. See PBAERRRPT2 for more info. Write to PBAXSNDTX when PBAXSNDSTAT[snd_in_progress] = 1 OR PBAXCFG[pbax_en] = 0 Per queue Push queue underflow: Store to PBAXSHINC when PBAXSHCS[push_empty]. Per queue Push queue overflow: PBAXRCV decode but Push Q is full.
36	RWX	WOX_AND	WOX_OR	PBAFIR_AXSND_DHI_RTYTO: PBAXSND engine retry threshold reached sending Phase 1.
37	RWX	WOX_AND	WOX_OR	PBAFIR_AXSND_DLO_RTYTO: PBAXSND engine retry threshold reached sending Phase 2.
38	RWX	WOX_AND	WOX_OR	PBAFIR_AXSND_RSVTO: PBAXSND Reservation Timeout.
39	RWX	WOX_AND	WOX_OR	PBAFIR_AXSND_RSVERR: PBAXSND Reservation Error. Reservation request and Reservations not enabled, push queue not enabled, or push queue is full.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
40	RWX	WOX_AND	WOX_OR	PBAFIR_PB_ACKDEAD_FW_WR: PB CRESP ACK Dead response received for Forwarded Write request to a foreign link. The Buffer allocated for this request will continue unless PBACFG[chsw_hang_on_adrerror] = 1. See PBAERRRPT0 for per-queue information.
41	RWX	WOX_AND	WOX_OR	PBAFIR_Reserved_41: Spare.
42	RWX	WOX_AND	WOX_OR	PBAFIR_Reserved_42: Spare.
43	RWX	WOX_AND	WOX_OR	PBAFIR_Reserved_43: Spare.
44	RWX	WOX_AND	WOX_OR	PBAFIR_FIR_PARITY_ERR2: Internal FIR parity error duplicate.
45	RWX	WOX_AND	WOX_OR	PBAFIR_FIR_PARITY_ERR: nternal FIR parity error.
46:63	RO	RO	RO	Constant = 0b0000000000000000

Register Name	PBA Local Fault Isolation Mask Register
Mnemonic	BRIDGE.PBA.PBAFIRMASK
Address	0000000005012843 (SCOM) 0000000005012844 (SCOM1) 0000000005012845 (SCOM2)
Description	PBA Local Fault Isolation Mask Register. Reset value of PBAFIRMSK set according to RAS FIR Review for DD1.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	PBAFIRMASK_OCI_APAR_ERR_MASK: oci_apar_err_mask.
1	RW	WO_AND	WO_OR	PBAFIRMASK_PB_RDADRERR_FW_MASK: pb_rdadrerr_fw_mask.
2	RW	WO_AND	WO_OR	PBAFIRMASK_PB_RDDATATO_FW_MASK: pb_rddatato_fw_mask.
3	RW	WO_AND	WO_OR	PBAFIRMASK_PB_SUE_FW_MASK: pb_sue_fw_mask.
4	RW	WO_AND	WO_OR	PBAFIRMASK_PB_UE_FW_MASK: pb_ue_fw_mask.
5	RW	WO_AND	WO_OR	PBAFIRMASK_PB_CE_FW_MASK: pb_ce_fw_mask.
6	RW	WO_AND	WO_OR	PBAFIRMASK_OCI_SLAVE_INIT_MASK: oci_slave_init_mask.
7	RW	WO_AND	WO_OR	PBAFIRMASK_OCI_WRPAR_ERR_MASK: oci_wrpar_err_mask.
8	RW	WO_AND	WO_OR	PBAFIRMASK_Reserved_8: Reserved.
9	RW	WO_AND	WO_OR	PBAFIRMASK_PB_UNEXPCRESP_MASK: pb_unexpcresp_mask.
10	RW	WO_AND	WO_OR	PBAFIRMASK_PB_UNEXPDATA_MASK: pb_unexpdata_mask.
11	RW	WO_AND	WO_OR	PBAFIRMASK_PB_PARITY_ERR_MASK: pb_parity_err_mask.
12	RW	WO_AND	WO_OR	PBAFIRMASK_PB_WRADRERR_FW_MASK: pb_wradrerr_fw_mask.
13	RW	WO_AND	WO_OR	PBAFIRMASK_PB_BADCRESP_MASK: pb_badcresp_mask.
14	RW	WO_AND	WO_OR	PBAFIRMASK_PB_ACKDEAD_FW_RD_MASK: pb_ackdead_fw_rd_mask.
15	RW	WO_AND	WO_OR	PBAFIRMASK_PB_OPERTO_MASK: pb_operto_mask.
16	RW	WO_AND	WO_OR	PBAFIRMASK_BCUE_SETUP_ERR_MASK: bcue_setup_err_mask.
17	RW	WO_AND	WO_OR	PBAFIRMASK_BCUE_PB_ACK_DEAD_MASK: bcue_pb_ack_dead_mask.
18	RW	WO_AND	WO_OR	PBAFIRMASK_BCUE_PB_ADRERR_MASK: bcue_pb_adrerr_mask.
19	RW	WO_AND	WO_OR	PBAFIRMASK_BCUE_OCI_DATERR_MASK: bcue_oci_daterr_mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
20	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_SETUP_ERR_MASK: bcde_setup_err_mask.
21	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_PB_ACK_DEAD_MASK: bcde_pb_ack_dead_mask.
22	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_PB_ADRERR_MASK: bcde_pb_adrerr_mask.
23	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_RDDATATO_ERR_MASK: bcde_rddatato_err_mask.
24	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_SUE_ERR_MASK: bcde_sue_err_mask.
25	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_UE_ERR_MASK: bcde_ue_err_mask.
26	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_CE_MASK: bcde_ce_mask.
27	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_OCI_DATERR_MASK: bcde_oci_daterr_mask.
28	RW	WO_AND	WO_OR	PBAFIRMASK_INTERNAL_ERR_MASK: internal_err_mask.
29	RW	WO_AND	WO_OR	PBAFIRMASK_ILLEGAL_CACHE_OP_MASK: illegal_cache_op_mask.
30	RW	WO_AND	WO_OR	PBAFIRMASK_OCI_BAD_REG_ADDR_MASK: oci_bad_reg_addr_mask.
31	RW	WO_AND	WO_OR	PBAFIRMASK_AXPUSH_WRERR_MASK: axpush_wrerr_mask.
32	RW	WO_AND	WO_OR	PBAFIRMASK_AXRCV_DLO_ERR_MASK: axrcv_dlo_err_mask.
33	RW	WO_AND	WO_OR	PBAFIRMASK_AXRCV_DLO_TO_MASK: axrcv_dlo_to_mask.
34	RW	WO_AND	WO_OR	PBAFIRMASK_AXRCV_RSVDATA_TO_MASK: axrcv_rsvdata_to_mask.
35	RW	WO_AND	WO_OR	PBAFIRMASK_AXFLOW_ERR_MASK: axflow_err_mask.
36	RW	WO_AND	WO_OR	PBAFIRMASK_AXSND_DHI_RTYTO_MASK: axsnd_dhi_rtyto_mask.
37	RW	WO_AND	WO_OR	PBAFIRMASK_AXSND_DLO_RTYTO_MASK: axsnd_dlo_rtyto_mask.
38	RW	WO_AND	WO_OR	PBAFIRMASK_AXSND_RSVTO_MASK: axsnd_rsvto_mask.
39	RW	WO_AND	WO_OR	PBAFIRMASK_AXSND_RSVERR_MASK: axsnd_rsverr_mask.
40	RW	WO_AND	WO_OR	PBAFIRMASK_PB_ACKDEAD_FW_WR_MASK: pb_ackdead_fw_wr_mask.
41:43	RW	WO_AND	WO_OR	PBAFIRMASK_Reserved_41_43: Reserved.
44	RW	WO_AND	WO_OR	PBAFIRMASK_FIR_PARITY_ERR2_MASK: fir_parity_err2_mask.
45	RW	WO_AND	WO_OR	PBAFIRMASK_FIR_PARITY_ERR_MASK: fir_parity_err_mask.
46:63	RO	RO	RO	Constant = 0b000000000000000000

Register Name	PBA Local Fault Isolation Action 0 Register
Mnemonic	BRIDGE.PBA.PBAFIRACT0
Address	0000000005012846 (SCOM)
Description	PBA Local Fault Isolation Action0 Register. All Errors are configured as 'Recoverable' in this register by the hardware as the default value.

Bits	SCOM	Field Mnemonic: Description
0:45	RW	PBAFIRACT0_FIR_ACTION0: MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (PBA_TC_RECOV) (1,0,0) = Checkstop Error (PBA_TC_XSTOP) (1,1,0) = No Error reported (x,x,1) = MASKED.

Bits	SCOM	Field Mnemonic: Description
46:63	RO	Constant = 0b000000000000000000

Register Name	OCC Local Fault Isolation Action 1 Register
Mnemonic	BRIDGE.PBA.PBAFIRACT1
Address	0000000005012847 (SCOM)
Description	OCC Local Fault Isolation Action1 Register. All Errors are configured as 'Recoverable' in this register by the hardware as the default value.

Bits	SCOM	Field Mnemonic: Description
0:45	RW	PBAFIRACT1_FIR_ACTION1: MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (PBA_TC_RECOV) (1,0,0) = Checkstop Error (PBA_TC_XSTOP) (1,1,0) = No Error reported (x,x,1) = MASKED.
46:63	RO	Constant = 0b000000000000000000

Register Name	PBA OCC Action Register
Mnemonic	BRIDGE.PBA.PBAOCCACT
Address	000000000501284A (SCOM)
Description	This register controls whether an error input to the FIR will pulse the pba_occ_error indication to the OCC logic. This register resets to all zero and is must be initialized by OCC Firmware. It is recommended that the following bits be set: 7, 14, 18:25, 27:28, 35.

Bits	SCOM	Field Mnemonic: Description
0:43	RW	PBAOCCACT_OCC_ACTION_SET: OCC Action Set 0 = FIR Input does not cause pba_occ_error to be pulsed. 1 = FIR input causes pba_occ_error to be pulsed.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Configuration Register
Mnemonic	BRIDGE.PBA.PBACFG
Address	000000000501284B (SCOM)
Description	specific settings for the processor bus and for Debug Chicken Switches

Bits	SCOM	Field Mnemonic: Description
0	RW	PBACFG_PBREQ_SLVFW_MAX_PRIORITY: Max processor bus Drop Priority for Forwarded requests This bit controls the Maximum processor bus Drop Priority that can be used to forward OCI requests. It should be set to 'HI'.
1	RW	PBACFG_PBREQ_EXIT_ON_HANG: Exit processor bus RdWr operation on Operational Hang When set, the PBA will abort a processor bus Read or Write request using the tc_pba_hang_pulse detected when a processor bus command is outstanding. (new for POWER9).
2	RW	PBACFG_PBREQ_BCE_MAX_PRIORITY: Max processor bus Drop Priority for Block Copy Engine requests This bit controls the Maximum processor bus Drop Priority that can be used by the Block copy Engine. It should be set to 'HI'.

Bits	SCOM	Field Mnemonic: Description
3	RW	PBACFG_PBREQ_EXIT_ON_HANG_PBAX: Exit processor bus PBAX operation on Operational Hang When set, the PBA will abort a processor bus PBAX request using the tc_pba_hang_pulse detected when a processor bus command is outstanding. (new for POWER9).
4:8	RW	PBACFG_PBREQ_DATA_HANG_DIV: Processor bus Data Hang Timeout Divider. Initializes when clocks are started. Divides the processor bus Data hang pulse to control the Read Data Timeout.
9:13	RW	PBACFG_PBREQ_OPER_HANG_DIV: Processor bus Operational Hang Timeout Divider. Initializes when clocks are started. Divides the processor bus Operational hang pulse to control the Livelockhang rty_other response to the processor bus Hang Check command.
14:19	RW	PBACFG_PBREQ_DROP_PRIORITY_MASK: Processor bus Drop Priority Mask Mask to control the probability that a request that received a rty_drop CRESP should increase its priority. Mask bits control probability from 1:1 (all ones) to 64:1 (all zeroes).
20:23	RW	PBACFG_PBREQ_EXIT_HANG_DIV: Processor bus Exit Hang divider. Initializes to zero when clocks are started. Used for the upper 4 bits of a 5-bit divider of the tc_pba_hang pulse to use for the exit_hang function enabled in pbreq_exit_on_hang andor pbreq_exit_on_hang_pbax.
24	RW	PBACFG_CHSW_HANG_ON_ADRERROR: Enable PBA OCI Slave Hang on processor bus Address error. 0 = Address error on processor bus request will self-recover (Default). 1 = Address error on processor bus request will need SLVRST to recover otherwise it will hang.
25	RW	PBACFG_CHSW_DIS_OCIABUSPAR_CHECK: Disable OCI Address Parity Checking and Generation OFF - PBA OCI Slave uses oci_pba_s_addrparen to control whether address parity is checked. PBA OCI Master asserts pba_oci_m_addrparen. ON - PBA OCI Slave does not check address parity. PBA OCI Master does not assert pba_oci_m_addrparen.
26	RW	PBACFG_CHSW_DIS_OCIBEPAR_CHECK: Disable OCI BE Parity Checking and Generation OFF - PBA OCI Slave uses oci_pba_s_beparen to control whether BE parity is checked. PBA OCI Master asserts pba_oci_m_beparen. ON - PBA OCI Slave does not check BE parity. PBA OCI Master does not assert pba_oci_m_beparen.
27	RW	PBACFG_CHSW_HANG_ON_DERROR: Enable PBA OCI Slave hang on processor bus Data Error 0 = Processor bus data error will self-recover after sending RDDACK w an error response to the OCI Master (Default) 1 = Processor bus data error will cause hang after sending RDDACK w an error response. Buffer FSM cannot be reset.
28	RW	PBACFG_Reserved_28: Spare.
29	RW	PBACFG_CHSW_DIS_WRITE_MATCH_REARB: Disable PBA OCI Slave Write Ordering Match. Disable Rearb for incoming write that matches in the same cache line as a pending write. This will allow sequential, non-gathered writes to get queued. This will allow overlapping writes to get out of order if the pending write is retried by the Memory Controller.
30	RW	PBACFG_CHSW_DIS_OCIDATAPAR_GEN: Disable OCI Data Parity Generation This bit is used to control data parity generate by the PBA OCI Master and OCI Slave. OFF = BA OCI Slave assert pba_oci_s_rdbusparen with valid read data. PBA OCI Master assert pba_oci_m_wrbusparen with valid write data. ON = PBA OCI Slave does not assert pba_oci_s_rdbusparen with valid read data. PBA OCI Master does not assert pba_oci_m_wrbusparen with valid write data.
31	RW	PBACFG_CHSW_DIS_OCIDATAPAR_CHECK: Disable OCI Data Parity Checking OFF = PBA OCI Slave uses oci_pba_s_wrbusparen to control whether the write data parity is checked. PBA OCI Master uses pba_oci_m_rdbusparen to control whether the read data parity is checked. ON = PBA OCI Slave does not check write data parity. PBA OCI Master does not check read data parity.
32	RW	PBACFG_CHSW_DIS_OPER_HANG: Disable Operational Hang Pulse preventing processor bus Livelock Warning.
33	RW	PBACFG_CHSW_DIS_DATA_HANG: Disable Data Hang pulse preventing processor bus Timeout.
34	RW	PBACFG_CHSW_DIS_ECC_CHECK: Disable ECC Checking on inbound processor bus data.
35	RW	PBACFG_CHSW_DIS_RETRY_BACKOFF: Disable Retry Backoff on processor bus.

Bits	SCOM	Field Mnemonic: Description
36	RW	PBACFG_CHSW_EXIT_ON_INVALID_CRESP: Enable Exit on Invalid processor bus CRESP. (otherwise will retry).
37	RW	PBACFG_Reserved_37: Spare.
38	RW	PBACFG_CHSW_DIS_GROUP_SCOPE: Disable Group Scope Used to eliminate Group Scope for debugproblem workaround. If the starting scope or an increased scope from a nodal scope is required, the scopeis Vg(S).
39	RW	PBACFG_CHSW_DIS_RTAG_PARITY_CHK: Disable Powerbus parity check on dpx_RTAG. Only used in designer sim.
40	RW	PBACFG_CHSW_DIS_PB_PARITY_CHK: Disable processor bus parity check on RCMD0 addr, CRESP ATAG and ttag. Only used in designer sim.
41	RW	PBACFG_CHSW_SKIP_GROUP_SCOPE: Skip group scope on rty_inc . Does not eliminate Group scope. Used in a chip = group to control the masters scope progression. For PBA only atomic ops make use of this bit On a rty_inc, next scope is Vg(S).
42	RW	PBACFG_CHSW_USE_PR_DMA_INJ: Force pr_dma_inj as default Controls the starting processor bus write ttype to use when PBASLVCTL[write_ttype] = DMA for a partial cache line op. (new for POWER9) 0-- Starting ttype is dma_pr_w 1-- Starting ttype is pr_dma_inj.
43	RW	PBACFG_CHSW_USE_CL_DMA_INJ: Force cl_dma_inj as default Controls the starting processor bus write ttype to use when PBASLVCTL[write_ttype] = DMA for a cache line op. (new for POWER9) 0-- Starting ttype is cl_dma_w 1-- Starting ttype is cl_dma_inj.
44:47	RW	PBACFG_Reserved_44_47: Spare.
48:63	RO	Constant = 0b0000000000000000

Register Name	**PBA Error Report 0 Register**
Mnemonic	BRIDGE.PBA.PBAERRRPT0
Address	000000000501284C (SCOM)
Description	PBA Error Report Register 0 (read/clear c_err_rpt) shows the 'hold' condition from the c_err_rpt logic for each individual error detected by the PBA. Writing any value to the PBAERRRPT0 will force a reset to clear all hold bits in all the PBAERRPTn. CERR_RST: CERR reset for PBA.

Bits	SCOM	Field Mnemonic: Description
0:5	RWX_WCLRPART	PBAERRRPT0_CERR_PB_RDDATATO_FW: CERR_OBS: PBAFIR(2) PB Read Data Timeout for Forwarded Request 0:5 - Per Read queue(0:5).
6:11	RWX_WCLRPART	PBAERRRPT0_CERR_PB_RDADRERR_FW: CERR_OBS: PBAFIR(1) PB CRESP Addr Error Received for Forwarded Read Request 0:5 - Per Read queue (0:5).
12:15	RWX_WCLRPART	PBAERRRPT0_CERR_PB_WRADRERR_FW: CERR_OBS: PBAFIR(12) PB CRESP Addr Error Received for Forwarded Write Request 0:1 = Per Write queue (0:1), f 2 = PBAXSND 3 = PBAXRCV.
16:21	RWX_WCLRPART	PBAERRRPT0_CERR_PB_ACKDEAD_FW_RD: CERR_OBS: PBAFIR(14) Ackdead response received for forwarded read request 0:5 - Per Read queue(0:5),
22:23	RWX_WCLRPART	PBAERRRPT0_CERR_PB_ACKDEAD_FW_WR: CERR_OBS: PBAFIR(40) Ackdead response received for forwarded write request 0:1 - Per Write queue.(0:1).

Bits	SCOM	Field Mnemonic: Description
24:34	RWX_WCLRPART	PBAERRRPT0_CERR_PB_UNEXPCRESP: CERR_OBS: PBAFIR(9) Unexpected CRESP received for request. 0:5 = Per Read queue.(0:5) 6:7 = Per Write queue(0:1) 8:9 = Per BCUE write queue 10 = PBAXSND,
35:40	RWX_WCLRPART	PBAERRRPT0_CERR_PB_UNEXPDATA: CERR_OBS: PBAFIR(10) Unexpected Data response received 0:5 - Per Read queue(0:5).
41:63	RO	Constant = 0b00000000000000000000000

Register Name	PBA Error Report 1 Register
Mnemonic	BRIDGE.PBA.PBAERRRPT1
Address	000000000501284D (SCOM)
Description	PBA Error Report Register 1shows the 'hold' condition from the c_err_rpt logic for each individual error detected by the PBA. Writing any value to the PBAERRRPT0 will force a reset to clear all hold bits in all the PBAERRPTn.

Bits	SCOM	Field Mnemonic: Description
0:11	ROX	PBAERRRPT1_CERR_PB_BADCRESP: CERR_OBS: PBAFIR(13) Invalid CRESP received. 0:5 - Per Read queue(0:5), 6:9 - Per Write queue(0:3), 10 - PBAXSND, 11 - PBAXRCV.
12:23	ROX	PBAERRRPT1_CERR_PB_OPERTO: CERR_OBS: PBAFIR(15) Operational Timeout. 0:5 = Per Read queue(0:5) 6:9 = Per Write queue(0:3) 10 = PBAXSND 11 = PBAXRCV
24:29	ROX	PBAERRRPT1_Reserved_24_29: Reserved tied to zero.
30:31	ROX	PBAERRRPT1_CERR_BCDE_SETUP_ERR: CERR_OBS: PBAFIR(20) BCDE Setup Error 0 - unexpected start when already running, 1 - processor bus address error.
32:33	ROX	PBAERRRPT1_CERR_BCUE_SETUP_ERR: CERR_OBS: PBAFIR(16) BCUE Setup Error ' 0 - unexpected start when already running, 1 - processor bus address error.
34:35	ROX	PBAERRRPT1_CERR_BCUE_OCI_DATAERR: CERR_OBS: PBAFIR(19) 0 - BCUE received MRDERR, 1 - BCUE Read Parity Error.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	PBA Error Report 2 Register
Mnemonic	BRIDGE.PBA.PBAERRRPT2
Address	000000000501284E (SCOM)
Description	PBA Error Report Register 2 (read/clear c_err_rpt) shows the 'hold' condition from the c_err_rpt logic for each individual error detected by the PBA. Writing any value to the PBAERRRPT0 will force a reset to clear all hold bits in all the PBAERRPTn.

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	PBAERRRPT2_CERR_SLV_INTERNAL_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error (OCI Slave) 0 - Multi address match 1 - Multip rdbuf start 2 - Unexp rdbuf start 3 - Cancel rdbuf start 4 - Bad Region or Marker Address in PBAMODE register 5 - RDBUFFSM illegal State 6 - WRBUFFSM illegal State 7 - not defined.

Bits	SCOM	Field Mnemonic: Description
8:11	ROX	PBAERRRPT2_CERR_BCDE_INTERNAL_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error (BCDE) 0 - Unexp addrack 1 - Unexp dataack 2 - wrfsm illegal state 3 - bcefsm illegal state.
12:15	ROX	PBAERRRPT2_CERR_BCUE_INTERNAL_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error (BCDE) 0 - Unexp addrack 1 - Unexp dataack 2 - not defined. 3 - bcefsm illegal state.
16	ROX	PBAERRRPT2_CERR_BAR_PARITY_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error - BAR Parity Error.
17	ROX	PBAERRRPT2_CERR_SCOMTB_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error - Trusted Scom fsm error.
18:19	ROX	PBAERRRPT2_CERR_SPARE: CERR_OBS: PBAFIR(28) PBA Internal Error - Unused.
20	ROX	PBAERRRPT2_CERR_PBDOUT_PARITY_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error - Parity error detected on outbound write data. Forced bad ECC.
21:23	ROX	PBAERRRPT2_CERR_PB_PARITY_ERR: CERR_OBS: PBAFIR(11) processor bus parity error detected 0 - CRESP TTAG or ATAG parity error 1 - DPX_RTAG parity error 2 - RCMD0 ADDR parity error.
24:28	ROX	PBAERRRPT2_CERR_AXFLOW_ERR: CERR_OBS.PBAFIR(35) PBAX Flow error 0 - axflow Setup 1:2 - axflow Underflow per qid. 3:4 - axflow Overflow per qid.
29:30	ROX	PBAERRRPT2_CERR_AXPUSH_WRERR: CERR_OBS.PBAFIR(31) PBAX Push Write Error 0 = push queue 0 1 = push queue 1.
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	PBA Read Buffer Value 0 Register
Mnemonic	BRIDGE.PBA.PBARBUFVAL0
Address	0000000005012850 (SCOM)
Description	These are read only status registers for the PBA Slave that contain vital information regarding the processor bus Read data buffer state. These registers are used for debug and error recovery.

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL0_RD_SLVNUM: Rd_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected.
2:24	ROX	PBARBUFVAL0_CUR_RD_ADDR: Current Rd Address 128-byte cache line address for the current buffer. It is set by the OCI Slave Control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL0_PREFETCH: Prefetch Status This bit is set when the next cache line is prefetched and is used as extra info to decide if the buffer can be reused for another operation and forced to the Timeout state when the buffer is in the Valid, PB CRESP Error, or PB Data Error state. This bit is cleared when an OCI Request matches the address or when the Rd Buffer Status goes to the Empty State. 0FF - OCI Read Address requested this buffered address ON - processor bus Read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00
31	ROX	PBARBUFVAL0_ABORT: Abort Status This bit is set when the OCI Master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the Rd Buffer Status goes to the Empty State. OFF - Request has not been aborted ON - Request has been aborted.
32	RO	Constant = 0b0
33:39	ROX	PBARBUFVAL0_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started.

Bits	SCOM	Field Mnemonic: Description
40	RO	Constant = 0b0
41:43	ROX	PBARBUFVAL0_MASTERID: Master Id These bits indicate the Master Id that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Read Buffer Value 1 Register
Mnemonic	BRIDGE.PBA.PBARBUFVAL1
Address	0000000005012851 (SCOM)
Description	These are read only status registers for the PBA Slave that contain vital information regarding the processor bus Read data buffer state. These registers are used for debug and error recovery.

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL1_RD_SLVNUM: Rd_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected.
2:24	ROX	PBARBUFVAL1_CUR_RD_ADDR: Current Rd Address 128-byte cache line address for the current buffer. It is set by the OCI Slave Control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL1_PREFETCH: Prefetch Status This bit is set when the next cache line is prefetched and is used as extra info to decide if the buffer can be reused for another operation and forced to the Timeout state when the buffer is in the Valid, PB CRESP Error, or PB Data Error state. This bit is cleared when an OCI Request matches the address or when the Rd Buffer Status goes to the Empty State. 0FF - OCI Read Address requested this buffered address ON - processor bus Read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00
31	ROX	PBARBUFVAL1_ABORT: Abort Status This bit is set when the OCI Master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the Rd Buffer Status goes to the Empty State. OFF - Request has not been aborted ON - Request has been aborted.
32	RO	Constant = 0b0
33:39	ROX	PBARBUFVAL1_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started.
40	RO	Constant = 0b0
41:43	ROX	PBARBUFVAL1_MASTERID: Master Id These bits indicate the Master Id that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Read Buffer Value 2 Register
Mnemonic	BRIDGE.PBA.PBARBUFVAL2
Address	0000000005012852 (SCOM)
Description	These are read only status registers for the PBA Slave that contain vital information regarding the processor bus Read data buffer state. These registers are used for debug and error recovery.

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL2_RD_SLVNUM: Rd_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected.

Bits	SCOM	Field Mnemonic: Description
2:24	ROX	PBARBUFVAL2_CUR_RD_ADDR: Current Rd Address 128-byte cache line address for the current buffer. It is set by the OCI Slave Control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL2_PREFETCH: Prefetch Status This bit is set when the next cache line is prefetched and is used as extra info to decide if the buffer can be reused for another operation and forced to the Timeout state when the buffer is in the Valid, PB CRESP Error, or PB Data Error state. This bit is cleared when an OCI Request matches the address or when the Rd Buffer Status goes to the Empty State. OFF - OCI Read Address requested this buffered address ON - processor bus read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00
31	ROX	PBARBUFVAL2_ABORT: Abort Status This bit is set when the OCI Master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the Rd Buffer Status goes to the Empty State. OFF - Request has not been aborted ON - Request has been aborted.
32	RO	Constant = 0b0
33:39	ROX	PBARBUFVAL2_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started.
40	RO	Constant = 0b0
41:43	ROX	PBARBUFVAL2_MASTERID: Master Id These bits indicate the Master Id that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Read Buffer Value 3 Register
Mnemonic	BRIDGE.PBA.PBARBUFVAL3
Address	0000000005012853 (SCOM)
Description	These are read only status registers for the PBA Slave that contain vital information regarding the processor bus Read data buffer state. These registers are used for debug and error recovery.

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL3_RD_SLVNUM: Rd_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected.
2:24	ROX	PBARBUFVAL3_CUR_RD_ADDR: Current Rd Address 128-byte cache line address for the current buffer. It is set by the OCI Slave Control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL3_PREFETCH: Prefetch Status This bit is set when the next cache line is prefetched and is used as extra info to decide if the buffer can be reused for another operation and forced to the Timeout state when the buffer is in the Valid, PB CRESP Error, or PB Data Error state. This bit is cleared when an OCI Request matches the address or when the Rd Buffer Status goes to the Empty State. OFF - OCI Read Address requested this buffered address ON - processor bus Read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00
31	ROX	PBARBUFVAL3_ABORT: Abort Status This bit is set when the OCI Master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the Rd Buffer Status goes to the Empty State. OFF - Request has not been aborted ON - Request has been aborted.
32	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
33:39	ROX	PBARBUFVAL3_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started.
40	RO	Constant = 0b0
41:43	ROX	PBARBUFVAL3_MASTERID: Master Id These bits indicate the Master ID that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Read Buffer Value 4 Register
Mnemonic	BRIDGE.PBA.PBARBUFVAL4
Address	0000000005012854 (SCOM)
Description	These are read only status registers for the PBA Slave that contain vital information regarding the processor bus Read data buffer state. These registers are used for debug and error recovery.

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL4_RD_SLVNUM: Rd_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected.
2:24	ROX	PBARBUFVAL4_CUR_RD_ADDR: Current Rd Address 128-byte cache line address for the current buffer. It is set by the OCI Slave Control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL4_PREFETCH: Prefetch Status This bit is set when the next cache line is prefetched and is used as extra info to decide if the buffer can be reused for another operation and forced to the Timeout state when the buffer is in the Valid, PB CRESP Error, or PB Data Error state. This bit is cleared when an OCI Request matches the address or when the Rd Buffer Status goes to the Empty State. OFF - OCI Read Address requested this buffered address ON - processor bus Read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00
31	ROX	PBARBUFVAL4_ABORT: Abort Status This bit is set when the OCI Master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the Rd Buffer Status goes to the Empty State. OFF - Request has not been aborted ON - Request has been aborted.
32	RO	Constant = 0b0
33:39	ROX	PBARBUFVAL4_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started.
40	RO	Constant = 0b0
41:43	ROX	PBARBUFVAL4_MASTERID: Master Id These bits indicate the Master ID that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Read Buffer Value 5 Register
Mnemonic	BRIDGE.PBA.PBARBUFVAL5
Address	0000000005012855 (SCOM)
Description	These are read only status registers for the PBA Slave that contain vital information regarding the processor bus Read data buffer state. These registers are used for debug and error recovery.

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL5_RD_SLVNUM: Rd_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected.
2:24	ROX	PBARBUFVAL5_CUR_RD_ADDR: Current Rd Address 128-byte cache line address for the current buffer. It is set by the OCI Slave Control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL5_PREFETCH: Prefetch Status This bit is set when the next cache line is prefetched and is used as extra info to decide if the buffer can be reused for another operation and forced to the Timeout state when the buffer is in the Valid, PB CRESP Error, or PB Data Error state. This bit is cleared when an OCI Request matches the address or when the Rd Buffer Status goes to the Empty State. OFF - OCI Read Address requested this buffered address ON - processor bus Read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00
31	ROX	PBARBUFVAL5_ABORT: Abort Status This bit is set when the OCI Master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the Rd Buffer Status goes to the Empty State. OFF - Request has not been aborted ON - Request has been aborted.
32	RO	Constant = 0b0
33:39	ROX	PBARBUFVAL5_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started.
40	RO	Constant = 0b0
41:43	ROX	PBARBUFVAL5_MASTERID: Master Id These bits indicate the Master Id that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Write Buffer Value 0 Register
Mnemonic	BRIDGE.PBA.PBAWBUFVAL0
Address	0000000005012858 (SCOM)
Description	These are read only status registers for the PBA Slave that contain vital information regarding the processor bus Write data buffer state. These registers are used for debug and error recovery.

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBAWBUFVAL0_WR_SLVNUM: Wr_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected.
2:31	ROX	PBAWBUFVAL0_START_WR_ADDR: Starting Write Address These bits save the starting OCI address for the gathered write operation and are valid only If the write buffer status is not EMPTY.
32:34	RO	Constant = 0b000
35:39	ROX	PBAWBUFVAL0_WR_BUFFER_STATUS: Write Buffer Status These bits indicate which bit is set in the one-hot Write in Progress state machine. Zero is not a valid state after clocks have started.
40	RO	Constant = 0b0
41:47	ROX	PBAWBUFVAL0_WR_BYTE_COUNT: Write Byte Count These bits are the number of bytes in the gathered write operation. Starting Write Address plus Write Byte Count is the Next Write Address from the same master required to continue gathering. 0000000 - 128 bytes 0000001 - 1 byte 0000010 - 2 bytes 0000011 - 3 bytes . . . 1111111 - 127 bytes.
48:63	RO	Constant = 0b0000000000000000

Register Name	PBA Write Buffer Value 1 Register
Mnemonic	BRIDGE.PBA.PBAWBUFVAL1
Address	0000000005012859 (SCOM)
Description	These are read only status registers for the PBA Slave that contain vital information regarding the processor bus Write data buffer state. These registers are used for debug and error recovery.

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBAWBUFVAL1_WR_SLVNUM: Wr_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected.
2:31	ROX	PBAWBUFVAL1_START_WR_ADDR: Starting Write Address These bits save the starting OCI address for the gathered write operation and are valid only If the write buffer status is not EMPTY.
32:34	RO	Constant = 0b000
35:39	ROX	PBAWBUFVAL1_WR_BUFFER_STATUS: Write Buffer Status These bits indicate which bit is set in the one-hot Write in Progress state machine. Zero is not a valid state after clocks have started.
40	RO	Constant = 0b0
41:47	ROX	PBAWBUFVAL1_WR_BYTE_COUNT: Write Byte Count These bits are the number of bytes in the gathered write operation. Starting Write Address plus Write Byte Count is the Next Write Address from the same master required to continue gathering. 0000000 = 128 bytes 0000001 = 1 byte 0000010 - 2 bytes 0000011 = 3 bytes . . . 1111111 - 127 bytes.
48:63	RO	Constant = 0b0000000000000000

Register Name	HTM Collection Mode Register
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_MODE
Address	0000000005012880 (SCOM)
Description	HTM Collection Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MODE_HTM_ENABLE: HTM enable, must be set by software to start HTM trace.
1:2	RW	HTMSC_MODE_CONTENT_SEL: These bits define the NHTM Trace Mode.
3	RW	HTMSC_MODE_SPARE3: Spare bit.

Bits	SCOM	Field Mnemonic: Description
4:12	RW	HTMSC_MODE_CAPTURE: HTM capture mode bit definition according to Trace Mode. When htm_mode_q(1 TO 2) = = 00, that is, FABRIC. 456789012. 0xxxx0000 = Ignore HTM generated data writes. 1xxxx0000 = Capture htm generated data writes. x0xxx0000 = Filtering ignored on PMISC (always trace PMISC and Report Hang). x1xxx0000 = Filtering applied on ttype = PMISC and ttype = report hang. xx00x0000 = CRESP Mode: Flush CRESP Queue to avoid overrun (default). xx01x0000 = CRESP Mode: Reserved. xx10x0000 = CRESP Mode: Enable Precise CRESP Mode. xx11x0000 = CRESP Mode: Ignore CRESP. xxxx00000 = Pre-Allocate maximum memory buffers (8). xxxx10000 = Pre-Allocate fewer memory buffers (4). When htm_mode_q(1 TO 2) = = 01, that is, OTHER. 00000xxxx = Pre-Allocate maximum memory buffers (8). 00001xxxx = Pre-Allocate fewer memory buffers (4). 0000xmmmx = mmm for optional external multiplexer control. 0000xxxx0 = Both -other- trace buses to NHTM0. 0000xxxx1 = Other trace bus0 to nhtm0, trace bus1 to nhtm1. High BW. When htm_mode_q(1 TO 2) = = 10, that is, OCC. 00000xxx0 = Pre-Allocate maximum memory buffers (8). 00001xxx0 = Pre-Allocate fewer memory buffers (4). 0000xmmm0 = mmm for optional external multiplexer control.
13	RW	HTMSC_MODE_WRAP: Enable Trace Wrap Mode. 0 = Stop trace when top of Trace Memory is reached. 1 = Wrap trace to beginning of Trace Memory.
14	RW	HTMSC_MODE_DIS_TSTAMP: Disable TimeStamp Writes. 0 = Write of timestamps enabled to indicate elapsed time between records. 1 = Timestamps written only to indicate record loss.
15	RW	HTMSC_MODE_SINGLE_TSTAMP: Disable Overflow Timestamps. 0 = Timestamp written to indicate elapsed time overflow. 1 = Only one timestamp is written between entries, overflow indication is lost.
16	RW	HTMSC_MODE_SPARE16: Not used in NHTM.
17	RW	HTMSC_MODE_MARKERS_ONLY: Enable Stamp/Marker Only Mode. 0 = Normal trace. 1 = Ignore incoming trace data and save only markers caused by HTM_TRIG writes, Global HTM markers enabled to be inserted into the trace record and enabled stamps.
18	RW	HTMSC_MODE_DIS_FORCE_GROUP_SCOPE: Disable Group Scope. This is a processor bus debug bit. 0 = htm write ops sent with group scope. 1 = htm write ops sent with Vg scope using programmed target bits.
19:21	RW	HTMSC_MODE_SYNC_STAMP_FORCE: Control the number of cycles to wait to force a synchronization stamp or reset the timer.
22	RW	HTMSC_MODE_WRITETOIO: HTM Trace memory in IO space, use ci_pr_st op. 0 = Use HTM_CL_Write operation to target system memory. Do pre-allocation sequence. (default). 1 = Use ci_pr_st operation to target anywhere else. Dont do pre-allocate sequence.
23	RW	HTMSC_MODE_SPARE23: Not used in NHTM.
24:39	RW	HTMSC_MODE_VGTARGET: Vg Target bits should be configured if HTM_MEM[scope] is Vg. or if Disable Group Scope = 1.
40:43	RW	HTMSC_MODE_SPARE4043: NOt used in NHTM.
44:63	RO	Constant = 0b00000000000000000000

Register Name	HTM Memory Configuration Register
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_MEM
Address	0000000005012881 (SCOM)
Description	HTM Memory Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MEM_ALLOC: 0 = memory based address not configured, 1 = memory address configured. This bit must be written to zero before setting since the HTM looks for. the 0 -> 1 transition on this bit to indicate the memory address has. been updated.
1:3	RW	HTMSC_MEM_SCOPE: Processor bus Scope to use when writing the HTM Trace memory. If the scope is not large enough, the HTM will get an address error. If the scope is too large, HTM will experience excessive delay.
4	RW	HTMSC_MEM_PRIORITY: Starting processor bus Priority. Configure the Starting priority used when writing the HTM Trace memory. Leave at default 000 unless there is a very good reason to change.
5	RW	HTMSC_MEM_SIZE_SMALL: Trace Memory Size Range. 0 = Trace Mem Size from 512M to 256G. 1 = Trace Mem Size from 16M to 8G.
6:7	RW	HTMSC_MEM_SPARE67: Not Used.
8:39	RW	HTMSC_MEM_BASE: Trace memory base address (8:39). The Trace Memory Base Address must be aligned on a Trace Memory Size boundary.
40:48	RW	HTMSC_MEM_SIZE: Trace Memory Size. When htmsc_mem_size_small = 0, these bits define the mask to bits (26:35) of the Trace Memory Base Address and define the size of the trace memory between 512MB and 256GB. When htmsc_mem_size_small = 1, these bits define the mask to bits (31:39) of the Trace Memory Base address and define the size of the trace memory between 16MB and 8GB.
49:63	RO	Constant = 0b000000000000000

Register Name	HTM Status Register
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_STAT
Address	0000000005012882 (SCOM)
Description	HTM Status Register

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	HTMCO_STATUS_SPARE: Spare bits.
2	ROX	HTMCO_STATUS_CRESP_OV: Asserted on detection of a CRESP queue overwrite condition. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
3	ROX	HTMCO_STATUS_REPAIR: Asserted on occurence of address error to indicate the need of software to clear and update HTM_MEM. Will stay high until HTM_MEM updated.
4	ROX	HTMCO_STATUS_BUF_WAIT: Asserted on condition of data buffers full in tracing state. Any markers, stamps, and trace data recieved when this bit is set will be lost.
5	ROX	STATUS_TRIG_DROPPED_Q: Asserted on buffer overrun due to trigger lost at least once in the last trace. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
6	ROX	HTMCO_STATUS_ADDR_ERROR: Asserted on address error when write buffer was allocated. Need to set new address range after htmco_status_repair is asserted.
7	ROX	STATUS_REC_DROPPED_Q: Asserted on buffer overrun due to trace data lost at least once in the last trace. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.

Bits	SCOM	Field Mnemonic: Description
8	ROX	HTMCO_STATUS_INIT: Asserted when htm_cofsm is in Init state.
9	ROX	HTMCO_STATUS_PREREQ: Asserted when htm_cofsm is in Pre-req state.
10	ROX	HTMCO_STATUS_READY: Asserted when htm_cofsm is in Ready state.
11	ROX	HTMCO_STATUS_TRACING: Asserted when htm_cofsm is in Tracing state.
12	ROX	HTMCO_STATUS_PAUSED: Asserted when htm_cofsm is in Paused state.
13	ROX	HTMCO_STATUS_FLUSH: Asserted when htm_cofsm is in Flush state.
14	ROX	HTMCO_STATUS_COMPLETE: Asserted when htm_cofsm is in Complete state.
15	ROX	HTMCO_STATUS_ENABLE: Asserted when htm_cofsm is in Enable state.
16	ROX	HTMCO_STATUS_STAMP: Asserted when htm_cofsm is in Stamp state.
17	ROX	STATUS_SCOM_ERROR: Asserted to indicate that a SCOM error indication was received from the SCOM satellite. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
18	ROX	STATUS_PARITY_ERROR: Asserted to indicate a parity error was detected on the processor bus. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
19	ROX	STATUS_INVALID_CRESP: Asserted to indicate an invalid CRESP was received from the processor bus. NHTM is hung. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	HTM Last Address Register
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_LAST
Address	0000000005012883 (SCOM)
Description	HTM Last Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:56	ROX	HTM_LAST_ADDRESS: The last cache line address of the memory trace. Guaranteed valid only when HTM is in the Complete state.
57:63	RO	Constant = 0b0000000

Register Name	HTM SCOM Trigger Register
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_TRIG
Address	0000000005012884 (SCOM)
Description	HTM SCOM Trigger Register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_TRIG_START: Start trigger.
1	RW	HTMSC_TRIG_STOP: Stop trigger.
2	RW	HTMSC_TRIG_PAUSE: Pause trigger.
3	RW	HTMSC_TRIG_STOP_ALT: Stop trigger 2. Legacy bit that used to be the Freeze Trigger in POWER6 implementation.
4	RW	HTMSC_TRIG_RESET: Reset trigger.
5	RW	HTMSC_TRIG_MARK_VALID: Mark type valid.

Bits	SCOM	Field Mnemonic: Description
6:15	RW	HTMSC_TRIG_MARK_TYPE: Mark type is put into Mark Record when bit 5 is set.
16:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	HTM Trigger Control Register
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_CTRL
Address	0000000005012885 (SCOM)
Description	HTM Trigger Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	HTMSC_CTRL_TRIG: Trigger Control. 00 = local triggers are not forwarded to the processor bus, it is inserted into the trace when tracing. Both local and global triggers control the HTM. 01 = local triggers are not forwarded to the processor bus, it is inserted into the trace when tracing. Only local triggers control the HTM. 1x = local triggers are forwarded to the processor bus, it is not inserted into the trace when tracing. Only global triggers control the HTM.
2:3	RW	Reserved.
4:5	RW	HTMSC_CTRL_MARK: Marker Control. 00 local markers are not forwarded to the processor bus. Both local and global markers are inserted into the trace. 01 = local markers are not forwarded to the processor bus. Only local markers are inserted into the trace. 10 = local markers are forwarded to the processor bus. Only global markers are inserted into the trace. 11 = local markers are forwarded to the processor bus. Markers are not inserted into the trace (Fabric Trace Mode).
6	RW	HTMSC_CTRL_DBG0_STOP: Enable Stop on PB Chiplet Debug Trigger 0.
7	RW	HTMSC_CTRL_DBG1_STOP: Enable Stop on PB Chiplet Debug Trigger 1.
8	RW	HTMSC_CTRL_RUN_STOP: Enable Stop on falling edge of PB Chiplet trace_run.
9	RW	HTMSC_CTRL_OTHER_DBG0_STOP: Enable Stop using OCC Control.
10:12	RW	HTMSC_CTRL_SPARE1012: Spare bits.
13	RW	HTMSC_CTRL_XSTOP_STOP: Enable Stop on chiplet XSTOP.
14:15	RW	HTMSC_CTRL_SPARE1415: Spare bits.
16:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	HTM Filter Control Register
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_FILT
Address	0000000005012886 (SCOM)
Description	HTM Filter Control Register

Bits	SCOM	Field Mnemonic: Description
0:22	RW	HTMSC_FILT_PAT: Filter Pattern. In Fabric Trace Mode, Defines the TTAG/Scope/Source pattern to Match in the RCMD and CRESP. 0:3 = RCMD_ttag(0:2) Group ID Pattern for RCMD and CRESP filtering. 4:6 = RCMD_ttag(3:5) Chip ID Pattern for RCMD and CRESP filtering. 7:16 = RCMD_ttag(6:13) Unit ID Pattern for RCMD and CRESP (if from this chip) filtering. 17:19 = RCMD_scope(0:2) Scope Pattern for RCMD and CRESP filtering. 20:21 = RCMD_source(0:1) Source Pattern for RCMD filtering. 22 = Powerbus PORT pattern for RCMD and CRESP filtering. In OCC Trace Mode, Defines the occ_trace_data(0:22) pattern to match. 0:22 = occ_trace_data(0:22) Pattern.
23:26	RW	Reserved.
27:31	RW	HTMSC_FILT_CRESP_PAT: CRESP Filter Pattern. In Fabric Trace Mode, Defines the CRESP pattern to match.
32:54	RW	HTMSC_FILT_MASK: Pattern mask. Bits set to 1 in this mask do not need to match w/ the Filter Pattern. If all mask bits are set, No pattern matching is done.
55:58	RW	Reserved.
59:63	RW	HTMSC_FILT_CRESP_MASK: CRESP Filter Mask. Bits set to 1 in this mask do not need to match w/ the CRESP Filter Pattern. If all mask bits are set, no pattern matching is done.

Register Name	**HTM TTYPE Filter Control Register**
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_TTYPEFILT
Address	0000000005012887 (SCOM)
Description	HTM Ttype Filter Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1:7	RW	HTMSC_TTYPEFILT_PAT: TTYPE Pattern. In Fabric Trace Mode, Defines the TTYPE pattern to Match.
8:15	RW	HTMSC_TSIZEFILT_PAT: TSIZE Pattern. In Fabric Trace Mode, Defines the TSIZE pattern to Match.
16	RW	Reserved.
17:23	RW	HTMSC_TTYPEFILT_MASK: TTYPE Pattern mask. TTYPE Bits set to 1 in this mask do not need to match w/ the Pattern. If all mask bits are set, No TTYPE pattern/masking is done.
24:31	RW	HTMSC_TSIZEFILT_MASK: TSIZE Pattern mask. TSIZE Bits set to 1 in this mask do not need to match w/ the Pattern. If all mask bits are set, No TSIZE pattern/masking is done.
32	RW	HTMSC_TTYPEFILT_INVERT: TTYPE/TSIZE Capture Invert. 0 = Capture record based on ttype/tsize pattern matching. 1 = Capture record based on ttype/tsize pattern NOT matching.
33	RW	HTMSC_CRESPFILT_INVERT: CRESP Filter Capture Invert. 0 = Capture record based on CRESP filter pattern matching. 1 = Capture record based on CRESP filter pattern NOT matching.
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	HTM Configuration Register
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_CFG
Address	0000000005012888 (SCOM)
Description	HTM Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:4	RW	HTMSC_CFG_OPER_HANG_DIV_RATIO: Processor bus Operational Hang Divider. This register is used to set the hang count divider for operational. hangs. If this register is NOT initialized, the default hang_div_ratio. is b01000 setup on the first functional clock.
5:8	RW	HTMSC_CFG_RTY_DRP_COUNT: Processor bus Retry Drop Counter Max. This is the maximum value to count RTY_DRP CRESP before increasing the drop priority. used when sending the next command. If this register is NOT initialized, the default. max count is b0111 setup on the first functional clock.
9	RW	HTMSC_CFG_DIS_DRP_PRIORITY_INCR: Disable Increase of Drop Priority.
10	RW	HTMSC_CFG_DIS_RETRY_BACKOFF: Disable processor bus Retry Backoff. 0 = Powerbus Retry Backoff works according to PB Arch Ver 3xx. 1 = Powerbus Retry Backoff disabled, retry immediately if receive retry cresp.
11	RW	HTMSC_CFG_DIS_OPER_HANG: Disable processor bus Operational Hang Detect. 0 = Powerbus Operation Hang Detect works according to PB Arch Ver 3xx. 1 = Powerbus Operation Hang Detect disabled, PRSP Rty_Other never asserted.
12:19	RW	Reserved.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	HTM Flex Multiplexer Register
Mnemonic	BRIDGE.NHTM.NHTM0.SC.HTM_FLEX
Address	0000000005012889 (SCOM)
Description	HTM Flex Multiplexer Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	HTMSC_FMUX_RGRPSEL0: RCMD Group 0 Select for RCMD record bits(19:22). Default is 1100 for RCMDx_adr(58:61).
4:7	RW	HTMSC_FMUX_RGRPSEL1: RCMD Group 1 Select for RCMD record bits(23:26). Default is 1011 for RCMDx_ttag(18:21).
8:11	RW	HTMSC_FMUX_RGRPSEL2: RCMD Group 2 Select for RCMD record bits(27:30). Default is 0011 for RCMDx_adr(16:19).
12:15	RW	HTMSC_FMUX_RGRPSEL3: RCMD Group 3 Select for RCMD record bits(31:34). Default is 0100 for RCMDx_adr(20:23).
16:19	RW	HTMSC_FMUX_RGRPSEL4: RCMD Group 4 Select for RCMD record bits(35:38). Default is 0101 for RCMDx_adr(24:27).
20:23	RW	HTMSC_FMUX_RGRPSEL5: RCMD Group 5 Select for RCMD record bits(39:42). Default is 0110 for RCMDx_adr(28:31).
24:27	RW	HTMSC_FMUX_CGRPSEL0: CRESP Flex Group 0 Select for CRESP record bits(122:123). Default is 0001 for crx_target(0:1).
28:31	RW	HTMSC_FMUX_CGRPSEL1: CRESP Flex Group 1 Select for CRESP record bits(124:125). Default is 0010 for crx_target(2:3).

Bits	SCOM	Field Mnemonic: Description
32:35	RW	HTMSC_FMUX_CGRPSEL2: CRESP Flex Group 2 Select for CRESP record bits(126:127). Default is 1001 for crx_ds(0:1).
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	HTM Collection Mode Register
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_MODE
Address	00000000050128C0 (SCOM)
Description	HTM Collection Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MODE_HTM_ENABLE: HTM enable, must be set by software to start HTM trace.
1:2	RW	HTMSC_MODE_CONTENT_SEL: These bits define the NHTM Trace Mode.
3	RW	HTMSC_MODE_SPARE3: Spare bit.
4:12	RW	HTMSC_MODE_CAPTURE: HTM capture mode bit definition according to Trace Mode. When htm_mode_q(1 TO 2) = = 00, that is, FABRIC. 456789012. 0xxxx0000 = Ignore HTM generated data writes. 1xxxx0000 = Capture htm generated data writes. x0xxx0000 = Filtering ignored on PMISC (always trace PMISC and Report Hang). x1xxx0000 = Filtering applied on ttype = PMISC and ttype = report hang. xx00x0000 = CRESP Mode: Flush CRESP Queue to avoid overrun (default). xx01x0000 = CRESP Mode: Reserved. xx10x0000 = CRESP Mode: Enable Precise CRESP Mode. xx11x0000 = CRESP Mode: Ignore CRESP. xxxx00000 = Pre-Allocate maximum memory buffers (8). xxxx10000 = Pre-Allocate fewer memory buffers (4). When htm_mode_q(1 TO 2) = = 01, that is, OTHER. 00000xxxx = Pre-Allocate maximum memory buffers (8). 00001xxxx = Pre-Allocate fewer memory buffers (4). 0000xmmmx = mmm for optional external multiplexer control. 0000xxxx0 = Both -other- trace buses to NHTM0. 0000xxxx1 = Other trace bus0 to nhtm0, trace bus1 to nhtm1. High BW. When htm_mode_q(1 TO 2) = = 10, that is, OCC. 00000xxx0 = Pre-Allocate maximum memory buffers (8). 00001xxx0 = Pre-Allocate fewer memory buffers (4). 0000xmmm0 = mmm for optional external multiplexer control.
13	RW	HTMSC_MODE_WRAP: Enable Trace Wrap Mode. 0 = Stop trace when top of Trace Memory is reached. 1 = Wrap trace to beginning of Trace Memory.
14	RW	HTMSC_MODE_DIS_TSTAMP: Disable TimeStamp Writes. 0 = Write of timestamps enabled to indicate elapsed time between records. 1 = Timestamps written only to indicate record loss.
15	RW	HTMSC_MODE_SINGLE_TSTAMP: Disable Overflow Timestamps. 0 = Timestamp written to indicate elapsed time overflow. 1 = Only one timestamp is written between entries, overflow indication is lost.
16	RW	HTMSC_MODE_SPARE16: Not used in NHTM.
17	RW	HTMSC_MODE_MARKERS_ONLY: Enable Stamp/Marker Only Mode. 0 = Normal trace. 1 = Ignore incoming trace data and save only markers caused by HTM_TRIG writes, Global HTM markers enabled to be inserted into the trace record and enabled stamps.

Bits	SCOM	Field Mnemonic: Description
18	RW	HTMSC_MODE_DIS_FORCE_GROUP_SCOPE: Disable Group Scope. This is a processor bus debug bit. 0 = htm write ops sent with group scope. 1 = htm write ops sent with Vg scope using programmed target bits.
19:21	RW	HTMSC_MODE_SYNC_STAMP_FORCE: Control the number of cycles to wait to force a synchronization stamp or reset the timer.
22	RW	HTMSC_MODE_WRITETOIO: HTM Trace memory in IO space, use ci_pr_st op. 0 = Use HTM_CL_Write operation to target system memory. Do pre-allocation sequence. (default). 1 = Use ci_pr_st operation to target anywhere else. Dont do pre-allocate sequence.
23	RW	HTMSC_MODE_SPARE23: Not used in NHTM.
24:39	RW	HTMSC_MODE_VGTARGET: Vg Target bits should be configured if HTM_MEM[scope] is Vg. or if Disable Group Scope = 1.
40:43	RW	HTMSC_MODE_SPARE4043: NOt used in NHTM.
44:63	RO	Constant = 0b00000000000000000000

Register Name	HTM Memory Configuration Register
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_MEM
Address	00000000050128C1 (SCOM)
Description	HTM Memory Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MEM_ALLOC: 0 = memory based address not configured, 1 = memory address configured. This bit must be written to zero before setting since the HTM looks for. the 0 -> 1 transition on this bit to indicate the memory address has. been updated.
1:3	RW	HTMSC_MEM_SCOPE: Processor bus Scope to use when writing the HTM Trace memory. If the scope is not large enough, the HTM will get an address error. If the scope is too large, HTM will experience excessive delay.
4	RW	HTMSC_MEM_PRIORITY: Starting processor bus Priority. Configure the Starting priority used when writing the HTM Trace memory. Leave at default 000 unless there is a very good reason to change.
5	RW	HTMSC_MEM_SIZE_SMALL: Trace Memory Size Range. 0 = Trace Mem Size from 512M to 256G. 1 = Trace Mem Size from 16M to 8G.
6:7	RW	HTMSC_MEM_SPARE67: Not Used.
8:39	RW	HTMSC_MEM_BASE: Trace memory base address (8:39). The Trace Memory Base Address must be aligned on a Trace Memory Size boundary.
40:48	RW	HTMSC_MEM_SIZE: Trace Memory Size. When htmsc_mem_size_small = 0, these bits define the mask to bits (26:35) of the Trace Memory Base Address and define the size of the trace memory between 512MB and 256GB. When htmsc_mem_size_small = 1, these bits define the mask to bits (31:39) of the Trace Memory Base address and define the size of the trace memory between 16MB and 8GB.
49:63	RO	Constant = 0b000000000000000

Register Name	HTM Status Register
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_STAT
Address	00000000050128C2 (SCOM)
Description	HTM Status Register

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	HTMCO_STATUS_SPARE: Spare bits.
2	ROX	HTMCO_STATUS_CRESP_OV: Asserted on detection of a CRESP queue overwrite condition. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
3	ROX	HTMCO_STATUS_REPAIR: Asserted on occurence of address error to indicate the need of software to clear and update HTM_MEM. Will stay high until HTM_MEM updated.
4	ROX	HTMCO_STATUS_BUF_WAIT: Asserted on condition of data buffers full in tracing state. Any markers, stamps, and trace data recieved when this bit is set will be lost.
5	ROX	STATUS_TRIG_DROPPED_Q: Asserted on buffer overrun due to trigger lost at least once in the last trace. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
6	ROX	HTMCO_STATUS_ADDR_ERROR: Asserted on address error when write buffer was allocated. Need to set new address range after htmco_status_repair is asserted.
7	ROX	STATUS_REC_DROPPED_Q: Asserted on buffer overrun due to trace data lost at least once in the last trace. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
8	ROX	HTMCO_STATUS_INIT: Asserted when htm_cofsm is in Init state.
9	ROX	HTMCO_STATUS_PREREQ: Asserted when htm_cofsm is in Pre-req state.
10	ROX	HTMCO_STATUS_READY: Asserted when htm_cofsm is in Ready state.
11	ROX	HTMCO_STATUS_TRACING: Asserted when htm_cofsm is in Tracing state.
12	ROX	HTMCO_STATUS_PAUSED: Asserted when htm_cofsm is in Paused state.
13	ROX	HTMCO_STATUS_FLUSH: Asserted when htm_cofsm is in Flush state.
14	ROX	HTMCO_STATUS_COMPLETE: Asserted when htm_cofsm is in Complete state.
15	ROX	HTMCO_STATUS_ENABLE: Asserted when htm_cofsm is in Enable state.
16	ROX	HTMCO_STATUS_STAMP: Asserted when htm_cofsm is in Stamp state.
17	ROX	STATUS_SCOM_ERROR: Asserted to indicate that a SCOM error indication was received from the SCOM satellite. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
18	ROX	STATUS_PARITY_ERROR: Asserted to indicate a parity error was detected on the processor bus. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
19	ROX	STATUS_INVALID_CRESP: Asserted to indicate an invalid CRESP was received from the processor bus. NHTM is hung. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	HTM Last Address Register
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_LAST
Address	00000000050128C3 (SCOM)
Description	HTM Last Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000

Bits	SCOM	Field Mnemonic: Description
8:56	ROX	HTM_LAST_ADDRESS: The last cache line address of the memory trace. Guaranteed valid only when HTM is in the Complete state.
57:63	RO	Constant = 0b0000000

Register Name	HTM SCOM Trigger Register
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_TRIG
Address	00000000050128C4 (SCOM)
Description	HTM SCOM Trigger Register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_TRIG_START: Start trigger.
1	RW	HTMSC_TRIG_STOP: Stop trigger.
2	RW	HTMSC_TRIG_PAUSE: Pause trigger.
3	RW	HTMSC_TRIG_STOP_ALT: Stop trigger 2. Legacy bit that used to be the Freeze Trigger in POWER6 implementation.
4	RW	HTMSC_TRIG_RESET: Reset trigger.
5	RW	HTMSC_TRIG_MARK_VALID: Mark type valid.
6:15	RW	HTMSC_TRIG_MARK_TYPE: Mark type is put into Mark Record when bit 5 is set.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	HTM Trigger Control Register
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_CTRL
Address	00000000050128C5 (SCOM)
Description	HTM Trigger Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	HTMSC_CTRL_TRIG: Trigger Control. 00 = local triggers are not forwarded to the processor bus, it is inserted into the trace when tracing. Both local and global triggers control the HTM. 01 = local triggers are not forwarded to the processor bus, it is inserted into the trace when tracing. Only local triggers control the HTM. 1x = local triggers are forwarded to the processor bus, it is not inserted into the trace when tracing. Only global triggers control the HTM.
2:3	RW	Reserved.
4:5	RW	HTMSC_CTRL_MARK: Marker Control. 00 local markers are not forwarded to the processor bus. Both local and global markers are inserted into the trace. 01 = local markers are not forwarded to the processor bus. Only local markers are inserted into the trace. 10 = local markers are forwarded to the processor bus. Only global markers are inserted into the trace. 11 = local markers are forwarded to the processor bus. Markers are not inserted into the trace (Fabric Trace Mode).
6	RW	HTMSC_CTRL_DBG0_STOP: Enable Stop on PB Chiplet Debug Trigger 0.
7	RW	HTMSC_CTRL_DBG1_STOP: Enable Stop on PB Chiplet Debug Trigger 1.
8	RW	HTMSC_CTRL_RUN_STOP: Enable Stop on falling edge of PB Chiplet trace_run.

Bits	SCOM	Field Mnemonic: Description
9	RW	HTMSC_CTRL_OTHER_DBG0_STOP: Enable Stop using OCC Control.
10:12	RW	HTMSC_CTRL_SPARE1012: Spare bits.
13	RW	HTMSC_CTRL_XSTOP_STOP: Enable Stop on chiplet XSTOP.
14:15	RW	HTMSC_CTRL_SPARE1415: Spare bits.
16:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	**HTM Filter Control Register**
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_FILT
Address	00000000050128C6 (SCOM)
Description	HTM Filter Control Register

Bits	SCOM	Field Mnemonic: Description
0:22	RW	HTMSC_FILT_PAT: Filter Pattern. In Fabric Trace Mode, Defines the TTAG/Scope/Source pattern to Match in the RCMD and CRESP. 0:3 = RCMD_ttag(0:2) Group ID Pattern for RCMD and CRESP filtering. 4:6 = RCMD_ttag(3:5) Chip ID Pattern for RCMD and CRESP filtering. 7:16 = RCMD_ttag(6:13) Unit ID Pattern for RCMD and CRESP (if from this chip) filtering. 17:19 = RCMD_scope(0:2) Scope Pattern for RCMD and CRESP filtering. 20:21 = RCMD_source(0:1) Source Pattern for RCMD filtering. 22 = Powerbus PORT pattern for RCMD and CRESP filtering. In OCC Trace Mode, Defines the occ_trace_data(0:22) pattern to match. 0:22 = occ_trace_data(0:22) Pattern.
23:26	RW	Reserved.
27:31	RW	HTMSC_FILT_CRESP_PAT: CRESP Filter Pattern. In Fabric Trace Mode, Defines the CRESP pattern to match.
32:54	RW	HTMSC_FILT_MASK: Pattern mask. Bits set to 1 in this mask do not need to match w/ the Filter Pattern. If all mask bits are set, No pattern matching is done.
55:58	RW	Reserved.
59:63	RW	HTMSC_FILT_CRESP_MASK: CRESP Filter Mask. Bits set to 1 in this mask do not need to match w/ the CRESP Filter Pattern. If all mask bits are set, no pattern matching is done.

Register Name	**HTM TTYPE Filter Control Register**
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_TTYPEFILT
Address	00000000050128C7 (SCOM)
Description	HTM Ttype Filter Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1:7	RW	HTMSC_TTYPEFILT_PAT: TTYPE Pattern. In Fabric Trace Mode, Defines the TTYPE pattern to Match.
8:15	RW	HTMSC_TSIZEFILT_PAT: TSIZE Pattern. In Fabric Trace Mode, Defines the TSIZE pattern to Match.

Bits	SCOM	Field Mnemonic: Description
16	RW	Reserved.
17:23	RW	HTMSC_TTYPEFILT_MASK: TTYPE Pattern mask. TTYPE Bits set to 1 in this mask do not need to match w/ the Pattern. If all mask bits are set, No TTYPE pattern/masking is done.
24:31	RW	HTMSC_TSIZEFILT_MASK: TSIZE Pattern mask. TSIZE Bits set to 1 in this mask do not need to match w/ the Pattern. If all mask bits are set, No TSIZE pattern/masking is done.
32	RW	HTMSC_TTYPEFILT_INVERT: TTYPE/TSIZE Capture Invert. 0 = Capture record based on ttype/tsize pattern matching. 1 = Capture record based on ttype/tsize pattern NOT matching.
33	RW	HTMSC_CRESPFILT_INVERT: CRESP Filter Capture Invert. 0 = Capture record based on CRESP filter pattern matching. 1 = Capture record based on CRESP filter pattern NOT matching.
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	**HTM Configuration Register**
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_CFG
Address	00000000050128C8 (SCOM)
Description	HTM Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:4	RW	HTMSC_CFG_OPER_HANG_DIV_RATIO: Processor bus Operational Hang Divider. This register is used to set the hang count divider for operational. hangs. If this register is NOT initialized, the default hang_div_ratio. is b01000 setup on the first functional clock.
5:8	RW	HTMSC_CFG_RTY_DRP_COUNT: Processor bus Retry Drop Counter Max. This is the maximum value to count RTY_DRP CRESP before increasing the drop priority. used when sending the next command. If this register is NOT initialized, the default. max count is b0111 setup on the first functional clock.
9	RW	HTMSC_CFG_DIS_DRP_PRIORITY_INCR: Disable Increase of Drop Priority.
10	RW	HTMSC_CFG_DIS_RETRY_BACKOFF: Disable processor bus Retry Backoff. 0 = Powerbus Retry Backoff works according to PB Arch Ver 3xx. 1 = Powerbus Retry Backoff disabled, retry immediately if receive retry cresp.
11	RW	HTMSC_CFG_DIS_OPER_HANG: Disable processor bus Operational Hang Detect. 0 = Powerbus Operation Hang Detect works according to PB Arch Ver 3xx. 1 = Powerbus Operation Hang Detect disabled, PRSP Rty_Other never asserted.
12:19	RW	Reserved.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	**HTM Flex Multiplexer Register**
Mnemonic	BRIDGE.NHTM.NHTM1.SC.HTM_FLEX
Address	00000000050128C9 (SCOM)
Description	HTM Flex Multiplexer Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	HTMSC_FMUX_RGRPSEL0: RCMD Group 0 Select for RCMD record bits(19:22). Default is 1100 for RCMDx_adr(58:61).
4:7	RW	HTMSC_FMUX_RGRPSEL1: RCMD Group 1 Select for RCMD record bits(23:26). Default is 1011 for RCMDx_ttag(18:21).
8:11	RW	HTMSC_FMUX_RGRPSEL2: RCMD Group 2 Select for RCMD record bits(27:30). Default is 0011 for RCMDx_adr(16:19).
12:15	RW	HTMSC_FMUX_RGRPSEL3: RCMD Group 3 Select for RCMD record bits(31:34). Default is 0100 for RCMDx_adr(20:23).
16:19	RW	HTMSC_FMUX_RGRPSEL4: RCMD Group 4 Select for RCMD record bits(35:38). Default is 0101 for RCMDx_adr(24:27).
20:23	RW	HTMSC_FMUX_RGRPSEL5: RCMD Group 5 Select for RCMD record bits(39:42). Default is 0110 for RCMDx_adr(28:31).
24:27	RW	HTMSC_FMUX_CGRPSEL0: CRESP Flex Group 0 Select for CRESP record bits(122:123). Default is 0001 for crx_target(0:1).
28:31	RW	HTMSC_FMUX_CGRPSEL1: CRESP Flex Group 1 Select for CRESP record bits(124:125). Default is 0010 for crx_target(2:3).
32:35	RW	HTMSC_FMUX_CGRPSEL2: CRESP Flex Group 2 Select for CRESP record bits(126:127). Default is 1001 for crx_ds(0:1).
36:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	**PSI Host Bridge FIR Register**
Mnemonic	BRIDGE.PSIHB.PSIHB_FIR_REG
Address	0000000005012900 (SCOM) 0000000005012901 (SCOM1) 0000000005012902 (SCOM2)
Description	PSI Host Bridge FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_ECC_ERR_CE: CE from processor bus data.
1	RWX	WOX_AND	WOX_OR	PB_ECC_ERR_UE: UE from processor bus data.
2	RWX	WOX_AND	WOX_OR	PB_ECC_ERR_SUE: SUE from processor bus data.
3	RWX	WOX_AND	WOX_OR	INTERRUPT_FROM_ERROR: Interrupt Condition present in PSIHB.
4	RWX	WOX_AND	WOX_OR	INTERRUPT_FROM_FSP: Interrupt from FSP is being processed.
5	RWX	WOX_AND	WOX_OR	FSP_ECC_ERR_CE: CE from PSILL data.
6	RWX	WOX_AND	WOX_OR	FSP_ECC_ERR_UE: UE from PSILL data.
7	RWX	WOX_AND	WOX_OR	ERROR_STATE: Error bit set, ignores the interrupt mask.
8	RWX	WOX_AND	WOX_OR	INVALID_TTYPE: Invalid TType Hit on PHB or FSP bar.
9	RWX	WOX_AND	WOX_OR	INVALID_CRESP: Invalid CRESP returned to command issued by PSIHB.
10	RWX	WOX_AND	WOX_OR	PB_DATA_TIME_OUT: Processor bus time out waiting for data grant.
11	RWX	WOX_AND	WOX_OR	PB_PARITY_ERROR: PB parity error.
12	RWX	WOX_AND	WOX_OR	FSP_ACCESS_TRUSTED_SPACE: FSP tried access to trusted space.
13	RWX	WOX_AND	WOX_OR	UNEXPECTED_PB: Unexpected PB CRESP or DATA.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
14	RWX	WOX_AND	WOX_OR	INTERRUPT_REG_CHANGE_WHILE_ACTIVE: Interrupt register change while interrupt still pending.
15	RWX	WOX_AND	WOX_OR	INTERRUPT0_ADDRESS_ERROR: PSI Interrupt address Error.
16	RWX	WOX_AND	WOX_OR	INTERRUPT1_ADDRESS_ERROR: OCC Interrupt address Error.
17	RWX	WOX_AND	WOX_OR	INTERRUPT2_ADDRESS_ERROR: FSI Interrupt address Error.
18	RWX	WOX_AND	WOX_OR	INTERRUPT3_ADDRESS_ERROR: LPC Interrupt address Error.
19	RWX	WOX_AND	WOX_OR	INTERRUPT4_ADDRESS_ERROR: LOCAL ERROR Interrupt address Error.
20	RWX	WOX_AND	WOX_OR	INTERRUPT5_ADDRESS_ERROR: HOST ERROR Interrupt address Error.
21	RWX	WOX_AND	WOX_OR	TCBR_TP_PSI_GLB_ERR_0: PSI global error bit 0.
22	RWX	WOX_AND	WOX_OR	TCBR_TP_PSI_GLB_ERR_1: PSI global error bit 1.
23	RWX	WOX_AND	WOX_OR	UPSTREAM_FIR: Upstream error.
24:26	RWX	WOX_AND	WOX_OR	SPARE_FIR: Spare fir.
27	RWX	WOX_AND	WOX_OR	SCOM_ERROR: SCOM error.
28	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERROR: FIR parity Error.
29:45	RO	RO	RO	Constant = 0b00000000000000000

Register Name	PSI Host Bridge FIR Mask Register
Mnemonic	BRIDGE.PSIHB.PSIHB_FIR_MASK_REG
Address	0000000005012903 (SCOM) 0000000005012904 (SCOM1) 0000000005012905 (SCOM2)
Description	PSI Host Bridge FIR Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	PB_ECC_ERR_CE_MASK: Mask for CE from processor bus data.
1	RW	WO_AND	WO_OR	PB_ECC_ERR_UE_MASK: Mask for UE from processor bus data.
2	RW	WO_AND	WO_OR	PB_ECC_ERR_SUE_MASK: Mask for SUE from processor bus data.
3	RW	WO_AND	WO_OR	INTERRUPT_FROM_ERROR_MASK: Mask for Interrupt Condition present in PSIHB.
4	RW	WO_AND	WO_OR	INTERRUPT_FROM_FSP_MASK: Mask for Interrupt from FSP is being processed.
5	RW	WO_AND	WO_OR	FSP_ECC_ERR_CE_MASK: Mask for CE from PSILL data.
6	RW	WO_AND	WO_OR	FSP_ECC_ERR_UE_MASK: Mask for UE from PSILL data.
7	RW	WO_AND	WO_OR	ERROR_STATE_MASK: Mask for Error bit set, ignores the interrupt mask.
8	RW	WO_AND	WO_OR	INVALID_TTYPE_MASK: Mask for Invalid TType Hit on PHB or FSP bar.
9	RW	WO_AND	WO_OR	INVALID_CRESP_MASK: Mask for Invalid CRESP returned to command issued by PSIHB.
10	RW	WO_AND	WO_OR	PB_DATA_TIME_OUT_MASK: Mask for processor bus time out waiting for data grant.
11	RW	WO_AND	WO_OR	PB_PARITY_ERROR_MASK: PB parity error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
12	RW	WO_AND	WO_OR	FSP_ACCESS_TRUSTED_SPACE_MASK: FSP tried access to trusted space.
13	RW	WO_AND	WO_OR	UNEXPECTED_PB_MASK: Unexpected PB CRESP or DATA.
14	RW	WO_AND	WO_OR	INTERRUPT_REG_CHANGE_WHILE_ACTIVE_MASK: Interrupt register change while interrupt still pending.
15	RW	WO_AND	WO_OR	INTERRUPT0_ADDRESS_ERROR_MASK: PSI Interrupt address error_mask.
16	RW	WO_AND	WO_OR	INTERRUPT1_ADDRESS_ERROR_MASK: OCC Interrupt address error_mask.
17	RW	WO_AND	WO_OR	INTERRUPT2_ADDRESS_ERROR_MASK: FSI Interrupt address error_mask.
18	RW	WO_AND	WO_OR	INTERRUPT3_ADDRESS_ERROR_MASK: LPC Interrupt address error_mask.
19	RW	WO_AND	WO_OR	INTERRUPT4_ADDRESS_ERROR_MASK: LOCAL error_mask Interrupt address error_mask.
20	RW	WO_AND	WO_OR	INTERRUPT5_ADDRESS_ERROR_MASK: HOST error_mask Interrupt address error_mask.
21	RW	WO_AND	WO_OR	TCBR_TP_PSI_GLB_ERR_0_MASK: PSI global_mask error bit 0.
22	RW	WO_AND	WO_OR	TCBR_TP_PSI_GLB_ERR_1_MASK: PSI global_mask error bit 1.
23	RW	WO_AND	WO_OR	UPSTREAM_FIR_MASK: Upstream error.
24:26	RW	WO_AND	WO_OR	SPARE_FIR_MASK: Spare fir.
27	RW	WO_AND	WO_OR	SCOM_ERROR_MASK: SCOM Error.
28	RW	WO_AND	WO_OR	FIR_PARITY_ERROR_MASK: FIR parity Error.
29:45	RO	RO	RO	Constant = 0b00000000000000000

Register Name	PSI Host Bridge FIR Action0 Register
Mnemonic	BRIDGE.PSIHB.PSIHB_FIR_ACTION0_REG
Address	0000000005012906 (SCOM)
Description	PSI Host Bridge FIR Action0 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = No Error (0,1) = recoverable error (1,0) = Checkstop Error (1,1) = unused

Bits	SCOM	Field Mnemonic: Description
0	RO	PB_ECC_ERR_CE_ACTION0: Action0 for CE from processor bus data.
1	RO	PB_ECC_ERR_UE_ACTION0: Action0 for UE from processor bus data.
2	RO	PB_ECC_ERR_SUE_ACTION0: Action0 for SUE from processor bus data.
3	RO	INTERRUPT_FROM_ERROR_ACTION0: Action0 for Interrupt Condition present in PSIHB.
4	RO	INTERRUPT_FROM_FSP_ACTION0: Action0 for Interrupt from FSP is being processed.
5	RO	FSP_ECC_ERR_CE_ACTION0: Action0 for CE from PSILL data.
6	RO	FSP_ECC_ERR_UE_ACTION0: Action0 for UE from PSILL data.

Bits	SCOM	Field Mnemonic: Description
7	RO	ERROR_STATE_ACTION0: Action0 for Error bit set, ignores the interrupt mask.
8	RO	INVALID_TTYPE_ACTION0: Action0 for Invalid TType Hit on PHB or FSP bar.
9	RO	INVALID_CRESP_ACTION0: Action0 for Invalid CRESP returned to command issued by PSIHB.
10	RO	PB_DATA_TIME_OUT_ACTION0: Action0 for processor bus time out waiting for data grant.
11	RO	PB_PARITY_ERROR_ACTION0: PB parity error.
12	RO	FSP_ACCESS_TRUSTED_SPACE_ACTION0: FSP tried access to trusted space.
13	RO	UNEXPECTED_PB_ACTION0: Unexpected PB CRESP or DATA.
14	RO	INTERRUPT_REG_CHANGE_WHILE_ACTIVE_ACTION0: Interrupt register change while interrupt still pending.
15	RO	INTERRUPT0_ADDRESS_ERROR_ACTION0: PSI Interrupt address error_action0.
16	RO	INTERRUPT1_ADDRESS_ERROR_ACTION0: OCC Interrupt address error_action0.
17	RO	INTERRUPT2_ADDRESS_ERROR_ACTION0: FSI Interrupt address error_action0.
18	RO	INTERRUPT3_ADDRESS_ERROR_ACTION0: LPC Interrupt address error_action0.
19	RO	INTERRUPT4_ADDRESS_ERROR_ACTION0: LOCAL error_action0 Interrupt address error_action0.
20	RO	INTERRUPT5_ADDRESS_ERROR_ACTION0: HOST error_action0 Interrupt address error_action0.
21	RO	TCBR_TP_PSI_GLB_ERR_0_ACTION0: PSI global_action0 error bit 0.
22	RO	TCBR_TP_PSI_GLB_ERR_1_ACTION0: PSI global_action0 error bit 1.
23	RO	UPSTREAM_FIR_ACTION0: Upstream error.
24:26	RO	SPARE_FIR_ACTION0: Spare fir.
27	RO	SCOM_ERROR_ACTION0: SCOM Error.
28	RO	FIR_PARITY_ERROR_ACTION0: FIR parity Error.
29:49	RO	Constant = 0b00000000000000000000

Register Name	**PSI Host Bridge FIR Action1 Register**
Mnemonic	BRIDGE.PSIHB.PSIHB_FIR_ACTION1_REG
Address	0000000005012907 (SCOM)
Description	PSI Host Bridge FIR action1 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = No Error (0,1) = recoverable error (1,0) = Checkstop Error (1,1) = unused

Bits	SCOM	Field Mnemonic: Description
0	RO	PB_ECC_ERR_CE_ACTION1: Action1 for CE from processor bus data.
1	RO	PB_ECC_ERR_UE_ACTION1: Action1 for UE from processor bus data.
2	RO	PB_ECC_ERR_SUE_ACTION1: Action1 for SUE from processor bus data.
3	RO	INTERRUPT_FROM_ERROR_ACTION1: Action1 for Interrupt Condition present in PSIHB.
4	RO	INTERRUPT_FROM_FSP_ACTION1: Action1 for Interrupt from FSP is being processed.
5	RO	FSP_ECC_ERR_CE_ACTION1: Action1 for CE from PSILL data.
6	RO	FSP_ECC_ERR_UE_ACTION1: Action1 for UE from PSILL data.

Bits	SCOM	Field Mnemonic: Description
7	RO	ERROR_STATE_ACTION1: Action1 for Error bit set, ignores the interrupt mask.
8	RO	INVALID_TTYPE_ACTION1: Action1 for Invalid TType Hit on PHB or FSP bar.
9	RO	INVALID_CRESP_ACTION1: Action1 for Invalid CRESP returned to command issued by PSIHB.
10	RO	PB_DATA_TIME_OUT_ACTION1: Action1 for processor bus time out waiting for data grant.
11	RO	PB_PARITY_ERROR_ACTION1: PB parity error.
12	RO	FSP_ACCESS_TRUSTED_SPACE_ACTION1: FSP tried access to trusted space.
13	RO	UNEXPECTED_PB_ACTION1: Unexpected PB CRESP or DATA.
14	RO	INTERRUPT_REG_CHANGE_WHILE_ACTIVE_ACTION1: Interrupt register change while interrupt still pending.
15	RO	INTERRUPT0_ADDRESS_ERROR_ACTION1: PSI Interrupt address error_action1.
16	RO	INTERRUPT1_ADDRESS_ERROR_ACTION1: OCC Interrupt address error_action1.
17	RO	INTERRUPT2_ADDRESS_ERROR_ACTION1: FSI Interrupt address error_action1.
18	RO	INTERRUPT3_ADDRESS_ERROR_ACTION1: LPC Interrupt address error_action1.
19	RO	INTERRUPT4_ADDRESS_ERROR_ACTION1: LOCAL error_action1 Interrupt address error_action1.
20	RO	INTERRUPT5_ADDRESS_ERROR_ACTION1: HOST error_action1 Interrupt address error_action1.
21	RO	TCBR_TP_PSI_GLB_ERR_0_ACTION1: PSI global_action1 error bit 0.
22	RO	TCBR_TP_PSI_GLB_ERR_1_ACTION1: PSI global_action1 error bit 1.
23	RO	UPSTREAM_FIR_ACTION1: Upstream error.
24:26	RO	SPARE_FIR_ACTION1: Spare fir.
27	RO	SCOM_ERROR_ACTION1: SCOM Error.
28	RO	FIR_PARITY_ERROR_ACTION1: FIR parity Error.
29:49	RO	Constant = 0b00000000000000000000

Register Name	PSI Host Bridge BAR Register
Mnemonic	BRIDGE.PSIHB.PSI_BRIDGE_BAR_REG
Address	000000000501290A (SCOM)
Description	PSI Host Bridge Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:43	RWX	PSI_BRIDGE_BAR: The Bridge Base Address Register contains the address range which contains the MMIO accessible PSIHB unit registers. Address bits 8 to 43 of the PSI unit base address are specified with this IDial.
44:62	RO	Constant = 0b00000000000000000000
63	RWX	PSI_BRIDGE_BAR_EN: this Switch is set to ON to indicate the base address contained in the PSIHB Base Address Register is valid and enabled.

Register Name	PSI Host Bridge FSP BAR Register
Mnemonic	BRIDGE.PSIHB.PSI_BRIDGE_FSP_BAR_REG
Address	000000000501290B (SCOM)
Description	FSP Base Address Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:43	RWX	FSP_BAR: The FSP Base Address Register contains the address range which contains the MMIO accessible FSP unit registers. Address bits 8 to 43 of the FSP base address are specified with this IDial.

Register Name	PSI Host Bridge FSP MMR Register
Mnemonic	BRIDGE.PSIHB.PSI_FSP_MMR_REG
Address	000000000501290C (SCOM)
Description	FSP Memory Mask Register

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Constant = 0b00000000000000000000000000000000
32:43	RWX	FSP_MMR: The FSP Mem ory Mask Register contains the mask which modifies which bits of the FSP Base Address are used in the detection of matching addresses. Bits 32 to 43 of the memory mask are specified with this IDial.

Register Name	PSI Host Bridge Status Control Register
Mnemonic	BRIDGE.PSIHB.PSIHB_STATUS_CTL_REG
Address	000000000501290E (SCOM) 0000000005012912 (SCOM1) 0000000005012913 (SCOM2)
Description	PSI Host Bridge Control/Status Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_OR	WOX_CLEAR	FSP_CMD_ENABLE: When set to 0 , all DMA and Interrupt commands issued by the FSP are ignored by the GX unit. When set to 1 , all DMA and interrupt commands issued by the FSP are accepted and executed.
1	RWX	WOX_OR	WOX_CLEAR	FSP_MMIO_ENABLE: When set to 0 , the FSPBAR is ignored and no MMIO operations are issued to the FSP. When set to 1 , MMIO operations to the FSP memory region defined by the FSPBAR are accepted and transmitted to the FSP.
2	RWX	WOX_OR	WOX_CLEAR	PHBCSR_SPARE: Spare.
3	RWX	WOX_OR	WOX_CLEAR	FSP_INT_ENABLE: Enables incoming PSI interrupt commands to interrupt the CEC when set to 1.
4	RWX	WOX_OR	WOX_CLEAR	FSP_ERR_RSP_ENABLE: Enables launch of error response packet from GXC to FSP when errors are detected on incoming DMA commands.
5	RWX	WOX_OR	WOX_CLEAR	PSI_LINK_ENABLE: This bit indicates the PSI link is enabled when set to 1. A 0 indicates the PSI link is disabled.
6	RWX	WOX_OR	WOX_CLEAR	FSP_RESET: When this bit transitions from 0 to 1 , an encoded reset sequence is sent to the FSP.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
7	WOX_6P	WOX_6P	NCX	PSIHBC_RESET: When this bit transitions from 0 to 1 , the internal state machines in the GX FSP attach function are erset to idle.
8:11	RWX	WOX_OR	WOX_CLEAR	FSP_MMIO_MASK: This LDial controls the use of system address bits 32:35 when transmitting an address to the FSP. The mask size selected corresponds to an address mask which is ANDed with address bits 32:35 of addresses passed from the CEC to the PSI/FSP. All upper address bits, 18:31, are stripped and replaced with 0s.
12:15	RO	RO	RO	Constant = 0b0000
16	ROX	NCX	NCX	CEC_PSI_INTERRUPT: Read Only - Set to 1 by hardware when an interruption is present in the GXC FSP attachment function.
17	RWX	WOX_OR	WOX_CLEAR	FSP_INTERRUPT: Set to 1 when an Interrupt set command is received from the incoming PSI interface. Set to 0 when an Interrupt reset command is received from the incoming PSI interface.
18	ROX	NCX	NCX	FSP_LINK_ACTIVE: Set to 1 when the PSI link is active and working.
19	ROX	NCX	NCX	FSP_OUTBOUND_ACTIVE: Set to 1 when the outbound queue or controls are busy.
20	ROX	NCX	NCX	FSP_INBOUND_ACTIVE: Set to 1 when the inbound queue or controls are busy.
21	ROX	NCX	NCX	PSIFSP_LOAD_OUTSTANDING: Set to 1 when an MMIO is received, reset when data is delivered to fabric.
22	ROX	NCX	NCX	PSIFSP_DMAR_OUTSTANDING: Set to 1 when a dmar is received, reset when data is delivered to PSI.
23	ROX	NCX	NCX	PSIFSP_INT_BUSY: Set to 1 whenever int state machine is not idle.
24:31	RO	RO	RO	Constant = 0b00000000
32	ROX	NCX	NCX	PSI_XMIT_ERROR: Set to 1 when the PSI macro detects a fatal error.
33	RWX	WOX_OR	WOX_CLEAR	PSI_LINK_INACTIVE_TRANS: Set to 1 when the PSI link transitions from 1 to 0.
34	RWX	WOX_OR	WOX_CLEAR	PSIFSP_ACK_TIMEOUT: Set when a command to the FSP interface has not been acknowledged within TBD cycles.
35	RWX	WOX_OR	WOX_CLEAR	PSIFSP_MMIO_LOAD_TIMEOUT: Set when a reply packet is not received within TBD cycles after an MMIO is sent to the FSP.
36	RWX	WOX_OR	WOX_CLEAR	PSIFSP_MMIO_LENGTH_ERR: Set when an MMIO is targets the region defined by the PSIBAR and has a length of anything other than 8 bytes.
37	RWX	WOX_OR	WOX_CLEAR	PSIFSP_MMIO_ADDR_ERR: Set when an MMIO operation targets the region defined by the PSIBAR but does not target one of the defined registers.
38	RWX	WOX_OR	WOX_CLEAR	PSIFSP_MMIO_TYPE_ERR: Set when an operation targets the region defined by the PSIBAR or FSPBAR but does not have a valid ttype.
39	RWX	WOX_OR	WOX_CLEAR	PSI_UE: Set when an uncorrectable error is detected on the incoming PSI link.
40	RWX	WOX_OR	WOX_CLEAR	PSIFSP_PERR: Set when a parity error is detected in the PSI FSP attach function.
41	RWX	WOX_OR	WOX_CLEAR	PSI_ALERT1: Set the FSP detects an error with an MMIO command, but is able to continue processing MMIO commands.
42	RWX	WOX_OR	WOX_CLEAR	PSI_ALERT2: Set the FSP detects an error with an MMIO command, and is unable to continue processing MMIO commands.
43	RWX	WOX_OR	WOX_CLEAR	PSIFSP_DMA_ERR: Set the PSIC detects any error with an incoming DMA command.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
44:47	RO	RO	RO	Constant = 0b0000
48	RWX	WOX_OR	WOX_CLEAR	PSIFSP_DMA_ADDR_ERR: Set when a DMA access targets a system memory address that does not exist.
49	RWX	WOX_OR	WOX_CLEAR	PSIFSP_TCE_EXTENT_ERR: Set when a DMA access would result in a TCE fetch beyond the end of the TCE table in system memory.
50	RWX	WOX_OR	WOX_CLEAR	PSIFSP_PAGE_FAULT: Set when a DMA access uses a TCE entry that is inconsistent with the access control bits of the TCE.
51	RWX	WOX_OR	WOX_CLEAR	PSIFSP_INV_OP: Set when an incoming PSI command does not contain a valid opcode.
52	RWX	WOX_OR	WOX_CLEAR	FSP_INV_READ: Set when a read DMA operation is received before read response data has been received for a prior DMA read.

Register Name	**PSI Host Bridge Error Mask Register**
Mnemonic	BRIDGE.PSIHB.PSIHB_ERROR_MASK_REG
Address	000000000501290F (SCOM)
Description	PSI Host Bridge Error Mask Register

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:27	RWX	ERROR_DISABLE_1: Any bit when set to 1 prevents hardware from setting the corresponding bit in PSIHBC bits 32:43. Entry into the error state is also prevented.
28:31	RO	Constant = 0b0000
32:43	RWX	INTERRUPT_DISABLE: Any bit when set to 1 prevents hardware from signaling an interrupt to the INTP when the corresponding bit in the PSIHBC bits 32:43 is set.
44:47	RO	Constant = 0b0000
48:52	RWX	ERROR_DISABLE_2: Any bit when set to 1 prevents hardware from setting the corresponding bit in PSIHBC bits 48:52.

Register Name	**PSI Host Bridge Debug Register**
Mnemonic	BRIDGE.PSIHB.PSIHB_DEBUG_REG
Address	0000000005012911 (SCOM)
Description	PSI Host Bridge Debug Service Register

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	PSIHB2FSP_INJ_ERR_BITS: Setting a single bit will cause a correctable error when inject once or constant is set. Setting both bits will cause an uncorrectable error when inject once or constant is set.
2	RWX	PSIHB2FSP_INJ_ONCE: This bit will cause a single CE or UE depending on how the error bits are set.
3	RWX	PSIHB2FSP_INJ_CONST: This bit will cause a constant CE or UE depending on how the error bits are set.
4:7	RO	Constant = 0b0000
8:9	RWX	PSIHB2PB_INJ_ERR_BITS: Setting a single bit will cause a correctable error when inject once or constant is set. Setting both bits will cause an uncorrectable error when inject once or constant is set.
10	RWX	PSIHB2PB_INJ_ONCE: This bit will cause a single CE or UE depending on how the error bits are set.
11	RWX	PSIHB2PB_INJ_CONST: This bit will cause a constant CE or UE depending on how the error bits are set.

Bits	SCOM	Field Mnemonic: Description
12:15	RO	Constant = 0b0000
16:19	RWX	TRACE_SEL: Used to select different sets of signals to be traced.

Register Name	PSI Host Bridge DMA Upper Bits Address Register
Mnemonic	BRIDGE.PSIHB.DMA_UP_ADDR
Address	0000000005012914 (SCOM)
Description	DMA ADDR Upper bits

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	DMA_BASE_UPPER_BITS: DMA base upper bits 8:15.
8:15	RO	Constant = 0b00000000
16:63	RW	DMA_ESCAPE_ADDRESS: DMA escape address 16:63, defaults to FFFFFFFFFFF8. It actually inverts the output of the register to create this default.

Register Name	PSI Host Bridge Interrupt Control Register
Mnemonic	BRIDGE.PSIHB.PSIHB_INTERRUPT_CONTROL
Address	0000000005012915 (SCOM)
Description	PSI Host Bridge Interrupt Control Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	ESB_OR_LSI_INTERRUPTS: Selects ESB or LSI interrupt handling, 0 - ESB.
1	WOX_6P	INTERRUPT_SM_RESET: When this bit transitions from 0 to 1, an encoded reset sequence is sent to the Interrupt.

Register Name	PSI Host Bridge ESB CI Base Address Register
Mnemonic	BRIDGE.PSIHB.ESB_CI_BASE
Address	0000000005012916 (SCOM)
Description	ESB CI Base address

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:47	RWX	ESB_BASE: ESB CI BASE 8:51.
48:62	RO	Constant = 0b000000000000000
63	RWX	ESB_BASE_VALID: ESB CI Base valid.

Register Name	PSI Host Bridge ESB Notification Address Register
Mnemonic	BRIDGE.PSIHB.ESB_NOTIFY
Address	0000000005012917 (SCOM)
Description	ESB Notification address

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:60	RWX	ESB_NOTIFY_ADDR: ESB Notify Address 8:60.
61:62	RO	Constant = 0b00
63	RWX	ESB_NOTIFY_VALID: ESB Notify Address valid.

Register Name	PSI Host Bridge IVT Offset Register
Mnemonic	BRIDGE.PSIHB.IVT_OFFSET
Address	0000000005012918 (SCOM)
Description	ESB Notification address

Bits	SCOM	Field Mnemonic: Description
0:27	RWX	IVT_OFFSET_PAYLOAD: IVT OFFSET.
28:63	RO	Constant = 0b000000000000000000000000000000000000

Register Name	PSI Interrupt Level Register
Mnemonic	BRIDGE.PSIHB.PSIHB_INTERRUPT_LEVEL
Address	0000000005012919 (SCOM)
Description	PSI Interrupt Level Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7:10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13	ROX	Reserved.
14	ROX	Reserved.
15	ROX	Reserved.
16	ROX	Reserved.
17:18	ROX	Reserved.
19	RW	Reserved.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	PSI Interrupt Status Register
Mnemonic	BRIDGE.PSIHB.PSIHB_INTERRUPT_STATUS
Address	000000000501291A (SCOM)
Description	PSI Interrupt Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7:10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13	ROX	Reserved.
14:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	HCA EH FIR Register
Mnemonic	BRIDGE.HCA.EHHCA_FIR_REG
Address	0000000005012980 (SCOM) 0000000005012981 (SCOM1) 0000000005012982 (SCOM2)
Description	HCA EH FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	CE1_0_OUT: array0_a CE.
1	RWX	WOX_AND	WOX_OR	CE2_0_OUT: array0_b CE.
2	RWX	WOX_AND	WOX_OR	UE1_0_OUT: array0_a UE.
3	RWX	WOX_AND	WOX_OR	UE2_0_OUT: array0_b UE.
4	RWX	WOX_AND	WOX_OR	CE1_1_OUT: array1_a CE.
5	RWX	WOX_AND	WOX_OR	CE2_1_OUT: array1_b CE.
6	RWX	WOX_AND	WOX_OR	UE1_1_OUT: array1_a UE.
7	RWX	WOX_AND	WOX_OR	UE2_1_OUT: array1_b UE.
8	RWX	WOX_AND	WOX_OR	CE1_2_OUT: array2_a CE.
9	RWX	WOX_AND	WOX_OR	CE2_2_OUT: array2_b CE.
10	RWX	WOX_AND	WOX_OR	UE1_2_OUT: array2_a UE.
11	RWX	WOX_AND	WOX_OR	UE2_2_OUT: array2_b UE.
12	RWX	WOX_AND	WOX_OR	CE1_3_OUT: array3_a CE.
13	RWX	WOX_AND	WOX_OR	CE2_3_OUT: array3_b CE.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
14	RWX	WOX_AND	WOX_OR	UE1_3_OUT: array3_a UE.
15	RWX	WOX_AND	WOX_OR	UE2_3_OUT: array3_b UE.
16	RWX	WOX_AND	WOX_OR	CE1_4_OUT: array4_a CE.
17	RWX	WOX_AND	WOX_OR	CE2_4_OUT: array4_b CE.
18	RWX	WOX_AND	WOX_OR	UE1_4_OUT: array4_a UE.
19	RWX	WOX_AND	WOX_OR	UE2_4_OUT: array4_b UE.
20	RWX	WOX_AND	WOX_OR	CE1_5_OUT: array5_a CE.
21	RWX	WOX_AND	WOX_OR	CE2_5_OUT: array5_b CE.
22	RWX	WOX_AND	WOX_OR	UE1_5_OUT: array5_a UE.
23	RWX	WOX_AND	WOX_OR	UE2_5_OUT: array5_b UE.
24	RWX	WOX_AND	WOX_OR	CE1_6_OUT: array6_a CE.
25	RWX	WOX_AND	WOX_OR	CE2_6_OUT: array6_b CE.
26	RWX	WOX_AND	WOX_OR	UE1_6_OUT: array6_a UE.
27	RWX	WOX_AND	WOX_OR	UE2_6_OUT: array6_b UE.
28	RWX	WOX_AND	WOX_OR	CE1_7_OUT: array7_a CE.
29	RWX	WOX_AND	WOX_OR	CE2_7_OUT: array7_b CE.
30	RWX	WOX_AND	WOX_OR	UE1_7_OUT: array7_a UE.
31	RWX	WOX_AND	WOX_OR	UE2_7_OUT: array7_b UE.
32	RWX	WOX_AND	WOX_OR	DROP_COUNTER_FULL: Drop Counter Full.
33	RWX	WOX_AND	WOX_OR	INTERNAL_ERROR: Internal Error.
34	RWX	WOX_AND	WOX_OR	SCOM_ERROR: Internal Error.
35	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERROR: Internal Error.

Register Name	HCA EN FIR Mask Register
Mnemonic	BRIDGE.HCA.EHHCA_FIR_MASK_REG
Address	0000000005012983 (SCOM) 0000000005012984 (SCOM1) 0000000005012985 (SCOM2)
Description	HCA EN FIR MASK Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	CE1_0_OUT_MASK: array0_a CE.
1	RW	WO_AND	WO_OR	CE2_0_OUT_MASK: array0_b CE.
2	RW	WO_AND	WO_OR	UE1_0_OUT_MASK: array0_a UE.
3	RW	WO_AND	WO_OR	UE2_0_OUT_MASK: array0_b UE.
4	RW	WO_AND	WO_OR	CE1_1_OUT_MASK: array1_a CE.
5	RW	WO_AND	WO_OR	CE2_1_OUT_MASK: array1_b CE.
6	RW	WO_AND	WO_OR	UE1_1_OUT_MASK: array1_a UE.
7	RW	WO_AND	WO_OR	UE2_1_OUT_MASK: array1_b UE.
8	RW	WO_AND	WO_OR	CE1_2_OUT_MASK: array2_a CE.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RW	WO_AND	WO_OR	CE2_2_OUT_MASK: array2_b CE.
10	RW	WO_AND	WO_OR	UE1_2_OUT_MASK: array2_a UE.
11	RW	WO_AND	WO_OR	UE2_2_OUT_MASK: array2_b UE.
12	RW	WO_AND	WO_OR	CE1_3_OUT_MASK: array3_a CE.
13	RW	WO_AND	WO_OR	CE2_3_OUT_MASK: array3_b CE.
14	RW	WO_AND	WO_OR	UE1_3_OUT_MASK: array3_a UE.
15	RW	WO_AND	WO_OR	UE2_3_OUT_MASK: array3_b UE.
16	RW	WO_AND	WO_OR	CE1_4_OUT_MASK: array4_a CE.
17	RW	WO_AND	WO_OR	CE2_4_OUT_MASK: array4_b CE.
18	RW	WO_AND	WO_OR	UE1_4_OUT_MASK: array4_a UE.
19	RW	WO_AND	WO_OR	UE2_4_OUT_MASK: array4_b UE.
20	RW	WO_AND	WO_OR	CE1_5_OUT_MASK: array5_a CE.
21	RW	WO_AND	WO_OR	CE2_5_OUT_MASK: array5_b CE.
22	RW	WO_AND	WO_OR	UE1_5_OUT_MASK: array5_a UE.
23	RW	WO_AND	WO_OR	UE2_5_OUT_MASK: array5_b UE.
24	RW	WO_AND	WO_OR	CE1_6_OUT_MASK: array6_a CE.
25	RW	WO_AND	WO_OR	CE2_6_OUT_MASK: array6_b CE.
26	RW	WO_AND	WO_OR	UE1_6_OUT_MASK: array6_a UE.
27	RW	WO_AND	WO_OR	UE2_6_OUT_MASK: array6_b UE.
28	RW	WO_AND	WO_OR	CE1_7_OUT_MASK: array7_a CE.
29	RW	WO_AND	WO_OR	CE2_7_OUT_MASK: array7_b CE.
30	RW	WO_AND	WO_OR	UE1_7_OUT_MASK: array7_a UE.
31	RW	WO_AND	WO_OR	UE2_7_OUT_MASK: array7_b UE.
32	RW	WO_AND	WO_OR	DROP_COUNTER_FULL_MASK: Drop Counter Full.
33	RW	WO_AND	WO_OR	INTERNAL_ERROR_MASK: Internal Error.
34	RW	WO_AND	WO_OR	SCOM_ERROR_MASK: Internal Error.
35	RW	WO_AND	WO_OR	FIR_PARITY_ERROR_MASK: Internal Error.

Register Name	**HCA EN FIR Action0 Register**
Mnemonic	BRIDGE.HCA.EHHCA_FIR_ACTION0_REG
Address	0000000005012986 (SCOM)
Description	HCA EN FIR ACTION0 Register

Bits	SCOM	Field Mnemonic: Description
0	RO	CE1_0_OUT_ACTION0: array0_a CE.
1	RO	CE2_0_OUT_ACTION0: array0_b CE.
2	RO	UE1_0_OUT_ACTION0: array0_a UE.
3	RO	UE2_0_OUT_ACTION0: array0_b UE.
4	RO	CE1_1_OUT_ACTION0: array1_a CE.

Bits	SCOM	Field Mnemonic: Description
5	RO	CE2_1_OUT_ACTION0: array1_b CE.
6	RO	UE1_1_OUT_ACTION0: array1_a UE.
7	RO	UE2_1_OUT_ACTION0: array1_b UE.
8	RO	CE1_2_OUT_ACTION0: array2_a CE.
9	RO	CE2_2_OUT_ACTION0: array2_b CE.
10	RO	UE1_2_OUT_ACTION0: array2_a UE.
11	RO	UE2_2_OUT_ACTION0: array2_b UE.
12	RO	CE1_3_OUT_ACTION0: array3_a CE.
13	RO	CE2_3_OUT_ACTION0: array3_b CE.
14	RO	UE1_3_OUT_ACTION0: array3_a UE.
15	RO	UE2_3_OUT_ACTION0: array3_b UE.
16	RO	CE1_4_OUT_ACTION0: array4_a CE.
17	RO	CE2_4_OUT_ACTION0: array4_b CE.
18	RO	UE1_4_OUT_ACTION0: array4_a UE.
19	RO	UE2_4_OUT_ACTION0: array4_b UE.
20	RO	CE1_5_OUT_ACTION0: array5_a CE.
21	RO	CE2_5_OUT_ACTION0: array5_b CE.
22	RO	UE1_5_OUT_ACTION0: array5_a UE.
23	RO	UE2_5_OUT_ACTION0: array5_b UE.
24	RO	CE1_6_OUT_ACTION0: array6_a CE.
25	RO	CE2_6_OUT_ACTION0: array6_b CE.
26	RO	UE1_6_OUT_ACTION0: array6_a UE.
27	RO	UE2_6_OUT_ACTION0: array6_b UE.
28	RO	CE1_7_OUT_ACTION0: array7_a CE.
29	RO	CE2_7_OUT_ACTION0: array7_b CE.
30	RO	UE1_7_OUT_ACTION0: array7_a UE.
31	RO	UE2_7_OUT_ACTION0: array7_b UE.
32	RO	DROP_COUNTER_FULL_ACTION0: Drop Counter Full.
33	RO	INTERNAL_ERROR_ACTION0: Internal Error.
34	RO	SCOM_ERROR_ACTION0: Internal Error.
35	RO	FIR_PARITY_ERROR_ACTION0: Internal Error.

Register Name	HCA EN FIR Action1 Register
Mnemonic	BRIDGE.HCA.EHHCA_FIR_ACTION1_REG
Address	0000000005012987 (SCOM)
Description	HCA EN FIR ACTION1 Register

Bits	SCOM	Field Mnemonic: Description
0	RO	CE1_0_OUT_ACTION1: array0_a CE.

Bits	SCOM	Field Mnemonic: Description
1	RO	CE2_0_OUT_ACTION1: array0_b CE.
2	RO	UE1_0_OUT_ACTION1: array0_a UE.
3	RO	UE2_0_OUT_ACTION1: array0_b UE.
4	RO	CE1_1_OUT_ACTION1: array1_a CE.
5	RO	CE2_1_OUT_ACTION1: array1_b CE.
6	RO	UE1_1_OUT_ACTION1: array1_a UE.
7	RO	UE2_1_OUT_ACTION1: array1_b UE.
8	RO	CE1_2_OUT_ACTION1: array2_a CE.
9	RO	CE2_2_OUT_ACTION1: array2_b CE.
10	RO	UE1_2_OUT_ACTION1: array2_a UE.
11	RO	UE2_2_OUT_ACTION1: array2_b UE.
12	RO	CE1_3_OUT_ACTION1: array3_a CE.
13	RO	CE2_3_OUT_ACTION1: array3_b CE.
14	RO	UE1_3_OUT_ACTION1: array3_a UE.
15	RO	UE2_3_OUT_ACTION1: array3_b UE.
16	RO	CE1_4_OUT_ACTION1: array4_a CE.
17	RO	CE2_4_OUT_ACTION1: array4_b CE.
18	RO	UE1_4_OUT_ACTION1: array4_a UE.
19	RO	UE2_4_OUT_ACTION1: array4_b UE.
20	RO	CE1_5_OUT_ACTION1: array5_a CE.
21	RO	CE2_5_OUT_ACTION1: array5_b CE.
22	RO	UE1_5_OUT_ACTION1: array5_a UE.
23	RO	UE2_5_OUT_ACTION1: array5_b UE.
24	RO	CE1_6_OUT_ACTION1: array6_a CE.
25	RO	CE2_6_OUT_ACTION1: array6_b CE.
26	RO	UE1_6_OUT_ACTION1: array6_a UE.
27	RO	UE2_6_OUT_ACTION1: array6_b UE.
28	RO	CE1_7_OUT_ACTION1: array7_a CE.
29	RO	CE2_7_OUT_ACTION1: array7_b CE.
30	RO	UE1_7_OUT_ACTION1: array7_a UE.
31	RO	UE2_7_OUT_ACTION1: array7_b UE.
32	RO	DROP_COUNTER_FULL_ACTION1: Drop Counter Full.
33	RO	INTERNAL_ERROR_ACTION1: Internal Error.
34	RO	SCOM_ERROR_ACTION1: Internal Error.
35	RO	FIR_PARITY_ERROR_ACTION1: Internal Error.

Register Name	Write to HCA BAR and Range Register
Mnemonic	BRIDGE.HCA.HCA_BAR
Address	000000000501298A (SCOM)
Description	Write to HCA BAR and Range Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:31	RW	HCA_BAR_ADDR: HCA Base Address. These bits and the hca_bar_range bits define how the address is mapped to the Power Bus. Bits(8:22) - Used as is on the processor bus. Bits(23:31) - Maskable w/ hca_bar_range.
32:42	RW	HCA_BAR_RANGE: Memory size. These bits indicate memory size behind the MC. It is used to define the Bar address.
43:61	RO	Constant = 0b0000000000000000000
62	RW	PAGE_SIZE_64K: Page size 64K enable.
63	RW	HCA_BAR_VALID: Bar valid. Indicates that the BAR is valid.

Register Name	Read HCA Count BAR Register
Mnemonic	BRIDGE.HCA.HCA_COUNT_BAR
Address	000000000501298B (SCOM)
Description	Read HCA COUNT BAR Register

Bits	SCOM	Field Mnemonic: Description
0:20	RO	Constant = 0b00000000000000000000
21:44	RW	HCA_COUNT_BAR_ADDR: HCA Counter Base Address. These bits and the hca_count_bar_range bits define how the address is mapped to the Power Bus. Bits(21:31) - Maskable with hca_bar_range. Bits(31:40) - Maskable with hca_bar_range - 4 K page mode. Bits(32:33) - Used as is on the processor bus - 64 K page mode. Bits(34:44) - Maskable with hca_bar_range - 64 K page mode.
45:62	RO	Constant = 0b000000000000000000
63	RW	HCA_COUNT_BAR_VALID: Count Bar valid. Indicates that the COUNT BAR is valid.

Register Name	Read HCA REF BAR Register
Mnemonic	BRIDGE.HCA.HCA_REF_BAR
Address	000000000501298E (SCOM)
Description	Read HCA REF BAR Register

Bits	SCOM	Field Mnemonic: Description
0:20	RO	Constant = 0b00000000000000000000

Bits	SCOM	Field Mnemonic: Description
21:45	RW	HCA_REF_BAR_ADDR: HCA ref Base Address. These bits and the hca_bar_range bits define how the address is mapped to the Power Bus. Bits(21:31) - Maskable with hca_bar_range. Bits(31:41) - Maskable with hca_bar_range - 4K page mode. Bits(32:34) - Used as is on the processor bus - 64K page mode. Bits(35:45) - Maskable with hca_bar_range - 64K page mode.
46:62	RO	Constant = 0b00000000000000000
63	RW	HCA_REF_BAR_VALID: ref Bar valid. Indicates that the ref BAR is valid.

Register Name	**HCA Mode Register**
Mnemonic	BRIDGE.HCA.HCA_MODES
Address	000000000501298F (SCOM)
Description	HCA MODE Register

Bits	SCOM	Field Mnemonic: Description
0:4	RO	Constant = 0b00000
5:12	RW	HCA_FULLMASK: HCA Counter Full Mask. These bits specify how many bit the counter will be used. The counter is 12 bits, so each bit will disable each corresponding upper bits.
13:16	RW	HCA_ERROR_INJECT: HCA Error Inject to Counter Cache. Bits(0:1) - Inversion mask for Tag portion of array. Bits(2:3) - Inversion mask for counter portion of array.
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	**HCA Flush Register**
Mnemonic	BRIDGE.HCA.HCA_FLUSH
Address	0000000005012990 (SCOM)
Description	HCA FLUSH Register

Bits	SCOM	Field Mnemonic: Description
0:8	RWX	HCA_FLUSH_INDEX: HCA Index of Counter Cache to flush. Bits(0:8) - Specify the address into the Counter cache to flush.
9:16	RWX	HCA_FLUSH_CONG: HCA Congruent set to flush. Bits(0:7) - By setting any bits and in conjuntion with hca_flush_index. the HCA Castout the counter address by hca_flush_index and. the set specified by hca_flush_cong. These bits will stay. on until the operation is completed.
17:25	RWX	HCA_FLUSH_COUNT: HCA flush repeat count.
26:63	RO	Constant = 0b00000000000000000000000000000000000000

Register Name	HCA Drop Register
Mnemonic	BRIDGE.HCA.HCA_DROP
Address	0000000005012991 (SCOM)
Description	HCA DROP Register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	HCA_PIPE_DROP_COUNTER: HCA Count RCMD dropped due to lack of pipeline resources to access the array.
16:31	ROX	HCA_WRITE_DROP_COUNTER: HCA Count RCMD dropped due to lack of write resources into the array.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	HCA Reset Register
Mnemonic	BRIDGE.HCA.HCA_RESET
Address	0000000005012992 (SCOM)
Description	HCA RESET Register

Bits	SCOM	Field Mnemonic: Description
0:63	RO	not implemented.

Register Name	HCA Mirror BAR and Range Register
Mnemonic	BRIDGE.HCA.HCA_MIRROR_BAR
Address	0000000005012993 (SCOM)
Description	HCA Mirror BAR and Range Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:32	RW	HCA_MIRROR_BAR_ADDR: HCA mirror_Base Address. These bits and the hca_mirror_bar_range bits define how the address is mapped to the Power Bus. Bits(8:24) - Used as is on the processor bus. Bits(25:32) - Maskable with hca_mirror_bar_range.
33:62	RO	Constant = 0b00000000000000000000000000000000
63	RW	HCA_MIRROR_BAR_VALID: Bar valid. Indicates that the BAR is valid.

Register Name	LPC Synchronize FIR Register
Mnemonic	BRIDGE.LPC.SYNC_FIR_REG
Address	00000000050129C0 (SCOM) 00000000050129C1 (SCOM1) 00000000050129C2 (SCOM2)
Description	PBAM low sped part FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	INVALID_TRANSFER_SIZE: OPB Master LS received a transfer size value unequal to 1- or 2- or 4-Byte.
1	RWX	WOX_AND	WOX_OR	INVALID_COMMAND: OPB Master LS received a invalid command no_ci store and no_ci_load.
2	RWX	WOX_AND	WOX_OR	INVALID_ADDRESS_ALIGNMENT: OPB Master LS received a address which was not aligned to the received transfer size.
3	RWX	WOX_AND	WOX_OR	OPB_ERROR: OPB Master LS detected OPB ErrAck which was activated by the accessed OPB slave.
4	RWX	WOX_AND	WOX_OR	OPB_TIMEOUT: The OPB Arbiter activated the OPB Timeout signal Typical reason is that the OPB access did not hit any available OPB slave.
5	RWX	WOX_AND	WOX_OR	OPB_MASTER_HANG_TIMEOUT: The OPB Master LS was not able to end the requested OPB access within the OPB Master LS hang timeout time.
6	RWX	WOX_AND	WOX_OR	CMD_BUFFER_PAR_ERR: A parity error was detected in the OPB Master LS command buffer.
7	RWX	WOX_AND	WOX_OR	DAT_BUFFER_PAR_ERR: A parity error was detected in the OPB Master LS data buffer.
8	RWX	WOX_AND	WOX_OR	RETURNQ_ERR: Reserved bit 1 tied to zero.
9	RWX	WOX_AND	WOX_OR	Reserved: Reserved bit 0 tied to zero.
10	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERR2: Local FIR Parity Error RAS duplicate.
11	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERR: Local FIR Parity Error of ACTION/MASK registers.
12:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	**LPC Synchronize FIR Mask Register**
Mnemonic	BRIDGE.LPC.SYNC_FIR_MASK_REG
Address	00000000050129C3 (SCOM) 00000000050129C4 (SCOM1) 00000000050129C5 (SCOM2)
Description	PBAM_low_speed_part_FIR_Mask_Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	INVALID_TRANSFER_SIZE_MASK: mask for invalid transfer size.
1	RW	WO_AND	WO_OR	INVALID_COMMAND_MASK: mask for invalid command.
2	RW	WO_AND	WO_OR	INVALID_ADDRESS_ALIGNMENT_MASK: mask for invalid address alignment.
3	RW	WO_AND	WO_OR	OPB_ERROR_MASK: mask for OPB error.
4	RW	WO_AND	WO_OR	OPB_TIMEOUT_MASK: mask for OPB timeout.
5	RW	WO_AND	WO_OR	OPB_MASTER_HANG_TIMEOUT_MASK: mask_for_OPB_master_hang_timeout.
6	RW	WO_AND	WO_OR	CMD_BUFFER_PAR_ERR_MASK: mask_for_OPB_master_cmd_buffer_parity_error.
7	RW	WO_AND	WO_OR	DAT_BUFFER_PAR_ERR_MASK: mask_for_OPB_master_dat_buffer_parity_error.
8	RW	WO_AND	WO_OR	RETURNQ_ERR_MASK: mask_for_Reserved_bit_1.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RW	WO_AND	WO_OR	Reserved_MASK: mask_for_Reserved_bit_0.
10	RW	WO_AND	WO_OR	SYNC_SCOM_PARITY_ERR2_MASK: mask_for_Local FIR Parity Error RAS duplicate.
11	RW	WO_AND	WO_OR	SYNC_SCOM_PARITY_ERR_MASK: Mask Local FIR Parity Error of ACTION/MASK registers.
12:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PBAM FIR Action0 Register
Mnemonic	BRIDGE.LPC.SYNC_FIR_ACTION0_REG
Address	00000000050129C6 (SCOM)
Description	GX Nest FIR Action0 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = No Error (0,1) = recoverable error (1,0) = Checkstop Error (1,1) = unused

Bits	SCOM	Field Mnemonic: Description
0	RO	INVALID_TRANSFER_SIZE_ACTION0: action0_for_invalid_transfer_size.
1	RO	INVALID_COMMAND_ACTION0: action0_for_invalid_command.
2	RO	INVALID_ADDRESS_ALIGNMENT_ACTION0: action0_for_invalid_address_alignment.
3	RO	OPB_ERROR_ACTION0: action0_for_OPB_error.
4	RO	OPB_TIMEOUT_ACTION0: action0_for_OPB_timeout.
5	RO	OPB_MASTER_HANG_TIMEOUT_ACTION0: action0_for_OPB_master_hang_timeout.
6	RO	CMD_BUFFER_PAR_ERR_ACTION0: action0_for_OPB_master_cmd_buffer_parity_error.
7	RO	DAT_BUFFER_PAR_ERR_ACTION0: action0_for_OPB_master_dat_buffer_parity_error.
8	RO	RETURNQ_ERR_ACTION0: Reserved_bit_1.
9	RO	Reserved_ACTION0: action0_for_Reserved0.
10	RO	SYNC_SCOM_PARITY_ERR2_ACTION0: action0_for_Local FIR Parity Error RAS duplicate.
11	RO	SYNC_SCOM_PARITY_ERR_ACTION0: action0_for_Mask Local FIR Parity Error of ACTION/MASK registers.
12:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PBAM FIR Action1 Register
Mnemonic	BRIDGE.LPC.SYNC_FIR_ACTION1_REG
Address	00000000050129C7 (SCOM)
Description	GX Nest FIR action1 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = No Error (0,1) = recoverable error (1,0) = Checkstop Error (1,1) = unused

Bits	SCOM	Field Mnemonic: Description
0	RO	INVALID_TRANSFER_SIZE_ACTION1: action1_for_invalid_transfer_size.
1	RO	INVALID_COMMAND_ACTION1: action1_for_invalid_command.
2	RO	INVALID_ADDRESS_ALIGNMENT_ACTION1: action1_for_invalid_address_alignment.
3	RO	OPB_ERROR_ACTION1: action1_for_OPB_error.
4	RO	OPB_TIMEOUT_ACTION1: action1_for_OPB_timeout.
5	RO	OPB_MASTER_HANG_TIMEOUT_ACTION1: action1_for_OPB_master_hang_timeout.
6	RO	CMD_BUFFER_PAR_ERR_ACTION1: action1_for_OPB_master_cmd_buffer_parity_error.
7	RO	DAT_BUFFER_PAR_ERR_ACTION1: action1_for_OPB_master_dat_buffer_parity_error.
8	RO	RETURNQ_ERR_ACTION1: Reserved_bit_1.
9	RO	Reserved_ACTION1: action1_for_Reserved_bit_0.
10	RO	SYNC_SCOM_PARITY_ERR2_ACTION1: action1_for_Local FIR Parity Error RAS duplicate.
11	RO	SYNC_SCOM_PARITY_ERR_ACTION1: action1_for_Mask Local FIR Parity Error of ACTION/MASK registers.
12:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PBA Bar 0 Register
Mnemonic	BRIDGE.PBA.SCOMTRUST.PBABAR0
Address	0000000005012B00 (SCOM)
Description	This register is used with the PBABARMSK[n] to define the processor bus address range accessible by the request. It must be initialized by hypervisor before enabling and sending OCI transactions that target the PBA and before starting the Block Copy Engine. Even Data Parity is calculated and saved when this register is written. The 'PBA_FIR[Internal Err] indication is set when a parity error is detected.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	PBABAR0_CMD_SCOPE: Processor bus Command Scope These bits are initialized by hypervisor to indicate the command scope of the processor bus request. The PBA will always use the defined scope first. The request will be reissued with an increased scope if the original request gets a retry response that indicates a larger scope is required. Nodal Scope for dma and atomic write ttypes will be forced to a minimum of Group by PBA..
3	RW	PBABAR0_Reserved_3: Spare.
4:7	RO	Constant = 0b0000
8:43	RW	PBABAR0_ADDR: Processor bus_Base_Address These bits and the PBA Base Address Mask register define how the OCI address is mapped to the Power Bus by the PBA Slave and how the processor bus Address offset is mapped by the Block Copy Engine. 8:22 - PB Base Address bit not maskable. Used as-is on the Power Bus. 23:43 - PB Base Address bits maskable w PBABARMSKn.

Bits	SCOM	Field Mnemonic: Description
44:47	RO	Constant = 0b0000
48:63	RW	PBABAR0_VTARGET: Processor bus Vectored Group Target This may be initialized by software to specify the initial vectored group target when the cmd_scope is configured to Vectored Group Scope. If zero or not all 1's, PBA will update the Target value it uses when sending commands with scope = Vg based on the CRESP of the request when retrying the request. If set to FF, PBA will always drive the Target value to FF when sending commands with scope = Vg.

Register Name	PBA Bar 1 Register
Mnemonic	BRIDGE.PBA.SCOMTRUST.PBABAR1
Address	0000000005012B01 (SCOM)
Description	This register is used with the PBABARMSK[n] to define the processor bus address range accessible by the request. It must be initialized by hypervisor before enabling and sending OCI transactions that target the PBA and before starting the Block Copy Engine. Even Data Parity is calculated and saved when this register is written. The 'PBA_FIR[Internal Err] indication is set when a parity error is detected.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	PBABAR1_CMD_SCOPE: Processor bus Command Scope These bits are initialized by hypervisor to indicate the command scope of the processor bus request. The PBA will always use the defined scope first. The request will be reissued with an increased scope if the original request gets a retry response that indicates a larger scope is required. Nodal Scope for dma and atomic write ttypes will be forced to a minimum of Group by PBA..
3	RW	PBABAR1_Reserved_3: Spare.
4:7	RO	Constant = 0b0000
8:43	RW	PBABAR1_ADDR: Processor bus_Base_Address These bits and the PBA Base Address Mask register define how the OCI address is mapped to the Power Bus by the PBA Slave and how the processor bus Address offset is mapped by the Block Copy Engine. 8:22 - PB Base Address bit not maskable. Used as-is on the Power Bus. 23:43 - PB Base Address bits maskable w PBABARMSKn.
44:47	RO	Constant = 0b0000
48:63	RW	PBABAR1_VTARGET: Processor bus Vectored Group Target This may be initialized by software to specify the initial vectored group target when the cmd_scope is configured to Vectored Group Scope. If zero or not all 1's, PBA will update the Target value it uses when sending commands with scope = Vg based on the CRESP of the request when retrying the request. If set to FF, PBA will always drive the Target value to FF when sending commands with scope = Vg.

Register Name	PBA Bar 2 Register
Mnemonic	BRIDGE.PBA.SCOMTRUST.PBABAR2
Address	0000000005012B02 (SCOM)
Description	This register is used with the PBABARMSK[n] to define the processor bus address range accessible by the request. It must be initialized by hypervisor before enabling and sending OCI transactions that target the PBA and before starting the Block Copy Engine. Even Data Parity is calculated and saved when this register is written. The 'PBA_FIR[Internal Err] indication is set when a parity error is detected.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	PBABAR2_CMD_SCOPE: Processor bus Command Scope These bits are initialized by hypervisor to indicate the command scope of the processor bus request. The PBA will always use the defined scope first. The request will be reissued with an increased scope if the original request gets a retry response that indicates a larger scope is required. Nodal Scope for dma and atomic write ttypes will be forced to a minimum of Group by PBA..

Bits	SCOM	Field Mnemonic: Description
3	RW	PBABAR2_Reserved_3: Spare.
4:7	RO	Constant = 0b0000
8:43	RW	PBABAR2_ADDR: Processor bus_Base_Address These bits and the PBA Base Address Mask register define how the OCI address is mapped to the Power Bus by the PBA Slave and how the processor bus Address offset is mapped by the Block Copy Engine. 8:22 - PB Base Address bit not maskable. Used as-is on the Power Bus. 23:43 - PB Base Address bits maskable w PBABARMSKn.
44:47	RO	Constant = 0b0000
48:63	RW	PBABAR2_VTARGET: Processor bus Vectored Group Target This may be initialized by software to specify the initial vectored group target when the cmd_scope is configured to Vectored Group Scope. If zero or not all 1's, PBA will update the Target value it uses when sending commands with scope = Vg based on the CRESP of the request when retrying the request. If set to FF, PBA will always drive the Target value to FF when sending commands with scope = Vg.

Register Name	**PBA BAR 3 Register**
Mnemonic	BRIDGE.PBA.SCOMTRUST.PBABAR3
Address	0000000005012B03 (SCOM)
Description	This register is used with the PBABARMSK[n] to define the processor bus address range accessible by the request. It must be initialized by hypervisor before enabling and sending OCI transactions that target the PBA and before starting the Block Copy Engine. Even Data Parity is calculated and saved when this register is written. The 'PBA_FIR[Internal Err] indication is set when a parity error is detected.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	PBABAR3_CMD_SCOPE: Processor bus Command Scope These bits are initialized by hypervisor to indicate the command scope of the processor bus request. The PBA will always use the defined scope first. The request will be reissued with an increased scope if the original request gets a retry response that indicates a larger scope is required. Nodal Scope for dma and atomic write ttypes will be forced to a minimum of Group by PBA..
3	RW	PBABAR3_Reserved_3: Spare.
4:7	RO	Constant = 0b0000
8:43	RW	PBABAR3_ADDR: Processor bus_Base_Address These bits and the PBA Base Address Mask register define how the OCI address is mapped to the Power Bus by the PBA Slave and how the processor bus Address offset is mapped by the Block Copy Engine. 8:22 - PB Base Address bit not maskable. Used as-is on the Power Bus. 23:43 - PB Base Address bits maskable w PBABARMSKn.
44:47	RO	Constant = 0b0000
48:63	RW	PBABAR3_VTARGET: Processor bus Vectored Group Target This may be initialized by software to specify the initial vectored group target when the cmd_scope is configured to Vectored Group Scope. If zero or not all 1's, PBA will update the Target value it uses when sending commands with scope = Vg based on the CRESP of the request when retrying the request. If set to FF, PBA will always drive the Target value to FF when sending commands with scope = Vg.

Register Name	**PBA BAR Mask 0 Register**
Mnemonic	BRIDGE.PBA.SCOMTRUST.PBABARMSK0
Address	0000000005012B04 (SCOM)
Description	This register is used with the PBABARn to define the processor bus address range accessible by the request. It must be initialized by hypervisor before enabling and sending OCI transactions that target the PBA and before starting the Block Copy Engine. PBABARMSK3[mask] intializes to x000007 to define an 8Mbyte range at IPL time.

Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b00000000000000000000000
23:43	RW	PBABARMSK0_MSK: Processor bus_Base_Address_Mask When set to a '1', the OCI Address (5:11) and PBASLVCTL[ExtAddr(23:36)] is used instead of the PB Base Address in that bit position. See the diagram of the OCI Address Mapping to processor bus. Default to allow access to 1st 8M of memory.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA BAR Mask 1 Register
Mnemonic	BRIDGE.PBA.SCOMTRUST.PBABARMSK1
Address	0000000005012B05 (SCOM)
Description	This register is used with the PBABARn to define the processor bus address range accessible by the request. It must be initialized by hypervisor before enabling and sending OCI transactions that target the PBA and before starting the Block Copy Engine. PBABARMSK3[mask] intializes to x000007 to define an 8Mbyte range at IPL time.

Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b00000000000000000000000
23:43	RW	PBABARMSK1_MSK: Processor bus_Base_Address_Mask When set to a '1', the OCI Address (5:11) and PBASLVCTL[ExtAddr(23:36)] is used instead of the PB Base Address in that bit position. See the diagram of the OCI Address Mapping to processor bus. Default to allow access to 1st 8M of memory.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA BAR Mask 2 Register
Mnemonic	BRIDGE.PBA.SCOMTRUST.PBABARMSK2
Address	0000000005012B06 (SCOM)
Description	This register is used with the PBABARn to define the processor bus address range accessible by the request. It must be initialized by hypervisor before enabling and sending OCI transactions that target the PBA and before starting the Block Copy Engine. PBABARMSK3[mask] intializes to x000007 to define an 8Mbyte range at IPL time.

Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b00000000000000000000000
23:43	RW	PBABARMSK2_MSK: Processor bus_Base_Address_Mask When set to a '1', the OCI Address (5:11) and PBASLVCTL[ExtAddr(23:36)] is used instead of the PB Base Address in that bit position. See the diagram of the OCI Address Mapping to processor bus. Default to allow access to 1st 8M of memory.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA BAR Mask 3 Register
Mnemonic	BRIDGE.PBA.SCOMTRUST.PBABARMSK3
Address	0000000005012B07 (SCOM)
Description	This register is used with the PBABARn to define the processor bus address range accessible by the request. It must be initialized by hypervisor before enabling and sending OCI transactions that target the PBA and before starting the Block Copy Engine. PBABARMSK3[mask] intializes to x000007 to define an 8Mbyte range at IPL time.

Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b0000000000000000000000
23:43	RW	PBABARMSK3_MSK: Processor bus_Base_Address_Mask When set to a '1', the OCI Address (5:11) and PBASLVCTL[ExtAddr(23:36)] is used instead of the PB Base Address in that bit position. See the diagram of the OCI Address Mapping to processor bus. Default to allow access to 1st 8M of memory.
44:63	RO	Constant = 0b00000000000000000000

Register Name	No Trust BAR 0 Register
Mnemonic	BRIDGE.PSIHB.NOTRUST_BAR0
Address	0000000005012B40 (SCOM)
Description	notrust Bar0

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b000000000000000
14:43	RWX	UNTRUSTED_BAR0: Untrusted_Bar0 - defaults to all 1s.

Register Name	No Trust BAR 1 Register
Mnemonic	BRIDGE.PSIHB.NOTRUST_BAR1
Address	0000000005012B41 (SCOM)
Description	notrust bar1

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b000000000000000
14:43	RWX	UNTRUSTED_BAR1: Untrusted_bar1 - defaults to all 1s.

Register Name	No Trust BAR 0 Mask Register
Mnemonic	BRIDGE.PSIHB.NOTRUST_BAR0MASK
Address	0000000005012B42 (SCOM)
Description	notrust bar0mask

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b000000000000000
14:43	RWX	UNTRUSTED_BAR0MASK: Untrusted_bar0mask - defaults to all 0s.

Register Name	No Trust BAR 1 Mask Register
Mnemonic	BRIDGE.PSIHB.NOTRUST_BAR1MASK
Address	0000000005012B43 (SCOM)
Description	notrust bar1mask

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b000000000000000

Bits	SCOM	Field Mnemonic: Description
14:43	RWX	UNTRUSTED_BAR1MASK: Untrusted_bar1mask - defaults to all 0s.

Register Name	PSI TCE Address Register
Mnemonic	BRIDGE.PSIHB.PSI_TCE_ADDR_REG
Address	0000000005012B44 (SCOM)
Description	TCE Address Register

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b00000000000000
14:47	RWX	TCE_ADDR: The TCE Address Register contains the address used to look up higher order bits of DMA addresses when translation is enabled. Bits 18 to 47 of the TCE address are specified with this IDial. For address bits 14 to 15, need to set PSIHB ADDR Upper bits.
48:60	RO	Constant = 0b0000000000000
61:63	RWX	TCE_ENTRIES: The TCE Address Register contains a 3-bits to indicate how many TCE entries there are. No bits set to 1 means there are 8K entries, while a 1 in bit pos 1 means there are 512K entries. If bit pos 2 is set and bit pos 1 is not set, then there are 256k entries. If only bit pos 0 is set, then there are 16k entries. Bits 61-63 of TARTCE Register are specified with this IDial in the following order: TARTCE(61) = tce_entries(1); TARTCE(62) = tce_entries(2); TARTCE(63) = tce_entries(0).

Register Name	Secure Boot Control Register
Mnemonic	BRIDGE.PSIHB.TRUST_CONTROL
Address	0000000005012B45 (SCOM)
Description	Secure Boot Control

Bits	SCOM	Field Mnemonic: Description
0:1	RO	Constant = 0b00
2	RWX	FSP_TCE_ENABLE: This bit controls the use of TCE s to translate incoming FSP addresses to system memory addresses. When set to 1 , DMA operations within the low 32 bit FSP address space use the TCE mechanism to access the 48 bit system address space. This bit is similar to the Winnipeg PHB Configuration Register, bit 2.
3	ROX	Reserved.

Register Name	PBI CQ FIR Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_REG
Address	0000000005012C00 (SCOM) 0000000005012C01 (SCOM1) 0000000005012C02 (SCOM2)
Description	PBI CQ FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PBI_PE_FIR: PBI internal parity error.
1	RWX	WOX_AND	WOX_OR	PBUS_CMD_HANG_FIR: Processor bus command hang error.
2	RWX	WOX_AND	WOX_OR	PBUS_READ_ARE_FIR: Processor bus read address error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	PBUS_WRITE_ARE_FIR: Processor bus write address error.
4	RWX	WOX_AND	WOX_OR	PBUS_MISC_HW_FIR: Processor bus miscellaneous error.
5	RWX	WOX_AND	WOX_OR	RSVD_FIR: Reserved.
6	RWX	WOX_AND	WOX_OR	PBUS_XLAT_ECC_UE_FIR: Processor bus Xlate UE error.
7	RWX	WOX_AND	WOX_OR	PBUS_XLAT_ECC_SUE_FIR: Processor bus Xlate SUE error.
8	RWX	WOX_AND	WOX_OR	PBUS_ECC_CE_FIR: Processor bus CE error.
9	RWX	WOX_AND	WOX_OR	PBUS_ECC_UE_FIR: Processor bus UE error.
10	RWX	WOX_AND	WOX_OR	PBUS_ECC_SUE_FIR: Processor bus SUE error.
11	RWX	WOX_AND	WOX_OR	INBD_LCO_ARRAY_ECC_CE_FIR: Inbound LCO_ARRAY CE error.
12	RWX	WOX_AND	WOX_OR	INBD_LCO_ARRAY_ECC_UE_FIR: Inbound LCO_ARRAY UE error.
13	RWX	WOX_AND	WOX_OR	INBD_LCO_ARRAY_ECC_SUE_FIR: Inbound LCO_ARRAY SUE error.
14	RWX	WOX_AND	WOX_OR	INBD_ARRAY_ECC_CE_FIR: Inbound array CE error.
15	RWX	WOX_AND	WOX_OR	INBD_ARRAY_ECC_UE_FIR: Inbound array UE error.
16	RWX	WOX_AND	WOX_OR	INT_STATE_ERR_FIR: internal state error.
17	RWX	WOX_AND	WOX_OR	PBUS_LOAD_LINK_ERR_FIR: ACK_DEAD CRESP received by read command.
18	RWX	WOX_AND	WOX_OR	PBUS_STORE_LINK_ERR_FIR: ACK_DEAD CRESP received by write command.
19	RWX	WOX_AND	WOX_OR	PBUS_LINK_ABORT_FIR: Link check aborted while waiting on data.
20	RWX	WOX_AND	WOX_OR	FIR_SCOM_PE_FIR: FIR/SCOM satellite parity error.
21	RWX	WOX_AND	WOX_OR	FIR_SCOM_PE_DUP_FIR: FIR/SCOM satellite parity error duplicate.
22:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	PBI CQ FIR Mask Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_MASK_REG
Address	0000000005012C03 (SCOM) 0000000005012C04 (SCOM1) 0000000005012C05 (SCOM2)
Description	PBI CQ FIR Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:21	RW	WO_AND	WO_OR	NX_CQ_FIR_MASK:
22:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	PBI CQ FIR Action 0 Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_ACTION0_REG
Address	0000000005012C06 (SCOM)
Description	PBI CQ FIR Action0 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable (1,0) = Unused (1,1) = Local checkstop

Bits	SCOM	Field Mnemonic: Description
0:21	RW	NX_CQ_FIR_ACTION0:
22:63	RO	Constant = 0b0000000000000000000000000000000000000000000000

Register Name	PBI CQ FIR Action 1 Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_ACTION1_REG
Address	0000000005012C07 (SCOM)
Description	PBI CQ FIR Action1 Register Action select for corresponding bit in FIR (Action1,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable (1,0) = Unused (1,1) = Local checkstop

Bits	SCOM	Field Mnemonic: Description
0:20	RW	NX_CQ_FIR_ACTION1:
21	RW	Reserved.
22:63	RO	Constant = 0b0000000000000000000000000000000000000000000000

Register Name	PBI CQ FIR WOF Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_WOF_REG
Address	0000000005012C08 (SCOM)
Description	PBI CQ FIR WOF Register

Bits	SCOM	Field Mnemonic: Description
0:21	RWX_WCLRREG	Reserved.
22:63	RO	Constant = 0b0000000000000000000000000000000000000000000000

Register Name	NX Power Bus Debug Control 1 Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PB_DEBUG_REG
Address	0000000005012C10 (SCOM)
Description	Processor bus Debug Control Register 1

Bits	SCOM	Field Mnemonic: Description
0:7	RW	NXCQ_TRACE_CNTL: 0 - 0 = trace cq shim i/f; 1 = trace queues 1:2 - Reserved 3 - trace a fixed queue number when tracing queues 4:7 - queue number when tracing a fixed queue.
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	NX Power Bus Error Injection Configuration Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PB_ECC_REG
Address	0000000005012C11 (SCOM)
Description	NX processor bus Error Injection Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	NXCQ_ECC_INJECT_MODE: ecc_inject_mode determines the number of times to inject the ecc error.
2:3	RW	NXCQ_ECC_INJECT_TYPE: ecc_inject_type determines the type of ecc error injected.
4	RW	NXCQ_PBCQ_INJECT_ENABLE: Enable ecc inject on pbcq arrays.
5:8	RW	NXCQ_PBCQ_ARRAY: which pbcq array to force the error into.
9:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Power Bus Mode Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.MMCQ_PB_MODE_REG
Address	0000000005012C15 (SCOM)
Description	Processor Bus MODE Register

Bits	SCOM	Field Mnemonic: Description
0	RW	DMA_WR_DISABLE_LN: For DMA write machine requests 0: Master can request Ln scope. 1: Master shall not request Ln scope.
1	RW	DMA_WR_DISABLE_GROUP: For DMA write machine requests 0: Master can request G scope. 1: Master shall not request G scope.
2	RW	DMA_WR_DISABLE_VG_NOT_SYS: For DMA write machine requests 0: Master can request Vg scope. 1: Master shall not request Vg scope but may use Vg(sys).
3	RW	DMA_WR_DISABLE_NN_RN: For DMA write machine requests 0: Master can request Nn or Rn scope. 1: Master shall not request Nn or Rn scope.
4	RW	DMA_RD_DISABLE_LN: For DMA read machine requests 0: Master may request Ln scope. 1: Master shall not request Ln scope.
5	RW	DMA_RD_DISABLE_GROUP: For DMA read machine requests 0: Master may request G scope. 1: Master shall not request G scope.
6	RW	DMA_RD_DISABLE_VG_NOT_SYS: For DMA read machine requests: 0: Master may request Vg scope. 1: Master shall not request Vg scope but may use Vg(sys).

Bits	SCOM	Field Mnemonic: Description
7	RW	DMA_RD_DISABLE_NN_RN: For DMA read machine requests 0: Master may request Nn or Rn scope. 1: Master shall not request Nn or Rn scope.
8:10	RW	LCO_CRED_MASK: 111: Increment LCO credit count for 1 out of every 8 read commands sent. 011: Increment LCO credit count for 1 out of every 4 read commands sent. 001: Increment LCO credit count for 1 out of every 2 read commands sent. 000: Increment LCO credit count for 1 out of every 1 read commands sent.
11:14	RW	LCO_TARG_MIN: Minimum number of eligible LCO targets.
15:26	RW	LCO_TARG_CONFIG: Bit vector where there is one bit per valid LCO target.
27:30	RW	UNUSED: Unused.
31:32	RW	NX_FREEZE_MODES: Data arbitration priority percentage 00: Behaviour unchanged. 01: Pass data/ECC as is. 10: Freeze data pattern with good ECC. 11: Illegal.
33	RW	ADDR_BAR_MODE: Specifies the address mapping mode in use for the system. 0: Small system address map. Reduces the number of group ID bits to 2 and eliminates the chip ID bits. All chips have an ID of 0. Nn scope is not available in this mode. 1: Large system address map. Uses a 4 bits for the group ID and 3 bits for the chip id.
34	RW	SKIP_G: Scope mode control set by firmware when the topology is chip = group. Note that this CS does not disable the use of group scope. It modifies the progression of scope when the command starts at nodal scope. 0: The progression from nodal to group scope is followed when the combined response indicates rty_inc or sfStat (as applicable to the command) is set. 1: When the scope of the command is nodal and the command is in the Read, RWITM, or is an Atomic RMW and Fetch command (found in the Ack_BK group), and the combined response is rty_inc or the sfStat is set in the data, the command scope progression skips group and goes to Vg scope.
35:36	RW	Reserved.
37	RW	NXCQ_HANG_SM_ON_ARE: This is the control to enable or disable hanging the master FSM on a combined response of addr_error. When asserted (set to 1), a master getting an addr_error combined response will hang; this is used as a debug aid and should be disabled (set to 0) when shipped to the customer.
38	RW	NXCQ_HANG_SM_ON_LINK_FAIL: this is the control to enable or disable hanging the master FSM on a combined response of ack_*dead. When asserted (set to 1), a master getting an ack_*dead combined response will hang; this is used as a debug aid and should be disabled (set to 0) when shipped to the customer.
39	RW	CFG_PUMP_MODE: NX uses this control only for unit random backoff 0 chip_is_node. Ln scope is constrained to the master's chip Group scope is constrained to all chips specified by the topology as part of the group (coherent logical X link connections). 1 chip_is_group. Both Ln and G scope are constrained to the master's chip. In this mode is recommended that skip_g be set for best performance.
40:47	RW	DMA_RD_VG_RESET_TIMER_MASK: Mask for timer to reset read Vg scope predictor FF 64K cycles FE 32K cycles FC 16K cycles F8 8K cycles 80 512 cycles.
48:55	RW	DMA_WR_VG_RESET_TIMER_MASK: Mask for timer to reset write Vg scope predictor FF 64K cycles FE 32K cycles FC 16K cycles F8 8K cycles 80 512 cycles.
56:63	RO	Constant = 0b00000000

Register Name	NX CQ Scale Value For Epsilon Counter Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.MM_EPSILON_COUNTER_VALUE
Address	0000000005012C1D (SCOM)
Description	NX CQ Scale value for epsilon counter

Bits	SCOM	Field Mnemonic: Description
0:11	RW	WR_EPSILON_TIER_1_CNT_VAL: Reload value for write epsilon tier 1 counter. Counter decrements at nest_clk / Write Epsilon Tier 1 Divider rate. Tier 1 corresponds to Group pump.
12:15	RW	WR_EPSILON_TIER_1_DIV_VAL: Reload value for write epsilon tier 1 divider. If this field = 0 nest_clk is divided by 16, otherwise it is divided by 1 - 15.
16:27	RW	WR_EPSILON_TIER_2_CNT_VAL: Reload value for write epsilon tier 2 counter. Counter decrements at nest_clk / Write Epsilon Tier 2 Divider rate. Tier 2 corresponds to System pump.
28:31	RW	WR_EPSILON_TIER_2_DIV_VAL: Reload value for write epsilon tier 2 divided. If this field = 0 nest_clk is divided by 16; otherwise it is divded by 1 - 15.
32	RW	EPSILON_DISABLE: Disable.
33:56	RO	Constant = 0b00000000000000000000000

Register Name	Power Bus Parity Error Report 0 Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PB_ERR_RPT_0
Address	0000000005012C22 (SCOM)
Description	Processor bus parity Error Report Register

Bits	SCOM	Field Mnemonic: Description
0:51	RO	Reserved.
52	ROX	NX_PBI_WRITE_IDLE: All PBI write engines are idle.
53:63	RO	Constant = 0b00000000000

Register Name	NX Debug Snapshot 0 Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NX_DEBUG_SNAPSHOT_0
Address	0000000005012C24 (SCOM)
Description	NX Snapshot of Debug Bus bits 0 to 63

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	NX_DEBUG_SNAPSHOT_B0_63: NX Snapshot of Debug Bus bits 0 to 63.

Register Name	NX Debug Snapshot 1 Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NX_DEBUG_SNAPSHOT_1
Address	0000000005012C25 (SCOM)
Description	NX Snapshot of Debug Bus bits 64 to 87

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	NX_DEBUG_SNAPSHOT_B64_87: NX Snapshot of Debug Bus bits 64 to 87.

Bits	SCOM	Field Mnemonic: Description
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	NX PMU Control Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PMU_CONTROL_REG
Address	0000000005012C26 (SCOM)
Description	NX PMU Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PMU_CNT0_ENABLE: When = 1 this bit enables NX PMU Counter0.
1	RW	NX_PMU_CNT1_ENABLE: When = 1 this bit enables NX PMU Counter1.
2	RW	NX_PMU_CNT2_ENABLE: When = 1 this bit enables NX PMU Counter2.
3	RW	NX_PMU_CNT3_ENABLE: When = 1 this bit enables NX PMU Counter3.
4:6	RW	NX_PMU_PRESCALER_SEL: Determines which, if any, prescaler counter to apply to all 16bit PMU counters.
7	RW	NX_PMU_CNT0_POSEDGE_SEL: If this bit is 1, the PMU will only count the event rising edge. If this bit is 0, the PMU will count every cycle the event is asserted (high).
8	RW	NX_PMU_CNT1_POSEDGE_SEL: If this bit is 1, the PMU will only count the event rising edge. If this bit is 0, the PMU will count every cycle the event is asserted (high).
9	RW	NX_PMU_CNT2_POSEDGE_SEL: If this bit is 1, the PMU will only count the event rising edge. If this bit is 0, the PMU will count every cycle the event is asserted (high).
10	RW	NX_PMU_CNT3_POSEDGE_SEL: If this bit is 1, the PMU will only count the event rising edge. If this bit is 0, the PMU will count every cycle the event is asserted (high).
11	RW	NX_PMU_RESET: Indicates how counter should reset. 0 = free running 1 = reset on SCOM read.
12:13	RW	NX_PMU_CNT0_EVENT_SEL: Indication of which of the 4 event pairs (8 total events) to count in counter0.
14:15	RW	NX_PMU_CNT0_BIT_PAIR_SEL: Indicates how the event pairs should be combined to increment this PMU counter.
16:17	RW	NX_PMU_CNT1_EVENT_SEL: Indication of which of the 4 event pairs (8 total events) to count in counter0.
18:19	RW	NX_PMU_CNT1_BIT_PAIR_SEL: Indicates how the event pairs should be combined to increment this PMU counter.
20:21	RW	NX_PMU_CNT2_EVENT_SEL: Indication of which of the 4 event pairs (8 total events) to count in counter0.
22:23	RW	NX_PMU_CNT2_BIT_PAIR_SEL: Indicates how the event pairs should be combined to increment this PMU counter.
24:25	RW	NX_PMU_CNT3_EVENT_SEL: Indication of which of the 4 event pairs (8 total events) to count in counter0.
26:27	RW	NX_PMU_CNT3_BIT_PAIR_SEL: Indicates how the event pairs should be combined to increment this PMU counter.
28:29	RW	NX_PMU_PORT_SEL: Chooses final pmu events to feed to the counters.
30:31	RW	Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	NX PMU Counter Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_PMU_COUNTER_REG
Address	0000000005012C27 (SCOM)
Description	NX PMU Counter Register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	NX_PMU_COUNTER_0: NX PMU Counter 0.
16:31	ROX	NX_PMU_COUNTER_1: NX PMU Counter 1.
32:47	ROX	NX_PMU_COUNTER_2: NX PMU Counter 2.
48:63	ROX	NX_PMU_COUNTER_3: NX PMU Counter 3.

Register Name	NX Miscellaneous Control Register
Mnemonic	NMMU.MM_FBC.CQ_WRAP.NXCQ_SCOM.NX_MISC_CONTROL_REG
Address	0000000005012C28 (SCOM)
Description	NX Miscellaneous Control Register

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b0000
4:7	RW	HANG_POLL_SCALE: How many hang polls that need to be detected to indicate a hang poll to the logic.
8:11	RW	HANG_DATA_SCALE: How many data polls that need to be detected to indicate a data poll to the logic.
12:15	RW	HANG_SHM_SCALE: How many data polls that need to be detected to indicate a shm poll to the logic. A shim poll is created by the CQ logic to detect hangs of SMs while waiting on exchanges with the shim logic.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	NMMU FIR 1 Register
Mnemonic	NMMU.MM_FIR1_REG
Address	0000000005012C40 (SCOM) 0000000005012C41 (SCOM1) 0000000005012C42 (SCOM2)
Description	NMMU FIR1 Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MM_FIR1_FBC_XLAT_ARY_ECC_CE_DET: Fabric DIn xlat array CE error detected.
1	RWX	WOX_AND	WOX_OR	MM_FIR1_FBC_XLAT_ARY_ECC_UE_DET: Fabric DIn xlat array UE error detected.
2	RWX	WOX_AND	WOX_OR	MM_FIR1_FBC_XLAT_ARY_ECC_SUE_DET: Fabric DIn xlat array SUE error detected.
3	RWX	WOX_AND	WOX_OR	MM_FIR1_FBC_CQRD_ARY_ECC_CE_DET: Fabric mst rd array CE error detected.
4	RWX	WOX_AND	WOX_OR	MM_FIR1_FBC_CQRD_ARY_ECC_UE_DET: Fabric mst rd array UE error detected.
5	RWX	WOX_AND	WOX_OR	MM_FIR1_FBC_CQRD_ARY_ECC_SUE_DET: Fabric mst rd array SUE error detected.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6	RWX	WOX_AND	WOX_OR	MM_FIR1_FBC_XLAT_PROT_ERR_DET: Fabric xlat protocol error detected.
7	RWX	WOX_AND	WOX_OR	MM_FIR1_FBC_XLAT_TIMEOUT_DET: Fabric xlat operation timeout detected.
8	RWX	WOX_AND	WOX_OR	MM_FIR1_SLB_DIR_PERR_DET: SLB directory parity error detected.
9	RWX	WOX_AND	WOX_OR	MM_FIR1_SLB_CAC_PERR_DET: SLB cache parity error detected.
10	RWX	WOX_AND	WOX_OR	MM_FIR1_SLB_LRU_PERR_DET: SLB lru parity error detected.
11	RWX	WOX_AND	WOX_OR	MM_FIR1_SLB_MULTIHIT_DET: SLB multi-hit error detected.
12	RWX	WOX_AND	WOX_OR	MM_FIR1_TLB_DIR_PERR_DET: TLB directory parity error detected.
13	RWX	WOX_AND	WOX_OR	MM_FIR1_TLB_CAC_PERR_DET: TLB cache parity error detected.
14	RWX	WOX_AND	WOX_OR	MM_FIR1_TLB_LRU_PERR_DET: TLB lru parity error detected.
15	RWX	WOX_AND	WOX_OR	MM_FIR1_TLB_MULTIHIT_DET: TLB multi-hit error detected.
16	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_SEG_FAULT_DET: Segment fault detected .
17	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_PG_FAULT_NOPTE_DET: Page fault detected due to no matching pte.
18	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_PG_FAULT_BPCHK_DET: Page fault detected due to basic prot chk fail.
19	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_PG_FAULT_VPCHK_DET: Page fault detected due to virt prot chk fail.
20	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_PG_FAULT_SEID_DET: Page fault detected due to seid mismatch .
21	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_ADD_ERR_CR_RD_DET: Address error CRESP detected by twsm for read .
22	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_PTE_UPD_FAIL_DET: PTE update fail due to armwf mismatch.
23	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_ADD_ERR_CR_WR_DET: Address error CRESP detected by twsm for write.
24	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_RDX_CFG_GUEST_DET: Unsupported radix configuration for guest-side .
25	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_RDX_CFG_HOST_DET: Unsupported radix configuration for host-side .
26	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_INVALID_WIMG_DET: Invalid wimg setting detected .
27	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_INV_RDX_QUAD_DET: Invalid radix quad access detected .
28	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_FOREIGN_ADDR_DET: Unexpected access to foreign address space .
29	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_PREFETCH_ABT_DET: Prefetch abort/fail detected .
30	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_CXT_CAC_PERR_DET: Context cache array parity error detected .
31	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_RDX_PWC_PERR_DET: Radix pwc array parity error detected .
32	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_SM_CTL_ERR_DET: Tablewalk sm control error detected .
33	RWX	WOX_AND	WOX_OR	MM_FIR1_CO_SM_CTL_ERR_DET: Castout sm control error detected .
34	RWX	WOX_AND	WOX_OR	MM_FIR1_CI_SM_CTL_ERR_DET: Check-in sm control error detected .

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
35	RWX	WOX_AND	WOX_OR	MM_FIR1_INV_SM_CTL_ERR_DET: Invalidate sm control error detected .
36	RWX	WOX_AND	WOX_OR	MM_FIR1_TW_TIMEOUT_ERR_DET: Tablewalk sm timeout error detected .
37	RWX	WOX_AND	WOX_OR	MM_FIR1_CO_TIMEOUT_ERR_DET: Castout sm timeout error detected .
38	RWX	WOX_AND	WOX_OR	MM_FIR1_CI_TIMEOUT_ERR_DET: Check-in sm timeout error detected .
39	RWX	WOX_AND	WOX_OR	MM_FIR1_INV_TIMEOUT_ERR_DET: Invalidate sm timeout error detected .
40	RWX	WOX_AND	WOX_OR	MM_FIR1_NX0_LXSTOP_ERR_DET: NX local checkstop error detected .
41	RWX	WOX_AND	WOX_OR	MM_FIR1_CP0_LXSTOP_ERR_DET: CP0 local checkstop error detected .
42	RWX	WOX_AND	WOX_OR	MM_FIR1_CP1_LXSTOP_ERR_DET: CP1 local checkstop error detected .
43	RWX	WOX_AND	WOX_OR	MM_FIR1_NPU_LXSTOP_ERR_DET: NPU local checkstop error detected .
44	RWX	WOX_AND	WOX_OR	MM_FIR1_FBC_LXSTOP_ERR_DET: FBC local checkstop error detected .
45	RWX	WOX_AND	WOX_OR	MM_FIR1_SPARE: FBC local checkstop error detected .
46	RWX	WOX_AND	WOX_OR	MM_FIR1_SCOM_PE_FIR: FIR/SCOM satellite parity error.
47	RWX	WOX_AND	WOX_OR	MM_FIR1_SCOM_PE_DUP_FIR: FIR/SCOM satellite parity error duplicate.
48:63	RO	RO	RO	Constant = 0b0000000000000000

Register Name	**NMMU FIR 1 Mask Register**
Mnemonic	NMMU.MM_FIR1_MASK_REG
Address	0000000005012C43 (SCOM) 0000000005012C44 (SCOM1) 0000000005012C45 (SCOM2)
Description	NMMU FIR1 Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:47	RW	WO_AND	WO_OR	MM_FIR1_MASK:
48:63	RO	RO	RO	Constant = 0b0000000000000000

Register Name	**NMMU FIR 1 Action 0 Register**
Mnemonic	NMMU.MM_FIR1_ACTION0_REG
Address	0000000005012C46 (SCOM)
Description	NMMU FIR1 Action0 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable (1,0) = Unused (1,1) = Local checkstop

Bits	SCOM	Field Mnemonic: Description
0:47	RW	MM_FIR1_ACTION0:

Bits	SCOM	Field Mnemonic: Description
48:63	RO	Constant = 0b0000000000000000

Register Name	NMMU FIR 1 Action 1 Register
Mnemonic	NMMU.MM_FIR1_ACTION1_REG
Address	0000000005012C47 (SCOM)
Description	NMMU FIR1 Action1 Register Action select for corresponding bit in FIR (Action1,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable (1,0) = Unused (1,1) = Local checkstop

Bits	SCOM	Field Mnemonic: Description
0:47	RW	MM_FIR1_ACTION1:
48:63	RO	Constant = 0b0000000000000000

Register Name	NMMU FIR 1 WOF Register
Mnemonic	NMMU.MM_FIR1_WOF_REG
Address	0000000005012C48 (SCOM)
Description	NMMU FIR1 WOF Register

Bits	SCOM	Field Mnemonic: Description
0:47	RWX_WCLRREG	Reserved.
48:63	RO	Constant = 0b0000000000000000

Register Name	NMMU Hypervisor Real Mode Offset Register
Mnemonic	NMMU.MM_CFG_NMMU_XLAT_CTL_REG0
Address	0000000005012C4A (SCOM)
Description	NMMU Hypervisor Real Mode Offset Register (HRMOR)

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MM_CFG_XLAT_CTL_HRMOR: Details the HRMOR register for hypervisor RA mode when DR = 0,HV = 1,EA(0) = 0. Only bits 8:51 valid.

Register Name	NMMU Partition Table Control Register
Mnemonic	NMMU.MM_CFG_NMMU_XLAT_CTL_REG1
Address	0000000005012C4B (SCOM)
Description	NMMU Partition Table Control Register (PTCR)

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MM_CFG_XLAT_CTL_PTCR: Details the Partition Table Control Register set up by the hypervisor. 0 - valid, 1:52 - PPTB (table base addr), 59:63 - PPTS (table size).

Register Name	NMMU SEID Base Address Register
Mnemonic	NMMU.MM_CFG_NMMU_XLAT_CTL_REG2
Address	0000000005012C4C (SCOM)
Description	NMMU SEID Base Address Register (SEIDBAR)

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MM_CFG_XLAT_CTL_SEIDBAR: Details the base address for the hashed SEID table as set up by ultravisor for ACM/Redbox support.

Register Name	NMMU State Machine Control Register
Mnemonic	NMMU.MM_CFG_NMMU_CTL_SM
Address	0000000005012C52 (SCOM)
Description	NMMU State Machine Control Register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	MM_CFG_NMMU_CTL_SM_TWSM_DIS: Per sm disables for tablewalk state machines. At least one must always be enabled w/i NMMU.
12:19	RW	MM_CFG_NMMU_CTL_SM_CKINSM_DIS: Per sm disables for check-in state machines. At least one must always be enabled w/i NMMU.
20	RW	MM_CFG_NMMU_CTL_SM_INV_SINGLE_THREAD_EN: Enables single-thread mode for snoop invalidates within fbc macro.
21	RW	MM_CFG_NMMU_CTL_TW_CXT_CAC_DIS: Disables twsm from allocating into the Context cache.
22:23	RW	Reserved.
24	RW	MM_CFG_NMMU_CTL_SM_ISS487_EN: Enables fix for iss487 where NX traffic runs as ST under DMT mode.
25	RW	Reserved.
26	RW	MM_CFG_NMMU_CTL_SM_ISS526_EN: Enables fix for iss526 where snp inv ops run as ST under DMT mode.
27:29	RW	Reserved.
30	RW	MM_CFG_NMMU_CTL_DYN_ST_FREQ_MULT: For dynamic single-thread mode, defines the interval over which slowdown pulses will be counted 0b00000 = Triggers frequency period of 1 k cycles 0b00001 = Triggers frequency period of 2 k cycles 0b00010 = Triggers frequency period of 3 k cycles 0b00100 = Triggers frequency period of 4 k cycles 0b00111 = Triggers frequency period of 8k cycles 0b01111 = Triggers frequency period of 16k cycles 0b11111 = Triggers frequency period of 32k cycles.
31	RW	MM_CFG_NMMU_CTL_TW_MPSS_DIS: Disable TW from finding MPSS (HPT) PTE hits.
32:39	RW	MM_CFG_NMMU_CTL_NCU_SNP_TLBIE_CNT_THRESH: Defines ncscoms_cfg_tlbie_cnt_thresh in nmmu ncu snooper for tlbie throttling mechanism.

Bits	SCOM	Field Mnemonic: Description
40	RW	MM_CFG_NMMU_CTL_TW_ATT_HPT_SAO_FOLD_DIS: Disables twsm from allowing SAO WIMG encoding for HPT to fold into normal mem category.
41	RW	MM_CFG_NMMU_CTL_TW_ATT_RDX_SAO_FOLD_DIS: Disables twsm from allowing SAO WIMG encoding for Rdx to fold into normal mem category.
42	RW	MM_CFG_NMMU_CTL_TW_ATT_RDX_NIO_FOLD_DIS: Disables twsm from allowing non-idempotent i/o encoding for Rdx to fold into cache-inh mem category.
43	RW	MM_CFG_NMMU_CTL_TW_ATT_RDX_TIO_FOLD_DIS: Disables twsm from allowing tolerant i/o encoding for Rdx to fold into cache-inh mem category.
44	RW	MM_CFG_NMMU_CTL_TW_LCO_RDX_EN: Enables twsm to attempt lateral castouts for all Radix guest and host pte cache lines for performance.
45	RW	MM_CFG_NMMU_CTL_TW_LCO_RDX_P_DIS: Disables twsm from attempting lateral castouts for Radix parent host/guest pte cache lines.
46	RW	MM_CFG_NMMU_CTL_TW_LCO_RDX_C_DIS: Disables twsm from attempting lateral castouts for Radix child host pte cache lines.
47	RW	MM_CFG_NMMU_CTL_TW_LCO_RDX_PWC_L2_DIS: Disables twsm from attempting lateral castouts for Radix pwc l2 pte cache lines.
48	RW	MM_CFG_NMMU_CTL_TW_LCO_RDX_PWC_L3_DIS: Disables twsm from attempting lateral castouts for Radix pwc l3 pte cache lines.
49	RW	MM_CFG_NMMU_CTL_TW_LCO_RDX_PWC_L4_DIS: Disables twsm from attempting lateral castouts for Radix pwc l4 pte cache lines.
50	RW	MM_CFG_NMMU_CTL_TW_LCO_RDX_PDE_EN: Enables twsm to attempt lateral castouts for Radix pde cache lines.
51	RW	Reserved.
52	RW	MM_CFG_NMMU_CTL_TW_RDX_PWC_DIS: Disables twsm from allocating into Radix page-walk cache.
53	RW	MM_CFG_NMMU_CTL_TW_RDX_INT_PWC_DIS: Disables twsm from allocating intermediate xlatns into Radix page-walk cache.
54	RW	MM_CFG_NMMU_CTL_TW_RDX_INT_TLB_DIS: Disables twsm from allocating intermediate xlatns into TLB.
55	RW	MM_CFG_NMMU_CTL_TW_RDX_PWC_SPLIT_EN: Drives twsm to split Radix page-walk cache in half for guest and half for host entries.
56	RW	MM_CFG_NMMU_CTL_TW_RDX_PWC_VA_HASH: Radix page-walk cache CGC hash only uses VA bits, Lpid,Pid treated as zeros.
57	RW	Reserved.
58	RW	MM_CFG_NMMU_CTL_TW_PTE_UPD_INTR_EN: Force Atomic PTE Update exception whenever a PTE Update is required.
59	RW	MM_CFG_NMMU_CTL_NCU_SNP_TLBIE_PACING_CNT_EN: Defines ncscoms_cfg_tlbie_pacing_cnt_en in nmmu ncu snooper for tlbie throttling mechanism.
60:63	RW	MM_CFG_NMMU_CTL_DYN_ST_FREQ_MULT: For dynamic single-thread mode, defines the interval over which slowdown pulses will be counted: 0b00000 = Triggers frequency period of 1 k cycles 0b00001 = Triggers frequency period of 2 k cycles 0b00010 = Triggers frequency period of 3 k cycles 0b00100 = Triggers frequency period of 4 k cycles 0b00111 = Triggers frequency period of 8 k cycles 0b01111 = Triggers frequency period of 16 k cycles 0b11111 = Triggers frequency period of 32 k cycles.

Register Name	NMMU Miscellaneous Control Register
Mnemonic	NMMU.MM_CFG_NMMU_CTL_MISC
Address	0000000005012C53 (SCOM)
Description	NMMU Miscellaneous Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1	RW	MM_CFG_NMMU_CTL_MISC_BKINV_INTERLOCK_DIS: Disables ctl sm interlock on lower-barrier phase of a back-invalidate sequence.
2	RW	MM_CFG_NMMU_CTL_MISC_DYN_ST_MODE_EN: Enables dynamic single-thread mode under multi-thread operation (that is, single-thread mode disabled).
3	RW	MM_CFG_NMMU_CTL_MISC_DYN_ST_MODE_HANGP_EN: Enables dynamic single-thread mode with every unit hang pulse under multi-thread operation.
4:7	RW	MM_CFG_NMMU_CTL_MISC_DYN_ST_MODE_THRESHOLD: Defines threshold of slowdown condition determintes pulses before engaging dynamic single-thread mode. 0b00000000 = Triggers dynamic state mode sequence w/ every slowdown condition determines pulse during frequency period/interval 0b00000001 = Triggers dynamic state mode sequence w/ every other slowdown condition determines pulse during frequency period/interval 0b00000010 = Triggers dynamic state mode sequence w/ every 1/3 slowdown condition determines pulse during frequency period/interval 0b00000011 = Triggers dynamic state mode sequence w/ every 1/4 slowdown condition determines pulse during frequency period/interval 0b00000111 = Triggers dynamic state mode sequence w/ every 1/8 slowdown condition determines pulse during frequency period/interval 0b00001111 = Triggers dynamic state mode sequence w/ every 1/16 slowdown condition determines pulse during frequency period/interval 0b00011111 = Triggers dynamic state mode sequence w/ every 1/32 slowdown condition determines pulse during frequency period/interval 0b00111111 = Triggers dynamic state mode sequence w/ every 1/64 slowdown condition determines pulse during frequency period/interval 0b01111111 = Triggers dynamic state mode sequence w/ every 1/128 slowdown condition determines pulse during frequency period/interval 0b11111111 = Triggers dynamic state mode sequence w/ every 1/256 slowdown condition determines pulse during frequency period/interval.
8	RW	MM_CFG_NMMU_CTL_MISC_CTL_LFSR_DIS: Disables ctl lbs LFSR.
9	RW	MM_CFG_NMMU_CTL_MISC_FBC_LFSR_DIS: Disables fbc lbs LFSR.
10	RW	MM_CFG_NMMU_CTL_MISC_FBC_INV_AMORT_DIS: Disables fbc bkinvsm from amortizing multiple inv ops under a single barrier to inclusive agent.
11	RW	Reserved.
12	RW	MM_CFG_NMMU_CTL_MISC_FBC_DIN_ECC_CHK_DIS: Disables fbc din mstr rd array ecc checks.
13	RW	MM_CFG_NMMU_CTL_MISC_FBC_XLAT_ECC_CHK_DIS: Disables fbc din xlat array ecc checks.
14	RW	MM_CFG_NMMU_CTL_MISC_FBC_XLAT_PROT_ERR_CHK_DIS: Disables fbc xlat protocol error checks.
15	RW	MM_CFG_NMMU_CTL_MISC_FBC_XLAT_TIMEOUT_CHK_DIS: Disables fbc xlat timeout error checks.
16	RW	MM_CFG_NMMU_CTL_MISC_CO_PROT_ERR_CHK_DIS: Disables castout sm protocol error checks.
17	RW	MM_CFG_NMMU_CTL_MISC_CO_TIMEOUT_CHK_DIS: Disables castout sm timeout error checks.
18	RW	MM_CFG_NMMU_CTL_MISC_CKIN_PROT_ERR_CHK_DIS: Disables checkin sm protocol error checks.
19	RW	MM_CFG_NMMU_CTL_MISC_CKIN_TIMEOUT_CHK_DIS: Disables checkin sm timeout error checks.
20	RW	MM_CFG_NMMU_CTL_MISC_INV_PROT_ERR_CHK_DIS: Disables inv sm protocol error checks.

Bits	SCOM	Field Mnemonic: Description
21	RW	MM_CFG_NMMU_CTL_MISC_INV_TIMEOUT_CHK_DIS: Disables inv sm timeout error checks.
22	RW	MM_CFG_NMMU_CTL_MISC_TW_PROT_ERR_CHK_DIS: Disables twalk sm protocol error checks.
23	RW	MM_CFG_NMMU_CTL_MISC_TW_TIMEOUT_CHK_DIS: Disables twalk sm timeout error checks.
24	RW	MM_CFG_NMMU_CTL_MISC_FBC_SNP_PROT_ERR_CHK_DIS: Disables fbc snp protocol error checks.
25	RW	MM_CFG_NMMU_CTL_MISC_FBC_SNP_TIMEOUT_CHK_DIS: Disables fbc snp timeout error checks.
26	RW	MM_CFG_NMMU_CTL_MISC_FBC_CMD_PROT_ERR_CHK_DIS: Disables fbc command protocol error checks.
27	RW	Reserved.
28:31	RW	MM_CFG_NMMU_CTL_MISC_DYN_ST_MODE_THRESHOLD: Defines threshold of slowdown cond det pulses before engaging dynamic single-thread mode. 0b00000000 = Triggers dynamic state mode sequence with every slowdown condition determines pulse during frequency period/interval 0b00000001 = Triggers dynamic state mode sequence with every other slowdown condition determines pulse during frequency period/interval 0b00000010 = Triggers dynamic state mode sequence with every 1/3 slowdown condition determines pulse during frequency period/interval 0b00000011 = Triggers dynamic state mode sequence with every 1/4 slowdown condition determines pulse during frequency period/interval 0b00000111 = Triggers dynamic state mode sequence with every 1/8 slowdown condition determines pulse during frequency period/interval 0b00001111 = Triggers dynamic state mode sequence with every 1/16 slowdown condition determines pulse during frequency period/interval 0b00011111 = Triggers dynamic state mode sequence with every 1/32 slowdown condition determines pulse during frequency period/interval 0b00111111 = Triggers dynamic state mode sequence with every 1/64 slowdown condition determines pulse during frequency period/interval 0b01111111 = Triggers dynamic state mode sequence with every 1/128 slowdown condition determines pulse during frequency period/interval 0b11111111 = Triggers dynamic state mode sequence with every 1/256 slowdown condition determines pulse during frequency period/interval.
32:47	RW	MM_CFG_NMMU_CTL_MISC_HANG_PLS_MULT: Defines base hang pulse multiplier in forming unit hang pulse timer. Base pulse is every 1 k cycles.
48:55	RW	MM_CFG_NMMU_CTL_MISC_NCU_SNP_TLBIE_INC_RATE: Defines ncscoms_cfg_tlbie_inc_rate in nmmu ncu snooper for tlbie throttling mechanism.
56:63	RW	MM_CFG_NMMU_CTL_MISC_NCU_SNP_TLBIE_DEC_RATE: Defines ncscoms_cfg_tlbie_dec_rate in nmmu ncu snooper for tlbie throttling mechanism.

Register Name	**NMMU SLB Control Register**
Mnemonic	NMMU.MM_CFG_NMMU_CTL_SLB
Address	0000000005012C54 (SCOM)
Description	NMMU SLB Control Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MM_CFG_NMMU_CTL_SLB_MBR_DIS: Per member disables for slb dir/cache per cgc. Coarse-granularity for disables, as follows. no configuration disables set for any mbr = ways 00-15 enabled - configuration disables for any mbr 00-03 = ways 00-15 enabled - configuration disables for any mbr 04-07 = ways 04-15 disabled - configuration disables for any mbr 08-11 = ways 08-15 disabled - configuration disables for any mbr 12-15 = ways 12-15 disabled.

Bits	SCOM	Field Mnemonic: Description
16	RW	MM_CFG_NMMU_CTL_SLB_SNGL_THD_EN: Enables single-thread mode for xlat ops through slb pipe.
17	RW	MM_CFG_NMMU_CTL_SLB_CAC_ALLOC_DIS: Disables all SLB cache allocations. Instead, forces tablewalk always. -- Reserved BIT.
18	RW	MM_CFG_NMMU_CTL_SLB_DMAP_MODE_EN: Enables SLB direct-mapped mode. Not used in p9 dd1.
19	RW	MM_CFG_NMMU_CTL_SLB_ALT_SEGSZ_DIS: Disables use of alternate segment size within SLB.
20	RW	MM_CFG_NMMU_CTL_SLB_DIR_PERR_CHK_DIS: Disables slb directory parity error checks.
21	RW	MM_CFG_NMMU_CTL_SLB_CAC_PERR_CHK_DIS: Disables slb cache parity error checks.
22	RW	MM_CFG_NMMU_CTL_SLB_LRU_PERR_CHK_DIS: Disables slb lru parity error checks.
23	RW	MM_CFG_NMMU_CTL_SLB_MULTIHIT_CHK_DIS: Disables slb multi-hit error checks.
24	RW	MM_CFG_NMMU_CTL_SLB_ISS505_FIX_DIS: Disable fix for issue505 override of tw_dir_wr status for lock release xltype.
25	RW	MM_CFG_NMMU_CTL_SLB_ISS510_FIX_DIS: Disable fix for issue510 tags active SLS override of lock_snp_val.
26	RW	MM_CFG_NMMU_CTL_SLB_ISS511_FIX_DIS: Disable fix for issue511 abort operation holdoff of chkout slow_retry generator.
27	RW	MM_CFG_NMMU_CTL_SLB_ISS544_FIX_DIS: Disable fix for issue544 for tag compare of error promote operation with current single-thd operation.
28	RW	MM_CFG_NMMU_CTL_SLB_ISS554_FIX_DIS: Disable fix for issue554 for holding off TLBIE commands until subsequent st wdw grants token to TLBIE command.
29:31	RW	Reserved.
32:35	RW	MM_CFG_NMMU_CTL_SLB_DBG_BUS0_STG0_SEL: NMMU SLB macro bus0 stage0 multiplexer select.
36:39	RW	MM_CFG_NMMU_CTL_SLB_DBG_BUS1_STG0_SEL: NMMU SLB macro bus1 stage0 multiplexer select.
40:51	RW	Reserved.
52	RW	MM_CFG_NMMU_CTL_SLB_ISS542_FIX_DIS: Disables slb fix for iss542 where inuse bits are allowed to impact lru state calculation.
53:63	RW	Reserved.

Register Name	NMMU TLB Control Register
Mnemonic	NMMU.MM_CFG_NMMU_CTL_TLB
Address	0000000005012C55 (SCOM)
Description	NMMU TLB Control Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MM_CFG_NMMU_CTL_TLB_MBR_DIS: Per member disables for tlb dir/cache per cgc. Coarse-granularity for disables, as follows. no configuration disables set for any mbr = ways 00-15 enabled - configuration disables for any mbr 00-03 = ways 00-15 enabled - configuration disables for any mbr 04-07 = ways 04-15 disabled - configuration disables for any mbr 08-11 = ways 08-15 disabled - configuration disables for any mbr 12-15 = ways 12-15 disabled.
16	RW	MM_CFG_NMMU_CTL_TLB_SNGL_THD_EN: Enables single-thread mode for xlat ops through tlb pipe.
17	RW	MM_CFG_NMMU_CTL_TLB_CAC_ALLOC_DIS: Disables all TLB cache allocations. Instead, forces tablewalk always. -- Reserved bit.
18	RW	MM_CFG_NMMU_CTL_TLB_DMAP_MODE_EN: Enables TLB direct-mapped mode.

Bits	SCOM	Field Mnemonic: Description
19	RW	MM_CFG_NMMU_CTL_TLB_MPSS_DIS: Disables mpss mode within TLB.
20	RW	MM_CFG_NMMU_CTL_TLB_HASH_LPID_DIS: Disables lpid influence within tlb hash.
21	RW	MM_CFG_NMMU_CTL_TLB_HASH_PID_DIS: Disables pid influence within tlb hash.
22	RW	MM_CFG_NMMU_CTL_TLB_DIR_PERR_CHK_DIS: Disables tlb directory parity error checks.
23	RW	MM_CFG_NMMU_CTL_TLB_CAC_PERR_CHK_DIS: Disables tlb cache parity error checks.
24	RW	MM_CFG_NMMU_CTL_TLB_LRU_PERR_CHK_DIS: Disables tlb lru parity error checks.
25	RW	MM_CFG_NMMU_CTL_TLB_MULTIHIT_CHK_DIS: Disables tlb multi-hit error checks.
26	RW	MM_CFG_NMMU_CTL_TLB_EA_RANGE_CHK_DIS: Disables tlb ea(2:11) range check for exerciser purposes.
27	RW	MM_CFG_NMMU_CTL_TLB_ISS426_FIX_DIS: Disables fix for iss426 for twsm handoff of mpss cgc, instead of base cgc, for nearhit.
28	RW	MM_CFG_NMMU_CTL_TLB_ISS486_FIX_DIS: Disable fix for issue486 generating a stat = x6 for sec resv behind another sec resv/lock.
29	RW	MM_CFG_NMMU_CTL_TLB_ISS505_FIX_DIS: Disable fix for issue505 override of tw_dir_wr status for lock release xltype.
30	RW	MM_CFG_NMMU_CTL_TLB_ISS510_FIX_DIS: Disable fix for issue510 TA-SLS and virt_real terms into car0 host_replay calc.
31	RW	MM_CFG_NMMU_CTL_TLB_ISS512_FIX_DIS: Disable fix for issue512 slb recyc release all locks sending promote with ST arbiter error flag.
32:35	RW	MM_CFG_NMMU_CTL_TLB_DBG_BUS0_STG0_SEL: NMMU TLB macro bus0 stage0 multiplexer select.
36:39	RW	MM_CFG_NMMU_CTL_TLB_DBG_BUS1_STG0_SEL: NMMU TLB macro bus1 stage0 multiplexer select.
40	RW	MM_CFG_NMMU_CTL_TLB_ISS534_FIX_DIS: Disable fix for issue534 for fast retry of an operation immediately following a recycle with exception.
41	RW	MM_CFG_NMMU_CTL_TLB_ISS537_FIX_DIS: Disable fix for issue537 of sending Radix demote operation from TLB to SLB to clear local inUse latches.
42	RW	MM_CFG_NMMU_CTL_TLB_ISS540_FIX_DIS: Disable fix for issue540 for DD2 only.
43	RW	MM_CFG_NMMU_CTL_TLB_ISS543_FIX_DIS: Disables tlb fix for iss543 to override xltype dependency on the flush operation behind int dir read.
44:47	RW	MM_CFG_NMMU_CTL_TLB_GUEST_PREF_PGSZ: Defines preferred Radix guest page size when mpss is disabled within the TLB pipe.
48:51	RW	MM_CFG_NMMU_CTL_TLB_HOST_PREF_PGSZ: Defines preferred Radix host page size when mpss is disabled within the TLB pipe.
52	RW	MM_CFG_NMMU_CTL_TLB_ISS542_FIX_DIS: Disables tlb fix for iss542 where inuse bits are allowed to impact lru state calculation.
53	RW	MM_CFG_NMMU_CTL_TLB_ISS543B_FIX_EN: Enables tlb fix for iss543 part b to broaden fast-retry for any adjacent operation to a flush.
54:63	RW	Reserved.

Register Name	**NMMU Error Log Register**
Mnemonic	NMMU.MM_NMMU_ERR_LOG
Address	0000000005012C57 (SCOM)
Description	NMMU Error Log Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MM_ERR_LOG: Details the NMMU Error Log Register - TBD.

Register Name	NMMU Error Inject Register
Mnemonic	NMMU.MM_NMMU_ERR_INJ
Address	0000000005012C58 (SCOM)
Description	NMMU Error Inject Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MM_ERR_INJ: Details the NMMU Error Inject Register - TBD.

Register Name	NMMU Debug Mode Register
Mnemonic	NMMU.MM_NMMU_DBG_MODE
Address	0000000005012C59 (SCOM)
Description	NMMU Debug Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MM_DBG_MODE_EN: Enables NMMU Debug Bus mode latches.
1	RW	MM_DBG_MODE_PRV_BUS0_STG2_SEL: NMMU prv macro bus0 stage2 multiplexer select.
2	RW	MM_DBG_MODE_PRV_BUS1_STG2_SEL: NMMU prv macro bus1 stage2 multiplexer select.
3	RW	MM_DBG_MODE_FBC_BUS0_STG2_SEL: NMMU fbc macro bus0 stage2 multiplexer select.
4	RW	MM_DBG_MODE_FBC_BUS1_STG2_SEL: NMMU fbc macro bus1 stage2 multiplexer select.
5	RW	MM_DBG_MODE_MSC_BUS0_STG2_SEL: NMMU msc macro bus0 stage2 multiplexer select.
6	RW	MM_DBG_MODE_MSC_BUS1_STG2_SEL: NMMU msc macro bus1 stage2 multiplexer select.
7	RW	MM_DBG_MODE_SLB_BUS0_STG2_SEL: NMMU SLB macro bus0 stage2 multiplexer select.
8	RW	MM_DBG_MODE_SLB_BUS1_STG2_SEL: NMMU SLB macro bus1 stage2 multiplexer select.
9	RW	MM_DBG_MODE_TW_BUS0_STG2_SEL: NMMU TW macro bus0 stage2 multiplexer select.
10	RW	MM_DBG_MODE_TW_BUS1_STG2_SEL: NMMU TW macro bus1 stage2 multiplexer select.
11	RW	MM_DBG_MODE_RDX_BUS0_STG2_SEL: NMMU RDX macro bus0 stage2 multiplexer select.
12	RW	MM_DBG_MODE_RDX_BUS1_STG2_SEL: NMMU RDX macro bus1 stage2 multiplexer select.
13	RW	MM_DBG_MODE_TLB_BUS0_STG2_SEL: NMMU TLB macro bus0 stage2 multiplexer select.
14	RW	MM_DBG_MODE_TLB_BUS1_STG2_SEL: NMMU TLB macro bus1 stage2 multiplexer select.
15	RW	MM_DBG_MODE_FBC_BUS0_STG1_SEL: NMMU fbc macro bus0 stage1 multiplexer select.
16	RW	MM_DBG_MODE_FBC_BUS1_STG1_SEL: NMMU fbc macro bus1 stage1 multiplexer select.
17	RW	MM_DBG_MODE_MSC_BUS0_STG1_SEL: NMMU msc macro bus0 stage1 multiplexer select.
18	RW	MM_DBG_MODE_MSC_BUS1_STG1_SEL: NMMU msc macro bus1 stage1 multiplexer select.
19	RW	MM_DBG_MODE_SLB_BUS0_STG1_SEL: NMMU SLB macro bus0 stage1 multiplexer select.
20	RW	MM_DBG_MODE_SLB_BUS1_STG1_SEL: NMMU SLB macro bus1 stage1 multiplexer select.
21	RW	MM_DBG_MODE_TW_BUS0_STG1_SEL: NMMU TW macro bus0 stage1 multiplexer select.
22	RW	MM_DBG_MODE_TW_BUS1_STG1_SEL: NMMU TW macro bus1 stage1 multiplexer select.

Bits	SCOM	Field Mnemonic: Description
23	RW	MM_DBG_MODE_RDX_BUS0_STG1_SEL: NMMU RDX macro bus0 stage1 multiplexer select.
24	RW	MM_DBG_MODE_RDX_BUS1_STG1_SEL: NMMU RDX macro bus1 stage1 multiplexer select.
25	RW	MM_DBG_MODE_TLB_BUS0_STG1_SEL: NMMU TLB macro bus0 stage1 multiplexer select.
26	RW	MM_DBG_MODE_TLB_BUS1_STG1_SEL: NMMU TLB macro bus1 stage1 multiplexer select.
27:31	RW	Reserved.
32:35	RW	MM_DBG_MODE_FBC_BUS0_STG0_SEL: NMMU FBC macro bus0 stage0 multiplexer select.
36:39	RW	MM_DBG_MODE_FBC_BUS1_STG0_SEL: NMMU FBC macro bus1 stage0 multiplexer select.
40:43	RW	MM_DBG_MODE_MSC_BUS0_STG0_SEL: NMMU MSC macro bus0 stage0 multiplexer select.
44:47	RW	MM_DBG_MODE_MSC_BUS1_STG0_SEL: NMMU MSC macro bus1 stage0 multiplexer select.
48:53	RW	MM_DBG_MODE_TW_BUS0_STG0_SEL: NMMU TW macro bus0 stage0 multiplexer select.
54:59	RW	MM_DBG_MODE_TW_BUS1_STG0_SEL: NMMU TW macro bus1 stage0 multiplexer select.
60:61	RW	MM_DBG_MODE_RDX_BUS0_STG0_SEL: NMMU RDX macro bus0 stage0 multiplexer select.
62:63	RW	MM_DBG_MODE_RDX_BUS1_STG0_SEL: NMMU RDX macro bus1 stage0 multiplexer select.

Register Name	**Software Initiated Interrupt Response Register**
Mnemonic	INT.INT_CQ.INT_CQ_SWI_RSP
Address	0000000005013009 (SCOM)
Description	This register is cleared whenever software writes to any of the above five Software Initiated Interrupt Command ports. When the command completes on the processor bus, this register will be loaded with the result. A write to this register has no effect.

Bits	SCOM	Field Mnemonic: Description
0	ROX	INT_CQ_SWI_RSP_HIST_DONE: Histogram command completed.
1	ROX	INT_CQ_SWI_RSP_POLL_DONE: Poll command completed.
2	ROX	INT_CQ_SWI_RSP_BCAST_DONE: Broadcast command completed.
3	ROX	INT_CQ_SWI_RSP_ASSIGN_DONE: Assign command completed.
4	ROX	INT_CQ_SWI_RSP_BLK_UPDT_DONE: Block Update command completed.
5	ROX	INT_CQ_SWI_RSP_Z: Zero responders. For the Poll-group commands (Poll, Assign, Broadcast), this equates to Ack types of: Ack0, AckC, AckP. For the Ack-group commands (Histogram, Block Update), this equates to Ack types of: HAck0, HAckP.
6	ROX	INT_CQ_SWI_RSP_O: One responder. For the Poll-group commands (Poll, Assign, Broadcast), this equates to Ack types of: Ack1, Ack1x. For the Ack-group commands (Histogram, Block Update), this equates to the Ack type of: HAckN. Please note that for these commands, there is no need. to distinguish between one responder vs. multiple responders.
7	ROX	INT_CQ_SWI_RSP_M: Multiple responders. For the Poll-group commands (Poll, Assign, Broadcast), this equates to the Ack type of: AckN. For the Ack-group commands (Histogram, Block Update), this equates to the Ack type of: HAckN.
8:12	ROX	INT_CQ_SWI_RSP_CRESP_0_4: Combined Response - cResp(0:4).
13	ROX	INT_CQ_SWI_RSP_Reserved_13: Reserved.
14	ROX	INT_CQ_SWI_RSP_COLLISON: Collision - ATAG(17).
15	ROX	INT_CQ_SWI_RSP_PRECLUDE: Precluded - ATAG(16).

Bits	SCOM	Field Mnemonic: Description
16:31	ROX	INT_CQ_SWI_RSP_ATAG_0_15: Combined Response ATAG(0:15). This is the final sequential ATAG, after having rearranged the bits by moving bit 18 into bit 12s position.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus General Configuration Register
Mnemonic	INT.INT_CQ.INT_CQ_CFG_PB_GEN
Address	000000000501300A (SCOM)
Description	General processor bus configuration information. The bits in this register must be set to the same value across all INT units in the system.

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_CQ_CFG_PB_GEN_ADDR_BAR_MODE: System Address Mapping Mode - INT_CQ uses this for initial scope selection during master commands.
1	RW	INT_CQ_CFG_PB_GEN_PUMP_MODE: Pump Mode - This alters the physical reach of G scope, and it allows the INT unit to infer the system topology. Both Ln and G scope are constrained to the masters chip. While in this mode, it is recommended that skip_G be set for best performance.
2	RW	INT_CQ_CFG_PB_GEN_PHYP_SCOPE: Hypervisor scope range - This is used to determine the scope of certain commands that are intended to stay within a pHyps span of control. When. chip_is_node, I use this pHyp scope to distinguish between a HE 4x4 system or a 16x4 CCSM system.
3	ROX	INT_CQ_CFG_PB_GEN_PB_INIT: Processor bus initialized. This read-only bit is equal to the pb_int_pb_init input.
4	RW	INT_CQ_CFG_PB_GEN_MODE_128K_VP: 128K VP Mode - The block offset field in Interrupt commands is limited to 17 bits (128K) rather than the normal 19-bits. Therefore, the upper two. bits are always zero. INT_CQ uses this fact to shuffle address bits on the processor bus during Interrupt commands to guarantee that Addr(17:18) are. always equal to the two LSBs of my Group ID. This mode is related to the processor bus Fabrics behavior of using Addr(15:18) to create the target vector. during Vg scope commands. It is anticipated that this mode will only be enabled in HE system configurations (4x4). Please note that this mode bit. must be set consistent across all INT units.
5:15	RW	INT_CQ_CFG_PB_GEN_Reserved_5_15: Reserved.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Processor Cores Enabled for Message Send Register
Mnemonic	INT.INT_CQ.INT_CQ_MSGSND
Address	000000000501300B (SCOM)
Description	Identifies which of the 24 possible core chiplets are enabled and available to receive the MsgSnd processor bus command. A MsgSnd command that targets an enabled core will be given a pResp of lpc_ack. A MsgSnd command that targets a disabled core will be ignored. Note that CQ does not need to be explicitly aware of Normal-core vs. Fused-core mode. Regardless of the mode, CQ will always use PB Addr(23:27) to index into this register.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INT_CQ_MSGSND_CORES_ENABLED_0_23: In Normal Core Mode, these 24 bits reference the 24 logical 4-threaded cores. bit 0 = core 0 (0 is dead, 1 is active). bit 1 = core 1. bit 2 = core 2. (and so on). In Fused Core Mode, these 12 pairs of bits reference the 12 logical 8-threaded cores. bits 0:1 = core 0 (set to either 00 or 11). bits 2:3 = core 1. bits 4:5 = core 2. (and so on).
24:63	RO	Constant = 0b000000000000000000000000000000000000000000000000

Register Name	**INT Unit Event Selection for CNPM Register**
Mnemonic	INT.INT_CQ.INT_CQ_CNPM_SEL
Address	000000000501300F (SCOM)
Description	Controls the 32-bit POWER9 Event Bus outputs of the INT unit, which go to the Common Nest Performance Monitor (CNPM) logic.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	INT_CQ_CNPM_SEL_PMON_MUX_BYTE0_0_2: Controls events sent to CNPM event bus, byte 0. 0 = zeros. 1 = PC events. 2 = VC events. 3 = CQ events.
3:5	RW	INT_CQ_CNPM_SEL_PMON_MUX_BYTE1_0_2: Controls events sent to CNPM event bus, byte 1. (same selection encodes as listed for byte 0).
6:8	RW	INT_CQ_CNPM_SEL_PMON_MUX_BYTE2_0_2: Controls events sent to CNPM event bus, byte 2. (same selection encodes as listed for byte 0).
9:11	RW	INT_CQ_CNPM_SEL_PMON_MUX_BYTE3_0_2: Controls events sent to CNPM event bus, byte 3. (same selection encodes as listed for byte 0).
12:23	RW	INT_CQ_CNPM_SEL_Reserved_12_23: Reserved.
24:39	RW	INT_CQ_CNPM_SEL_EBUS_ENABLE_0_15: Drives the INT_PB_EBUS_ENABLE(0:15) outputs of INT.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	**Interrupt Controller Base Address Register**
Mnemonic	INT.INT_CQ.INT_CQ_IC_BAR
Address	0000000005013010 (SCOM)
Description	Used during inbound cache inhibited (CI) reads/writes. This BAR points to a fixed size of eight pages (either eight 4 K pages resulting in a 32 K range, or eight 64 K pages resulting in a 512 K range).

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_CQ_IC_BAR_VALID: Valid - When this bit is a 1, the BAR is enabled to actively participate in comparing its memory pointer to inbound operations.
1	RWX	INT_CQ_IC_BAR_PAGE_SIZE_64K: Page size for IC BAR: 0 = 4 K, 1 = 64 K.
2:7	RO	Constant = 0b000000

Bits	SCOM	Field Mnemonic: Description
8:48	RWX	INT_CQ_IC_BAR_ADDR_8_48: Pointer to a 32 K range in memory.
49:63	RO	Constant = 0b0000000000000000

Register Name	Thread Management Base Address 1 Register
Mnemonic	INT.INT_CQ.INT_CQ_TM1_BAR
Address	0000000005013012 (SCOM)
Description	Used during inbound cache inhibited (CI) reads/writes. Each BAR points to a fixed size of four pages (either four 4K pages resulting in a 16 K range, or four 64 K pages resulting in a 256 K range).

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_CQ_TM1_BAR_VALID: Valid - When this bit is a 1, the BAR is enabled to actively participate in comparing its memory pointer to inbound operations.
1	RWX	INT_CQ_TM1_BAR_PAGE_SIZE_64 K: Page size for TM BAR: 0 = 4 K, 1 = 64 K.
2:7	RO	Constant = 0b000000
8:49	RWX	INT_CQ_TM1_BAR_ADDR_8_49: Pointer to a 16K range in memory.
50:63	RO	Constant = 0b00000000000000

Register Name	Thread Management Base Address 2 Register
Mnemonic	INT.INT_CQ.INT_CQ_TM2_BAR
Address	0000000005013014 (SCOM)
Description	Used during inbound cache inhibited (CI) reads/writes. Each BAR points to a fixed size of four pages (either four 4 K pages resulting in a 16 K range, or four 64 K pages resulting in a 256 K range).

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_CQ_TM2_BAR_VALID: Valid - When this bit is a 1, the BAR is enabled to actively participate in comparing its memory pointer to inbound operations.
1	RWX	INT_CQ_TM2_BAR_PAGE_SIZE_64K: Page size for TM BAR: 0 = 4 K, 1 = 64 K.
2:7	RO	Constant = 0b000000
8:49	RWX	INT_CQ_TM2_BAR_ADDR_8_49: Pointer to a 16 K range in memory.
50:63	RO	Constant = 0b00000000000000

Register Name	Presentation Controller Base Address Register
Mnemonic	INT.INT_CQ.INT_CQ_PC_BAR
Address	0000000005013016 (SCOM)
Description	Used during inbound cache inhibited (CI) reads/writes. This BAR points to a variable size range, between 32 M - 256 G, by using the mask register described below.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_CQ_PC_BAR_VALID: Valid - When this bit is a 1, the BAR is enabled to actively participate in comparing its memory pointer to inbound operations.
1:7	RO	Constant = 0b0000000

Bits	SCOM	Field Mnemonic: Description
8:38	RWX	INT_CQ_PC_BAR_ADDR_8_38: Pointer to a variable size range in memory (from 32 M to 256 G).
39:63	RO	Constant = 0b00000000000000000000000000

Register Name	Presentation Controller Base Address Mask Register
Mnemonic	INT.INT_CQ.INT_CQ_PC_BARM
Address	0000000005013017 (SCOM)
Description	Used in conjunction with the PC_BAR register described above. The mask register selects which bits of the PC_BAR are used during address compares, and thus dictates the size of the memory range.

Bits	SCOM	Field Mnemonic: Description
0:25	RO	Constant = 0b00000000000000000000000000
26:38	RW	INT_CQ_PC_BARM_ADDR_26_38: Mask bits. 0 = Exclude the corresponding address bit in the compare. 1 = Include the corresponding address bit in the compare. 0b1111111111111 = selects a 32 M range. 0b1111111111110 = selects a 64 M range. - - - 0b1000000000000 = selects a 128 G range. 0b0000000000000 = selects a 256 G range.
39:63	RO	Constant = 0b00000000000000000000000000

Register Name	Virtualization Controller Base Address Register
Mnemonic	INT.INT_CQ.INT_CQ_VC_BAR
Address	0000000005013018 (SCOM)
Description	Used during inbound cache inhibited (CI) reads/writes. This BAR points to a variable size range, between 64 M - 8 T, by using the mask register described below.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_CQ_VC_BAR_VALID: Valid - When this bit is a 1, the BAR is enabled to actively participate in comparing its memory pointer to inbound operations.
1:7	RO	Constant = 0b0000000
8:37	RWX	INT_CQ_VC_BAR_ADDR_8_37: Pointer to a variable size range in memory (from 64 M to 8 T).
38:63	RO	Constant = 0b00000000000000000000000000

Register Name	Virtualization Controller Base Address Mask Register
Mnemonic	INT.INT_CQ.INT_CQ_VC_BARM
Address	0000000005013019 (SCOM)
Description	Used in conjunction with the VC_BAR register described above. The mask register selects which bits of the VC_BAR are used during address compares, and thus dictates the size of the memory range.

Bits	SCOM	Field Mnemonic: Description
0:20	RO	Constant = 0b00000000000000000000

Bits	SCOM	Field Mnemonic: Description
21:37	RW	INT_CQ_VC_BARM_ADDR_21_37: Mask bits. 0 = Exclude the corresponding address bit in the compare. 1 = Include the corresponding address bit in the compare. 0b11111111111111111 = selects a 64 M range. 0b11111111111111110 = selects a 128 M range. - - - 0b10000000000000000 = selects a 4 T range. 0b00000000000000000 = selects a 8 T range.
38:63	RO	Constant = 0b00000000000000000000000000

Register Name	Table Address Register
Mnemonic	INT.INT_CQ.INT_CQ_TAR
Address	000000000501301E (SCOM)
Description	Used in conjunction with the Table Data Register (below) to read/write various tables within CQ. Software first loads the Table Address Register to point to the desired table (and the entry within that table), then software can access that specific entry via reading/writing the Table Data Register.

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_CQ_TAR_AUTO_INC: Auto Increment - When this bit is a 1, any access to the Table Data Register will increment the Entry Pointer (in bits 26:31).
1:11	RO	Constant = 0b00000000000
12:15	RW	INT_CQ_TAR_TABLE_SEL_0_3: Table Select (0:3) - Selects which table is being accessed.
16:25	RO	Constant = 0b0000000000
26:31	RWX	INT_CQ_TAR_ENTRY_SEL_0_5: Entry Pointer (0:5) - When the Auto Increment bit is a 1, any access to the Table Data Register will increment this Entry Pointer.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus Input Control Register
Mnemonic	INT.INT_CQ.INT_CQ_PBI_CTL
Address	0000000005013020 (SCOM)
Description	Controls various functions relating to the processor bus input logic.

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_CQ_PBI_CTL_DIS_ECCCHK_PBI: Disable ECC data correction on the processor bus Data Ramp inputs.
1	RW	INT_CQ_PBI_CTL_DIS_ECCCHK_STO: Disable ECC data correction while reading the Store Data array.
2	RW	INT_CQ_PBI_CTL_Reserved_2: Reserved.
3	RW	INT_CQ_PBI_CTL_Reserved_3: Reserved.
4	RW	INT_CQ_PBI_CTL_Reserved_4: Reserved.
5	RW	INT_CQ_PBI_CTL_PAGE_SIZE_64K_PC: Page size for PC BAR: 0 = 4K, 1 = 64K.
6	RW	INT_CQ_PBI_CTL_PAGE_SIZE_64K_VC: Page size for VC BAR: 0 = 4K, 1 = 64K.
7	RW	INT_CQ_PBI_CTL_LINUX_TRIG_MODE: Linux Trigger Mode - During accesses to the Virtualization Controller BAR, if the EDT set type is "01", then rather than having a pair of pages (IPI.Trigger / EOI) selected by Addr(51), the PB command type (CI Write vs. CI Read) will determine whether the operation is a IPI Trigger or IVE SB EOI.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	INT_CQ_PBI_CTL_TRACE_BUS_SEL_0_1: Controls source of the INT debug trace bus: int_tc_0_trace_bus(0:87). 0 = zeros. 1 = PC trace bus. 2 = VC trace bus. 3 = CQ trace bus.
10:11	RW	INT_CQ_PBI_CTL_CQ_TRACE_SEL_0_1: Controls source of CQs trace bus contribution. 0 = zeros. 1 = CI Store and CI Load FSM state information. 2 = Outbound Read and Write FSM state information. 3 = Outbound Interrupt FSM state information.
12	RW	INT_CQ_PBI_CTL_DIS_DMA_W: Disable accepting DMA Writes as IPI triggers through the VC BAR.
13	RW	INT_CQ_PBI_CTL_STRICT_IPI_RULES: Strict enforcement that IPI triggers target only even pages in the IPI range of the VC BAR (while not in Linux Trigger Mode).
14	WOX	INT_CQ_PBI_CTL_FORCE_ECC_CE: Force a single-shot ECC correctable error on the next cycle that data is written into the selected array. Data bit 0 is flipped.
15	WOX	INT_CQ_PBI_CTL_FORCE_ECC_UE: Force a single-shot ECC uncorrectable error on the next cycle that data is written into the selected array. Data bits 0 and 1 are flipped.
16	RW	INT_CQ_PBI_CTL_FORCE_ECC_SEL: Array selection when forcing ECC errors.
17	RW	INT_CQ_PBI_CTL_SPEC_CILD_G: Speculative CI Load scope requirement.
18	RW	INT_CQ_PBI_CTL_EN_SPEC_CILD_IVE: Enable speculative CI Load on AIB for IVE SB EOI (to VC).
19	RW	INT_CQ_PBI_CTL_EN_SPEC_CILD_EQD: Enable speculative CI Load on AIB for EQD SB EOI (to VC).
20	RW	INT_CQ_PBI_CTL_EN_SPEC_CILD_VPC_HW: Enable speculative CI Load on AIB for VPC access (to PC) when the command does not come from a processor core (TTAG bit 10 = 0).
21	RW	INT_CQ_PBI_CTL_EN_SPEC_CILD_VPC_SW: Enable speculative CI Load on AIB for VPC access (to PC) when the command comes from a processor core (TTAG bit 10 = 1).
22:31	RW	INT_CQ_PBI_CTL_Reserved_22_31: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	**Power Bus Output Control Register**
Mnemonic	INT.INT_CQ.INT_CQ_PBO_CTL
Address	0000000005013021 (SCOM)
Description	Controls various functions relating to the processor bus output logic.

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_CQ_PBO_CTL_DIS_ECCCHK_LDO: Disable ECC data correction while reading the Load Data array.
1	RW	INT_CQ_PBO_CTL_DIS_ECCCHK_WRO: Disable ECC data correction while reading the Write Data array.
2	RW	INT_CQ_PBO_CTL_DIS_ECCCHK_CLO: Disable ECC data correction while reading the Cache Line Buffer.
3	RW	INT_CQ_PBO_CTL_Reserved_3: Reserved.
4	RW	INT_CQ_PBO_CTL_STRICT_ORDER: Force strict ordering on all outbound processor bus operations. In other words, all operations are sent on the processor bus in the exact order that they are. received on AIB.
5	RW	INT_CQ_PBO_CTL_FORCE_MAX_SCOPE_INTRP: Force the maximum scope on outbound Interrupt commands that is typical for the current system configuration. This applies to the four Interrupt commands. which access the Block Scope Table (Histogram, Poll, Assign, Broadcast).

Bits	SCOM	Field Mnemonic: Description
6	RW	INT_CQ_PBO_CTL_FORCE_VG_SYS_INTRP: Force Vg(sys) scope on outbound Interrupt commands. This applies to the four Interrupt commands which access the Block Scope Table (Histogram, Poll, Assign, Broadcast).
7	RW	INT_CQ_PBO_CTL_DROP_PRI_INTRP: Initial Drop Priority when issuing Interrupt commands. This applies to all five Interrupt commands (Histogram, Poll, Assign, Broadcast, BlkUpdate).
8	RW	INT_CQ_PBO_CTL_DROP_PRI_HPC_READ: Initial Drop Priority when issuing HPC Read commands.
9	RW	INT_CQ_PBO_CTL_DROP_PRI_DMA: Initial Drop Priority for the Read and Write machines.
10:15	RW	INT_CQ_PBO_CTL_DROP_MASK_0_5: Drop Priority Algorithm Mask - Used to adjust the probability of increasing the drop priority when rty_drp CRESP is received. ...
16	RW	INT_CQ_PBO_CTL_SLOW_CMD_RATE: Reduce the maximum master command rate to every other cycle.
17	RW	INT_CQ_PBO_CTL_EN_RANDOM_BACKOFF: Enable the random back-off mechanism of master commands.
18	RW	INT_CQ_PBO_CTL_EN_POLL_BACKOFF: Enable the AckC retry back-off mechanism of master Interrupt commands (Poll-group only). If three consecutive AckC retries occur, then that third. retry (and any subsequent consecutive AckC retry) must incur a random back off of 63-126 cycles prior to retry.
19	RW	INT_CQ_PBO_CTL_Reserved_19: Reserved.
20	WOX	INT_CQ_PBO_CTL_FORCE_ECC_CE: Force a single-shot ECC correctable error on the next cycle that data is written into the selected array. Data bit 0 is flipped.
21	WOX	INT_CQ_PBO_CTL_FORCE_ECC_UE: Force a single-shot ECC uncorrectable error on the next cycle that data is written into the selected array. Data bits 0 and 1 are flipped.
22:23	RW	INT_CQ_PBO_CTL_FORCE_ECC_SEL_0_1: Array selection when forcing ECC errors.
24	RW	INT_CQ_PBO_CTL_DISABLE_INJECT: Disable use of Inject group commands. This is a total disabling of any inject commands. The Inject attribute is ignored on AIB In when receiving. cmds from VC/PC, and I ignore any combined response direction to convert to an inject group command.
25	RW	INT_CQ_PBO_CTL_FORCE_CL_INJECT: Force all cache line DMA Writes to be cl_dma_inj, even though VC/PC may not assert the Inject attribute within the AIB command. This bit only. modifies the command as it is received on AIB; a CRESP directing me to change to a non-Inject command is still honored.
26	RW	INT_CQ_PBO_CTL_FORCE_PR_INJECT: Force all partial DMA Writes to be pr_dma_inj, even though VC/PC may not assert the Inject attribute within the AIB command. This bit only modifies. the command as it is received on AIB; a CRESP directing me to change to a non-Inject command is still honored.
27	RW	INT_CQ_PBO_CTL_HANG_ON_ADDR_ERROR: When set to 1, master write machines will hang and preserve their state if they receive an addr_error combined response. This bit has no effect on. master read or master interrupt machines (which will always hang on this condition).
28	RW	INT_CQ_PBO_CTL_HANG_ON_ACK_DEAD: When set to 1, master write machines will hang and preserve their state if they receive an ack_dead combined response. This bit has no effect on. master read or master interrupt machines (which will always hang on this condition).
29	RW	INT_CQ_PBO_CTL_POLL_BCST_RTY_MON: Whenever any master Poll or Broadcast command has received 3+ consecutive retries, then the max_poll_bcast_1(0:4) value is temporarily reduced to the. max_poll_bcast_2(0:4) level until this retry condition no longer exists. This bit controls which types of Poll and Broadcast count consecutive. retries.
30:34	RW	INT_CQ_PBO_CTL_MAX_POLL_BCAST_1_0_4: Maximum number of outstanding master Poll and Broadcast commands. (all types) allowed at any given time.

Bits	SCOM	Field Mnemonic: Description
35:39	RW	INT_CQ_PBO_CTL_MAX_POLL_BCAST_2_0_4: Maximum number of outstanding master Poll and Broadcast commands (Group) allowed at any given time. This must be equal to or less than max_poll_bcast_1(0:4).
40:44	RW	INT_CQ_PBO_CTL_MAX_POLL_BCAST_3_0_4: Maximum number of outstanding master Poll and Broadcast commands ("remote" Group) allowed at any given time. This must be equal to or less than max_poll_bcast_2(0:4). The term "remote" has a different meaning depending on the system configuration. A group poll/broadcast is "remote" when: chip_is_group: I am targeting beyond my group of four chips. 4x4 system: I am using Vg scope. 64s system: Never, since the pHyp scope is constrained to 4 chips.
45	RW	INT_CQ_PBO_CTL_DISABLE_NN_RN: Never use Nn or Rn scope while mastering a command on the processor bus. Scope calculations are modified as follows: Nn -> G, Rn -> Vg(0). This bit does not apply to Interrupt commands.
46	RW	INT_CQ_PBO_CTL_DISABLE_VG_NOT_SYS: Disable Vg scope with the exception of Vg(sys). Scope calculation is modified as follows: Vg(x) -> Vg(sys). This bit does not apply to Interrupt commands.
47	RW	INT_CQ_PBO_CTL_DISABLE_G: Never use G scope while mastering a command on the processor bus. Scope calculation is modified as follows: G -> Vg(sys). This bit does not apply to Interrupt commands.
48	RW	INT_CQ_PBO_CTL_DISABLE_LN: Never use Ln scope while mastering a command on the processor bus. Scope calculation is modified as follows: Ln -> G. This bit does not apply to Interrupt commands.
49	RW	INT_CQ_PBO_CTL_SKIP_G: This bit does not disable the use of group scope, it causes P3CQ to modify the progression of scope when the command starts at nodal scope. In other. words, if the scope is currently at Ln or Nn, and if I am instructed to increment the scope (via CRESP or sfstat), then skip G scope, and go straight. to Vg(sys) scope. It is recommended to set this bit to a 1 when chip_is_group. This bit does not apply to Interrupt commands.
50:63	RW	INT_CQ_PBO_CTL_Reserved_50_63: Reserved.

Register Name	AIB Control Register
Mnemonic	INT.INT_CQ.INT_CQ_AIB_CTL
Address	0000000005013022 (SCOM)
Description	Controls various functions relating to the AIB logic.

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_CQ_AIB_CTL_DIS_ECCCHK_AIB_IN: Disable ECC data correction while receiving data on AIB.
1:3	RW	INT_CQ_AIB_CTL_EXTRA_CMD_SPACING_0_2: The AIB arbiter allows a peak command rate of one command every two cycles. The value in this field is added to that minimum spacing of one cycle. With regard to the requirement that "responses" on certain AIB paths be limited to once every four cycles, the value in this field must be greater than two before it will begin to have any effect on such responses. Valid values for this field are 0 - 6.
4:7	RW	INT_CQ_AIB_CTL_EXTRA_DAT_SPACING_0_3: The AIB arbiter allows back-to-back data transfers with zero cycle separation. The value in this field is added to that minimum spacing of zero cycles. Valid values for this field are 0 - 8.
8:11	RW	INT_CQ_AIB_CTL_PC_PRIORITY_LIMIT_0_3: As the AIB arbiter selects between CQ and VC in sending commands to the PC, CQ has top priority. This field specifies the number of consecutive times that VC will lose, after which VC will be given top priority for one command.

Bits	SCOM	Field Mnemonic: Description
12:15	RW	INT_CQ_AIB_CTL_VC_PRIORITY_LIMIT_0_3: As the AIB arbiter selects between CQ and PC in sending commands to VC, CQ has top priority. This field specifies the number of consecutive times that PC will lose, after which PC will be given top priority for one command.
16:19	RW	INT_CQ_AIB_CTL_CQ_PRIORITY_LIMIT_0_3: As the AIB arbiter selects between VC and PC in sending commands to CQ, VC has top priority. This field specifies the number of consecutive times that PC will lose, after which PC will be given top priority for one command.
20	RW	INT_CQ_AIB_CTL_BLOCK_CMD_OVERLAP: Modify AIB arbitration to block command overlap. Overlap is defined as allowing a command-only operation to begin during the data transfer cycles (except for the last data transfer cycle) of a previous command-data operation; whereas any kind of operation (command-only or command-data) is permitted to begin on the last data transfer cycle of a previous command-data operation. Also, when this bit is a 1, responses that require a minimum four-cycle separation with other responses will not allow any kind of command to begin during the subsequent three dead cycles.
21:31	RW	INT_CQ_AIB_CTL_Reserved_21_31: Reserved.
32:37	RW	INT_CQ_AIB_CTL_CH0_CMD_CREDITS_0_5: Available channel 0 command credits advertised to both PC and VC, for use during outbound write requests (DMA or CI).
38:43	RW	INT_CQ_AIB_CTL_CH1_CMD_CREDITS_0_5: Available channel 1 command credits advertised to both PC and VC, for use during outbound read requests (DMA, CI, or RWITM).
44:49	RW	INT_CQ_AIB_CTL_CH1_DAT_CREDITS_0_5: Available channel 1 data credits advertised to both PC and VC, for use during outbound RWITM.
50:55	RW	INT_CQ_AIB_CTL_CH2_CMD_CREDITS_PC_0_5: Available channel 2 command credits advertised to PC, for use during outbound interrupt requests.
56:61	RW	INT_CQ_AIB_CTL_CH2_CMD_CREDITS_VC_0_5: Available channel 2 command credits advertised to VC, for use during outbound interrupt requests.
62	RW	INT_CQ_AIB_CTL_Reserved_62: Reserved.
63	WOX	INT_CQ_AIB_CTL_REINIT_CREDITS: When this bit is loaded with a 1, CQ re-advertises its credits to PC and VC by asserting the CRD_INIT signals just as is done at POR or a synchronous. reset. This bit auto-resets.

Register Name	Interrupt Unit Reset Control Register
Mnemonic	INT.INT_CQ.INT_CQ_RST_CTL
Address	0000000005013023 (SCOM)
Description	Interrupt Unit Reset Control Register

Bits	SCOM	Field Mnemonic: Description
0	WOX	INT_CQ_RST_CTL_SYNC_RESET: Interrupt unit synchronous reset. This bit auto-resets after 128 cycles.
1	RWX	INT_CQ_RST_CTL_QUIESCE_PB: Quiesce the processor bus in preparation for a warm boot.
2	ROX	INT_CQ_RST_CTL_MASTER_IDLE: Processor bus master (outbound) machines are all idle - the Read, Write and Interrupt machines.
3	ROX	INT_CQ_RST_CTL_SLAVE_IDLE: Processor bus slave (inbound) machines are all idle - the Store and Load machines.
4	WOX	INT_CQ_RST_CTL_PB_BAR_RESET: Processor bus BAR Reset - Writing a 1 to this bit will cause the four BARs (IC_BAR, TM[n]_BAR, PC_BAR, VC_BAR) to be reset to all zeros. This bit auto- resets. The four BARs are not affected by the normal synchronous reset (see bit 0), and thus this bit gives software the flexibility to either reset. or preserve the BAR contents when resetting the Interrupt unit.
5:7	WOX	INT_CQ_RST_CTL_Reserved_5_7: Reserved.

Bits	SCOM	Field Mnemonic: Description
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	CI Store Queue Configuration 1 Register
Mnemonic	INT.INT_CQ.INT_CQ_CFG_STQ1
Address	0000000005013024 (SCOM)
Description	Configuration settings for the CI Store Queue.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INT_CQ_CFG_STQ1_STQ_IPI_MIN_0_4: Number of dedicated CI Store machines for IPI interrupt triggers.
5:9	RW	INT_CQ_CFG_STQ1_STQ_IPI_MAX_0_4: Max allowed CI Store machines for IPI interrupt triggers.
10:14	RW	INT_CQ_CFG_STQ1_STQ_HW_MIN_0_4: Number of dedicated CI Store machines for HW interrupt triggers.
15:19	RW	INT_CQ_CFG_STQ1_STQ_HW_MAX_0_4: Max allowed CI Store machines for HW interrupt triggers.
20:24	RW	INT_CQ_CFG_STQ1_STQ_OS_MIN_0_4: Number of dedicated CI Store machines for OS level escalation.
25:29	RW	INT_CQ_CFG_STQ1_STQ_OS_MAX_0_4: Max allowed CI Store machines for OS level escalation.
30:34	RW	INT_CQ_CFG_STQ1_STQ_HYP_MIN_0_4: Number of dedicated CI Store machines for Hyp level escalation.
35:39	RW	INT_CQ_CFG_STQ1_STQ_HYP_MAX_0_4: Max allowed CI Store machines for Hyp level escalation.
40:44	RW	INT_CQ_CFG_STQ1_STQ_RDI_MIN_0_4: Number of dedicated CI Store machines for Redistribution triggers.
45:49	RW	INT_CQ_CFG_STQ1_STQ_RDI_MAX_0_4: Max allowed CI Store machines for Redistribution triggers.
50:54	RW	INT_CQ_CFG_STQ1_STQ_THR_MIN_0_4: Number of dedicated CI Store machines for Thread Mgmt accesses.
55:59	RW	INT_CQ_CFG_STQ1_STQ_THR_MAX_0_4: Max allowed CI Store machines for Thread Mgmt accesses.
60:63	RW	INT_CQ_CFG_STQ1_Reserved_60_63: Reserved.

Register Name	CI Store Queue Configuration 2 Register
Mnemonic	INT.INT_CQ.INT_CQ_CFG_STQ2
Address	0000000005013025 (SCOM)
Description	Configuration settings for the CI Store Queue.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INT_CQ_CFG_STQ2_STQ_VPC_MIN_0_4: Number of dedicated CI Store machines for VPC accesses.
5:9	RW	INT_CQ_CFG_STQ2_STQ_VPC_MAX_0_4: Max allowed CI Store machines for VPC accesses.
10:14	RW	INT_CQ_CFG_STQ2_STQ_REG_MIN_0_4: Number of dedicated CI Store machines for Internal Reg / LSI trig.
15:19	RW	INT_CQ_CFG_STQ2_STQ_REG_MAX_0_4: Max allowed CI Store machines for Internal Reg / LSI trig.
20:31	RW	INT_CQ_CFG_STQ2_Reserved_20_31: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CI Load Queue Configuration Register
Mnemonic	INT.INT_CQ.INT_CQ_CFG_LDQ
Address	0000000005013026 (SCOM)
Description	Configuration settings for the CI Load Queue.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INT_CQ_CFG_LDQ_LDQ_IVE_MIN_0_4: Number of dedicated CI Load machines for IVE SB EOI.
5:9	RW	INT_CQ_CFG_LDQ_LDQ_IVE_MAX_0_4: Max allowed CI Load machines for IVE SB EOI.
10:14	RW	INT_CQ_CFG_LDQ_LDQ_EQD_MIN_0_4: Number of dedicated CI Load machines for EQD SB EOI.
15:19	RW	INT_CQ_CFG_LDQ_LDQ_EQD_MAX_0_4: Max allowed CI Load machines for EDQ SB EOI.
20:24	RW	INT_CQ_CFG_LDQ_LDQ_THR_MIN_0_4: Number of dedicated CI Load machines for Thread Mgmt accesses.
25:29	RW	INT_CQ_CFG_LDQ_LDQ_THR_MAX_0_4: Max allowed CI Load machines for Thread Mgmt accesses.
30:34	RW	INT_CQ_CFG_LDQ_LDQ_VPC_MIN_0_4: Number of dedicated CI Load machines for VPC accesses.
35:39	RW	INT_CQ_CFG_LDQ_LDQ_VPC_MAX_0_4: Max allowed CI Load machines for VPC accesses.
40:44	RW	INT_CQ_CFG_LDQ_LDQ_REG_MIN_0_4: Number of dedicated CI Load machines for Internal Reg / LSI EOI.
45:49	RW	INT_CQ_CFG_LDQ_LDQ_REG_MAX_0_4: Max allowed CI Load machines for Internal Reg / LSI EOI.
50	RW	INT_CQ_CFG_LDQ_LDQ_REG_ORDER_ALL: Force the CI Load response for accesses to internal registers to be ordered behind all previous CI Stores.
51:63	RW	INT_CQ_CFG_LDQ_Reserved_51_63: Reserved.

Register Name	Performance Counter Control
Mnemonic	INT.INT_CQ.INT_CQ_PM_CTL
Address	0000000005013027 (SCOM)
Description	Controls the behavior of the eight common performance counters within the INT unit.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INT_CQ_PM_CTL_ENABLE_0_7: Enable / Freeze individual counters 0-7. 0 = Freeze (or hold) current counter value. 1 = Enable counter to increment.
8:15	WOX	INT_CQ_PM_CTL_RESET_0_7: Reset individual counters 0-7 (non-persistent). Can be done anytime (for example, simultaneous with enabling counter).
16:17	RW	INT_CQ_PM_CTL_SOURCE_SUBUNIT_0_1: Sub-unit selection to increment the counters. 0 = (none, all zeros). 1 = PC events. 2 = VC events. 3 = CQ events.
18:22	RW	INT_CQ_PM_CTL_CQ_GROUP_SEL_0_4: CQ group select - The decode of these 5-bits selects one of 32 8-bit groups to be used as the "CQ events" for both the internal performance counters. (controlled by this register) and the external common nest performance monitor logic (see INT_CQ_CNPM_SEL).
23:63	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	Performance Counter 0 Register
Mnemonic	INT.INT_CQ.INT_CQ_PMC_0
Address	0000000005013028 (SCOM)
Description	Performance Counter 0 Register. CQ contains a common set of eight performance counters that can be utilized by all components of INT (VC, PC and CQ). Both VC and PC send a group of counter increment signals to CQ, which CQ merges to form the final increment signal for each counter. Each counter has the following characteristics: - 48-bits wide (39 hours to hit the maximum value when counting all cycles) - Enabled / disabled / reset functions are all under software control (see PM_CTL) - All counters freeze their current value if any counter reaches all 1s

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	ROX	INT_CQ_PMC_0_COUNT_0_47: Performance counter contents.

Register Name	Performance Counter 1 Register
Mnemonic	INT.INT_CQ.INT_CQ_PMC_1
Address	0000000005013029 (SCOM)
Description	CQ contains a common set of eight performance counters that can be utilized by all components of INT (VC, PC and CQ). Both VC and PC send a group of counter increment signals to CQ, which CQ merges to form the final increment signal for each counter. Each counter has the following characteristics: - 48-bits wide (39 hours to hit maximum value when counting all cycles) - Enabled / Disabled / Reset functions are all under software control (see PM_CTL) - All counters freeze their current value if any counter reaches all 1s

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	ROX	INT_CQ_PMC_1_COUNT_0_47: Performance counter contents.

Register Name	Performance Counter 2 Register
Mnemonic	INT.INT_CQ.INT_CQ_PMC_2
Address	000000000501302A (SCOM)
Description	CQ contains a common set of eight performance counters that can be utilized by all components of INT (VC, PC and CQ). Both VC and PC send a group of counter increment signals to CQ, which CQ merges to form the final increment signal for each counter. Each counter has the following characteristics: - 48-bits wide (39 hours to hit maximum value when counting all cycles) - Enabled / Disabled / Reset functions are all under software control (see PM_CTL) - All counters freeze their current value if any counter reaches all 1s

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	ROX	INT_CQ_PMC_2_COUNT_0_47: Performance counter contents.

Register Name	Performance Counter 3 Register
Mnemonic	INT.INT_CQ.INT_CQ_PMC_3
Address	000000000501302B (SCOM)
Description	CQ contains a common set of eight performance counters that can be utilized by all components of INT (VC, PC and CQ). Both VC and PC send a group of counter increment signals to CQ, which CQ merges to form the final increment signal for each counter. Each counter has the following characteristics: - 48-bits wide (39 hours to hit maximum value when counting all cycles) - Enabled / Disabled / Reset functions are all under software control (see PM_CTL) - All counters freeze their current value if any counter reaches all 1s

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	ROX	INT_CQ_PMC_3_COUNT_0_47: Performance counter contents.

Register Name	Performance Counter 4 Register
Mnemonic	INT.INT_CQ.INT_CQ_PMC_4
Address	000000000501302C (SCOM)
Description	CQ contains a common set of eight performance counters that can be utilized by all components of INT (VC, PC and CQ). Both VC and PC send a group of counter increment signals to CQ, which CQ merges to form the final increment signal for each counter. Each counter has the following characteristics: - 48-bits wide (39 hours to hit maximum value when counting all cycles) - Enabled / Disabled / Reset functions are all under software control (see PM_CTL) - All counters freeze their current value if any counter reaches all 1s

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	ROX	INT_CQ_PMC_4_COUNT_0_47: Performance counter contents.

Register Name	Performance Counter 5 Register
Mnemonic	INT.INT_CQ.INT_CQ_PMC_5
Address	000000000501302D (SCOM)
Description	CQ contains a common set of eight performance counters that can be utilized by all components of INT (VC, PC and CQ). Both VC and PC send a group of counter increment signals to CQ, which CQ merges to form the final increment signal for each counter. Each counter has the following characteristics: - 48-bits wide (39 hours to hit maximum value when counting all cycles) - Enabled / Disabled / Reset functions are all under software control (see PM_CTL) - All counters freeze their current value if any counter reaches all 1s

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	ROX	INT_CQ_PMC_5_COUNT_0_47: Performance counter contents.

Register Name	Performance Counter 6 Register
Mnemonic	INT.INT_CQ.INT_CQ_PMC_6
Address	000000000501302E (SCOM)
Description	CQ contains a common set of eight performance counters that can be utilized by all components of INT (VC, PC and CQ). Both VC and PC send a group of counter increment signals to CQ, which CQ merges to form the final increment signal for each counter. Each counter has the following characteristics: - 48-bits wide (39 hours to hit maximum value when counting all cycles) - Enabled / Disabled / Reset functions are all under software control (see PM_CTL) - All counters freeze their current value if any counter reaches all 1s

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	ROX	INT_CQ_PMC_6_COUNT_0_47: Performance counter contents.

Register Name	Performance Counter 7 Register
Mnemonic	INT.INT_CQ.INT_CQ_PMC_7
Address	000000000501302F (SCOM)
Description	CQ contains a common set of eight performance counters that can be utilized by all components of INT (VC, PC and CQ). Both VC and PC send a group of counter increment signals to CQ, which CQ merges to form the final increment signal for each counter. Each counter has the following characteristics: - 48-bits wide (39 hours to hit maximum value when counting all cycles) - Enabled / Disabled / Reset functions are all under software control (see PM_CTL) - All counters freeze their current value if any counter reaches all 1s

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	ROX	INT_CQ_PMC_7_COUNT_0_47: Performance counter contents.

Register Name	INT CQ FIR Register
Mnemonic	INT.INT_CQ.INT_CQ_FIR
Address	0000000005013030 (SCOM) 0000000005013031 (SCOM1) 0000000005013032 (SCOM2)
Description	Primary Error Register for INT_CQ. This contains all of the individual errors detected by INT_CQ, plus summary error indicators from VC and PC (see bits 49:63).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PI_ECC_CE: Correctable ECC error detected while consuming data from the processor bus data ramp. See INT_CQ_ERR_INFO2 for details. Recoverable error.
1	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PI_ECC_UE: Uncorrectable ECC error detected while consuming data from the processor bus data ramp. See INT_CQ_ERR_INFO2 for details. Fatal error.
2	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PI_ECC_SUE: Special uncorrectable ECC error detected while consuming data from the processor bus data ramp. Fatal error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_ST_ECC_CE: Correctable ECC error detected while reading the CI Store Data Array. See INT_CQ_ERR_INFO2 for details. Recoverable error.
4	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_ST_ECC_UE: Uncorrectable ECC error detected while reading the CI Store Data Array. See INT_CQ_ERR_INFO2 for details. Fatal error.
5	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_LD_ECC_CE: Correctable ECC error detected while reading the CI Load Data Array. See INT_CQ_ERR_INFO2 for details. Recoverable error.
6	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_LD_ECC_UE: Uncorrectable ECC error detected while reading the CI Load Data Array. See INT_CQ_ERR_INFO2 for details. Fatal error.
7	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_CL_ECC_CE: Correctable ECC error detected while reading the Cache Line Buffer. See INT_CQ_ERR_INFO2 for details. Recoverable error.
8	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_CL_ECC_UE: Uncorrectable ECC error detected while reading the Cache Line Buffer. See INT_CQ_ERR_INFO2 for details. Fatal error.
9	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_WR_ECC_CE: Correctable ECC error detected while reading the DMA Write Data Array. See INT_CQ_ERR_INFO2 for details. Recoverable error.
10	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_WR_ECC_UE: Uncorrectable ECC error detected while reading the DMA Write Data Array. See INT_CQ_ERR_INFO2 for details. Fatal error.
11	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_RD_ECC_CE: Correctable ECC error detected while reading the DMA Read Data Array. See INT_CQ_ERR_INFO2 for details. Recoverable error.
12	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_RD_ECC_UE: Uncorrectable ECC error detected while reading the DMA Read Data Array. See INT_CQ_ERR_INFO2 for details. Fatal error.
13	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_AI_ECC_CE: Correctable ECC error detected while consuming data on the AIB Data Bus. See INT_CQ_ERR_INFO2 for details. Recoverable error.
14	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_AI_ECC_UE: Uncorrectable ECC error detected while consuming data on the AIB Data Bus. See INT_CQ_ERR_INFO2 for details. Fatal error.
15	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_AIB_IN_CMD_CTL_PERR: Parity error detected on AIB Command Control. Fatal error.
16	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_AIB_IN_CMD_PERR: Parity error detected on AIB Command Bus. Fatal error.
17	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_AIB_IN_DAT_CTL_PERR: Parity error detected on AIB Data Control. Fatal error.
18	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PB_PARITY_ERROR: Parity error detected on one of the following processor bus interfaces (RCMDx, cRespx, Data RTAG). See INT_CQ_ERR_INFO0 for details. Fatal error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
19	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PB_RCMDX_CI_ERR1: Slave CI Store or CI Load to an improper location. See INT_CQ_ERR_INFO1 for details. Fatal error.
20	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PB_RCMDX_CI_ERR2: Slave CI Store or CI Load to an invalid domain table entry. See INT_CQ_ERR_INFO1 for details. Fatal error.
21	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PB_RCMDX_CI_ERR3: Slave CI Store or CI Load with an unsupported tsize for the specific category selected, or the starting address is not byte aligned based on the. transfer size specified. See INT_CQ_ERR_INFO1 for details. Fatal error.
22	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_RCVD_POISONED_CIST_DATA: Poisoned data received during a slave CI store operation. Recoverable error.
23	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_MRT_ERR_NOT_VALID: Migration Register Table (MRT) access - invalid entry selected. When this error occurs, the operation proceeds as if it was not a migration operation. - Fatal error --
24	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_MRT_ERR_PSIZE: Migration Register Table (MRT) access - The Table Size received in the AIB command is greater than the Target Page Size in the MRT entry. This error detection is done "on the side," and its occurrence has no effect on the flow of the DMA operation. - Fatal error --
25	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_SCOM_S_ERR: SCOM satellite error. - Fatal error --
26	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_TCTXT_PRESP_ERROR: pResp received from TCTXT but it was not expected, or I expected a pResp from TCTXT but it was not received. - Fatal error --
27	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_WRQ_OP_HANG: Master Write Queue has flagged a processor bus operational hang. - Recoverable error --
28	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_RDQ_OP_HANG: Master Read Queue has flagged a processor bus operational hang. - Recoverable error --
29	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_INTQ_OP_HANG: Master Interrupt Queue has flagged a processor bus operational hang. - Recoverable error --
30	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_RDQ_DATA_HANG: Master Read Queue has flagged a processor bus data hang. - Recoverable error --
31	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_STQ_DATA_HANG: CI Store Queue has flagged a processor bus data hang. - Recoverable error --

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
32	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_LDQ_DATA_HANG: CI Load Queue has flagged an AIB data hang - Once a CI Load request has been sent on AIB, you can use the processor bus data hang timer mechanism (the.rpt_hang.data cmd) as a timer tick while waiting for the data response on AIB. - Recoverable error --
33	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_WRQ_BAD_CRESP: Bad CRESP received during a Master Write command. This means CRESP = addr_error or CRESP = ack_dead. - Fatal error --
34	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_RDQ_BAD_CRESP: Bad CRESP received during a Master Read command. This means CRESP = addr_error, CRESP = ack_dead or CRESP = ack_ed_dead. In addition, for Read Group command, this includes a CRESP of {go_me_ed, go_me_lpc, go_mu_ed, go_me_cond_ed, go_mu_cond_ed}. - Fatal error --
35	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_INTQ_BAD_CRESP: Bad CRESP received during a Master Interrupt command. For the Poll-group interrupt commands (Poll, Assign, Broadcast), this is caused by either CRESP = poll_error, or by a consistency check fail where the. cResp and ATAG values do not agree with each other. For the Ack-group interrupt commands (Histogram, Block Update), this is caused by CRESP = addr_error or CRESP = ack_dead. - Fatal error --
36	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_BAD_128K_VP_OP: An interrupt command is received on AIB while "128K VP mode" is enabled, but the upper two bits of the Block Offset are non-zero. - Fatal error --
37	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_RDQ_ABORT_OP: A processor bus abort_op received that matches an outbound Read machine that is waiting for data. - Informational error --
38	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PC_CRD_PERR: Parity error detected on AIB credit signals from PC. - Fatal error --
39	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PC_CRD_AVAIL_PERR: Parity error detected on AIB credit available signals from PC. - Fatal error --
40	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_VC_CRD_PERR: Parity error detected on AIB credit signals from VC. - Fatal error --
41	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_VC_CRD_AVAIL_PERR: Parity error detected on AIB credit available signals from VC. - Fatal error --
42	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_CMD_QX_SEVERE_ERR: Command Queue (FSM) severe error summary. See INT_CQ_ERR_INFO3 for details. This includes queue overflows and FSM parity errors. - Fatal error --
43	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_RDQ_ABORT_TRM: A Master Read machine received CRESP of abort_trm or abort_trm_ed. In addition to setting this error bit, the Read machine behaved as if the CRESP was. rty. - Recoverable error --

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
44	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_UNSOLICITED_CRESP: Received an unsolicited master Combined Response - The master CRESP TTAG(0:14) matched my topology ID, but TTAG(15:21) pointed to TxIDs associated. with slave machines or to master machines that either do not exist or which are not expecting a CRESP. - Fatal error --
45	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_UNSOLICITED_PBDATA: Received unsolicited processor bus data - The RTAG(0:14) of incoming PB data matched my topology ID, but RTAG(15:21) pointed to TxIDs that never receive. data or to machines which receive data but which are not expecting any data. - Fatal error --
46	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_FIR_PARITY_ERR: The Local Error Module (c_local_fir) asserted it parity error output. - Fatal error --
47	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PGM_DBG_ACCESS: An inbound CI Read or CI Write targeted either of the two INT_CQ_PGM_DBG[n] registers. - Informational error --
48	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_Reserved_48: Reserved.
49:51	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PC_FATAL_ERROR_0_2: PC fatal error summary, as indicated on pc_cq_fatal_error(0:2).
52:54	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PC_RECOV_ERROR_0_2: PC recoverable error summary, as indicated on pc_cq_recov_error(0:2).
55:57	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_PC_INFO_ERROR_0_2: PC informational error summary, as indicated on pc_cq_info_error(0:2).
58:59	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_VC_FATAL_ERROR_0_1: VC fatal error summary, as indicated on vc_cq_fatal_error(0:1). For bit 58, look next at the INT_VC_FATAL_ERR_G0 register. For bit 59, look next at the INT_VC_FATAL_ERR_G1 register.
60:61	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_VC_RECOV_ERROR_0_1: VC recoverable error summary, as indicated on vc_cq_recov_error(0:1). For bit 60, look next at the INT_VC_RECOV_ERR_G0 register. For bit 61, look next at the INT_VC_RECOV_ERR_G1 register.
62:63	RWX	WOX_AND	WOX_OR	INT_CQ_FIR_VC_INFO_ERROR_0_1: VC informational error summary, as indicated on vc_cq_info_error(0:1). For bit 62, look next at the INT_VC_INFO_ERR_G0 register. For bit 63, look next at the INT_VC_INFO_ERR_G1 register.

Register Name	**INT CQ FIR Mask Register**
Mnemonic	INT.INT_CQ.INT_CQ_FIRMASK
Address	0000000005013033 (SCOM) 0000000005013034 (SCOM1) 0000000005013035 (SCOM2)
Description	This register allow software the ability to mask off individual FIR bits.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RW	WO_AND	WO_OR	INT_CQ_FIRMASK_FIR_MASK: A mask register for INT_CQ_FIR.

Register Name	INT CQ Action 0 Register
Mnemonic	INT.INT_CQ.INT_CQ_ACTION0
Address	0000000005013036 (SCOM)
Description	This register, in conjunction with the Action 1 register, defines how errors are reported. These two vectors are used pairwise to select: 00 = Checkstop error 01 = Recoverable error 10 = Recoverable interrupt 11 = Reserved, nothing reported The Action registers only look at unmasked error bits. In other words, the sequence of observation is: FIR -> FIR_MASK -> ACTION -> Output error pins.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	INT_CQ_ACTION0_ACTION0: Action 0 register.

Register Name	INT CQ Action 1 Register
Mnemonic	INT.INT_CQ.INT_CQ_ACTION1
Address	0000000005013037 (SCOM)
Description	This register, in conjunction with the Action 0 register, defines how errors are reported. These two vectors are used pairwise to select: 00 = Checkstop error 01 = Recoverable error 10 = Recoverable interrupt 11 = Reserved, nothing reported The Action registers only look at unmasked error bits. In other words, the sequence of observation is: FIR -> FIR_MASK -> ACTION -> Output error pins.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	INT_CQ_ACTION1_ACTION1: Action 1 register.

Register Name	CQ Error Hold Out Register
Mnemonic	INT.INT_CQ.INT_CQ_ERR_RPT_HOLD
Address	0000000005013039 (SCOM)
Description	This register presents the error_hold output of CQs c_err_rpt macro. Reading this register resets the hold latches within the c_err_rpt.

Bits	SCOM	Field Mnemonic: Description
0:48	ROX	INT_CQ_ERR_RPT_HOLD_ERR_HOLD_0_48: This is the output of the c_err_rpt macro within CQ. The unlatched error outputs of the c_err_rpt feed the c_local_fir. When this register is read. by software, that action will cause the hold latches in the c_err_rpt to be reset.
49:63	RO	Constant = 0b000000000000000

Register Name	Error Information 0 Register
Mnemonic	INT.INT_CQ.INT_CQ_ERR_INFO0
Address	000000000501303A (SCOM)
Description	This register contains details relating to all processor bus parity errors (FIR bit 18). This information is captured when the first applicable error occurs, and will be held until reset by software. Writing this register with any data will clear the whole register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	INT_CQ_ERR_INFO0_INFO_CAPTURED: A 1 indicates that an error has occurred, information has been captured, and the contents below are valid.
1	RWX_WCLRPART	INT_CQ_ERR_INFO0_RCMD0_ADDR_PERR: RCMD0 Address Parity Error.
2	RWX_WCLRPART	INT_CQ_ERR_INFO0_RCMD1_ADDR_PERR: RCMD1 Address Parity Error.
3	RWX_WCLRPART	INT_CQ_ERR_INFO0_RCMD2_ADDR_PERR: RCMD2 Address Parity Error.
4	RWX_WCLRPART	INT_CQ_ERR_INFO0_RCMD3_ADDR_PERR: RCMD3 Address Parity Error.
5	RWX_WCLRPART	INT_CQ_ERR_INFO0_RCMD0_TTAG_PERR: RCMD0 TTAG Parity Error.
6	RWX_WCLRPART	INT_CQ_ERR_INFO0_RCMD1_TTAG_PERR: RCMD1 TTAG Parity Error.
7	RWX_WCLRPART	INT_CQ_ERR_INFO0_RCMD2_TTAG_PERR: RCMD2 TTAG Parity Error.
8	RWX_WCLRPART	INT_CQ_ERR_INFO0_RCMD3_TTAG_PERR: RCMD3 TTAG Parity Error.
9	RWX_WCLRPART	INT_CQ_ERR_INFO0_CR0_TTAG_PERR: cResp0 TTAG Parity Error.
10	RWX_WCLRPART	INT_CQ_ERR_INFO0_CR1_TTAG_PERR: cResp1 TTAG Parity Error.
11	RWX_WCLRPART	INT_CQ_ERR_INFO0_CR2_TTAG_PERR: cResp2 TTAG Parity Error.
12	RWX_WCLRPART	INT_CQ_ERR_INFO0_CR3_TTAG_PERR: cResp3 TTAG Parity Error.
13	RWX_WCLRPART	INT_CQ_ERR_INFO0_CR0_ATAG_PERR: cResp0 ATAG Parity Error.
14	RWX_WCLRPART	INT_CQ_ERR_INFO0_CR1_ATAG_PERR: cResp1 ATAG Parity Error.
15	RWX_WCLRPART	INT_CQ_ERR_INFO0_CR2_ATAG_PERR: cResp2 ATAG Parity Error.
16	RWX_WCLRPART	INT_CQ_ERR_INFO0_CR3_ATAG_PERR: cResp3 ATAG Parity Error.
17	RWX_WCLRPART	INT_CQ_ERR_INFO0_RTAG_PERR: Data In Routing Tag Parity Error.
18:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	Error Information 1 Register
Mnemonic	INT.INT_CQ.INT_CQ_ERR_INFO1
Address	000000000501303B (SCOM)
Description	This register contains details relating to CI Store/Load errors (FIR bits 19, 20, 21). This information is captured when the first applicable error occurs, and will be held until reset by software. Writing this register with any data will clear the whole register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	INT_CQ_ERR_INFO1_INFO_CAPTURED: A 1 indicates that an error has occurred, information has been captured, and the contents below are valid.
1	RWX_WCLRPART	INT_CQ_ERR_INFO1_CI_WRITE: The offending PB command was a CI Write.
2	RWX_WCLRPART	INT_CQ_ERR_INFO1_CI_READ: The offending PB command was a CI Read.
3	RWX_WCLRPART	INT_CQ_ERR_INFO1_DMA_WRITE: The offending PB command was a DMA Write (aka IPI trigger).
4:6	RWX_WCLRPART	INT_CQ_ERR_INFO1_TSIZE_4_6: The 3-bit size field of a CI Write or CI Read.
7:10	RWX_WCLRPART	INT_CQ_ERR_INFO1_BAR_VEC_0_3: BAR compare vector (0:3). bit 0 = PB address matched the IC BAR. bit 1 = PB address matched the TM BAR. bit 2 = PB address matched the PC BAR. bit 3 = PB address matched the VC BAR.
11:27	RWX_WCLRPART	INT_CQ_ERR_INFO1_TTAG_0_16: The processor bus TTAG (0:16) of the offending command. bits 0:3 = Group ID of the master. bits 4:6 = Chip ID of the master. bits 7:16 = Unit ID of the master.
28:63	RWX_WCLRPART	INT_CQ_ERR_INFO1_ADDRESS_28_63: The processor bus Address (28:63) of the offending command.

Register Name	Error Information 2 Register
Mnemonic	INT.INT_CQ.INT_CQ_ERR_INFO2
Address	000000000501303C (SCOM)
Description	This register contains details relating to correctable and uncorrectable ECC errors (FIR 0, 1, 3-14). Here are the seven sources of ECC errors and the information that is captured for each one: PB Data In - (Hi, Lo, Syndrome hi, Syndrome lo) CI Store Data Array - (Lo, Read address, Syndrome lo) CI Load Data Array - (Hi, Lo, Syndrome hi, Syndrome lo) DMA Read Data Array - (Hi, Lo, Read address, Syndrome hi, Syndrome lo) DMA Write Data Array - (Hi, Lo, Read address, Syndrome hi, Syndrome lo) CL Buffer Array - (Hi, Lo, Read address, Syndrome hi, Syndrome lo) AIB Data In - (Hi, Lo, Syndrome hi, Syndrome lo) This information is captured when the first applicable error occurs, and will be held until reset by software. Writing this register with any data will clear the whole register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	INT_CQ_ERR_INFO2_INFO_CAPTURED: A 1 indicates that an error has occurred, information has been captured, and the contents within the fields below are valid.
1:5	RWX_WCLRPART	INT_CQ_ERR_INFO2_Reserved_1_5: Reserved.
6	RWX_WCLRPART	INT_CQ_ERR_INFO2_HI: Error occurred on the high 8 bytes of data.

Bits	SCOM	Field Mnemonic: Description
7	RWX_WCLRPART	INT_CQ_ERR_INFO2_LO: Error occurred on the low 8 bytes of data.
8:15	RWX_WCLRPART	INT_CQ_ERR_INFO2_RD_ADDR_0_7: For errors involved with reading an SRAM, this field contains the Read Address of the SRAM.
16:23	RWX_WCLRPART	INT_CQ_ERR_INFO2_SYN_HI_0_7: The syndrome of the high 8 bytes.
24:31	RWX_WCLRPART	INT_CQ_ERR_INFO2_SYN_LO_0_7: The syndrome of the low 8 bytes.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Error Information 3 Register
Mnemonic	INT.INT_CQ.INT_CQ_ERR_INFO3
Address	000000000501303D (SCOM)
Description	This register contains details relating to Command Queue (or FSM) severe errors (FIR bit 42). This information is captured when the first applicable error occurs, and will be held until reset by software. Writing this register with any data will clear the whole register.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRPART	INT_CQ_ERR_INFO3_INFO_CAPTURED: A 1 indicates that an error has occurred, information has been captured, and the contents below are valid.
1	RWX_WCLRPART	INT_CQ_ERR_INFO3_STQ_FSM_PERR: Slave CI Store Queue - FSM Parity Error.
2	RWX_WCLRPART	INT_CQ_ERR_INFO3_LDQ_FSM_PERR: Slave CI Load Queue - FSM Parity Error.
3	RWX_WCLRPART	INT_CQ_ERR_INFO3_WRQ_FSM_PERR: Master Write Queue - FSM Parity Error.
4	RWX_WCLRPART	INT_CQ_ERR_INFO3_RDQ_FSM_PERR: Master Read Queue - FSM Parity Error.
5	RWX_WCLRPART	INT_CQ_ERR_INFO3_INTQ_FSM_PERR: Master Interrupt Queue - FSM Parity Error.
6	RWX_WCLRPART	INT_CQ_ERR_INFO3_WRQ_OVERFLOW: Master Write Queue Overflow.
7	RWX_WCLRPART	INT_CQ_ERR_INFO3_RDQ_OVERFLOW: Master Read Queue Overflow.
8	RWX_WCLRPART	INT_CQ_ERR_INFO3_INTQ_OVERFLOW: Master Interrupt Queue Overflow.
9:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	TCTXT Configuration Register
Mnemonic	INT.INT_PC.INT_TCTXT_CFG
Address	0000000005013100 (SCOM)
Description	Thread context configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_TCTXT_CFG_CFG_BLOCK_GROUP_EN: Enables block grouping.

Bits	SCOM	Field Mnemonic: Description
1	RW	INT_TCTXT_CFG_CFG_TARGET_EN: Enables Hypervisor target mode support.
2	RW	INT_TCTXT_CFG_Reserved_2: Spare.
3	RW	INT_TCTXT_CFG_CFG_ACM_EN: Enables ACM support.
4	RW	INT_TCTXT_CFG_CFG_FUSE_CORE_EN: Enables Fused core mode (for LSI and MsgSnd broadcast notify selection).
5	RW	INT_TCTXT_CFG_Reserved_5: Spare.
6:7	RW	INT_TCTXT_CFG_CFG_SMT_MODE: Configures the core MST mode (only used for clockgating). "00": ST. "01": SMT2. "10": SMT4. "11": SMT8 (default, no additional clockgating).
8	RW	INT_TCTXT_CFG_CFG_HARD_CHIPID_IN_BLOCK_EN: Moves the chipid into block field for hardwired CAM compares. Block offset value is adjusted to 0b0..01 and ThrdId.
9	RW	INT_TCTXT_CFG_CFG_CHIPID_OVERRIDE: Overrides hardwired chip ID with the chip ID field (bits12:15).
10:11	RW	INT_TCTXT_CFG_Reserved_10_11: Spare.
12:15	RW	INT_TCTXT_CFG_CFG_CHIPID: Chip ID for thread context thas is applied as override.
16	RW	INT_TCTXT_CFG_CFG_INT_TCTXT_EN: Enables the interrupt lines to the cores (EBB, OS, Hyp).
17	RW	INT_TCTXT_CFG_CFG_INT_MSGSND: Enables the MsgSnd line to the cores.
18:19	RW	INT_TCTXT_CFG_Reserved_18_19: Spare.
20:23	RW	INT_TCTXT_CFG_CFG_INT_PULSE_WIDTH: Configures the length of interrupt pulses (MsgSnd).
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	TCTXT Track Register
Mnemonic	INT.INT_PC.INT_TCTXT_TRACK
Address	0000000005013101 (SCOM)
Description	Thread context block track configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_TCTXT_TRACK_CFG_BLOCK_TRACK_EN: Enables block tracking and exchange of block ownership information between Interrupt controllers.
1:3	RW	INT_TCTXT_TRACK_Reserved_1_3: Spare.
4	RW	INT_TCTXT_TRACK_CFG_BLOCK_FILTER_EN: Enables filtering of incomint Interrupt RCMDs based on the target BlockID such that commands for non-owned blocks are not sent to the thread context. and do not need ro reserve a CRESP CAM entry.
5	RW	INT_TCTXT_TRACK_CFG_BLOCK_FILTER_VPC_EN: Enables block ownership for which the NVT is owned irrespective of whether the blocks are active in any thread context.
6:9	RW	INT_TCTXT_TRACK_Reserved_6_9: Spare.
10:15	RW	INT_TCTXT_TRACK_CFG_BLOCK_RESET_DELAY: Configures the delay after which a block update is triggered once the number of enabled thread contexts using that block ID has reached 0.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Indirect Thread Context Access 0 Register
Mnemonic	INT.INT_PC.INT_TCTXT_INDIR0
Address	0000000005013104 (SCOM)
Description	Indirect thread access register0

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_TCTXT_INDIR0_INDIR_VLD: Indirect access valid.
1:8	RO	Constant = 0b00000000
9:15	RW	INT_TCTXT_INDIR0_INDIR_THRDID: Indirect access thread id.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Indirect Thread Context Access 1 Register
Mnemonic	INT.INT_PC.INT_TCTXT_INDIR1
Address	0000000005013105 (SCOM)
Description	Indirect thread access register0

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_TCTXT_INDIR1_INDIR_VLD: Indirect access valid.
1:8	RO	Constant = 0b00000000
9:15	RW	INT_TCTXT_INDIR1_INDIR_THRDID: Indirect access thread id.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Indirect Thread Context Access 2 Register
Mnemonic	INT.INT_PC.INT_TCTXT_INDIR2
Address	0000000005013106 (SCOM)
Description	Indirect thread access register0

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_TCTXT_INDIR2_INDIR_VLD: Indirect access valid.
1:8	RO	Constant = 0b00000000
9:15	RW	INT_TCTXT_INDIR2_INDIR_THRDID: Indirect access thread id.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Indirect Thread Context Access 3 Register
Mnemonic	INT.INT_PC.INT_TCTXT_INDIR3
Address	0000000005013107 (SCOM)
Description	Indirect thread access register0

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_TCTXT_INDIR3_INDIR_VLD: Indirect access valid.

Bits	SCOM	Field Mnemonic: Description
1:8	RO	Constant = 0b00000000
9:15	RW	INT_TCTXT_INDIR3_INDIR_THRDID: Indirect access thread id.
16:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Physical Thread Enable 0 Register
Mnemonic	INT.INT_PC.INT_TCTXT_EN0
Address	0000000005013108 (SCOM)
Description	Physical Thread Enable register for fused cores 0:7

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INT_TCTXT_EN0_CFG_THRD_C0_EN: Thread enable for fused core 0.
8:15	RW	INT_TCTXT_EN0_CFG_THRD_C1_EN: Thread enable for fused core 1.
16:23	RW	INT_TCTXT_EN0_CFG_THRD_C2_EN: Thread enable for fused core 2.
24:31	RW	INT_TCTXT_EN0_CFG_THRD_C3_EN: Thread enable for fused core 3.
32:39	RW	INT_TCTXT_EN0_CFG_THRD_C4_EN: Thread enable for fused core 4.
40:47	RW	INT_TCTXT_EN0_CFG_THRD_C5_EN: Thread enable for fused core 5.
48:55	RW	INT_TCTXT_EN0_CFG_THRD_C6_EN: Thread enable for fused core 6.
56:63	RW	INT_TCTXT_EN0_CFG_THRD_C7_EN: Thread enable for fused core 7.

Register Name	Physical Thread Enable 1 Register
Mnemonic	INT.INT_PC.INT_TCTXT_EN1
Address	000000000501310C (SCOM)
Description	Physical Thread Enable register for fused cores 8:11

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INT_TCTXT_EN1_CFG_THRD_C8_EN: Thread enable for fused core 8.
8:15	RW	INT_TCTXT_EN1_CFG_THRD_C9_EN: Thread enable for fused core 9.
16:23	RW	INT_TCTXT_EN1_CFG_THRD_C10_EN: Thread enable for fused core 10.
24:31	RW	INT_TCTXT_EN1_CFG_THRD_C11_EN: Thread enable for fused core 11.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	P3PC Global Configuration Register
Mnemonic	INT.INT_PC.INT_PC_GLOBAL_CFG
Address	0000000005013110 (SCOM)
Description	P3VC global configuration register

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Constant = 0b00000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
32	RW	INT_PC_GLOBAL_CFG_INDIRECT_MODE: When set, access to memory structures may be indirect. Software must set this bit if the "i" bit is set in any VSD.
33:39	RW	INT_PC_GLOBAL_CFG_Reserved_33_39: Spare.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	VSD Table Address Register
Mnemonic	INT.INT_PC.INT_PC_VSD_TABLE_ADDR
Address	0000000005013111 (SCOM)
Description	This register along with the VSD table data register allows Software to load VSDs in the ATX BAR SRAM

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_PC_VSD_TABLE_ADDR_AUTO_INCREMENT: When set, each rd/wr access to the BAR data register increments the table_address field once the current operation is completed.
1:3	RW	INT_PC_VSD_TABLE_ADDR_Reserved_1_3: Spare.
4:11	RO	Constant = 0b00000000
12	RW	INT_PC_VSD_TABLE_ADDR_Reserved_12: Spare.
13:15	RW	INT_PC_VSD_TABLE_ADDR_TABLE_SELECT: Table select: "000":IVE. "001": Reserved. "010":EQD. "011":VPD. "1xx":Reserved.
16:23	RO	Constant = 0b00000000
24:26	RW	INT_PC_VSD_TABLE_ADDR_Reserved_24_26: Spare.
27:31	RWX	INT_PC_VSD_TABLE_ADDR_TABLE_ADDRESS: Offset within the selected table. Blockid 0 to 31 if selected table is VPD. Blockid 0 to 15 if selected table is IVE, or EQD.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	IVE Block Mode Register
Mnemonic	INT.INT_PC.INT_PC_IVE_BLOCK_MODE
Address	0000000005013113 (SCOM)
Description	This register holds the mode defined for each ive block. Whenever the Software does a write to ive VSDs in BAR SRAM, the defined mode bits are also copied in this register. This register should never be written except for debug.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	INT_PC_IVE_BLOCK_MODE_IVE_BLOCK_MODE: (2*n:n*2+1) IVE block n. 00invalid, 01shared, 10exclusive, 11forward.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	EQD Block Mode Register
Mnemonic	INT.INT_PC.INT_PC_EQD_BLOCK_MODE
Address	0000000005013114 (SCOM)
Description	This register holds the mode defined for each EQD block. Whenever the Software does a write to EQD VSDs in BAR SRAM, the defined mode bits are also copied in this register. This register should never be written except for debug.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	INT_PC_EQD_BLOCK_MODE_EQD_BLOCK_MODE: (2*n:n*2+1) EQD block n. 00invalid, 01shared, 10exclusive, 11forward.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	VPD Block Mode Register
Mnemonic	INT.INT_PC.INT_PC_VPD_BLOCK_MODE
Address	0000000005013115 (SCOM)
Description	This register holds the mode defined for each VPD block. Whenever the Software does a write to VPD VSDs in BAR SRAM, the defined mode bits are also copied in this register. This register should never be written except for debug.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	INT_PC_VPD_BLOCK_MODE_VPD_BLOCK_MODE: (2*n:n*2+1) VPD block n. 00invalid, 01shared, 10exclusive, 11forward.

Register Name	AT Indirect Kill Register
Mnemonic	INT.INT_PC.INT_PC_AT_KILL
Address	0000000005013116 (SCOM)
Description	This registers, along with kill mask register is used to kill entries in AT CAM.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_PC_AT_KILL_VALID: Valid bit. Set per Software to initiate a kill command. Cleared by hardware when kill command is completed. Software must have written the kill mask. register prior of setting this bit.
1:23	RO	Constant = 0b00000000000000000000000
24:26	RW	INT_PC_AT_KILL_Reserved_24_26: Spare.
27:31	RW	INT_PC_AT_KILL_BLOCKID: 5-bit BlockId.
32:47	RO	Constant = 0b0000000000000000
48:60	RW	INT_PC_AT_KILL_OFFSET: 13-bit offset.
61:63	RW	INT_PC_AT_KILL_Reserved_61_63: Spare.

Register Name	AT Indirect Kill Mask Register
Mnemonic	INT.INT_PC.INT_PC_AT_KILL_MASK
Address	0000000005013117 (SCOM)
Description	This register, along with kill register is used to kill entries in AT CAM. CAM entries are killed if (blockid and blockid_mask) = (cam_blockid and blockid_mask) AND (offset and offset_mask) = (cam_offset and offset_mask)

Bits	SCOM	Field Mnemonic: Description
0:23	RO	Constant = 0b000000000000000000000000
24:26	RW	INT_PC_AT_KILL_MASK_Reserved_24_26: Spare.
27:31	RW	INT_PC_AT_KILL_MASK_BLOCKID: 5-bit BlockId mask.
32:47	RO	Constant = 0b0000000000000000
48:60	RW	INT_PC_AT_KILL_MASK_OFFSET: 13-bit offset mask.
61:63	RW	INT_PC_AT_KILL_MASK_Reserved_61_63: Spare.

Register Name	PCMD Arbiter Register
Mnemonic	INT.INT_PC.INT_PC_PCMD_ARB
Address	0000000005013118 (SCOM)
Description	Pcmd Arbiter Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_PC_PCMD_ARB_Reserved_0: Spare.
1:3	RW	INT_PC_PCMD_ARB_CFG_PCMD_ARB_PRIO_LSI: Priority for LSI requests. 0XX - Use round robin. 100 - Priority 0 (highest). 101 - Priority 1. 110 - Priority 2. 111 - Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
4	RW	INT_PC_PCMD_ARB_Reserved_4: Spare.
5:7	RW	INT_PC_PCMD_ARB_CFG_PCMD_ARB_PRIO_MMIO: Priority for MMIO requests. 0XX - Use round robin. 100 - Priority 0 (highest). 101 - Priority 1. 110 - Priority 2. 111 - Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
8	RW	INT_PC_PCMD_ARB_Reserved_8: Spare.
9:11	RW	INT_PC_PCMD_ARB_CFG_PCMD_ARB_PRIO_VRQ_REQ: Priority for VRQ requests. 0XX - Use round robin. 100 - Priority 0 (highest). 101 - Priority 1. 110 - Priority 2. 111 - Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
12	RW	INT_PC_PCMD_ARB_Reserved_12: Spare.

Bits	SCOM	Field Mnemonic: Description
13:15	RW	INT_PC_PCMD_ARB_CFG_PCMD_ARB_PRIO_VRQ_RSP: Priority for VRQ responses. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
16	RW	INT_PC_PCMD_ARB_Reserved_16: Spare.
17:19	RW	INT_PC_PCMD_ARB_CFG_PCMD_ARB_PRIO_RR: Priority for Round Robin requests/responses. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3. Note: This field must be set to 1XX if any of the PCmd sources are set to use round robin.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	MMIO Arbiter Register
Mnemonic	INT.INT_PC.INT_PC_MMIO_ARB
Address	000000000501311A (SCOM)
Description	MMIO Arbiter Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INT_PC_MMIO_ARB_CFG_MMIO_LDST_ARB_PRIO_SET_LD: Defines arbitration order for MMIO Set operations. 0X: round robin between loads and stores. 10: Ld has priority over St. 11: St has priority over Ld.
2:3	RW	INT_PC_MMIO_ARB_CFG_MMIO_LDST_ARB_PRIO_RSP_LD: Defines arbitration order for MMIO Rsp operations. 0X: round robin between loads and stores. 10: Ld has priority over St. 11: St has priority over Ld.
4:5	RW	INT_PC_MMIO_ARB_Reserved_4_5: Spare.
6:7	RW	INT_PC_MMIO_ARB_CFG_MMIO_DONE_PARSE_PULL_RR_SEL: Enables round robin arbitration for Pull requests among threads within a core (6: Hyp, 7: OS).
8:9	RW	INT_PC_MMIO_ARB_CFG_MMIO_DONE_PARSE_IACK_RR_SEL: Enables round robin arbitration for Store Ack requests among threads within a core (8: Hyp, 9: OS).
10:11	RW	INT_PC_MMIO_ARB_CFG_MMIO_DONE_ARB_PULL_PRIO_HYP: Defines arbitration order for Pull operations. 0X: round robin between Hyp and OS. 10: Hyp has priority over OS. 11: OS has priority over Hyp.
12:13	RW	INT_PC_MMIO_ARB_CFG_MMIO_DONE_ARB_IACK_PRIO_HYP: Defines arbitration order for Store Ack operations. 0X: round robin between Hyp and OS. 10: Hyp has priority over OS. 11: OS has priority over Hyp.

Bits	SCOM	Field Mnemonic: Description
14:15	RW	INT_PC_MMIO_ARB_CFG_MMIO_DONE_ARB_PRIO_IACK: Defines arbitration order between Pull and Store Ack. 0X: round robin between Pull and Store Ack. 10: Store Ack has priority over Pull. 11: Pull has priority over Store Ack.
16	RW	INT_PC_MMIO_ARB_Reserved_16: Spare.
17:19	RW	INT_PC_MMIO_ARB_CFG_MMIO_PCMD_ARB_PRIO_LDST_SET: Priority for MMIO PCmd Ld/St Set operations. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
20	RW	INT_PC_MMIO_ARB_Reserved_20: Spare.
21:23	RW	INT_PC_MMIO_ARB_CFG_MMIO_PCMD_ARB_PRIO_LDST_RSP: Priority for MMIO PCmd Ld/St Rsp operations. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
24	RW	INT_PC_MMIO_ARB_Reserved_24: Spare.
25:27	RW	INT_PC_MMIO_ARB_CFG_MMIO_PCMD_ARB_PRIO_DONE: Priority for MMIO PCmd Done operations. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
28	RW	INT_PC_MMIO_ARB_Reserved_28: Spare.
29:31	RW	INT_PC_MMIO_ARB_CFG_MMIO_PCMD_ARB_PRIO_RR: Priority for Round Robin MMIO PCmd requests. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3. Note: This field must be set to 1XX if any of the MMIO PCmd sources are set to use round robin.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	VRQ Configuration Register
Mnemonic	INT.INT_PC.INT_PC_VRQ_CFG
Address	000000000501311C (SCOM)
Description	VRQ Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_PC_VRQ_CFG_CFG_VRQ_CORE_PUSH_EN: Enables VPD store operations from the cores.
1:2	RW	INT_PC_VRQ_CFG_Reserved_1_2: Spare.

Bits	SCOM	Field Mnemonic: Description
3:7	RW	INT_PC_VRQ_CFG_CFG_VRQ_QUEUE_SIZE_PULL: VRQ TCTXT pull queue size in multiple of 8. needs to be < = 30.
8:10	RW	INT_PC_VRQ_CFG_Reserved_8_10: Spare.
11:15	RW	INT_PC_VRQ_CFG_CFG_VRQ_QUEUE_SIZE_PUSH_LCL: VRQ TCTXT push queue size in multiple of 8. needs to be > VRQ pull queue size and < = 31.
16:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	VRQ Pending Arbiter Register
Mnemonic	INT.INT_PC.INT_PC_VRQ_PEND_ARB
Address	000000000501311D (SCOM)
Description	VRQ Pending Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_PC_VRQ_PEND_ARB_CFG_VRQ_PEND_PARSE_QUERY_RR_SEL: Enables round robin arbitration for Pending Query requests among threads within a core.
1	RW	INT_PC_VRQ_PEND_ARB_Reserved_1: Spare.
2:3	RW	INT_PC_VRQ_PEND_ARB_CFG_VRQ_PEND_PARSE_PULL_RR_SEL: Enables round robin arbitration for Pending Pull requests among threads within a core (2: Hyp, 3: OS).
4:5	RW	INT_PC_VRQ_PEND_ARB_CFG_VRQ_PEND_PARSE_PUSH_RR_SEL: Enables round robin arbitration for Pending Push requests among threads within a core (4: Hyp, 5: OS).
6:7	RW	INT_PC_VRQ_PEND_ARB_Reserved_6_7: Spare.
8:9	RW	INT_PC_VRQ_PEND_ARB_CFG_VRQ_PEND_ARB_PULL_PRIO_HYP: Defines arbitration order for Pending Pull requests. 0X: round robin between Hyp and OS. 10: Hyp has priority over OS. 11: OS has priority over Hyp.
10:11	RW	INT_PC_VRQ_PEND_ARB_CFG_VRQ_PEND_ARB_PUSH_PRIO_HYP: Defines arbitration order for Pending Push requests. 0X: round robin between Hyp and OS. 10: Hyp has priority over OS. 11: OS has priority over Hyp.
12:16	RW	INT_PC_VRQ_PEND_ARB_Reserved_12_16: Spare.
17:19	RW	INT_PC_VRQ_PEND_ARB_CFG_VRQ_PEND_ARB_PRIO_QUERY: Priority for VRQ PCmd Pending Query requests. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
20	RW	INT_PC_VRQ_PEND_ARB_Reserved_20: Spare.
21:23	RW	INT_PC_VRQ_PEND_ARB_CFG_VRQ_PEND_ARB_PRIO_PUSH: Priority for VRQ PCmd Pending Push requests. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.

Bits	SCOM	Field Mnemonic: Description
24	RW	INT_PC_VRQ_PEND_ARB_Reserved_24: Spare.
25:27	RW	INT_PC_VRQ_PEND_ARB_CFG_VRQ_PEND_ARB_PRIO_PULL: Priority for VRQ PCmd Pending Pull requests. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
28	RW	INT_PC_VRQ_PEND_ARB_Reserved_28: Spare.
29:31	RW	INT_PC_VRQ_PEND_ARB_CFG_VRQ_PEND_ARB_PRIO_RR: Priority for Round Robin VRQ PCmd requests. 0XX = Use round robin. 100 = Priority 0 (highest). 101 = Priority 1. 110 = Priority 2. 111 = Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3. Note: This field must be set to 1XX if any of the VRQ PCmd sources are set to use round robin.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	VRQ VPC Credit Register
Mnemonic	INT.INT_PC.INT_PC_VRQ_VPC_CRD
Address	000000000501311E (SCOM)
Description	VRQ Credit Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INT_PC_VRQ_VPC_CRD_Reserved_0_1: Spare.
2:7	RW	INT_PC_VRQ_VPC_CRD_CFG_VRQ_CRD_PULL_RSVD: VPC Pull Local requests Reserved credits.
8:9	RW	INT_PC_VRQ_VPC_CRD_Reserved_8_9: Spare.
10:15	RW	INT_PC_VRQ_VPC_CRD_CFG_VRQ_VPC_CRD_PULL_LMIT: VPC Pull Local requests max outstanding.
16:17	RW	INT_PC_VRQ_VPC_CRD_Reserved_16_17: Spare.
18:23	RW	INT_PC_VRQ_VPC_CRD_CFG_VRQ_VPC_CRD_PUSH_LCL_RSVD: VPC Push Local requests Reserved credits.
24:25	RW	INT_PC_VRQ_VPC_CRD_Reserved_24_25: Spare.
26:31	RW	INT_PC_VRQ_VPC_CRD_CFG_VRQ_VPC_CRD_PUSH_LCL_LMIT: VPC Push Local requests max outstanding.
32:33	RW	INT_PC_VRQ_VPC_CRD_Reserved_32_33: Spare.
34:39	RW	INT_PC_VRQ_VPC_CRD_CFG_VRQ_CRD_PUSH_ARX_RSVD: VPC Push ARX requests Reserved credits.
40:41	RW	INT_PC_VRQ_VPC_CRD_Reserved_40_41: Spare.
42:47	RW	INT_PC_VRQ_VPC_CRD_CFG_VRQ_VPC_CRD_PUSH_ARX_LMIT: VPC Push ARX requests max outstanding.
48:49	RW	INT_PC_VRQ_VPC_CRD_Reserved_48_49: Spare.
50:55	RW	INT_PC_VRQ_VPC_CRD_CFG_VRQ_CRD_MAX: VPC requests using Shared credits max outstanding. Note: The sum of the reserved credit values will be decremented from this field value to determine maximum outstanding for shared credits (for example, 24 - 4 - 4 -4 = 12).

Bits	SCOM	Field Mnemonic: Description
56:63	RO	Constant = 0b00000000

Register Name	VRQ VPC Arbiter Register
Mnemonic	INT.INT_PC.INT_PC_VRQ_VPC_ARB
Address	000000000501311F (SCOM)
Description	VRQ Arbiter Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_PC_VRQ_VPC_ARB_Reserved_0: Spare.
1:3	RW	INT_PC_VRQ_VPC_ARB_CFG_VRQ_ARB_PRIO_RSVD: Priority for VPC requests that can use a Reserved credit. 0XX - Use round robin. 100 - Priority 0 (highest). 101 - Priority 1. 110 - Priority 2. 111 - Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3. Note: Reserved. Should always be set to the highest priority used.
4	RW	INT_PC_VRQ_VPC_ARB_CFG_VRQ_ARB_STALL_PULL: Stall Pull Local arbitration.
5:7	RW	INT_PC_VRQ_VPC_ARB_CFG_VRQ_ARB_PRIO_PULL: Priority for VPC Pull Local requests that can use a shared credit. 0XX - Use round robin. 100 - Priority 0 (highest). 101 - Priority 1. 110 - Priority 2. 111 - Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
8	RW	INT_PC_VRQ_VPC_ARB_CFG_VRQ_ARB_STALL_PUSH_LCL: Stall Push Local arbitration.
9:11	RW	INT_PC_VRQ_VPC_ARB_CFG_VRQ_ARB_PRIO_PUSH_LCL: Priority for VPC Push Local requests that can use a shared credit. 0XX - Use round robin. 100 - Priority 0 (highest). 101 - Priority 1. 110 - Priority 2. 111 - Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
12	RW	INT_PC_VRQ_VPC_ARB_CFG_VRQ_ARB_STALL_PUSH_ARX: Stall Push ARX arbitration.
13:15	RW	INT_PC_VRQ_VPC_ARB_CFG_VRQ_ARB_PRIO_PUSH_ARX: Priority for VPC Push ARX requests that can use a shared credit. 0XX - Use round robin. 100 - Priority 0 (highest). 101 - Priority 1. 110 - Priority 2. 111 - Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3.
16	RW	INT_PC_VRQ_VPC_ARB_Reserved_16: Spare.

Bits	SCOM	Field Mnemonic: Description
17:19	RW	INT_PC_VRQ_VPC_ARB_CFG_VRQ_ARB_PRIO_RR: Priority for Round Robin requests. 0XX - Use round robin. 100 - Priority 0 (highest). 101 - Priority 1. 110 - Priority 2. 111 - Priority 3 (lowest). Note: Max of 1 source can use each of Priority 0-3. Note: This field must be set to 1XX if any of the VRQ sources are set to use round robin.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	AIB RX Credit Initialization Timer Register
Mnemonic	INT.INT_PC.INT_PC_AIB_RX_CRD_INIT
Address	0000000005013120 (SCOM)
Description	AIB credit init timer

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_PC_AIB_RX_CRD_INIT_CRD_INIT_REQUEST: Credit init request. Set by Soft, Cleared by hardware.
1:7	RW	INT_PC_AIB_RX_CRD_INIT_Reserved_1_7: Spare.
8:15	RW	INT_PC_AIB_RX_CRD_INIT_CRD_INIT_TIMER: 8-bit value for credit initialization timer for AIB.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	AIB RX Command Credit Register
Mnemonic	INT.INT_PC.INT_PC_AIB_RX_CRD_CMD
Address	0000000005013121 (SCOM)
Description	AIB max command credit register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INT_PC_AIB_RX_CRD_CMD_Reserved_0_1: Spare.
2:7	RW	INT_PC_AIB_RX_CRD_CMD_PC_AIB_CH0_MAX_CMD_CRD: 6-bit value for initial maximum command credit value for channel 0.
8:9	RW	INT_PC_AIB_RX_CRD_CMD_Reserved_8_9: Spare.
10:15	RW	INT_PC_AIB_RX_CRD_CMD_PC_AIB_CH1_MAX_CMD_CRD: 6-bit value for initial maximum command credit value for channel 1.
16:17	RW	INT_PC_AIB_RX_CRD_CMD_Reserved_16_17: Spare.
18:23	RW	INT_PC_AIB_RX_CRD_CMD_PC_AIB_CH2_MAX_CMD_CRD: 6-bit value for initial maximum command credit value for channel 2.
24:25	RW	INT_PC_AIB_RX_CRD_CMD_Reserved_24_25: Spare.
26:31	RW	INT_PC_AIB_RX_CRD_CMD_PC_AIB_CH3_MAX_CMD_CRD: 6-bit value for initial maximum command credit value for channel 3.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	AIB RX Data Credit Register
Mnemonic	INT.INT_PC.INT_PC_AIB_RX_CRD_DAT
Address	0000000005013122 (SCOM)
Description	AIB max data credit register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INT_PC_AIB_RX_CRD_DAT_Reserved_0_1: Spare.
2:7	RW	INT_PC_AIB_RX_CRD_DAT_PC_AIB_CH0_MAX_DAT_CRD: 6-bit value for initial maximum data credit value for channel 0.
8:9	RW	INT_PC_AIB_RX_CRD_DAT_Reserved_8_9: Spare.
10:15	RW	INT_PC_AIB_RX_CRD_DAT_PC_AIB_CH1_MAX_DAT_CRD: 6-bit value for initial maximum data credit value for channel 1.
16:17	RW	INT_PC_AIB_RX_CRD_DAT_Reserved_16_17: Spare.
18:23	RW	INT_PC_AIB_RX_CRD_DAT_PC_AIB_CH2_MAX_DAT_CRD: 6-bit value for initial maximum data credit value for channel 2.
24:25	RW	INT_PC_AIB_RX_CRD_DAT_Reserved_24_25: Spare.
26:31	RW	INT_PC_AIB_RX_CRD_DAT_PC_AIB_CH3_MAX_DAT_CRD: 6-bit value for initial maximum data credit value for channel 3.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	AIB TX Initial Credit Counters Value Register
Mnemonic	INT.INT_PC.INT_PC_AIB_TX_CRD
Address	0000000005013124 (SCOM)
Description	This register defines the Reserved and pool credits for outbound read and write requests.

Bits	SCOM	Field Mnemonic: Description
0:23	RO	Constant = 0b00000000000000000000000000
24	RWX	INT_PC_AIB_TX_CRD_CRD_INIT_REQUEST: Credit init request. Set by Soft, Cleared by hardware.
25	RW	INT_PC_AIB_TX_CRD_Reserved_25: Spare.
26:27	RW	INT_PC_AIB_TX_CRD_RSD_CRD_DMA_READ: 2-bit Reserved crd count for all DMA reads other than AT macro.
28:29	RW	INT_PC_AIB_TX_CRD_RSD_CRD_VPC_LD_RMT: 2-bit Reserved crd count for VPC remote PC loads.
30:31	RW	INT_PC_AIB_TX_CRD_RSD_CRD_AT_MACRO: 2-bit Reserved crd count for AT macro DMA reads.
32:34	RW	INT_PC_AIB_TX_CRD_Reserved_32_34: Spare.
35:39	RW	INT_PC_AIB_TX_CRD_READ_CRD_POOL: Outbound reads credits pool. (Must = Total number of CQ read machines - Sum (all Reserved read credit counts, PC+VC) (assume 3 Reserved in VC).
40:47	RW	INT_PC_AIB_TX_CRD_Reserved_40_47: Spare.
48:49	RW	INT_PC_AIB_TX_CRD_RSD_CRD_TCTXT_WRITE: 2-bit Reserved crd count for all TCTXT DMA Writes.
50:51	RW	INT_PC_AIB_TX_CRD_Reserved_50_51: Spare.
52:53	RW	INT_PC_AIB_TX_CRD_RSD_CRD_DMA_WRITE: 2-bit Reserved crd count for all DMA Write other than TCTXT write.
54:55	RW	INT_PC_AIB_TX_CRD_RSD_CRD_VPC_ST_RMT_PC: 2-bit Reserved crd count for VPC remote PC stores.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	INT_PC_AIB_TX_CRD_RSD_CRD_VPC_ST_RMT_VC: 2-bit Reserved crd count for VPC remote VC stores.
58	RW	INT_PC_AIB_TX_CRD_Reserved_58: Spare.
59:63	RW	INT_PC_AIB_TX_CRD_WRITE_CRD_POOL: Outbound writes credits pool. (Must = Total number of CQ write machines - Sum (all Reserved write credit counts, PC+VC) (assume 4 Reserved in VC).

Register Name	AIB TX Commands Priority Register
Mnemonic	INT.INT_PC.INT_PC_AIB_TX_PRIO
Address	0000000005013125 (SCOM)
Description	This register defines the priority for each source of AIB TX commands 0 = High priority 1 = Medium priority 2 = Low priority

Bits	SCOM	Field Mnemonic: Description
0:39	RO	Constant = 0b000000000000000000000000000000000000000
40	RW	INT_PC_AIB_TX_PRIO_ATX_LIMIT_AT_DEM_IN_PIPE: 0: Multiple AT demand might be in ATX pipe. 1: Prevent multiple AT demand to be in ATX pipe.
41:43	RW	INT_PC_AIB_TX_PRIO_Reserved_41_43: Spare.
44:45	RW	INT_PC_AIB_TX_PRIO_ATX_PRIO_FOR_REGS: REGS: Registers read response.
46:47	RW	INT_PC_AIB_TX_PRIO_ATX_PRIO_FOR_TCTXT_RSP_WR: TCTXT load response / write.
48:49	RW	INT_PC_AIB_TX_PRIO_ATX_PRIO_FOR_BLCK_UPD: Block Interrupt update request.
50:51	RW	INT_PC_AIB_TX_PRIO_Reserved_50_51: Spare.
52:53	RW	INT_PC_AIB_TX_PRIO_ATX_PRIO_FOR_VPC_DMA: VPC: DMA read/write.
54:55	RW	INT_PC_AIB_TX_PRIO_ATX_PRIO_FOR_VPC_CI_LD: VPC: CI load response.
56:57	RW	INT_PC_AIB_TX_PRIO_ATX_PRIO_FOR_VPC_LD_RMT: VPC CI load remote PC.
58:59	RW	INT_PC_AIB_TX_PRIO_ATX_PRIO_FOR_VPC_ST_LCL_VC: VPC: CI store local VC.
60:61	RW	INT_PC_AIB_TX_PRIO_ATX_PRIO_FOR_VPC_ST_RMT_PC: VPC: CI store remote PC.
62:63	RW	INT_PC_AIB_TX_PRIO_ATX_PRIO_FOR_VPC_ST_RMT_VC: VPC: CI store remote VC.

Register Name	AIB TX Command Ordering Tags Register
Mnemonic	INT.INT_PC.INT_PC_AIB_TX_ORDER
Address	0000000005013126 (SCOM)
Description	This register holds the 8-bit AIB ordering tag to be used for each AIB TX commands.

Bits	SCOM	Field Mnemonic: Description
0:11	RO	Constant = 0b000000000000
12:13	RW	INT_PC_AIB_TX_ORDER_Reserved_12_13: Spare.
14	RW	INT_PC_AIB_TX_ORDER_RELAXED_WR_ORDERING: When asserted Relaxed write ordering is asserted on aib for any VPD DMA write/push.
15	RW	INT_PC_AIB_TX_ORDER_Reserved_15: Spare.
16:23	RW	INT_PC_AIB_TX_ORDER_REGS_ORDERING_TAG: REGS: Registers read response.

Bits	SCOM	Field Mnemonic: Description
24:31	RW	INT_PC_AIB_TX_ORDER_VPC_DMA_ORDERING_TAG: VPC: DMA Read/Write.
32:39	RW	INT_PC_AIB_TX_ORDER_VPC_LD_RSP_ORDERING_TAG: VPC CI load response.
40:47	RW	INT_PC_AIB_TX_ORDER_VPC_LD_RMT_ORDERING_TAG: VPC: CI load remote PC.
48:55	RW	INT_PC_AIB_TX_ORDER_VPC_ST_RMT_PC_ORDERING_TAG: EQC: CI store remote PC.
56:63	RW	INT_PC_AIB_TX_ORDER_VPC_ST_RMT_VC_ORDERING_TAG: EQC: CI store remote VC.

Register Name	Debug Timeout Register
Mnemonic	INT.INT_PC.INT_PC_DBG_TMOT
Address	0000000005013130 (SCOM)
Description	This register holds the timeout timer values used in the PC logic.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INT_PC_DBG_TMOT_Reserved_0_1: Spare.
2:7	RW	INT_PC_DBG_TMOT_ARX_TIMEOUT: DMA read timeout. The timeout valus is in the range of 2^(cfg_value) x [32ns .. 48 ns]. Setting bit 2 disables the timer.
8:9	RW	INT_PC_DBG_TMOT_Reserved_8_9: Spare.
10:15	RW	INT_PC_DBG_TMOT_MMIO_LDST_TIMEOUT: Thread context MMIO timeout. The timeout valus is in the range of 2^(cfg_value) x [32ns .. 48 ns]. Setting bit 10 disables the timer.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Debug ECC Register
Mnemonic	INT.INT_PC.INT_PC_DBG_ECC
Address	0000000005013131 (SCOM)
Description	This register holds the ECC correction and error injection information used in the PC logic.

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_PC_DBG_ECC_DIS_CRESP_ECC_CORR: Disable CRESP array ECC correction.
1:2	RW	INT_PC_DBG_ECC_DIS_ARX_DAT_ECC_CORR: Disable ARX data ECC correction.
3	RW	INT_PC_DBG_ECC_DIS_ARX_TAG_ECC_CORR: Disable ARX tag array ECC correction.
4	RW	INT_PC_DBG_ECC_DIS_MMIO_LDST_ECC_CORR: Disable MMIO LDST array ECC correction.
5	RW	INT_PC_DBG_ECC_DIS_MMIO_RSP_ECC_CORR: Disable MMIO RSP array ECC correction.
6	RW	INT_PC_DBG_ECC_DIS_VRQ_QUEUE_ECC_CORR: Disable VRQ Queue array ECC correction.
7	RW	INT_PC_DBG_ECC_DIS_AVX_ECC_CORR: Disable AVX data ECC correction.
8	RW	INT_PC_DBG_ECC_DIS_ATX_CMD_ECC_CORR: Disable ATX command array ECC correction.
9	RW	INT_PC_DBG_ECC_DIS_ATX_BAR_ECC_CORR: Disable ATX Bar array ECC correction.
10	RW	INT_PC_DBG_ECC_DIS_ATX_AT_ECC_CORR: Disable ATX AT array ECC correction.
11:15	RW	INT_PC_DBG_ECC_Reserved_11_15: Spare.
16	RWX	INT_PC_DBG_ECC_FORCE_SINGLE_BIT_ECC_ERR: Force single bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain lsb bit is flipped).

Bits	SCOM	Field Mnemonic: Description
17	RWX	INT_PC_DBG_ECC_FORCE_DOUBLE_BIT_ECC_ERR: Force double bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain 2 lsb bits are flipped).
18	RW	INT_PC_DBG_ECC_ARY_SELECT_CRESP_SRAM: Force error on CRESP SRAM.
19	RW	INT_PC_DBG_ECC_Reserved_19: Spare.
20	RW	INT_PC_DBG_ECC_ARY_SELECT_CMD_RSP_SRAM: Force error on command Rsp SRAM.
21	RW	INT_PC_DBG_ECC_ARY_SELECT_CMD_VRQ_SRAM: Force error on command Vrq SRAM.
22:23	RW	INT_PC_DBG_ECC_ARY_SELECT_ATX_CMD_SSA: Force error on ATX command SSA.
24:25	RW	INT_PC_DBG_ECC_ARY_SELECT_ATX_VPC_SSA: Force error on ATX VPC SSA.
26	RW	INT_PC_DBG_ECC_ARY_SELECT_ATX_BAR_SRAM: Force error on ATX BAR SRAM.
27	RW	INT_PC_DBG_ECC_ARY_SELECT_ATX_AT_SSA: Force error on ATX AT SSA.
28:29	RW	INT_PC_DBG_ECC_ARY_SELECT_ATX_AIB: Force error on ATX AIB data.
30:31	RW	INT_PC_DBG_ECC_Reserved_30_31: Spare.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Debug Trace Register
Mnemonic	INT.INT_PC.INT_PC_DBG_TRACE
Address	0000000005013133 (SCOM)
Description	This register holds the trace enable bits for the PC LBS1 trace logic.

Bits	SCOM	Field Mnemonic: Description
0	RW	INT_PC_DBG_TRACE_Reserved_0: TCTXT MMIO and Pipe trace enable.
1	RW	INT_PC_DBG_TRACE_Reserved_1: TCTXT-VPC trace enable.
2:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Debug PMC Register
Mnemonic	INT.INT_PC.INT_PC_DBG_PMC
Address	0000000005013134 (SCOM)
Description	PC LBS1 PMC selection. At most one bit may be enabled to avoid interference among PMC signals

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INT_PC_DBG_PMC_EN_ARX_PMC: ARX performance counter enable.
2:3	RW	INT_PC_DBG_PMC_EN_CRESP_PMC: CRESP performance counter enable.
4:13	RW	INT_PC_DBG_PMC_EN_CMD_PMC: command performance counter enable.
14:15	RW	INT_PC_DBG_PMC_Reserved_14_15: Spare.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Debug PMC ATX0 Register
Mnemonic	INT.INT_PC.INT_PC_DBG_PMC_ATX0
Address	0000000005013135 (SCOM)
Description	4-bit configuration for each possible performance event bit0: Enable count of request granted by the ATX arbiter bit 1:3 Performance counter selection.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INT_PC_DBG_PMC_ATX0_CNT_R0: Count of request(0).
4:7	RW	INT_PC_DBG_PMC_ATX0_CNT_R1R: Count of request(1rsp).
8:11	RW	INT_PC_DBG_PMC_ATX0_CNT_R1W: Count of request(1w).
12:15	RW	INT_PC_DBG_PMC_ATX0_CNT_R2: Count of request(2).
16:19	RW	INT_PC_DBG_PMC_ATX0_CNT_R3: Count of request(3).
20:23	RW	INT_PC_DBG_PMC_ATX0_CNT_R4R: Count of request(4r).
24:27	RW	INT_PC_DBG_PMC_ATX0_CNT_R4W: Count of request(4w).
28:31	RW	INT_PC_DBG_PMC_ATX0_CNT_R5: Count of request(5).
32:35	RW	INT_PC_DBG_PMC_ATX0_CNT_R6: Count of request(6).
36:39	RW	INT_PC_DBG_PMC_ATX0_CNT_R7: Count of request(7).
40:43	RW	INT_PC_DBG_PMC_ATX0_CNT_R8: Count of request(8).
44:47	RW	INT_PC_DBG_PMC_ATX0_CNT_R9: Count of request(9).
48:63	RO	Constant = 0b0000000000000000

Register Name	Debug PMC ATX1 Register
Mnemonic	INT.INT_PC.INT_PC_DBG_PMC_ATX1
Address	0000000005013136 (SCOM)
Description	4-bit configuration for each possible performance event bit 0: Enable count of request not presented immediately to the ATX arbiter because lack of credit bit 1:3 Performance counter selection

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INT_PC_DBG_PMC_ATX1_CNT_R0: Count of request(0).
4:7	RW	INT_PC_DBG_PMC_ATX1_CNT_R1R: Count of request(1rsp).
8:11	RW	INT_PC_DBG_PMC_ATX1_CNT_R1W: Count of request(1w).
12:15	RW	INT_PC_DBG_PMC_ATX1_CNT_R2: Count of request(2).
16:19	RW	INT_PC_DBG_PMC_ATX1_CNT_R3: Count of request(3).
20:23	RW	INT_PC_DBG_PMC_ATX1_CNT_R4R: Count of request(4r).
24:27	RW	INT_PC_DBG_PMC_ATX1_CNT_R4W: Count of request(4w).
28:31	RW	INT_PC_DBG_PMC_ATX1_CNT_R5: Count of request(5).
32:35	RW	INT_PC_DBG_PMC_ATX1_CNT_R6: Count of request(6).
36:39	RW	INT_PC_DBG_PMC_ATX1_CNT_R7: Count of request(7).
40:43	RW	INT_PC_DBG_PMC_ATX1_CNT_R8: Count of request(8).
44:47	RW	INT_PC_DBG_PMC_ATX1_CNT_R9: Count of request(9).

Bits	SCOM	Field Mnemonic: Description
48:63	RO	Constant = 0b0000000000000000

Register Name	Debug PMC ATX2 Register
Mnemonic	INT.INT_PC.INT_PC_DBG_PMC_ATX2
Address	0000000005013137 (SCOM)
Description	4-bit configuration for each possible performance event bit0: Enable count of request not served immediately because another requester is served bit 1:3 Performance counter selection

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INT_PC_DBG_PMC_ATX2_CNT_R0: Count of request(0).
4:7	RW	INT_PC_DBG_PMC_ATX2_CNT_R1R: Count of request(1rsp).
8:11	RW	INT_PC_DBG_PMC_ATX2_CNT_R1W: Count of request(1w).
12:15	RW	INT_PC_DBG_PMC_ATX2_CNT_R2: Count of request(2).
16:19	RW	INT_PC_DBG_PMC_ATX2_CNT_R3: Count of request(3).
20:23	RW	INT_PC_DBG_PMC_ATX2_CNT_R4R: Count of request(4r).
24:27	RW	INT_PC_DBG_PMC_ATX2_CNT_R4W: Count of request(4w).
28:31	RW	INT_PC_DBG_PMC_ATX2_CNT_R5: Count of request(5).
32:35	RW	INT_PC_DBG_PMC_ATX2_CNT_R6: Count of request(6).
36:39	RW	INT_PC_DBG_PMC_ATX2_CNT_R7: Count of request(7).
40:43	RW	INT_PC_DBG_PMC_ATX2_CNT_R8: Count of request(8).
44:47	RW	INT_PC_DBG_PMC_ATX2_CNT_R9: Count of request(9).
48:63	RO	Constant = 0b0000000000000000

Register Name	Error 0 Configuration 0 Register
Mnemonic	INT.INT_PC.INT_PC_ERR0_CFG0
Address	0000000005013140 (SCOM)
Description	This register is used to configure P3PC error0. 2-bit configuration for each possible error. 00 - Disable 01 - Fatal 10 - Recoverable 11 - Informational

Bits	SCOM	Field Mnemonic: Description
0:63	RW	INT_PC_ERR0_CFG0_ERROR_CONFIG0: Bit n is config(0) for error0 bit n.

Register Name	Error 0 Configuration 1 Register
Mnemonic	INT.INT_PC.INT_PC_ERR0_CFG1
Address	0000000005013141 (SCOM)
Description	This register is used to configure P3PC error0. 2-bit configuration for each possible error. 00 - Disable 01 - Fatal 10 - Recoverable 11 - Informational.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	INT_PC_ERR0_CFG1_ERROR_CONFIG0: Bit n is config(1) for error0 bit n.

Register Name	Error 0 WOF (Who's On First) Register
Mnemonic	INT.INT_PC.INT_PC_ERR0_WOF
Address	0000000005013142 (SCOM)
Description	This register captures the first non disabled group0 error reported. This register is cleared on read.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_ERR0_WOF_ERROR: Bit n in this register corresponds to error0 bit n.

Register Name	Error 0 WOF Detail Register
Mnemonic	INT.INT_PC.INT_PC_ERR0_WOF_DETAIL
Address	0000000005013143 (SCOM)
Description	This register captures the error detailed information of the error logged in corresponding WOF register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	INT_PC_ERR0_WOF_DETAIL_DETAIL:

Register Name	Error 0 Fatal Error Register
Mnemonic	INT.INT_PC.INT_PC_ERR0_FATAL
Address	0000000005013144 (SCOM)
Description	This register accumulates all the error0 fatal errors This register is cleared on read.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_ERR0_FATAL_ERROR: Bit n in this register corresponds to error0 bit n.

Register Name	Error 0 Recoverable Error Register
Mnemonic	INT.INT_PC.INT_PC_ERR0_RECOV
Address	0000000005013145 (SCOM)
Description	This register accumulates all the error0 recoverable errors This register is cleared on read.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_ERR0_RECOV_ERROR: Bit n in this register corresponds to error0 bit n.

Register Name	Error 0 Informational Error Register
Mnemonic	INT.INT_PC.INT_PC_ERR0_INFO
Address	0000000005013146 (SCOM)
Description	This register accumulates all the error0 informational errors This register is cleared on read.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_ERR0_INFO_ERROR: Bit n in this register corresponds to error0 bit n.

Register Name	Error 1 Configuration 0 Register
Mnemonic	INT.INT_PC.INT_PC_ERR1_CFG0
Address	0000000005013148 (SCOM)
Description	This register is used to configure P3PC error1. 2-bit configuration for each possible error. 00 - Disable 01 - Fatal 10 - Recoverable 11 - Informational.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	INT_PC_ERR1_CFG0_ERROR_CONFIG0: Bit n is config(0) for error1 bit n.

Register Name	Error 1 Configuration 1 Register
Mnemonic	INT.INT_PC.INT_PC_ERR1_CFG1
Address	0000000005013149 (SCOM)
Description	This register is used to configure P3PC error1. 2-bit configuration for each possible error. 00 - Disable 01 - Fatal 10 - Recoverable 11 - Informational.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	INT_PC_ERR1_CFG1_ERROR_CONFIG0: Bit n is config(1) for error1 bit n.

Register Name	Error 1 WOF (Who's On First) Register
Mnemonic	INT.INT_PC.INT_PC_ERR1_WOF
Address	000000000501314A (SCOM)
Description	This register captures the first non disabled group1 error reported. This register is cleared on read.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_ERR1_WOF_ERROR: Bit n in this register corresponds to error1 bit n.

Register Name	Error 1 WOF Detail Register
Mnemonic	INT.INT_PC.INT_PC_ERR1_WOF_DETAIL
Address	000000000501314B (SCOM)
Description	This register captures the error detailed information of the error logged in corresponding WOF register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	INT_PC_ERR1_WOF_DETAIL_DETAIL:

Register Name	Error 1 Fatal Error Register
Mnemonic	INT.INT_PC.INT_PC_ERR1_FATAL
Address	000000000501314C (SCOM)
Description	This register accumulates all the error1 fatal errors This register is cleared on read.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_ERR1_FATAL_ERROR: Bit n in this register corresponds to error1 bit n.

Register Name	Error 1 Recoverable Error Register
Mnemonic	INT.INT_PC.INT_PC_ERR1_RECOV
Address	000000000501314D (SCOM)
Description	This register accumulates all the error1 recoverable errors This register is cleared on read.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_ERR1_RECOV_ERROR: Bit n in this register corresponds to error1 bit n.

Register Name	Error 1 Informational Error Register
Mnemonic	INT.INT_PC.INT_PC_ERR1_INFO
Address	000000000501314E (SCOM)
Description	This register accumulates all the error1 informational errors This register is cleared on read.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_ERR1_INFO_ERROR: Bit n in this register corresponds to error1 bit n.

Register Name	VPC Maximum Number of Outstanding Outbound Requests Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD
Address	0000000005013160 (SCOM)
Description	Defines the maximum number of outstanding requests that VPC may issue. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:25	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_Reserved_0_25: Spare.

Bits	SCOM	Field Mnemonic: Description
26:31	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_CI_STORE_RMT_PC: VPC: CI Store Remote PC request.
32:33	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_Reserved_32_33: Spare.
34:39	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_CI_STORE_RMT_VC: VPC: CI Store Remote VC request.
40:41	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_Reserved_40_41: Spare.
42:47	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_CI_LOAD: VPC: CI Load Local or Remote request.
48:49	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_Reserved_48_49: Spare.
50:55	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_VPD_DMA_READ: VPC: VPD DMA Read request.
56:57	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_Reserved_56_57: Spare.
58:63	RWX	INT_PC_VPC_MAX_OUTSTANDING_OUTB_CMD_VPD_DMA_WRITE: VPC: VPD DMA Write request.

Register Name	**VPC Cache Enable Register**
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_CACHE_EN
Address	0000000005013161 (SCOM)
Description	This register enables the VPC cache. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	INT_PC_VPC_CACHE_EN_CACHE_ENABLE: 32-bit cache enable (one bit per blockid). May be cleared by scrub engine at flush completion.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	**VPC Cache Scrub Trigger Register**
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_SCRUB_TRIG
Address	0000000005013162 (SCOM)
Description	This register, along with scrub mask register, is used by Software to trigger a cache scrub. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_PC_VPC_SCRUB_TRIG_VALID: Scrub request. Set by Software to initiate a cache scrub. Reset by hardware when flush operation is completed.
1	RWX	INT_PC_VPC_SCRUB_TRIG_WANT_CACHE_DISABLE: Want cache disable. When set, cache is disabled for the selected blockid(s) at the end of scrub operation.
2	RWX	INT_PC_VPC_SCRUB_TRIG_WANT_INVALIDATE: Want invalidate. 0: Modified entries are written back. State is switched to exclusive 1: Exclusive entries are switched to invalidate. Modified entries are written back, state is switched to invalidate.
3:26	RO	Constant = 0b00000000000000000000000000
27:31	RWX	INT_PC_VPC_SCRUB_TRIG_BLOCKID: 5-bit scrub blockid.
32:44	RWX	INT_PC_VPC_SCRUB_TRIG_Reserved_32_44: Spare.
45:63	RWX	INT_PC_VPC_SCRUB_TRIG_OFFSET: 19-bit scrub offset.

Register Name	VPC Cache Scrub Mask Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_SCRUB_MASK
Address	0000000005013163 (SCOM)
Description	This register defines the block ids and offsets that need to be scrubbed. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:26	RO	Constant = 0b00000000000000000000000000
27:31	RWX	INT_PC_VPC_SCRUB_MASK_BLOCKID_MASK: 5-bit scrub blockid mask. 0:means ignore the corresponding blockid bit.
32:44	RWX	INT_PC_VPC_SCRUB_MASK_Reserved_32_44: Spare.
45:63	RWX	INT_PC_VPC_SCRUB_MASK_OFFSET_MASK: 19-bit scrub offset mask. 0:means ignore the corresponding offset bi t.

Register Name	VPC Configuration Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_CONFIG
Address	0000000005013164 (SCOM)
Description	Defines global VPC configuration. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:23	RO	Constant = 0b00000000000000000000000
24:25	RWX	INT_PC_VPC_CONFIG_Reserved_24_25: Spare.
26:31	RWX	INT_PC_VPC_CONFIG_PTAG_MAX_IN_USE: Maximum number of VPC ptags that can be in use at a time.
32	RWX	INT_PC_VPC_CONFIG_Reserved_32: Spare.
33:35	RWX	INT_PC_VPC_CONFIG_SYNC_DONE: 3-bit sync done. Cleared by Software. Set by hardware when sync operation is completed (33:vrq local pull, 34:vrq push local, 35:vrq push remote and vrq sw store).
36:39	RWX	INT_PC_VPC_CONFIG_Reserved_36_39: Spare.
40	RWX	INT_PC_VPC_CONFIG_LCL_FIRST_GRPSCAN_ENA: When '1', enable Pull Local First commands to do a Group Scan operation.
41	RWX	INT_PC_VPC_CONFIG_LCL_FIRST_GRPSCAN_RMT_ENA: When '1', enable Pull Local First commands to do a Remote Group Scan operation.
42	RWX	INT_PC_VPC_CONFIG_RMT_FIRST_GRPSCAN_ENA: When '1', enable Pull Remote First commands to do a Group Scan operation.
43	RWX	INT_PC_VPC_CONFIG_LSMFB_SCAN_ALL_PRIO_ENA: When '1', the LSMFB (Logical Server Most Favored Backlog) will look at all priority backlogs when doing a Group Scan. When '0', the LSMFB will only look at priority 7 up to the priority of the Pull command backlogs when doing a Group Scan.
44:46	RWX	INT_PC_VPC_CONFIG_P0_BACK2BACK_MODE_ENA: When '1', requests from the same source are allowed to win P0 arbitration in back-to-back arbitration cycles. When '0', at least one P0 arbitration cycle will occur between requests from the same source. 0: VRQ requests 1: Load requests 2: Local Group Scan requests.
47:51	RWX	INT_PC_VPC_CONFIG_Reserved_47_51: Spare.
52:55	RWX	INT_PC_VPC_CONFIG_BG_SCAN_RATE: 4-bit scrub background scan rate. 0:disable scan. Otherwise, scan rate = 2**n clock cycles (max of 16 micro-seconds).
56:58	RWX	INT_PC_VPC_CONFIG_Reserved_56_58: Spare.

Bits	SCOM	Field Mnemonic: Description
59:63	RWX	INT_PC_VPC_CONFIG_MAX_ENTRIES_IN_MODIFIED: 5-bit Max number of entries per set in modified state.

Register Name	VPC Cache Watch Specification Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_SPEC
Address	0000000005013167 (SCOM)
Description	This register along with cache watch data registers are used to Read and Write VPDs. Software specifies the VPD blockid and offset it wants to access. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0	NCX	INT_PC_VPC_CACHE_WATCH_SPEC_CONFLICT: Conflict: Forced to 0 when Software writes the register. Set to one by hardware if an internal VPC process references this VPD and its valid bit is on during the Software ReadModifyWrite sequence.
1:7	RWX	INT_PC_VPC_CACHE_WATCH_SPEC_Reserved_1_7: Spare.
8	RWX	INT_PC_VPC_CACHE_WATCH_SPEC_FULL: Full - if set to a one, then the contents of all data register fields replace the corresponding specified structure fields as long as the conflict bit is zero, else the structure is not modified; if F is set to a zero, then only the contents of data register fields that are hardware read-only replace the corresponding specific structure fields (everything except IPB and Backlogs), regardless of the state of the conflict bit.
9:26	RWX	INT_PC_VPC_CACHE_WATCH_SPEC_Reserved_9_26: Spare.
27:31	RWX	INT_PC_VPC_CACHE_WATCH_SPEC_BLOCKID: 5-bit blockid.
32:44	RWX	INT_PC_VPC_CACHE_WATCH_SPEC_Reserved_32_44: Spare.
45:63	RWX	INT_PC_VPC_CACHE_WATCH_SPEC_OFFSET: 19-bit VPD offset.

Register Name	VPC Cache Watch Data 0 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA0
Address	0000000005013168 (SCOM)
Description	Holds data for VPD words 0 and 1. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_PC_VPC_CACHE_WATCH_DATA0_VP: Valid bit for the VP portion (Words 0-7) of the VPD entry Read Modify Write operation : - Software writes cache watch specification register. This clears the Conflict bit. - Software does CI load of the data register 0. This triggers an internal read request of the targeted data defined in cache watch specification register - When the internal read operation is completed, data is loaded into the cache watch data registers - CI load response is generated - Software may issue CI load of data registers 1 to 7 to get full data - Software optionally does CI store of data registers 1 to 7. - Software writes data register 0. The write to data register 0 triggers an internal write of the VPD defined in cache watch specification register - The write operation is aborted if the hardware had set the Conflict bit and Full bit was 1. - Software reads the cache watch specification register. If C = 1 and F = 1 then Software has to retry the full sequence.
1:6	RO	Constant = 0b000000
7	RWX	INT_PC_VPC_CACHE_WATCH_DATA0_SECURE: Secure VP.
8:25	RO	Constant = 0b000000000000000000
26:31	RWX	INT_PC_VPC_CACHE_WATCH_DATA0_PGOFFIRSTLS: The physical grouping level of the first higher logical server.
32:35	RWX	INT_PC_VPC_CACHE_WATCH_DATA0_IVE_BLOCK: IVE Block for Pressure Relief interrupt.

Bits	SCOM	Field Mnemonic: Description
36:63	RWX	INT_PC_VPC_CACHE_WATCH_DATA0_IVE_INDEX: IVE Index for Pressure Relief interrupt.

Register Name	VPC Cache Watch Data 2 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA2
Address	000000000501316A (SCOM)
Description	Holds data for VPD words 4 and 5. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:23	RWX	INT_PC_VPC_CACHE_WATCH_DATA2_IPB: Interrupt Pending Bits.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	VPC Cache Watch Data 3 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA3
Address	000000000501316B (SCOM)
Description	Holds data for VPD words 6 and 7. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_PC_VPC_CACHE_WATCH_DATA3_MIG_REG: Migration register number.
4:7	RO	Constant = 0b0000
8:55	RWX	INT_PC_VPC_CACHE_WATCH_DATA3_CL: VP reporting cache line.
56:63	RO	Constant = 0b00000000

Register Name	VPC Cache Watch Data 4 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA4
Address	000000000501316C (SCOM)
Description	Holds data for VPD words 8 and 9. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_PC_VPC_CACHE_WATCH_DATA4_VG: Valid bit for the Group portion (Words 8-F) of the VPD entry.
1:25	RO	Constant = 0b0000000000000000000000000
26:31	RWX	INT_PC_VPC_CACHE_WATCH_DATA4_PGOFNEXTLS: The physical grouping level of the next higher logical server.
32:35	RO	Constant = 0b0000
36:39	RWX	INT_PC_VPC_CACHE_WATCH_DATA4_EQD_BLOCK: EQD Block for Redistribution interrupt.
40:60	RWX	INT_PC_VPC_CACHE_WATCH_DATA4_EQD_INDEX: EQD Index for Redistribution interrupt.
61:63	RO	Constant = 0b000

Register Name	VPC Cache Watch Data 6 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA6
Address	000000000501316E (SCOM)
Description	Holds data for VPD words C and D. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX	INT_PC_VPC_CACHE_WATCH_DATA6_BKLG0: Priority 0 Backlog counter.
16:31	RWX	INT_PC_VPC_CACHE_WATCH_DATA6_BKLG1: Priority 1 Backlog counter.
32:47	RWX	INT_PC_VPC_CACHE_WATCH_DATA6_BKLG2: Priority 2 Backlog counter.
48:63	RWX	INT_PC_VPC_CACHE_WATCH_DATA6_BKLG3: Priority 3 Backlog counter.

Register Name	VPC Cache Watch Data 7 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_CACHE_WATCH_DATA7
Address	000000000501316F (SCOM)
Description	Holds data for VPD words E and F. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX	INT_PC_VPC_CACHE_WATCH_DATA7_BKLG4: Priority 4 Backlog counter.
16:31	RWX	INT_PC_VPC_CACHE_WATCH_DATA7_BKLG5: Priority 5 Backlog counter.
32:47	RWX	INT_PC_VPC_CACHE_WATCH_DATA7_BKLG6: Priority 6 Backlog counter.
48:63	RWX	INT_PC_VPC_CACHE_WATCH_DATA7_BKLG7: Priority 7 Backlog counter.

Register Name	VPC Debug Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_DEBUG
Address	0000000005013170 (SCOM)
Description	This register holds ECC errors correction/injection and some VPC debug features. This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:29	RWX	INT_PC_VPC_DEBUG_Reserved_0_29: Spare.
30	RWX	INT_PC_VPC_DEBUG_DIS_LD_ECC_CORRECTION: Disable VPC Load array ECC correction.
31:38	RWX	INT_PC_VPC_DEBUG_DIS_TAG_ECC_CORRECTION: Disable TAG [0:7] arrays ECC correction.
39:40	RWX	INT_PC_VPC_DEBUG_DIS_STATE_ECC_CORRECTION: Disable STATE [0:1] array ECC correction.
41:43	RWX	INT_PC_VPC_DEBUG_DIS_PTAG_ECC_CORRECTION: Disable P1 PTAG Cmd,Ctrl,CL array ECC correction.
44:47	RWX	INT_PC_VPC_DEBUG_DIS_DATA_ECC_CORRECTION: Disable P1 DATA Backlog0,Backlog1,Ctrl,CL array ECC correction.
48	RWX	INT_PC_VPC_DEBUG_FORCE_SINGLE_BIT_ECC_ERR: Force single bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain lsb bit is flipped).
49	RWX	INT_PC_VPC_DEBUG_FORCE_DOUBLE_BIT_ECC_ERR: Force double bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain 2 lsb bits are flipped).
50:51	RWX	INT_PC_VPC_DEBUG_ECC_ERR_INJ_PARTITION_SEL: Partition selection for ECC error injection 00 P0 pipeline 01 P1 Pipeline 10 VPC Load.

Bits	SCOM	Field Mnemonic: Description
52:55	RWX	INT_PC_VPC_DEBUG_ECC_ERR_INJ_ARRAY_SEL: Array selection for ECC error injection P0 pipeline 0xxx = P0 TAG array where xxx = 0 to 7 100x = P0 STATE array where X = 0 or1 0000 = Data Backlog0 array ECC0 0001 = Data Backlog1 array ECC0 0010 = Data Backlog0 array ECC1 0011 = Data Backlog1 array ECC1 0100 = Data Ctrl0 array ECC0 0101 = Data Ctrl1 array ECC0 0110 = Data Ctrl0 array ECC1 0111 = Data Ctrl1 array ECC1 1000 = Data CL0 array 1001 = Data CL1 array 1100 = Ptag command array 1101 = Ptag Ctrl array 1110 = Ptag CL array VPC Load xxxx = VPC Load array (this field is a don't care)
56	RWX	INT_PC_VPC_DEBUG_TRACE_ENABLE: Enable VPC trace bus.
57	RWX	INT_PC_VPC_DEBUG_PMC_ENABLE: Enable VPC PMC bus.
58:59	RWX	INT_PC_VPC_DEBUG_Reserved_58_59: Spare.
60	RWX	INT_PC_VPC_DEBUG_USE_WATCH_TO_READ_CTRL_ARY: Use watch engine to read cache control arrays. When set, a cache watch read is replaced by a read of the cache control arrays. In such case, Cache Watch Address reg (58:62) define set index.
61:63	RWX	INT_PC_VPC_DEBUG_CACHE_CTRL_ARY_SELECT: When bit 60 is set, this field defines which cache control arrays to read 000 Tag A Watch data reg 0 [13:31] = TAG0 Watch data reg 0 [45:63] = TAG1 Watch data reg 1 [13:31] = TAG8 Watch data reg 1 [45:63] = TAG9 Watch data reg 2 [13:31] = TAG16 Watch data reg 2 [45:63] = TAG17 Watch data reg 3 [13:31] = TAG24 Watch data reg 3 [45:63] = TAG25 001 Tag B Watch data reg 0 [13:31] = TAG2 Watch data reg 0 [45:63] = TAG3 Watch data reg 1 [13:31] = TAG10 Watch data reg 1 [45:63] = TAG11 Watch data reg 2 [13:31] = TAG18 Watch data reg 2 [45:63] = TAG19 Watch data reg 3 [13:31] = TAG26 Watch data reg 3 [45:63] = TAG27 010 Tag C Watch data reg 0 [13:31] = TAG4 Watch data reg 0 [45:63] = TAG5 Watch data reg 1 [13:31] = TAG12 Watch data reg 1 [45:63] = TAG13 Watch data reg 2 [13:31] = TAG20 Watch data reg 2 [45:63] = TAG21 Watch data reg 3 [13:31] = TAG28 Watch data reg 3 [45:63] = TAG29 011 Tag D Watch data reg 0 [13:31] = TAG6 Watch data reg 0 [45:63] = TAG7 Watch data reg 1 [13:31] = TAG14 Watch data reg 1 [45:63] = TAG15 Watch data reg 2 [13:31] = TAG22 Watch data reg 2 [45:63] = TAG23 Watch data reg 3 [13:31] = TAG30 Watch data reg 3 [45:63] = TAG31 1xx Tag State + LRU Watch data reg 1 = STATE(0 to 15) Watch data reg 2 = STATE(16 to 31) Watch data reg 3 [32:63] = LRU(0 to 31).

Register Name	VPC Performance Events Selection 1 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_PERF_EVENT_SEL_1
Address	0000000005013171 (SCOM)
Description	4-bit configuration for each possible performance event bit0: Count enable. bits 1:3 Performance counter selection This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_VRQ_PULL: count of VRQ Pull commands processed.
4:7	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_VRQ_PUSH_LOCAL: count of VRQ Push Local commands processed.
8:11	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_VRQ_PUSH_REMOTE: count of VRQ Push Remote commands processed.
12:15	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_NON_SPEC_VC_LOAD: count of non-speculative LocalRemote VC CI Ld commands processed.

Bits	SCOM	Field Mnemonic: Description
16:19	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_NON_SPEC_SW_LOAD: count of non-speculative SW CI Ld commands processed.
20:23	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_NON_SPEC_PC_LOAD: count of non-speculative PC CI Ld commands processed.
24:27	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_LOCAL_GROUP_SCAN: count of Local Group Scan commands processed.
28:31	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_VRQ_CACHE_HIT: count of VRQ commands with cache hit.
32:35	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_LD_CACHE_HIT: count of CI Ld commands with cache hit.
36:39	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_GROUP_SCAN_CACHE_HIT: count of Local Group Scan commands with cache hit.
40:43	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_VICTIM_IS_LRU: count of selected victim is LRU.
44:47	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_VICTIM_IS_FIRST_USABLE: count of selected victim is first usable entry.
48:51	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_RETRY: count of command retry.
52:55	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_CNT_TOO_MANY_ENTRIES: count of VPD writebacks due to too many entries in modified state.
56:63	RWX	INT_PC_VPC_PERF_EVENT_SEL_1_Reserved_56_63: Spare.

Register Name	VPC Performance Events Selection 2 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_PERF_EVENT_SEL_2
Address	0000000005013172 (SCOM)
Description	4-bit configuration for each possible performance event bit0: Count enable. bits 1:3 Performance counter selection This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_VPD_WB: count of VPD Writebacks sent.
4:7	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_VPD_FETCH: count of VPD Fetches sent.
8:11	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RSP_LCL_TCTXT: count of responses to local Tctxt sent.
12:15	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RSP_LCL_VC: count of responses to local VC sent.
16:19	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RSP_RMT_PC: count of responses to remote PC sent.
20:23	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RSP_RMT_VC: count of responses to remote VC sent.
24:27	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RSP_SW_LD: count of responses to SW Loads sent.
28:31	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RMT_PULL_1STVP: count of Pull Remote First VP commands sent.
32:35	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RMT_PULL_1STGRP: count of Pull Remote First Grp commands sent.
36:39	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RMT_PULL_VP: count of Pull Remote VP commands sent.
40:43	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RMT_PULL_GRP: count of Pull Remote Grp commands sent.
44:47	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_LCL_PRESS_RELIEF: count of Local Pressure Relief commands sent.
48:51	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_LCL_REDIST: count of Local Redistribution commands sent.
52:55	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RMT_PUSH_PC: count of Remote Push PC commands sent.
56:59	RWX	INT_PC_VPC_PERF_EVENT_SEL_2_CNT_RMT_PUSH_VC: count of Remote Push VC commands sent.

Bits	SCOM	Field Mnemonic: Description
60:63	RO	Constant = 0b0000

Register Name	VPC Performance Events Selection 3 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_PERF_EVENT_SEL_3
Address	0000000005013173 (SCOM)
Description	4-bit configuration for each possible performance event bit0: Count enable. bits 1:3 Performance counter selection This register is located in VPC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_PC_VPC_PERF_EVENT_SEL_3_CNT_LCL_GRPSCAN_REPLAY: count of Local Group Scan replay.
4:7	RWX	INT_PC_VPC_PERF_EVENT_SEL_3_CNT_VPD_FETCH_REPLAY: count of VPD Fetch replay.
8:11	RWX	INT_PC_VPC_PERF_EVENT_SEL_3_CNT_RSP_TCTXT_REPLAY: count of response to local Tctxt replay.
12:15	RWX	INT_PC_VPC_PERF_EVENT_SEL_3_CNT_RSP_ATX_REPLAY: count of response to ATX replay.
16:19	RWX	INT_PC_VPC_PERF_EVENT_SEL_3_CNT_LD_REQ_REPLAY: count of CI Load request replay.
20:23	RWX	INT_PC_VPC_PERF_EVENT_SEL_3_CNT_ST_LCL_REPLAY: count of CI Store Local replay.
24:27	RWX	INT_PC_VPC_PERF_EVENT_SEL_3_CNT_ST_RMT_PC_REPLAY: count of CI Store Remote PC replay.
28:31	RWX	INT_PC_VPC_PERF_EVENT_SEL_3_CNT_ST_RMT_VC_REPLAY: count of CI Store Remote VC replay.
32:35	RWX	INT_PC_VPC_PERF_EVENT_SEL_3_CNT_SAME_VPD_REPLAY: count of Group Scan to Same VPD replay.
36:63	RO	Constant = 0b00000000000000000000000000000

Register Name	VPC Additional Performance 1 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_ADDITIONAL_PERF_1
Address	0000000005013174 (SCOM)
Description	This register is located in VPC sub-unit. MMIO offset = 0x7A0

Bits	SCOM	Field Mnemonic: Description
0	ROX	INT_PC_VPC_ADDITIONAL_PERF_1_P0_IS_IDLE: VPC P0 is idle.
1	ROX	INT_PC_VPC_ADDITIONAL_PERF_1_P1_IS_IDLE: VPC P1 is idle.
2:9	ROX	INT_PC_VPC_ADDITIONAL_PERF_1_Reserved_2_9: Spare.
10:15	ROX	INT_PC_VPC_ADDITIONAL_PERF_1_MAX_PTAG_IN_USE: Max reached number of ptag in use.
16:27	ROX	INT_PC_VPC_ADDITIONAL_PERF_1_Reserved_16_27: Spare.
28:31	ROX	INT_PC_VPC_ADDITIONAL_PERF_1_MAX_UNLOCK_IN_FIFO: Max reached number of unlock command in the unlock FIFO.
32:33	ROX	INT_PC_VPC_ADDITIONAL_PERF_1_Reserved_32_33: Spare.
34:39	ROX	INT_PC_VPC_ADDITIONAL_PERF_1_MAX_OUTSTANDING_WB: Max reached number of outstanding Writebacks.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	VPC Additional Performance 2 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_ADDITIONAL_PERF_2
Address	0000000005013175 (SCOM)
Description	This register is located in VPC sub-unit. MMIO offset = 0x7A8

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	INT_PC_VPC_ADDITIONAL_PERF_2_Reserved_0_1: Spare.
2:7	ROX	INT_PC_VPC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_VPD_FETCH: Max reached number of outstanding VPD fetch.
8:9	ROX	INT_PC_VPC_ADDITIONAL_PERF_2_Reserved_8_9: Spare.
10:15	ROX	INT_PC_VPC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_CI_LOAD: Max reached number of outstanding CI Load request.
16:17	ROX	INT_PC_VPC_ADDITIONAL_PERF_2_Reserved_16_17: Spare.
18:23	ROX	INT_PC_VPC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_ST_RMT_PC: Max reached number of outstanding CI Store Remote PC request.
24:25	ROX	INT_PC_VPC_ADDITIONAL_PERF_2_Reserved_24_25: Spare.
26:31	ROX	INT_PC_VPC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_ST_RMT_VC: Max reached number of outstanding CI Store Remote VC request.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	VPC Errors Configuration 0 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_ERR_CFG0
Address	0000000005013178 (SCOM)
Description	This register along with the next one is used to configure P3PC VPC errors. 2-bit configuration for each possible error. 00 - Disable, 01 - Fatal, 10 - Recoverable, 11 - Informational. MMIO offset = 0x7C0

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	INT_PC_VPC_ERR_CFG0_ERROR_CONFIG: Bit n is config(0) for error bit n.

Register Name	VPC Errors Configuration 1 Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_ERR_CFG1
Address	0000000005013179 (SCOM)
Description	Refer to INT_PC_VPC_ERR_CFG0 description. MMIO offset = 0x7C8

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	INT_PC_VPC_ERR_CFG1_ERROR_CONFIG: Bit n is config(1) for error bit n.

Register Name	VPC Who's On First Errors Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_WOF_ERR
Address	000000000501317A (SCOM)
Description	This register captures the first non disabled VPC error reported. This register is cleared on read. MMIO offset = 0x7D0

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_VPC_WOF_ERR_ERROR: Bit n in this register corresponds to VPC error bit n.

Register Name	VPC Error WOF Detail Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_WOF_ERR_DETAIL
Address	000000000501317B (SCOM)
Description	This register captures the error detailed information of the error logged in corresponding WOF register. MMIO offset = 0x7D8

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	INT_PC_VPC_WOF_ERR_DETAIL_ERROR:

Register Name	VPC Fatal Errors Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_FATAL_ERR
Address	000000000501317C (SCOM)
Description	This register accumulates all the VPC fatal errors. This register is cleared on read. MMIO offset = 0x7E0

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_VPC_FATAL_ERR_ERROR: Bit n in this register corresponds to VPC error bit n.

Register Name	VPC Recoverable Errors Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_RECOV_ERR
Address	000000000501317D (SCOM)
Description	This register accumulates all the VPC recoverable errors. This register is cleared on read. MMIO offset = 0x7E8

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_VPC_RECOV_ERR_ERROR: Bit n in this register corresponds to VPC error bit n.

Register Name	VPC Informational Errors Register
Mnemonic	INT.INT_PC.LBS2.INT_PC_VPC_INFO_ERR
Address	000000000501317E (SCOM)
Description	This register accumulates all the VPC informational errors. This register is cleared on read. MMIO offset = 0x7F0

Bits	SCOM	Field Mnemonic: Description
0:63	ROX_CLRPART	INT_PC_VPC_INFO_ERR_ERROR: Bit n in this register corresponds to VPC error bit n.

Register Name	P3VC Global Configuration Register
Mnemonic	INT.INT_VC.INT_VC_GLOBAL_CONFIG
Address	0000000005013200 (SCOM)
Description	P3VC global configuration register.

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Constant = 0b00000000000000000000000000000000
32	RWX	INT_VC_GLOBAL_CONFIG_INDIRECT_MODE: When set, access to memory structures may be indirect. Software must set this bit if the "i" bit is set in any VSD.
33:63	RWX	INT_VC_GLOBAL_CONFIG_Reserved_33_63: Spare bits.

Register Name	VSD Table Address Register
Mnemonic	INT.INT_VC.INT_VC_VSD_TABLE_ADDR
Address	0000000005013201 (SCOM)
Description	This register along with the VSD table data register allows Software to load VSDs in the ATX BAR SRAM.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_VC_VSD_TABLE_ADDR_AUTO_INCREMENT: When set, each rd/wr access to the BAR data register increments the table_address field once the current operation is completed.
1:12	RO	Constant = 0b000000000000
13:15	RWX	INT_VC_VSD_TABLE_ADDR_TABLE_SELECT: Table select: 000 = IVE. 001 = ESB. 010 = EQD. 011 =VPD. 1xx = IRQ.
16:26	RWX	INT_VC_VSD_TABLE_ADDR_Reserved_16_26: Spare.
27:31	RWX	INT_VC_VSD_TABLE_ADDR_TABLE_ADDRESS: Offset within the selected table. Blockid 0 to 31 if selected table is VPD. Blockid 0 to 15 if selected table is IVE, ESB or EQD. IRQ 0 to 5 if selected table is IRQ (0:IPI, 1:HWD, 2:First escalate, 3:Second escalate, 4:Redistribution, 5:IPI cascaded queue).
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	IVE and ISB Blocks Mode Register
Mnemonic	INT.INT_VC.INT_VC_IVE_ISB_BLOCK_MODE
Address	0000000005013203 (SCOM)
Description	This register holds the mode defined for each IVE and ISB blocks. Whenever the Software does a write to IVE or ESB VSDs in BAR SRAM, the defined mode bits are also copied in this register. This register should never be written except for debug. Note that if the interrupt controller owns an IVE block, it must also own the corresponding ISB block.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	INT_VC_IVE_ISB_BLOCK_MODE_IVE_BLOCK_MODE: (2*n:n*2+1) IVE block n. 00invalid, 01shared, 10exclusive, 11forward.

Bits	SCOM	Field Mnemonic: Description
32:63	RWX	INT_VC_IVE_ISB_BLOCK_MODE_ISB_BLOCK_MODE: 32+(2*n:n*2+1) ISB block n. 00invalid, 01shared, 10exclusive, 11forward.

Register Name	EQD Blocks Mode Register
Mnemonic	INT.INT_VC.INT_VC_EQD_BLOCK_MODE
Address	0000000005013204 (SCOM)
Description	This register holds the mode defined for each EQD block. Whenever the Software does a write to EQD VSDs in BAR SRAM, the defined mode bits are also copied in this register. This register should never be written except for debug.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	INT_VC_EQD_BLOCK_MODE_EQD_BLOCK_MODE: (2*n:n*2+1) EQD block n. 00invalid, 01shared, 10exclusive, 11forward.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	VPS Blocks Mode Register
Mnemonic	INT.INT_VC.INT_VC_VPS_BLOCK_MODE
Address	0000000005013205 (SCOM)
Description	This register holds the mode defined for each VPS block. Whenever the Software does a write to VPS VSDs in BAR SRAM, the defined mode bits are also copied in this register. This register should never be written except for debug. Note that this register holds mode for 32 entries but the hardware only uses blocks 0 to 28.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	INT_VC_VPS_BLOCK_MODE_VPS_BLOCK_MODE: (2*n:n*2+1) VPS block n. 00invalid, 01shared, 10exclusive, 11forward.

Register Name	ATX-IRQ ECC Control And Debug Register
Mnemonic	INT.INT_VC.INT_VC_LBS6_DEBUG
Address	0000000005013206 (SCOM)
Description	ATX-IRQ ECC control and debug register This register holds ECC errors correction/injection for ARX, ATX and IRQ sub units.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_VC_LBS6_DEBUG_DIS_AIB_IN_ECC_CORRECTION: Disable AIB IN ECC sbe correction.
1	RWX	INT_VC_LBS6_DEBUG_DIS_IRQ_ECC_CORRECTION: Disable IRQ elastic FIFO ECC sbe correction.
2	RWX	INT_VC_LBS6_DEBUG_DIS_AT_SRAM_ECC_CORRECTION: Disable ATX AT SRAM ECC sbe correction.
3	RWX	INT_VC_LBS6_DEBUG_DIS_BAR_SRAM_ECC_CORRECTION: Disable ATX BAR SRAM ECC sbe correction.
4	RWX	INT_VC_LBS6_DEBUG_DIS_TAG_SRAM_ECC_CORRECTION: Disable ARX TAG SRAM ECC sbe correction.
5	RWX	INT_VC_LBS6_DEBUG_IRQ_TRACE_ENABLE: IRQ trace enable.

Bits	SCOM	Field Mnemonic: Description
6	RWX	INT_VC_LBS6_DEBUG_FORCE_SINGLE_BIT_ECC_ERR: Force single bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain lsb bit is flipped).
7	RWX	INT_VC_LBS6_DEBUG_FORCE_DOUBLE_BIT_ECC_ERR: Force double bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain 2 lsb bits are flipped).
8:9	RWX	INT_VC_LBS6_DEBUG_Reserved_8_9: Spare bits.
10:15	RWX	INT_VC_LBS6_DEBUG_ECC_ERR_INJ_SELECTION: Selection for ECC error injection. "00xx00" = AIB out data(0:63). "00xx01" = AIB out data(64:127). "00xx1x" = ARX TAG SRAM. "01nnn0" = IRQ nnn data(0:63) where nnn may only be 0 to 5. "01nnn1" = IRQ nnn data(64:127). "1xxx00" = ATX WB SRAM(0:63). "1xxx01" = ATX WB SRAM(64:127). "1xxx10" = ATX BAR SRAM. "1xxx11" = ATX AT SRAM.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	**IRQ Configuration 0 Register**
Mnemonic	INT.INT_VC.INT_VC_IRQ_CONFIG_0
Address	0000000005013208 (SCOM)
Description	This register holds the configuration for each Interrupt Request Queue. n = 0: IPI queue, n = 1:Hardware queue, n = 2:First level escalate queue, n = 3:Second level escalate queue, n = 4:Redistribution queue,n = 5:IPI cascaded queue. MMIO offsets = 0x840, 0x848, 0x850, 0x858, 0x860, 0x868

Bits	SCOM	Field Mnemonic: Description
0:20	RWX	INT_VC_IRQ_CONFIG_0_Reserved_0_20: Spare bits.
21:26	RWX	INT_VC_IRQ_CONFIG_0_PREFETCH_DISTANCE: Defines, in multiple of two int triggers, the maximum distance between prefetch and demand.
27:31	RWX	INT_VC_IRQ_CONFIG_0_MAX_CRD_TO_CQ: Max number of interrupt credits given to CQ.
32:34	RWX	INT_VC_IRQ_CONFIG_0_Reserved_32_34: Spare bits.
35:39	RWX	INT_VC_IRQ_CONFIG_0_MAX_CRD_TO_PC: Max number of interrupt credits given to PC. Reset value is 0xF for IPI and redistribution queues, 0 for other queues as PC never issues interrupt requests to these queues.
40:41	RWX	INT_VC_IRQ_CONFIG_0_Reserved_40_41: Spare bits.
42	RWX	INT_VC_IRQ_CONFIG_0_PREFETCH_DISABLE: When set, IRQ never issue IVC/SBC prefetch lookup operation.
43	RWX	INT_VC_IRQ_CONFIG_0_QUEUE_DISABLE: When set, IRQ does not forward any EQ trigger to EQC.
44	RWX	INT_VC_IRQ_CONFIG_0_IVC_INTF_DISABLE: When set, IRQ to IVC lookup interface is disabled.
45	RWX	INT_VC_IRQ_CONFIG_0_ENABLE_MEMORY_BACKING: When 0, IRQ does not use system memory as internal FIFO extension. The FIFO is limited to the hardware internal FIFO size.
46:51	RWX	INT_VC_IRQ_CONFIG_0_MEM_SIZE: Defines the size of the memory backing store, power of 2^(n+12) memory size.
52	RWX	INT_VC_IRQ_CONFIG_0_Reserved_52: Spare bit.
53:55	RWX	INT_VC_IRQ_CONFIG_0_NB_WRITE_SLOT: Number of slots used for write.
56	RWX	INT_VC_IRQ_CONFIG_0_Reserved_56: Spare bit.
57:59	RWX	INT_VC_IRQ_CONFIG_0_NB_CLEAN_SLOT: Number of slots that will be kept clean.

Bits	SCOM	Field Mnemonic: Description
60	RWX	INT_VC_IRQ_CONFIG_0_FULL_WRITEBACK_ENABLE: Full Writeback enable. When set, all lines are written back to system memory.
61	ROX	INT_VC_IRQ_CONFIG_0_QUEUE_NOT_EMPTY: Queue is not empty.
62	ROX	INT_VC_IRQ_CONFIG_0_CREDIT_UPDATE_PENDING: A credit update is pending.
63	ROX_CLRPART	INT_VC_IRQ_CONFIG_0_FIFO_FULL: Set by hardware when the fifo is full. Cleared on read.

Register Name	**IRQ Configuration 1 Register**
Mnemonic	INT.INT_VC.INT_VC_IRQ_CONFIG_1
Address	0000000005013209 (SCOM)
Description	This register holds the configuration for each Interrupt Request Queue. n = 0: IPI queue n = 1: Hardware queue n = 2: First level escalate queue n = 3: Second level escalate queue n = 4: Redistribution queue n = 5: IPI cascaded queue. MMIO offsets = 0x840, 0x848, 0x850, 0x858, 0x860, 0x868

Bits	SCOM	Field Mnemonic: Description
0:20	RWX	INT_VC_IRQ_CONFIG_1_Reserved_0_20: Spare bits.
21:26	RWX	INT_VC_IRQ_CONFIG_1_PREFETCH_DISTANCE: Defines, in multiple of two int triggers, the maximum distance between prefetch and demand.
27:31	RWX	INT_VC_IRQ_CONFIG_1_MAX_CRD_TO_CQ: Max number of interrupt credits given to CQ.
32:34	RWX	INT_VC_IRQ_CONFIG_1_Reserved_32_34: Spare bits.
35:39	RWX	INT_VC_IRQ_CONFIG_1_MAX_CRD_TO_PC: Max number of interrupt credits given to PC. Reset value is 0xF for IPI and redistribution queues, 0 for other queues as PC never issues interrupt requests to these queues.
40:41	RWX	INT_VC_IRQ_CONFIG_1_Reserved_40_41: Spare bits.
42	RWX	INT_VC_IRQ_CONFIG_1_PREFETCH_DISABLE: When set, IRQ never issue IVC/SBC prefetch lookup operation.
43	RWX	INT_VC_IRQ_CONFIG_1_QUEUE_DISABLE: When set, IRQ does not forward any EQ trigger to EQC.
44	RWX	INT_VC_IRQ_CONFIG_1_IVC_INTF_DISABLE: When set, IRQ to IVC lookup interface is disabled.
45	RWX	INT_VC_IRQ_CONFIG_1_ENABLE_MEMORY_BACKING: When 0, IRQ does not use system memory as internal FIFO extension. The FIFO is limited to the hardware internal FIFO size.
46:51	RWX	INT_VC_IRQ_CONFIG_1_MEM_SIZE: Defines the size of the memory backing store, power of 2^(n+12) memory size.
52	RWX	INT_VC_IRQ_CONFIG_1_Reserved_52: Spare bit.
53:55	RWX	INT_VC_IRQ_CONFIG_1_NB_WRITE_SLOT: Number of slots used for write.
56	RWX	INT_VC_IRQ_CONFIG_1_Reserved_56: Spare bit.
57:59	RWX	INT_VC_IRQ_CONFIG_1_NB_CLEAN_SLOT: Number of slots that will be kept clean.
60	RWX	INT_VC_IRQ_CONFIG_1_FULL_WRITEBACK_ENABLE: Full Writeback enable. When set, all lines are written back to system memory.
61	ROX	INT_VC_IRQ_CONFIG_1_QUEUE_NOT_EMPTY: Queue is not empty.
62	ROX	INT_VC_IRQ_CONFIG_1_CREDIT_UPDATE_PENDING: A credit update is pending.
63	ROX_CLRPART	INT_VC_IRQ_CONFIG_1_FIFO_FULL: Set by hardware when the fifo is full. Cleared on read.

Register Name	IRQ Configuration 2 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_CONFIG_2
Address	000000000501320A (SCOM)
Description	This register holds the configuration for each Interrupt Request Queue. n = 0: IPI queue n = 1: Hardware queue n = 2: First level escalate queue n = 3: Second level escalate queue n = 4: Redistribution queue n = 5: IPI cascaded queue. MMIO offsets = 0x840, 0x848, 0x850, 0x858, 0x860, 0x868

Bits	SCOM	Field Mnemonic: Description
0:20	RWX	INT_VC_IRQ_CONFIG_2_Reserved_0_20: Spare bits.
21:26	RWX	INT_VC_IRQ_CONFIG_2_PREFETCH_DISTANCE: Defines, in multiple of two int triggers, the maximum distance between prefetch and demand.
27:31	RWX	INT_VC_IRQ_CONFIG_2_MAX_CRD_TO_CQ: Max number of interrupt credits given to CQ.
32:34	RWX	INT_VC_IRQ_CONFIG_2_Reserved_32_34: Spare bits.
35:39	RWX	INT_VC_IRQ_CONFIG_2_MAX_CRD_TO_PC: Max number of interrupt credits given to PC. Reset value is 0xF for IPI and redistribution queues, 0 for other queues as PC never issues interrupt requests to these queues.
40:41	RWX	INT_VC_IRQ_CONFIG_2_Reserved_40_41: Spare bits.
42	RWX	INT_VC_IRQ_CONFIG_2_PREFETCH_DISABLE: When set, IRQ never issue IVC/SBC prefetch lookup operation.
43	RWX	INT_VC_IRQ_CONFIG_2_QUEUE_DISABLE: When set, IRQ does not forward any EQ trigger to EQC.
44	RWX	INT_VC_IRQ_CONFIG_2_IVC_INTF_DISABLE: When set, IRQ to IVC lookup interface is disabled.
45	RWX	INT_VC_IRQ_CONFIG_2_ENABLE_MEMORY_BACKING: When 0, IRQ does not use system memory as internal FIFO extension. The FIFO is limited to the hardware internal FIFO size.
46:51	RWX	INT_VC_IRQ_CONFIG_2_MEM_SIZE: Defines the size of the memory backing store, power of 2^(n+12) memory size.
52	RWX	INT_VC_IRQ_CONFIG_2_Reserved_52: Spare bit.
53:55	RWX	INT_VC_IRQ_CONFIG_2_NB_WRITE_SLOT: Number of slots used for write.
56	RWX	INT_VC_IRQ_CONFIG_2_Reserved_56: Spare bit.
57:59	RWX	INT_VC_IRQ_CONFIG_2_NB_CLEAN_SLOT: Number of slots that will be kept clean.
60	RWX	INT_VC_IRQ_CONFIG_2_FULL_WRITEBACK_ENABLE: Full Writeback enable. When set, all lines are written back to system memory.
61	ROX	INT_VC_IRQ_CONFIG_2_QUEUE_NOT_EMPTY: Queue is not empty.
62	ROX	INT_VC_IRQ_CONFIG_2_CREDIT_UPDATE_PENDING: A credit update is pending.
63	ROX_CLRPART	INT_VC_IRQ_CONFIG_2_FIFO_FULL: Set by hardware when the fifo is full. Cleared on read.

Register Name	IRQ Configuration 3 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_CONFIG_3
Address	000000000501320B (SCOM)
Description	This register holds the configuration for each Interrupt Request Queue. n = 0: IPI queue n = 1: Hardware queue n = 2: First level escalate queue n = 3: Second level escalate queue n = 4: Redistribution queue n = 5: IPI cascaded queue. MMIO offsets = 0x840, 0x848, 0x850, 0x858, 0x860, 0x868

Bits	SCOM	Field Mnemonic: Description
0:20	RWX	INT_VC_IRQ_CONFIG_3_Reserved_0_20: Spare bits.
21:26	RWX	INT_VC_IRQ_CONFIG_3_PREFETCH_DISTANCE: Defines, in multiple of two int triggers, the maximum distance between prefetch and demand.
27:31	RWX	INT_VC_IRQ_CONFIG_3_MAX_CRD_TO_CQ: Max number of interrupt credits given to CQ.
32:34	RWX	INT_VC_IRQ_CONFIG_3_Reserved_32_34: Spare bits.
35:39	RWX	INT_VC_IRQ_CONFIG_3_MAX_CRD_TO_PC: Max number of interrupt credits given to PC. Reset value is 0xF for IPI and redistribution queues, 0 for other queues as PC never issues interrupt requests to these queues.
40:41	RWX	INT_VC_IRQ_CONFIG_3_Reserved_40_41: Spare bits.
42	RWX	INT_VC_IRQ_CONFIG_3_PREFETCH_DISABLE: When set, IRQ never issue IVC/SBC prefetch lookup operation.
43	RWX	INT_VC_IRQ_CONFIG_3_QUEUE_DISABLE: When set, IRQ does not forward any EQ trigger to EQC.
44	RWX	INT_VC_IRQ_CONFIG_3_IVC_INTF_DISABLE: When set, IRQ to IVC lookup interface is disabled.
45	RWX	INT_VC_IRQ_CONFIG_3_ENABLE_MEMORY_BACKING: When 0, IRQ does not use system memory as internal FIFO extension. The FIFO is limited to the hardware internal FIFO size.
46:51	RWX	INT_VC_IRQ_CONFIG_3_MEM_SIZE: Defines the size of the memory backing store, power of 2^(n+12) memory size.
52	RWX	INT_VC_IRQ_CONFIG_3_Reserved_52: Spare bit.
53:55	RWX	INT_VC_IRQ_CONFIG_3_NB_WRITE_SLOT: Number of slots used for write.
56	RWX	INT_VC_IRQ_CONFIG_3_Reserved_56: Spare bit.
57:59	RWX	INT_VC_IRQ_CONFIG_3_NB_CLEAN_SLOT: Number of slots that will be kept clean.
60	RWX	INT_VC_IRQ_CONFIG_3_FULL_WRITEBACK_ENABLE: Full Writeback enable. When set, all lines are written back to system memory.
61	ROX	INT_VC_IRQ_CONFIG_3_QUEUE_NOT_EMPTY: Queue is not empty.
62	ROX	INT_VC_IRQ_CONFIG_3_CREDIT_UPDATE_PENDING: A credit update is pending.
63	ROX_CLRPART	INT_VC_IRQ_CONFIG_3_FIFO_FULL: Set by hardware when the fifo is full. Cleared on read.

Register Name	IRQ Configuration 4 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_CONFIG_4
Address	000000000501320C (SCOM)
Description	This register holds the configuration for each Interrupt Request Queue. n = 0: IPI queue n = 1: Hardware queue n = 2: First level escalate queue n = 3: Second level escalate queue n = 4: Redistribution queue n = 5: IPI cascaded queue. MMIO offsets = 0x840, 0x848, 0x850, 0x858, 0x860, 0x868

Bits	SCOM	Field Mnemonic: Description
0:20	RWX	INT_VC_IRQ_CONFIG_4_Reserved_0_20: Spare bits.
21:26	RWX	INT_VC_IRQ_CONFIG_4_PREFETCH_DISTANCE: Defines, in multiple of two int triggers, the maximum distance between prefetch and demand.
27:31	RWX	INT_VC_IRQ_CONFIG_4_MAX_CRD_TO_CQ: Max number of interrupt credits given to CQ.
32:34	RWX	INT_VC_IRQ_CONFIG_4_Reserved_32_34: Spare bits.
35:39	RWX	INT_VC_IRQ_CONFIG_4_MAX_CRD_TO_PC: Max number of interrupt credits given to PC. Reset value is 0xF for IPI and redistribution queues, 0 for other queues as PC never issues interrupt requests to these queues.
40:41	RWX	INT_VC_IRQ_CONFIG_4_Reserved_40_41: Spare bits.
42	RWX	INT_VC_IRQ_CONFIG_4_PREFETCH_DISABLE: When set, IRQ never issue IVC/SBC prefetch lookup operation.
43	RWX	INT_VC_IRQ_CONFIG_4_QUEUE_DISABLE: When set, IRQ does not forward any EQ trigger to EQC.
44	RWX	INT_VC_IRQ_CONFIG_4_IVC_INTF_DISABLE: When set, IRQ to IVC lookup interface is disabled.
45	RWX	INT_VC_IRQ_CONFIG_4_ENABLE_MEMORY_BACKING: When 0, IRQ does not use system memory as internal FIFO extension. The FIFO is limited to the hardware internal FIFO size.
46:51	RWX	INT_VC_IRQ_CONFIG_4_MEM_SIZE: Defines the size of the memory backing store, power of 2^(n+12) memory size.
52	RWX	INT_VC_IRQ_CONFIG_4_Reserved_52: Spare bit.
53:55	RWX	INT_VC_IRQ_CONFIG_4_NB_WRITE_SLOT: Number of slots used for write.
56	RWX	INT_VC_IRQ_CONFIG_4_Reserved_56: Spare bit.
57:59	RWX	INT_VC_IRQ_CONFIG_4_NB_CLEAN_SLOT: Number of slots that will be kept clean.
60	RWX	INT_VC_IRQ_CONFIG_4_FULL_WRITEBACK_ENABLE: Full Writeback enable. When set, all lines are written back to system memory.
61	ROX	INT_VC_IRQ_CONFIG_4_QUEUE_NOT_EMPTY: Queue is not empty.
62	ROX	INT_VC_IRQ_CONFIG_4_CREDIT_UPDATE_PENDING: A credit update is pending.
63	ROX_CLRPART	INT_VC_IRQ_CONFIG_4_FIFO_FULL: Set by hardware when the fifo is full. Cleared on read.

Register Name	IRQ Configuration 5 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_CONFIG_5
Address	000000000501320D (SCOM)
Description	This register holds the configuration for each Interrupt Request Queue. n = 0: IPI queue n = 1: Hardware queue n = 2: First level escalate queue n = 3: Second level escalate queue n = 4: Redistribution queue n = 5: IPI cascaded queue. MMIO offsets = 0x840, 0x848, 0x850, 0x858, 0x860, 0x868

Bits	SCOM	Field Mnemonic: Description
0:20	RWX	INT_VC_IRQ_CONFIG_5_Reserved_0_20: Spare bits.
21:26	RWX	INT_VC_IRQ_CONFIG_5_PREFETCH_DISTANCE: Defines, in multiple of two int triggers, the maximum distance between prefetch and demand.
27:31	RWX	INT_VC_IRQ_CONFIG_5_MAX_CRD_TO_CQ: Max number of interrupt credits given to CQ.
32:34	RWX	INT_VC_IRQ_CONFIG_5_Reserved_32_34: Spare bits.
35:39	RWX	INT_VC_IRQ_CONFIG_5_MAX_CRD_TO_PC: Max number of interrupt credits given to PC. Reset value is 0xF for IPI and redistribution queues, 0 for other queues as PC never issues interrupt requests to these queues.
40:41	RWX	INT_VC_IRQ_CONFIG_5_Reserved_40_41: Spare bits.
42	RWX	INT_VC_IRQ_CONFIG_5_PREFETCH_DISABLE: When set, IRQ never issue IVC/SBC prefetch lookup operation.
43	RWX	INT_VC_IRQ_CONFIG_5_QUEUE_DISABLE: When set, IRQ does not forward any EQ trigger to EQC.
44	RWX	INT_VC_IRQ_CONFIG_5_IVC_INTF_DISABLE: When set, IRQ to IVC lookup interface is disabled.
45	RWX	INT_VC_IRQ_CONFIG_5_ENABLE_MEMORY_BACKING: When 0, IRQ does not use system memory as internal FIFO extension. The FIFO is limited to the hardware internal FIFO size.
46:51	RWX	INT_VC_IRQ_CONFIG_5_MEM_SIZE: Defines the size of the memory backing store, power of 2^(n+12) memory size.
52	RWX	INT_VC_IRQ_CONFIG_5_Reserved_52: Spare bit.
53:55	RWX	INT_VC_IRQ_CONFIG_5_NB_WRITE_SLOT: Number of slots used for write.
56	RWX	INT_VC_IRQ_CONFIG_5_Reserved_56: Spare bit.
57:59	RWX	INT_VC_IRQ_CONFIG_5_NB_CLEAN_SLOT: Number of slots that will be kept clean.
60	RWX	INT_VC_IRQ_CONFIG_5_FULL_WRITEBACK_ENABLE: Full Writeback enable. When set, all lines are written back to system memory.
61	ROX	INT_VC_IRQ_CONFIG_5_QUEUE_NOT_EMPTY: Queue is not empty.
62	ROX	INT_VC_IRQ_CONFIG_5_CREDIT_UPDATE_PENDING: A credit update is pending.
63	ROX_CLRPART	INT_VC_IRQ_CONFIG_5_FIFO_FULL: Set by hardware when the fifo is full. Cleared on read.

Register Name	IRQ to EQC Credits and Priority Management Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_TO_EQC_CREDITS
Address	000000000501320E (SCOM)
Description	Defines how the interface between IRQs and EQC behaves.

Bits	SCOM	Field Mnemonic: Description
0:2	RWX	INT_VC_IRQ_TO_EQC_CREDITS_IPI_PRIORITY: Defines priority for IPI queue (0 is the highest, 4 is the lowest, encoding 5 to 7 leads to priority 4). If multiple queues have same priority, round. robin is used to select which one to serve.
3:7	RWX	INT_VC_IRQ_TO_EQC_CREDITS_IPI_RSD_CREDITS: Define number of Reserved credits for IPI queue. Reserved credits are consumed first. If there is no longer Reserved credits, credits are consumed. from the pool.
8:10	RWX	INT_VC_IRQ_TO_EQC_CREDITS_HWD_PRIORITY: Same for hardware queue.
11:15	RWX	INT_VC_IRQ_TO_EQC_CREDITS_HWD_RSD_CREDITS: Same for hardware queue.
16:18	RWX	INT_VC_IRQ_TO_EQC_CREDITS_ESC1_PRIORITY: Same for first level escalate queue.
19:23	RWX	INT_VC_IRQ_TO_EQC_CREDITS_ESC1_RSD_CREDITS: Same for first level escalate queue.
24:26	RWX	INT_VC_IRQ_TO_EQC_CREDITS_ESC2_PRIORITY: Same for second level escalate queue.
27:31	RWX	INT_VC_IRQ_TO_EQC_CREDITS_ESC2_RSD_CREDITS: Same for second level escalate queue.
32:34	RWX	INT_VC_IRQ_TO_EQC_CREDITS_REDIS_PRIORITY: Same for redistribution queue.
35:39	RWX	INT_VC_IRQ_TO_EQC_CREDITS_REDIS_RSD_CREDITS: Same for redistribution queue.
40:42	RWX	INT_VC_IRQ_TO_EQC_CREDITS_Reserved_40_42: Spare bits.
43:47	RWX	INT_VC_IRQ_TO_EQC_CREDITS_POOL_CREDITS: Pool of credits that may be used when there is no longer Reserved credits available.
48:63	RO	Constant = 0b0000000000000000

Register Name	Maximum Number of Outstanding EQC Outbound Requests Register
Mnemonic	INT.INT_VC.INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD
Address	0000000005013210 (SCOM)
Description	Defines the maximum number of outstanding requests that EQC may issue. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:17	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_Reserved_0_17: Spare.
18:23	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_CI_STORE: CI store requests (Interrupt trigger forwarding).
24:25	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_Reserved_24_25: Spare.
26:31	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_INT_REQUEST: EQC: Interrupt request.
32:33	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_Reserved_32_33: Spare.
34:39	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_EQ_POST: EQC: EQ post.
40:41	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_Reserved_40_41: Spare.
42:47	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_CI_LOAD: EQC: Remote or local CI load request.
48:49	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_Reserved_48_49: Spare.
50:55	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_EQD_DMA_READ: EQC: EQD DMA Read.
56:57	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_Reserved_56_57: Spare.
58:63	RWX	INT_VC_MAX_OUTSTANDING_EQC_OUTB_CMD_EQD_DMA_WRITE: EQC: EQD DMA Write.

Register Name	EQC Cache Enable Register
Mnemonic	INT.INT_VC.INT_VC_EQC_CACHE_EN
Address	0000000005013211 (SCOM)
Description	This register enables EQC cache. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX	INT_VC_EQC_CACHE_EN_CACHE_ENABLE: 16-bit cache enable (one bit per blockid). May be cleared by scrub engine at flush completion.
16:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	EQC Cache Scrub Trigger Register
Mnemonic	INT.INT_VC.INT_VC_EQC_SCRUB_TRIG
Address	0000000005013212 (SCOM)
Description	This register, along with scrub mask register, is used by Software to trigger a cache scrub. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_VC_EQC_SCRUB_TRIG_VALID: Scrub request. Set by Software to initiate a cache scrub. Reset by hardware when flush operation is completed.
1	RWX	INT_VC_EQC_SCRUB_TRIG_WANT_CACHE_DISABLE: Want cache disable. When set, cache is disabled for the selected blockid(s) at the end of scrub operation.
2	RWX	INT_VC_EQC_SCRUB_TRIG_WANT_INVALIDATE: Want invalidate. 0: Modified entries are written back. State is switched to exclusive. 1: Exclusive entries are switched to invalidate. Modified entries are written back, state is switched to invalidate.
3:27	RO	Constant = 0b00000000000000000000000000
28:31	RWX	INT_VC_EQC_SCRUB_TRIG_BLOCKID: 4-bit scrub blockid.
32:39	RWX	INT_VC_EQC_SCRUB_TRIG_Reserved_32_39: Spare.
40:63	RWX	INT_VC_EQC_SCRUB_TRIG_OFFSET: 24-bit scrub offset.

Register Name	EQC Cache Scrub Mask Register
Mnemonic	INT.INT_VC.INT_VC_EQC_SCRUB_MASK
Address	0000000005013213 (SCOM)
Description	This register defines the block ids and offsets that need to be scrubbed. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:27	RO	Constant = 0b00000000000000000000000000
28:31	RWX	INT_VC_EQC_SCRUB_MASK_BLOCKID_MASK: 4-bit scrub blockid mask. 0:means ignores the corresponding blockid bit.
32:39	RWX	INT_VC_EQC_SCRUB_MASK_Reserved_32_39: Spare.
40:63	RWX	INT_VC_EQC_SCRUB_MASK_OFFSET_MASK: 24-bit scrub offset mask. 0:means ignores the corresponding offset bit.

Register Name	EQC Configuration Register
Mnemonic	INT.INT_VC.INT_VC_EQC_CONFIG
Address	0000000005013214 (SCOM)
Description	Defines global EQC configuration. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:31	RWX	INT_VC_EQC_CONFIG_PAGE_OFFSET_CFG: Defines which page offset to use when an EQ trigger has to be forwarded to another VC in the system. This field has 8 x 2-bit Encoding. "00" = Use offset 0x800 (goes to IPI queue). "01" = Use offset 0x880 (goes to HW queue). "10" = Use offset 0x900 (goes to 1esc queue). "11" = Use offset 0x980 (goes to 2esc queue). Note that if the EQ trigger comes from the redistribution queue, it is forwarded to redistribution queue using page offset 0xA00. bits 16:17 are used when EQ trigger comes from IPI. bits 18:19 are used when EQ trigger comes from HW. bits 20:21 are used when EQ trigger comes from 1esc. bits 22:23 are used when EQ trigger comes from 2esc. bits 24:25 are used when escalate is required and EQD H/W Dependent field(0:1) = "00". bits 26:27 are used when escalate is required and EQD H/W Dependent field(0:1) = "01". bits 28:29 are used when escalate is required and EQD H/W Dependent field(0:1) = "10". bits 30:31 are used when escalate is required and EQD H/W Dependent field(0:1) = "11".
32:36	RWX	INT_VC_EQC_CONFIG_SYNC_DONE: 5-bit sync done. Cleared by Software. Set by hardware when sync operation is completed (32:ipi, 33:hw, 34:1esc, 35:2esc, 36:redistrib).
37:45	RWX	INT_VC_EQC_CONFIG_Reserved_37_45: Spare bits.
46:51	RWX	INT_VC_EQC_CONFIG_MAX_PTAG_IN_USE: Defines the maximum number of ptag to be used.
52:55	RWX	INT_VC_EQC_CONFIG_BG_SCAN_RATE: 4-bit scrub background scan rate. 0:disable scan. Otherwise, scan rate = 2**n clock cycles (max of 16 micro-seconds).
56:58	RWX	INT_VC_EQC_CONFIG_Reserved_56_58: Spare bits.
59:63	RWX	INT_VC_EQC_CONFIG_MAX_ENTRIES_IN_MODIFIED: 5-bit Max number of entries per set in modified state.

Register Name	EQC Cache Watch Specification Register
Mnemonic	INT.INT_VC.INT_VC_EQC_CACHE_WATCH_SPEC
Address	0000000005013215 (SCOM)
Description	This register along with cache watch data registers are used to Read and Write EQDs. Software specifies the EQD blockid and offset it wants to access. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0	NCX	INT_VC_EQC_CACHE_WATCH_SPEC_CONFLICT: Conflict: Forced to 0 when Software writes the register. Set to one by hardware if an internal EQC process references this EQD and its valid bit is on. during the Software ReadModifyWrite sequence.
1:7	RWX	INT_VC_EQC_CACHE_WATCH_SPEC_Reserved_1_7: Spare.

Bits	SCOM	Field Mnemonic: Description
8	RWX	INT_VC_EQC_CACHE_WATCH_SPEC_FULL: Full - if set to a one, then the contents of all data register fields replace the corresponding specified structure fields as long as the conflict bit. is zero, else the structure is not modified; if "F" is set to a zero, then only the contents of data register fields that are hardware read-only. replace the corresponding specific structure fields (words 0 and 2-7), regardless of the state of the conflict bit.
9:27	RWX	INT_VC_EQC_CACHE_WATCH_SPEC_Reserved_9_27: Spare.
28:31	RWX	INT_VC_EQC_CACHE_WATCH_SPEC_BLOCKID: 4-bit blockid.
32:39	RWX	INT_VC_EQC_CACHE_WATCH_SPEC_Reserved_32_39: Spare.
40:63	RWX	INT_VC_EQC_CACHE_WATCH_SPEC_OFFSET: 24-bit EQD offset.

Register Name	**EQC Cache Watch Data 0 Register**
Mnemonic	INT.INT_VC.INT_VC_EQC_CACHE_WATCH_DATA0
Address	0000000005013216 (SCOM)
Description	Data register 0 holds EQD words 0 and 1. Data register 1 holds EQD words 2 and 3. Data register 2 holds EQD words 4 and 5. Data register 3 holds EQD words 6 and 7. These registers are located in EQC sub-unit. ,0x938,0x940,0x948

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	INT_VC_EQC_CACHE_WATCH_DATA0_DATA: Read Modify Write operation : - Software writes cache watch specification register. This clears the Conflict bit. - Software does CI load of the data register 0. This triggers an internal read request of the targeted data defined in cache watch specification. register. - When the internal read operation is completed, data is loaded into the cache watch data registers. - CI load response is generated. - Software may issue CI load of data registers 1 to 3 to get full data. - Software optionally does CI store of data registers 1 to 3. - Software write data register 0. - The write to register 0 triggers an internal write of the EQD defined in cache watch specification register. - The write operation is aborted if the hardware had set the "Conflict" bit and "Full" bit was 1. - Software reads the cache watch specification register. If C = 1 and F = 1 then Software has to retry the full sequence.

Register Name	**EQC Cache Watch Data 1 Register**
Mnemonic	INT.INT_VC.INT_VC_EQC_CACHE_WATCH_DATA1
Address	0000000005013217 (SCOM)
Description	Data register 0 holds EQD words 0 and 1. Data register 1 holds EQD words 2 and 3. Data register 2 holds EQD words 4 and 5. Data register 3 holds EQD words 6 and 7. These registers are located in EQC sub-unit. ,0x938,0x940,0x948

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	INT_VC_EQC_CACHE_WATCH_DATA1_DATA: Read Modify Write operation : - Software writes cache watch specification register. This clears the Conflict bit. - Software does CI load of the data register 0. This triggers an internal read request of the targeted data defined in cache watch specification. register. - When the internal read operation is completed, data is loaded into the cache watch data registers. - CI load response is generated. - Software may issue CI load of data registers 1 to 3 to get full data. - Software optionally does CI store of data registers 1 to 3. - Software write data register 0. - The write to register 0 triggers an internal write of the EQD defined in cache watch specification register. - The write operation is aborted if the hardware had set the "Conflict" bit and "Full" bit was 1. - Software reads the cache watch specification register. If C = 1 and F = 1 then Software has to retry the full sequence.

Register Name	EQC Cache Watch Data 2 Register
Mnemonic	INT.INT_VC.INT_VC_EQC_CACHE_WATCH_DATA2
Address	0000000005013218 (SCOM)
Description	Data register 0 holds EQD words 0 and 1. Data register 1 holds EQD words 2 and 3. Data register 2 holds EQD words 4 and 5. Data register 3 holds EQD words 6 and 7. These registers are located in EQC sub-unit. ,0x938,0x940,0x948

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	INT_VC_EQC_CACHE_WATCH_DATA2_DATA: Read Modify Write operation : - Software writes cache watch specification register. This clears the Conflict bit. - Software does CI load of the data register 0. This triggers an internal read request of the targeted data defined in cache watch specification. register. - When the internal read operation is completed, data is loaded into the cache watch data registers. - CI load response is generated. - Software may issue CI load of data registers 1 to 3 to get full data. - Software optionally does CI store of data registers 1 to 3. - Software write data register 0. - The write to register 0 triggers an internal write of the EQD defined in cache watch specification register. - The write operation is aborted if the hardware had set the "Conflict" bit and "Full" bit was 1. - Software reads the cache watch specification register. If C = 1 and F = 1 then Software has to retry the full sequence.

Register Name	EQC Cache Watch Data 3 Register
Mnemonic	INT.INT_VC.INT_VC_EQC_CACHE_WATCH_DATA3
Address	0000000005013219 (SCOM)
Description	Data register 0 holds EQD words 0 and 1. Data register 1 holds EQD words 2 and 3. Data register 2 holds EQD words 4 and 5. Data register 3 holds EQD words 6 and 7. These registers are located in EQC sub-unit. ,0x938,0x940,0x948

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	INT_VC_EQC_CACHE_WATCH_DATA3_DATA: Read Modify Write operation : - Software writes cache watch specification register. This clears the Conflict bit. - Software does CI load of the data register 0. This triggers an internal read request of the targeted data defined in cache watch specification. register. - When the internal read operation is completed, data is loaded into the cache watch data registers. - CI load response is generated. - Software may issue CI load of data registers 1 to 3 to get full data. - Software optionally does CI store of data registers 1 to 3. - Software write data register 0. - The write to register 0 triggers an internal write of the EQD defined in cache watch specification register. - The write operation is aborted if the hardware had set the "Conflict" bit and "Full" bit was 1. - Software reads the cache watch specification register. If C = 1 and F = 1 then Software has to retry the full sequence.

Register Name	EQC Debug Register
Mnemonic	INT.INT_VC.INT_VC_EQC_DEBUG
Address	000000000501321A (SCOM)
Description	This register holds ECC errors correction/injection and some EQC debug features. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:32	RWX	INT_VC_EQC_DEBUG_Reserved_0_32: Spare.
33	RWX	INT_VC_EQC_DEBUG_DIS_ARX_ECC_CORRECTION: Disable ARX interface ECC correction.
34:41	RWX	INT_VC_EQC_DEBUG_DIS_TAG_ECC_CORRECTION: Disable TAG [0:7] arrays ECC correction.
42:43	RWX	INT_VC_EQC_DEBUG_DIS_STATE_ECC_CORRECTION: Disable STATE [0:1] array ECC correction.
44	RWX	INT_VC_EQC_DEBUG_DIS_CTRLBUF_ECC_CORRECTION: Disable P1 CTRL array ECC correction.
45:48	RWX	INT_VC_EQC_DEBUG_DIS_DATA_ECC_CORRECTION: Disable P1 DATA [0:3] array ECC correction.
49	RWX	INT_VC_EQC_DEBUG_FORCE_SINGLE_BIT_ECC_ERR: Force single bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain lsb bit is flipped).
50	RWX	INT_VC_EQC_DEBUG_FORCE_DOUBLE_BIT_ECC_ERR: Force double bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain 2 lsb bits are flipped).
51:55	RWX	INT_VC_EQC_DEBUG_ECC_ERR_INJ_ARRAY_SEL: Array selection for ECC error injection. 00 xxx P0 TAG arrays. xxx = 0 to 7. 01 00x P0 STATE arrays x = 0-1. 10 000 P1 CTRL array. 11 xxy P1 data ecc xx = array 0 to 3, y = -left ecc/+right ecc.
56	RWX	INT_VC_EQC_DEBUG_TRACE_ENABLE: Enable EQC trace bus.
57:58	RWX	INT_VC_EQC_DEBUG_Reserved_57_58: Spare.
59	RWX	INT_VC_EQC_DEBUG_Reserved_59: Spare bit.
60	RWX	INT_VC_EQC_DEBUG_USE_WATCH_TO_READ_CTRL_ARY: Use watch engine to read cache control arrays. When set, a cache watch read is replaced by a read of the cache control arrays. In such case, Cache Watch Address reg (54-59) define set index.
61:63	RWX	INT_VC_EQC_DEBUG_CACHE_CTRL_ARY_SELECT: When bit 60 is set, this field defines which cache control arrays to read. 000 Tag A. Watch data reg 0 [9:31] = TAG0. Watch data reg 0 [41:63] = TAG1. Watch data reg 1 [9:31] = TAG8.

Bits	SCOM	Field Mnemonic: Description
		Watch data reg 1 [41:63] = TAG9. Watch data reg 2 [9:31] = TAG16. Watch data reg 2 [41:63] = TAG17. Watch data reg 3 [9:31] = TAG24. Watch data reg 3 [41:63] = TAG25. 001 Tag B. Watch data reg 0 [9:31] = TAG2. Watch data reg 0 [41:63] = TAG3. Watch data reg 1 [9:31] = TAG10. Watch data reg 1 [41:63] = TAG11. Watch data reg 2 [9:31] = TAG18. Watch data reg 2 [41:63] = TAG19. Watch data reg 3 [9:31] = TAG26. Watch data reg 3 [41:63] = TAG27. 010 Tag C. Watch data reg 0 [9:31] = TAG4. Watch data reg 0 [41:63] = TAG5. Watch data reg 1 [9:31] = TAG12. Watch data reg 1 [41:63] = TAG13. Watch data reg 2 [9:31] = TAG20. Watch data reg 2 [41:63] = TAG21. Watch data reg 3 [9:31] = TAG28. Watch data reg 3 [41:63] = TAG29. 011 Tag D. Watch data reg 0 [9:31] = TAG6. Watch data reg 0 [41:63] = TAG7. Watch data reg 1 [9:31] = TAG14. Watch data reg 1 [41:63] = TAG15. Watch data reg 2 [9:31] = TAG22. Watch data reg 2 [41:63] = TAG23. Watch data reg 3 [9:31] = TAG30. Watch data reg 3 [41:63] = TAG31. 1xx Tag State + LRU. Watch data reg 1 = STATE(0 to 15). Watch data reg 2 = STATE(16 to 31). Watch data reg 3 [32:63] = LRU(0 to 31).

Register Name	Maximum Number of Outstanding IVC Outbound Requests Register
Mnemonic	INT.INT_VC.INT_VC_MAX_OUTSTANDING_IVC_CMD
Address	0000000005013220 (SCOM)
Description	Defines the maximum number of outstanding requests that IVC may issue. This register is located in IVC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	RWX	INT_VC_MAX_OUTSTANDING_IVC_CMD_Reserved_48_50: Spare.
51:55	RWX	INT_VC_MAX_OUTSTANDING_IVC_CMD_SBC_LOOKUP: SBC lookup.
56:58	RWX	INT_VC_MAX_OUTSTANDING_IVC_CMD_Reserved_56_58: Spare.
59:63	RWX	INT_VC_MAX_OUTSTANDING_IVC_CMD_DMA_READ: DMA Read.

Register Name	IVC Cache Enable Register
Mnemonic	INT.INT_VC.INT_VC_IVC_CACHE_EN
Address	0000000005013221 (SCOM)
Description	This register enables IVC cache. This register is located in IVC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX	INT_VC_IVC_CACHE_EN_CACHE_ENABLE: 16-bit cache enable (one bit per blockid). May be cleared by scrub engine at flush completion.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	IVC Cache Scrub Trigger Register
Mnemonic	INT.INT_VC.INT_VC_IVC_SCRUB_TRIG
Address	0000000005013222 (SCOM)
Description	This register, along with scrub mask register, is used by Software to trigger a cache scrub. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_VC_IVC_SCRUB_TRIG_VALID: Scrub request. Set by Software to initiate a cache scrub. Reset by hardware when flush operation is completed.
1	RWX	INT_VC_IVC_SCRUB_TRIG_WANT_CACHE_DISABLE: Want cache disable. When set, cache is disabled for the selected blockid(s) at the end of scrub operation.
2:27	RO	Constant = 0b00000000000000000000000000
28:31	RWX	INT_VC_IVC_SCRUB_TRIG_BLOCKID: 4-bit scrub blockid.
32:35	RWX	INT_VC_IVC_SCRUB_TRIG_Reserved_32_35: Spare.
36:63	RWX	INT_VC_IVC_SCRUB_TRIG_OFFSET: 28-bit scrub offset.

Register Name	IVC Cache Scrub Mask Register
Mnemonic	INT.INT_VC.INT_VC_IVC_SCRUB_MASK
Address	0000000005013223 (SCOM)
Description	This register defines the block ids and offsets that need to be scrubbed. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:27	RO	Constant = 0b00000000000000000000000000
28:31	RWX	INT_VC_IVC_SCRUB_MASK_BLOCKID_MASK: 4-bit scrub blockid mask. 0:means ignores the corresponding blockid bit.
32:35	RWX	INT_VC_IVC_SCRUB_MASK_Reserved_32_35: Spare.
36:63	RWX	INT_VC_IVC_SCRUB_MASK_OFFSET_MASK: 28-bit scrub offset mask. 0:means ignores the corresponding offset bit.

Register Name	IVC Cache Watch Address Register
Mnemonic	INT.INT_VC.INT_VC_IVC_CACHE_WATCH_ADDR
Address	0000000005013225 (SCOM)
Description	This register along with cache watch data register is used in debug mode to allow Software to read the cache control arrays. This register is located in IVC sub-unit. MMIO offset = 0x9A8

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54:59	RWX	INT_VC_IVC_CACHE_WATCH_ADDR_SET_INDEX: 6-bit Set index.
60:63	RO	Constant = 0b0000

Register Name	IVC Cache Watch Data Register
Mnemonic	INT.INT_VC.INT_VC_IVC_CACHE_WATCH_DATA
Address	0000000005013226 (SCOM)
Description	This register is used in debug mode to allow Software to read the cache control arrays. This register is located in IVC sub-unit. MMIO offset = 0x9B0

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	INT_VC_IVC_CACHE_WATCH_DATA_DATA: Watch data. Software does CI load of the watch data register. This triggers an internal read request of the targeted array. When the internal read operation is completed, data is loaded into the cache watch data register and CI load response is generated.

Register Name	IVC Hash 1 Register
Mnemonic	INT.INT_VC.INT_VC_IVC_HASH_1
Address	0000000005013227 (SCOM)
Description	The IVC hash registers holds 7-bit hash configuration field for each possible hardware source and for IPI interrupts. This allows Software to limit the number of set indexes an interrupt source may use. The 7-bit encoding is : 1xxxxxx - 1 set - xxxxxx indicates the 6-bit set index. 01yyyyy - 2 sets - yyyyy indicates the 5-bit MSB set index, 1 LSB filled in using IVE offset(27). 001zzzz - 4 sets - zzzz indicated the 4-bit MSB set index, 2 LSBs filled in using IVE offset(26 to 27). 0001xxx - 8 sets - xxx indicates the 3-bit MSB set index, 3 LSBs filled in using IVE offset(25 to 27). 00001yy - 16 sets - yy indicates the 2-bit MSB set index, 4 LSBs filled in using IVE offset(24 to 27). 000001z - 32 sets - z indicates the MSB set index, 5 LSBs filled in using IVE offset(23 to 27). 000000x - 64 sets - set index bits filled in using IVE offset(22 to 27). This register is located in IVC sub-unit. MMIO offset = 0x9B8

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_VC_IVC_HASH_1_Reserved_0: Spare.
1:7	RWX	INT_VC_IVC_HASH_1_HWD_0: Hash configuration for hardware source 0.
8	RWX	INT_VC_IVC_HASH_1_Reserved_8: Spare.
9:15	RWX	INT_VC_IVC_HASH_1_HWD_1: Hash configuration for hardware source 1.
16	RWX	INT_VC_IVC_HASH_1_Reserved_16: Spare.
17:23	RWX	INT_VC_IVC_HASH_1_HWD_2: Hash configuration for hardware source 2.
24	RWX	INT_VC_IVC_HASH_1_Reserved_24: Spare.

Bits	SCOM	Field Mnemonic: Description
25:31	RWX	INT_VC_IVC_HASH_1_HWD_3: Hash configuration for hardware source 3.
32	RWX	INT_VC_IVC_HASH_1_Reserved_32: Spare.
33:39	RWX	INT_VC_IVC_HASH_1_HWD_4: Hash configuration for hardware source 4.
40	RWX	INT_VC_IVC_HASH_1_Reserved_40: Spare.
41:47	RWX	INT_VC_IVC_HASH_1_HWD_5: Hash configuration for hardware source 5.
48	RWX	INT_VC_IVC_HASH_1_Reserved_48: Spare.
49:55	RWX	INT_VC_IVC_HASH_1_HWD_6: Hash configuration for hardware source 6.
56	RWX	INT_VC_IVC_HASH_1_Reserved_56: Spare.
57:63	RWX	INT_VC_IVC_HASH_1_HWD_7: Hash configuration for hardware source 7.

Register Name	IVC Hash 2 Register
Mnemonic	INT.INT_VC.INT_VC_IVC_HASH_2
Address	0000000005013228 (SCOM)
Description	Refer to IVC hash register 1 description. This register is located in IVC sub-unit. MMIO offset = 0x9C0

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_VC_IVC_HASH_2_Reserved_0: Spare.
1:7	RWX	INT_VC_IVC_HASH_2_HWD_8: Hash configuration for hardware source 8.
8	RWX	INT_VC_IVC_HASH_2_Reserved_8: Spare.
9:15	RWX	INT_VC_IVC_HASH_2_HWD_9: Hash configuration for hardware source 9.
16	RWX	INT_VC_IVC_HASH_2_Reserved_16: Spare.
17:23	RWX	INT_VC_IVC_HASH_2_HWD_10: Hash configuration for hardware source 10.
24	RWX	INT_VC_IVC_HASH_2_Reserved_24: Spare.
25:31	RWX	INT_VC_IVC_HASH_2_HWD_11: Hash configuration for hardware source 11.
32	RWX	INT_VC_IVC_HASH_2_Reserved_32: Spare.
33:39	RWX	INT_VC_IVC_HASH_2_HWD_12: Hash configuration for hardware source 12.
40	RWX	INT_VC_IVC_HASH_2_Reserved_40: Spare.
41:47	RWX	INT_VC_IVC_HASH_2_HWD_13: Hash configuration for hardware source 13.
48	RWX	INT_VC_IVC_HASH_2_Reserved_48: Spare.
49:55	RWX	INT_VC_IVC_HASH_2_HWD_14: Hash configuration for hardware source 14.
56	RWX	INT_VC_IVC_HASH_2_Reserved_56: Spare.
57:63	RWX	INT_VC_IVC_HASH_2_HWD_15: Hash configuration for hardware source 15.

Register Name	IVC Hash 3 Register
Mnemonic	INT.INT_VC.INT_VC_IVC_HASH_3
Address	0000000005013229 (SCOM)
Description	Refer to IVC hash register 1 description. This register is located in IVC sub-unit. MMIO offset = 0x9C8

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_VC_IVC_HASH_3_Reserved_0: Spare.
1:7	RWX	INT_VC_IVC_HASH_3_IPI: Hash configuration for IPI queue.
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	IVC Debug Register
Mnemonic	INT.INT_VC.INT_VC_IVC_DEBUG
Address	000000000501322A (SCOM)
Description	This register holds ECC errors correction/injection and some IVC debug features. This register is located in IVC sub-unit. MMIO offset = 0x9D0

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Constant = 0b00000000000000000000000000000000
32	RWX	INT_VC_IVC_DEBUG_Reserved_32: Spare.
33:37	RWX	INT_VC_IVC_DEBUG_MAX_PTAG_IN_USE: Defines the maximum number of ptag to be used.
38:41	RWX	INT_VC_IVC_DEBUG_DIS_TAG_ECC_CORRECTION: Disable TAG [0:3] array ECC correction.
42	RWX	INT_VC_IVC_DEBUG_DIS_STATE_ECC_CORRECTION: Disable STATE array ECC correction.
43:44	RWX	INT_VC_IVC_DEBUG_Reserved_43_44: Spare.
45:46	RWX	INT_VC_IVC_DEBUG_DIS_DATA_ECC_CORRECTION: Disable P1 DATA [0:1] array ECC correction.
47:48	RWX	INT_VC_IVC_DEBUG_Reserved_47_48: Spare.
49	RWX	INT_VC_IVC_DEBUG_FORCE_SINGLE_BIT_ECC_ERR: Force single bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain lsb bit is flipped).
50	RWX	INT_VC_IVC_DEBUG_FORCE_DOUBLE_BIT_ECC_ERR: Force double bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain 2 lsb bits are flipped).
51:55	RWX	INT_VC_IVC_DEBUG_ECC_ERR_INJ_ARRAY_SEL: Array selection for ECC error injection. 00 xxy P0 TAG arrays. xx = SRAM# 0 to 3, y = -ECC0/+ECC1. 01 000 P0 STATE array. 11 000 P1 data 0. 11 001 P1 data 1.
56	RWX	INT_VC_IVC_DEBUG_TRACE_ENABLE: Enable IVC trace bus.
57:58	RWX	INT_VC_IVC_DEBUG_Reserved_57_58: Spare.
59	RWX	INT_VC_IVC_DEBUG_FAST_SB_LOOKUP_DISABLE: 0: IVC is able to trigger SB lookup before IVE DMA read completion. 1: IVC waits for DMA read completion to trigger SB lookup.
60:63	RWX	INT_VC_IVC_DEBUG_CACHE_CTRL_ARY_SELECT: Defines which cache control arrays to read during cache watch operation. Data watch register mapping. [0:31] [32:63]. 0000 STATE STATE. 0001 LRU x"0000"&LRU. 1xxx TAG TAG(2*xxx) TAG(2*xxx+1).

Register Name	AIB Timeout Register
Mnemonic	INT.INT_VC.INT_VC_AIB_TIMEOUT
Address	000000000501322B (SCOM)
Description	This register controls the watchdog timers used on any AIB outbound read operation issued by P3VC.

Bits	SCOM	Field Mnemonic: Description
0:57	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
58:63	RWX	INT_VC_AIB_TIMEOUT_DELAY: AIB Timeout is detected if AIB response comes later than 2**("delay"+4) x 3 clock cycles. In such case, a bit is set in FIR.

Register Name	AIB TX Command Ordering Tags 1 Register
Mnemonic	INT.INT_VC.INT_VC_AIB_TX_ORDERING_TAG_1
Address	000000000501322C (SCOM)
Description	This register holds the 8-bit AIB ordering tag to be used for each AIB TX commands.

Bits	SCOM	Field Mnemonic: Description
0:23	RO	Constant = 0b000000000000000000000000
24:31	RWX	INT_VC_AIB_TX_ORDERING_TAG_1_REGS_ORDERING_TAG: REGS: Registers read response.
32:39	RWX	INT_VC_AIB_TX_ORDERING_TAG_1_IRQ_ORDERING_TAG: IRQ: DMA Read/Write . 8-bit ordering tag is made of "5-bit configured tag and 3-bit Queue#" (bits 37:39 are overwritten by IRQ#).
40:47	RWX	INT_VC_AIB_TX_ORDERING_TAG_1_IVC_ORDERING_TAG: IVC: DMA Read.
48:55	RWX	INT_VC_AIB_TX_ORDERING_TAG_1_SBC_DMA_ORDERING_TAG: SBC: DMA Read/Write.
56:63	RWX	INT_VC_AIB_TX_ORDERING_TAG_1_SBC_EOI_ORDERING_TAG: SBC: EOI response.

Register Name	AIB TX Command Ordering Tags 2 Register
Mnemonic	INT.INT_VC.INT_VC_AIB_TX_ORDERING_TAG_2
Address	000000000501322D (SCOM)
Description	This register holds the 8-bit AIB ordering tag to be used for each AIB TX commands.

Bits	SCOM	Field Mnemonic: Description
0:19	RO	Constant = 0b00000000000000000000
20	RWX	INT_VC_AIB_TX_ORDERING_TAG_2_Reserved_20: Spare bits.
21	RWX	INT_VC_AIB_TX_ORDERING_TAG_2_RELAXED_WR_ORDERING_EQP: When asserted, Relaxed write ordering is asserted on aib for any EQ Post.
22	RWX	INT_VC_AIB_TX_ORDERING_TAG_2_RELAXED_WR_ORDERING_DMA: When asserted, Relaxed write ordering is asserted on aib for any EQD, SBC and IRQ DMA writes/push.
23	RWX	INT_VC_AIB_TX_ORDERING_TAG_2_DISABLE_IDX_IN_AIBTAG: When set, the AIB tag used for int, eq post requests and Software ESBn EOI responses are not overwritten by EQD offset (16:20).
24:31	RWX	INT_VC_AIB_TX_ORDERING_TAG_2_EQC_EOI_ESBE_ORDERING_TAG: EQC: EOI response for ESBe.
32:39	RWX	INT_VC_AIB_TX_ORDERING_TAG_2_EQC_CISTORE_ORDERING_TAG: EQC: EQ trigger forwarding.
40:47	RWX	INT_VC_AIB_TX_ORDERING_TAG_2_EQC_EOI_INT_EQP_ORDERING_TAG: EQC: EOI response for ESBn, Int request and EQ post. Ordering tag (3 to 7) are overwritten by EQD offset (16:20).

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	INT_VC_AIB_TX_ORDERING_TAG_2_EQC_CILOAD_ORDERING_TAG: EQC: CI load request (local or remote). Could be VPS/LSS or EOI.
56:63	RWX	INT_VC_AIB_TX_ORDERING_TAG_2_EQC_DMA_ORDERING_TAG: EQC: EQD DMA Read/Write.

Register Name	Maximum Number of Outstanding SBC Outbound Requests Register
Mnemonic	INT.INT_VC.INT_VC_MAX_OUTSTANDING_SBC_CMD
Address	0000000005013230 (SCOM)
Description	Defines the maximum number of outstanding requests that SBC may issue. This register is located in SBC sub-unit. MMIO offset = 0xA00

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:50	RWX	INT_VC_MAX_OUTSTANDING_SBC_CMD_Reserved_48_50: Spare.
51:55	RWX	INT_VC_MAX_OUTSTANDING_SBC_CMD_MAX_OUTSTANDING_DMA_READ: SBE DMA Read.
56:58	RWX	INT_VC_MAX_OUTSTANDING_SBC_CMD_Reserved_56_58: Spare.
59:63	RWX	INT_VC_MAX_OUTSTANDING_SBC_CMD_MAX_OUTSTANDING_DMA_WRITE: SBE DMA Write.

Register Name	SBC Cache Enable Register
Mnemonic	INT.INT_VC.INT_VC_SBC_CACHE_EN
Address	0000000005013231 (SCOM)
Description	This register enables SBC cache. This register is located in SBC sub-unit. MMIO offset = 0xA08

Bits	SCOM	Field Mnemonic: Description
0:15	RWX	INT_VC_SBC_CACHE_EN_CACHE_ENABLE: 16-bit cache enable (one bit per blockid). May be cleared by scrub engine at flush completion.
16:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000

Register Name	SBC Cache Scrub Trigger Register
Mnemonic	INT.INT_VC.INT_VC_SBC_SCRUB_TRIG
Address	0000000005013232 (SCOM)
Description	This register, along with scrub mask register, is used by Software to trigger a cache scrub. This register is located in SBC sub-unit. MMIO offset = 0xA10

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_VC_SBC_SCRUB_TRIG_VALID: Scrub request. Set by Software to initiate a cache scrub. Reset by hardware when flush operation is completed.
1	RWX	INT_VC_SBC_SCRUB_TRIG_WANT_CACHE_DISABLE: Want cache disable. When set, cache is disabled for the selected blockid(s) at the end of scrub operation.
2	RWX	INT_VC_SBC_SCRUB_TRIG_WANT_INVALIDATE: Want invalidate. 0: Modified entries are written back. State is switched to exclusive. 1: Exclusive entries are switched to invalidate. Modified entries are written back, state is switched to invalidate.

Bits	SCOM	Field Mnemonic: Description
3:27	RO	Constant = 0b000000000000000000000000
28:31	RWX	INT_VC_SBC_SCRUB_TRIG_BLOCKID: 4-bit scrub blockid.
32:40	RWX	INT_VC_SBC_SCRUB_TRIG_Reserved_32_40: Spare.
41:63	RWX	INT_VC_SBC_SCRUB_TRIG_OFFSET: 23-bit scrub offset.

Register Name	SBC Cache Scrub Mask Register
Mnemonic	INT.INT_VC.INT_VC_SBC_SCRUB_MASK
Address	0000000005013233 (SCOM)
Description	This register defines the block ids and offsets that need to be scrubbed. This register is located in SBC sub-unit. MMIO offset = 0xA18

Bits	SCOM	Field Mnemonic: Description
0:27	RO	Constant = 0b00000000000000000000000000
28:31	RWX	INT_VC_SBC_SCRUB_MASK_BLOCKID_MASK: 4-bit scrub blockid mask. 0:means ignores the corresponding blockid bit.
32:40	RWX	INT_VC_SBC_SCRUB_MASK_Reserved_32_40: Spare.
41:63	RWX	INT_VC_SBC_SCRUB_MASK_OFFSET_MASK: 23-bit scrub offset mask. 0:means ignores the corresponding offset bit.

Register Name	SBC Configuration Register
Mnemonic	INT.INT_VC.INT_VC_SBC_CONFIG
Address	0000000005013234 (SCOM)
Description	Defines how the SBC scrub engine controls the cache. This register is located in SBC sub-unit. MMIO offset = 0xA20

Bits	SCOM	Field Mnemonic: Description
0:43	RO	Constant = 0b00000000000000000000000000000000000000000000
44:46	RWX	INT_VC_SBC_CONFIG_Reserved_44_46: Spare.
47:51	RWX	INT_VC_SBC_CONFIG_MAX_PTAG_IN_USE: Defines the maximum number of ptag to be used.
52:55	RWX	INT_VC_SBC_CONFIG_BG_SCAN_RATE: 4-bit scrub background scan rate. 0:disable scan. Otherwhise, scan rate = 2**n clock cycles (max of 16 micro-seconds).
56:59	RWX	INT_VC_SBC_CONFIG_Reserved_56_59: Spare.
60:63	RWX	INT_VC_SBC_CONFIG_MAX_ENTRIES_IN_MODIFIED: 4-bit Max number of entries per set in modified state.

Register Name	SBC Cache Watch Address Register
Mnemonic	INT.INT_VC.INT_VC_SBC_CACHE_WATCH_ADDR
Address	0000000005013235 (SCOM)
Description	This register is used in debug mode to allow Software to read the cache control arrays. This register is located in SBC sub-unit. MMIO offset = 0xA28

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54:59	RWX	INT_VC_SBC_CACHE_WATCH_ADDR_SET_INDEX: 6-bit Set index.
60:63	RO	Constant = 0b0000

Register Name	SBC Cache Watch Data Register
Mnemonic	INT.INT_VC.INT_VC_SBC_CACHE_WATCH_DATA
Address	0000000005013236 (SCOM)
Description	This register is used in debug mode to allow Software to read the cache control arrays. This register is located in SBC sub-unit. MMIO offset = 0xA30

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	INT_VC_SBC_CACHE_WATCH_DATA_DATA: Watch data. Software does CI load of the watch data register. This triggers an internal read request of the targeted array. When the internal read operation is completed, data is loaded into the cache watch data register and CI load response is generated.

Register Name	SBC Soft Write Address Register
Mnemonic	INT.INT_VC.INT_VC_SBC_SOFTWR_ADDR
Address	0000000005013237 (SCOM)
Description	This register, along with Soft Write mask and data registers, is used to Write full cache line (Up to 32 PQ states). This register is located in SBC sub-unit. MMIO offset = 0xA38

Bits	SCOM	Field Mnemonic: Description
0:27	RO	Constant = 0b0000000000000000000000000000
28:31	RWX	INT_VC_SBC_SOFTWR_ADDR_BLOCKID: Block ID.
32:35	RWX	INT_VC_SBC_SOFTWR_ADDR_Reserved_32_35: Spare bits.
36:58	RWX	INT_VC_SBC_SOFTWR_ADDR_OFFSET: 23-bit cache line offset (32 PQ aligned). Auto incremented by hardware after operation completion.
59:63	RO	Constant = 0b00000

Register Name	SBC Soft Write Mask Register
Mnemonic	INT.INT_VC.INT_VC_SBC_SOFTWR_MASK
Address	0000000005013238 (SCOM)
Description	This register defines which PQ bits to update within the selected cache line. This register is located in SBC sub-unit. MMIO offset = 0xA40

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	INT_VC_SBC_SOFTWR_MASK_MSK: 1 means update the corresponding PQ state in cache line.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	SBC Soft Write Data Register
Mnemonic	INT.INT_VC.INT_VC_SBC_SOFTWR_DATA
Address	0000000005013239 (SCOM)
Description	This register defines new PQ state for the 32 cache line entries. This register is located in SBC sub-unit. MMIO offset = 0xA48

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	INT_VC_SBC_SOFTWR_DATA_PQ_STATE: Bits (n*2):(n*2+1) correspond to PQ state for offset n. Software sequence : 1) Write address register. 2) Write mask register. 3a) write data register. 3b) write data register (next cache line). 3c) write data register (next cache line). ..... and so on.

Register Name	SBC Debug Register
Mnemonic	INT.INT_VC.INT_VC_SBC_DEBUG
Address	000000000501323A (SCOM)
Description	This register holds ECC errors correction/injection and some SBC debug features . This register is located in SBC sub-unit. MMIO offset = 0xA50

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Constant = 0b00000000000000000000000000000000
32:33	RWX	INT_VC_SBC_DEBUG_Reserved_32_33: Spare.
34:37	RWX	INT_VC_SBC_DEBUG_DIS_TAG_ECC_CORRECTION: Disable TAG [0:3] array ECC correction.
38:41	RWX	INT_VC_SBC_DEBUG_Reserved_38_41: Spare.
42	RWX	INT_VC_SBC_DEBUG_DIS_STATE_ECC_CORRECTION: Disable STATE array ECC correction.
43:44	RWX	INT_VC_SBC_DEBUG_Reserved_43_44: Spare.
45:46	RWX	INT_VC_SBC_DEBUG_DIS_DATA_ECC_CORRECTION: Disable P1 DATA [0:1] array ECC correction.
47:48	RWX	INT_VC_SBC_DEBUG_Reserved_47_48: Spare.
49	RWX	INT_VC_SBC_DEBUG_FORCE_SINGLE_BIT_ECC_ERR: Force single bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain lsb bit is flipped).
50	RWX	INT_VC_SBC_DEBUG_FORCE_DOUBLE_BIT_ECC_ERR: Force double bit ECC error. Set by Software. Cleared by hardware when selected array is written (array datain 2 lsb bits are flipped).
51:55	RWX	INT_VC_SBC_DEBUG_ECC_ERR_INJ_ARRAY_SEL: Array selection for ECC error injection. 00 0xx P0 TAG arrays. xx = 0 to 3. 01 000 P0 STATE array. 11 000 P1 data 0. 11 001 P1 data 1.
56	RWX	INT_VC_SBC_DEBUG_TRACE_ENABLE: Enable SBC trace bus.
57:59	RWX	INT_VC_SBC_DEBUG_Reserved_57_59: Spare.

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	INT_VC_SBC_DEBUG_CACHE_CTRL_ARY_SELECT: Defines which cache control arrays to read during cache watch operation. Data watch register mapping. [0:31] [32:63]. 0000 STATE STATE(0:7) STATE(8:15). 0001 LRU x"0000"&LRU. 1xxx TAG TAG(2*xxx) TAG(2*xxx+1).

Register Name	Maximum Number of Outstanding IRQ DMA Operations Register
Mnemonic	INT.INT_VC.INT_VC_MAX_OUTSTANDING_IRQ_DMA
Address	000000000501323B (SCOM)
Description	This register defines the maximum number of outstanding DMA operations that IRQ may issue.

Bits	SCOM	Field Mnemonic: Description
0:17	RWX	INT_VC_MAX_OUTSTANDING_IRQ_DMA_Reserved_0_17: Spare bits.
18:23	RWX	INT_VC_MAX_OUTSTANDING_IRQ_DMA_MAX_IRQ_DMA_READ: IRQ: DMA Read.
24:25	RWX	INT_VC_MAX_OUTSTANDING_IRQ_DMA_Reserved_24_25: Spare bits.
26:31	RWX	INT_VC_MAX_OUTSTANDING_IRQ_DMA_MAX_IRQ_DMA_WRITE: IRQ: DMA Write.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	ATX Initial Credit Counters Value Register
Mnemonic	INT.INT_VC.INT_VC_ATX_INIT_CREDIT_COUNT
Address	000000000501323C (SCOM)
Description	This register defines the Reserved and pool credits for outbound read and write requests. MMIO offset = 0x8A0

Bits	SCOM	Field Mnemonic: Description
0:23	RO	Constant = 0b00000000000000000000000
24	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_CRD_INIT_REQUEST: Credit init request. Set by Soft, Cleared by hardware.
25	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_Reserved_25: Spare bit.
26:27	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_RSD_CRD_DMA_READ: 2-bit Reserved crd count for all DMA reads other than AT macro.
28:29	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_RSD_CRD_AT_MACRO: 2-bit Reserved crd count for AT macro DMA reads.
30:31	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_RSD_CRD_EQC_DOING_CI_LOAD: 2-bit Reserved crd count for EQC doing either VPC CI load request or auto-generated EOI (remote PC only).
32:33	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_Reserved_32_33: Spare bits.
34:39	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_READ_CRD_POOL: Outbound reads credits pool. (Must = Total number of CQ read machines - Sum (all Reserved read credit counts, PC+VC) (assume 3 Reserved in PC).
40:47	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_Reserved_40_47: Spare bits.
48:49	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_RSD_CRD_DMA_WRITE: 2-bit Reserved crd count for all DMA Write other than EQ post.
50:51	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_RSD_CRD_EQ_POST: 2-bit Reserved crd count for EQ post.

Bits	SCOM	Field Mnemonic: Description
52:53	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_RSD_CRD_TRIG_FWD_1: 2-bit Reserved crd count for EQ trigger forwarded by EQC to IPI or hardware queues.
54:55	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_RSD_CRD_TRIG_FWD_2: 2-bit Reserved crd count for EQ trigger forwarded by EQC to escalate or redistribution queues.
56:58	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_Reserved_56_58: Spare bits.
59:63	RWX	INT_VC_ATX_INIT_CREDIT_COUNT_WRITE_CRD_POOL: Outbound writes credits pool. (Must = Total number of CQ write machines - Sum (all Reserved write credit counts, PC+VC) (assume 4 Reserved in PC).

Register Name	**AIB TX Commands Priority Register**
Mnemonic	INT.INT_VC.INT_VC_AIB_TX_CMD_PRIORITY
Address	000000000501323D (SCOM)
Description	This register defines the priority for each source of AIB TX commands. 0: High priority, 1: Medium priority, 2: Low priority. MMIO offset = 0x8A8

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Constant = 0b00000000000000000000000000000000
32	RW	INT_VC_AIB_TX_CMD_PRIORITY_PREVENT_MTP_AT_DEM_IN_PIPE: 0: Multiple AT demand might be in ATX pipe. 1: Prevent multiple AT demand to be in ATX pipe.
33:43	RWX	INT_VC_AIB_TX_CMD_PRIORITY_Reserved_33_43: Spare bits.
44:45	RWX	INT_VC_AIB_TX_CMD_PRIORITY_ATX_PRIO_FOR_REGS: REGS: Registers read response.
46:47	RWX	INT_VC_AIB_TX_CMD_PRIORITY_ATX_PRIO_FOR_IRQ: IRQ: DMA Read/Write.
48:49	RWX	INT_VC_AIB_TX_CMD_PRIORITY_ATX_PRIO_FOR_IVC: IVC: DMA Read.
50:51	RWX	INT_VC_AIB_TX_CMD_PRIORITY_Reserved_50_51: Spare bits.
52:53	RWX	INT_VC_AIB_TX_CMD_PRIORITY_ATX_PRIO_FOR_SBC_EOI_RESP: SBC: EIO response.
54:55	RWX	INT_VC_AIB_TX_CMD_PRIORITY_ATX_PRIO_FOR_SBC_DMA: SBC: DMA Read/Write.
56:57	RWX	INT_VC_AIB_TX_CMD_PRIORITY_ATX_PRIO_FOR_INT_TRIG_FWD: EQC: Int trigger forwarding.
58:59	RWX	INT_VC_AIB_TX_CMD_PRIORITY_ATX_PRIO_FOR_EQC_EOI_INT_EQP: EQC: EOI response, Int request and EQ post.
60:61	RWX	INT_VC_AIB_TX_CMD_PRIORITY_ATX_PRIO_FOR_LSS_CI_LOAD: EQC: LSS CI load request (local or remote).
62:63	RWX	INT_VC_AIB_TX_CMD_PRIORITY_ATX_PRIO_FOR_EQD_DMA: EQC: EQD DMA Read/Write.

Register Name	**AIB AT Macro Indirect Kill Register**
Mnemonic	INT.INT_VC.INT_VC_AT_MACRO_KILL
Address	000000000501323E (SCOM)
Description	This registers, along with kill mask register is used to kill entries in AT CAM. MMIO offset = 0x8B0

Bits	SCOM	Field Mnemonic: Description
0	RWX	INT_VC_AT_MACRO_KILL_VALID: Valid bit. Set per Software to initiate a kill command. Cleared by hardware when kill command is completed. Software must have written the kill mask. register prior of setting this bit.

Bits	SCOM	Field Mnemonic: Description
1:13	RO	Constant = 0b0000000000000
14:15	RWX	INT_VC_AT_MACRO_KILL_VST_TYPE: 2-bit type (0:IRQ,1:IVC,2:SBC,3:EQD).
16:26	RO	Constant = 0b00000000000
27:31	RWX	INT_VC_AT_MACRO_KILL_BLOCKID: 5-bit blockid.
32:47	RO	Constant = 0b0000000000000000
48:60	RWX	INT_VC_AT_MACRO_KILL_OFFSET: 13-bit offset.
61:63	RO	Constant = 0b000

Register Name	**AIB AT Macro Indirect Kill Mask Register**
Mnemonic	INT.INT_VC.INT_VC_AT_MACRO_KILL_MASK
Address	000000000501323F (SCOM)
Description	This registers, along with kill register is used to kill entries in AT CAM. CAM entries are killed if (blockid and blockid_mask) = (cam_blockid and blockid_mask) AND (offset and offset_mask) = (cam_offset and offset_mask). MMIO offset = 0x8B8

Bits	SCOM	Field Mnemonic: Description
0:26	RO	Constant = 0b00000000000000000000000000000
27:31	RWX	INT_VC_AT_MACRO_KILL_MASK_BLOCKID: 5-bit blockid mask.
32:47	RO	Constant = 0b0000000000000000
48:60	RWX	INT_VC_AT_MACRO_KILL_MASK_OFFSET: 13-bit offset mask.
61:63	RO	Constant = 0b000

Register Name	**ATX Performance Events Selection 1 Register**
Mnemonic	INT.INT_VC.INT_VC_ATX_PERF_EVENT_SEL_1
Address	0000000005013240 (SCOM)
Description	4-bit configuration for each possible performance event. bit0: Enable count of request granted by the ATX arbiter. bit 1:3 Performance counter selection. MMIO offset = 0x8C0

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R0: Count of request(0).
4:7	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R1R: Count of request(1r).
8:11	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R1W: Count of request(1w).
12:15	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R2: Count of request(2).
16:19	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R3: Count of request(3).
20:23	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R4: Count of request(4).
24:27	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R5R: Count of request(5r).
28:31	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R5W: Count of request(5w).
32:35	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R6: Count of request(6).
36:39	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R7RSP: Count of request(7rsp).
40:43	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R7INT: Count of request(7int).

Bits	SCOM	Field Mnemonic: Description
44:47	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R7EQP: Count of request(7eqp).
48:51	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R8: Count of request(8).
52:55	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R9: Count of request(9).
56:59	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R10R: Count of request(10r).
60:63	RWX	INT_VC_ATX_PERF_EVENT_SEL_1_CNT_R10W: Count of request(10w).

Register Name	**ATX Performance Events Selection 2 Register**
Mnemonic	INT.INT_VC.INT_VC_ATX_PERF_EVENT_SEL_2
Address	0000000005013241 (SCOM)
Description	4-bit configuration for each possible performance event. bit0: Enable count of request not presented immediately to the ATX arbiter because lack of credit. bit 1:3 Performance counter selection. MMIO offset = 0x8C8

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R0: Count of request(0).
4:7	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R1R: Count of request(1r).
8:11	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R1W: Count of request(1w).
12:15	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R2: Count of request(2).
16:19	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R3: Count of request(3).
20:23	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R4: Count of request(4).
24:27	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R5R: Count of request(5r).
28:31	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R5W: Count of request(5w).
32:35	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R6: Count of request(6).
36:39	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R7RSP: Count of request(7rsp).
40:43	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R7INT: Count of request(7int).
44:47	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R7EQP: Count of request(7eqp).
48:51	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R8: Count of request(8).
52:55	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R9: Count of request(9).
56:59	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R10R: Count of request(10r).
60:63	RWX	INT_VC_ATX_PERF_EVENT_SEL_2_CNT_R10W: Count of request(10w).

Register Name	**ATX Performance Events Selection 3 Register**
Mnemonic	INT.INT_VC.INT_VC_ATX_PERF_EVENT_SEL_3
Address	0000000005013242 (SCOM)
Description	4-bit configuration for each possible performance event. bit0: Enable count of request not served immediately because another requester is served. bit 1:3 Performance counter selection. MMIO offset = 0x8D0

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R0: Count of request(0).
4:7	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R1R: Count of request(1r).

Bits	SCOM	Field Mnemonic: Description
8:11	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R1W: Count of request(1w).
12:15	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R2: Count of request(2).
16:19	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R3: Count of request(3).
20:23	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R4: Count of request(4).
24:27	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R5R: Count of request(5r).
28:31	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R5W: Count of request(5w).
32:35	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R6: Count of request(6).
36:39	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R7RSP: Count of request(7rsp).
40:43	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R7INT: Count of request(7int).
44:47	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R7EQP: Count of request(7eqp).
48:51	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R8: Count of request(8).
52:55	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R9: Count of request(9).
56:59	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R10R: Count of request(10r).
60:63	RWX	INT_VC_ATX_PERF_EVENT_SEL_3_CNT_R10W: Count of request(10w).

Register Name	EQC Performance Events Selection 1 Register
Mnemonic	INT.INT_VC.INT_VC_EQC_PERF_EVENT_SEL_1
Address	0000000005013250 (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_EQ_TRIGGER_FROM_IPI: count of number of EQ trigger from IPI queue processed.
4:7	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_EQ_TRIGGER_FROM_HWD: count of number of EQ trigger from hardware processed.
8:11	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_EQ_TRIGGER_FROM_1ESC: count of number of EQ trigger from 1st escalate queue processed.
12:15	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_EQ_TRIGGER_FROM_2ESC: count of number of EQ trigger from 2nd escalate queue processed.
16:19	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_EQ_TRIGGER_FROM_REDIS: count of number of EQ trigger from redistribution queue processed.
20:23	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_NON_SPEC_EOI: count of number of non speculative EOI processed.
24:27	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_LOCAL_ESCALATE: count of number of local escalate processed.
28:31	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_EQ_TRIG_CACHE_HIT: count of EQ triggers command cache hit.
32:35	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_EOI_CACHE_HIT: count of EOI command cache hit.
36:39	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_LOCAL_ESC_CACHE_HIT: count of local escalate command cache hit.

Bits	SCOM	Field Mnemonic: Description
40:43	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_VICTIM_IS_LRU: count of "selected victim is LRU".
44:47	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_VICTIM_IS_FIRST_USABLE: count of "selected victim is first usable entry".
48:51	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_RETRY: count of command retry.
52:55	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_CNT_TOO_MANY_ENTRIES: count of number of EQD writeback due to too many entries in modified state.
56:63	RWX	INT_VC_EQC_PERF_EVENT_SEL_1_Reserved_56_63: Spare.

Register Name	EQC Performance Events Selection 2 Register
Mnemonic	INT.INT_VC.INT_VC_EQC_PERF_EVENT_SEL_2
Address	0000000005013251 (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_EQD_FETCH: count of EQD fetch sent.
4:7	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_EQP: count of EQ Post sent.
8:11	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_RESUME_INT: count of user level resume Interrupt sent.
12:15	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_EBB_INT: count of user level EBB Interrupt sent.
16:19	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_VP_INT: count of VP Interrupt sent.
20:23	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_LS_INT: count of Logical Server interrupt sent.
24:27	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_BROADCAST_BL: count of Broadcast Backlog sent.
28:31	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_EQ_FWD: count of EQ trigger forwarding sent.
32:35	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_ESCALATE: count of escalate sent.
36:39	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_LOCAL_VPC_UPD: count of Local VPC update sent.
40:43	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_REMOTE_VPC_UPD: count of Remote VPC update sent.
44:47	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_LOCAL_SBC_UPD: count of Local SBC update sent.
48:51	RWX	INT_VC_EQC_PERF_EVENT_SEL_2_CNT_REMOTE_SBC_UPD: count of Remote SBC update sent.
52:63	RO	Constant = 0b000000000000

Register Name	EQC Performance Events Selection 3 Register
Mnemonic	INT.INT_VC.INT_VC_EQC_PERF_EVENT_SEL_3
Address	0000000005013252 (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_EQD_FETCH_REPLAY: count of EQD fetch replay.

Bits	SCOM	Field Mnemonic: Description
4:7	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_EQP_REPLAY: count of EQ Post replay.
8:11	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_INT_REPLAY: count of Interrupt replay.
12:15	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_CI_STORE_REPLAY: count of CI store replay.
16:19	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_LOCAL_ESC_REPLAY: count of Local escalate replay.
20:23	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_REMOTE_CI_LOAD_REPLAY: count of Remote CI load replay.
24:27	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_LOCAL_VPC_REPLAY: count of Local VPC CI load replay.
28:31	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_LOCAL_SBC_REPLAY: count of Local SBC CI load replay.
32:35	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_EOI_RESP_REPLAY: count of Software EOI response replay.
36:39	RWX	INT_VC_EQC_PERF_EVENT_SEL_3_CNT_NEW_CMD_STALLED: count number of commands processed by EQC P1 (could be new, replay, rearb or response).
40:63	RO	Constant = 0b00000000000000000000000

Register Name	EQC Additional Performance 1 Register
Mnemonic	INT.INT_VC.INT_VC_EQC_ADDITIONAL_PERF_1
Address	0000000005013253 (SCOM)
Description	This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0	ROX	INT_VC_EQC_ADDITIONAL_PERF_1_P0_IS_IDLE: EQC P0 is idle.
1	ROX	INT_VC_EQC_ADDITIONAL_PERF_1_P1_IS_IDLE: EQC P1 is idle.
2:7	RO	Constant = 0b000000
8:15	ROX	INT_VC_EQC_ADDITIONAL_PERF_1_MAX_PTAG_IN_USE: Max reached number of ptag in use.
16:23	ROX	INT_VC_EQC_ADDITIONAL_PERF_1_MAX_OUTSTANDING_EOI: Max reached number of outstanding EOI.
24:31	ROX	INT_VC_EQC_ADDITIONAL_PERF_1_MAX_UNLOCK_IN_FIFO: Max reached number of unlock command in the unlock FIFO.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	EQC Additional Performance 2 Register
Mnemonic	INT.INT_VC.INT_VC_EQC_ADDITIONAL_PERF_2
Address	0000000005013254 (SCOM)
Description	This register is located in EQC sub-unit.

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	INT_VC_EQC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_EQD_FETCH: Max reached number of outstanding EQD fetch.
8:15	ROX	INT_VC_EQC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_EQP: Max reached number of outstanding EQ Post.
16:23	ROX	INT_VC_EQC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_INT: Max reached number of outstanding Interrupt request.

Bits	SCOM	Field Mnemonic: Description
24:31	ROX	INT_VC_EQC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_CI_LOAD: Max reached number of outstanding CI load.
32:39	ROX	INT_VC_EQC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_CI_STORE: Max reached number of outstanding CI store.
40:47	ROX	INT_VC_EQC_ADDITIONAL_PERF_2_MAX_OUTSTANDING_EQD_WRITE: Max reached number of outstanding EQD writeback.
48:63	RO	Constant = 0b0000000000000000

Register Name	IVC Performance Events Selection 1 Register
Mnemonic	INT.INT_VC.INT_VC_IVC_PERF_EVENT_SEL_1
Address	0000000005013258 (SCOM)
Description	4-bit configuration for each possible performance event. bit0: Count enable. bits 1:3 Performance counter selection. This register is located in IVC sub-unit. MMIO offset = 0x9D8

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CNT_IPI_DOES_PRF_IVE: count of IPI queue prefetch for IVE lookup.
4:7	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CNT_IPI_DOES_PRF_IVE_SBC: count of IPI queue prefetch for IVE+SBC lookup.
8:11	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CNT_HWD_DOES_PRF_IVE: count of HW queue prefetch for IVE lookup.
12:15	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CNT_IPI_DOES_DEM_IVE: count of IPI queue demand for IVE lookup.
16:19	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CNT_IPI_DOES_DEM_IVE_SBC: count of IPI queue demand for IVE+SBC lookup.
20:23	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CND_HWD_DOES_DEM_IVE: count of HW queue demand for IVE lookup.
24:27	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CNT_PRF_CACHE_HIT: count of cache hit for a prefetch request.
28:31	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CNT_DEM_CACHE_HIT: count of cache hit for a demand request.
32:35	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CNT_VICTIM_IS_LRU: count of "selected victim is LRU".
36:39	RWX	INT_VC_IVC_PERF_EVENT_SEL_1_CNT_VICTIM_IS_1ST_USABLE: count of "selected victim is first usable entry".
40:63	RO	Constant = 0b000000000000000000000000

Register Name	IVC Performance Events Selection 2 Register
Mnemonic	INT.INT_VC.INT_VC_IVC_PERF_EVENT_SEL_2
Address	0000000005013259 (SCOM)
Description	4-bit configuration for each possible performance event. bit0: Count enable. bits 1:3 Performance counter selection. This register is located in IVC sub-unit. MMIO offset = 0x9E0

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_IVC_PERF_EVENT_SEL_2_CNT_IVE_FETCH: count of IVE fetch sent.
4:7	RWX	INT_VC_IVC_PERF_EVENT_SEL_2_CNT_SBC_LOOKUP: count of SBC lookup request sent.
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	IVC Performance Events Selection 3 Register
Mnemonic	INT.INT_VC.INT_VC_IVC_PERF_EVENT_SEL_3
Address	000000000501325A (SCOM)
Description	4-bit configuration for each possible performance event. bit0: Count enable. bits 1:3 Performance counter selection. This register is located in IVC sub-unit. MMIO offset = 0x9E8

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_IVC_PERF_EVENT_SEL_3_CNT_IVE_FETCH_REPLAY: count of IVE fetch replay.
4:7	RWX	INT_VC_IVC_PERF_EVENT_SEL_3_CNT_SBC_LOOKUP_REPLAY: count of SBC lookup replay.
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	IVC Additional Performance Register
Mnemonic	INT.INT_VC.INT_VC_IVC_ADDITIONAL_PERF
Address	000000000501325B (SCOM)
Description	This register is located in IVC sub-unit. MMIO offset = 0x9F0

Bits	SCOM	Field Mnemonic: Description
0	ROX	INT_VC_IVC_ADDITIONAL_PERF_P0_IS_IDLE: IVC P0 is idle.
1	ROX	INT_VC_IVC_ADDITIONAL_PERF_P1_IS_IDLE: IVC P1 is idle.
2:7	RO	Constant = 0b000000
8:15	ROX	INT_VC_IVC_ADDITIONAL_PERF_MAX_PTAG_IN_USE: Max reached number of ptag in use.
16:23	RO	Constant = 0b00000000
24:31	ROX	INT_VC_IVC_ADDITIONAL_PERF_MAX_UNLOCK_IN_FIFO: Max reached number of unlock command in the unlock FIFO.
32:47	RO	Constant = 0b0000000000000000
48:55	ROX	INT_VC_IVC_ADDITIONAL_PERF_MAX_OUTSTANDING_IVE_FETCH: Max reached number of outstanding IVE fetch.
56:63	ROX	INT_VC_IVC_ADDITIONAL_PERF_MAX_OUTSTANDING_SBC_LOOKUP: Max reached number of outstanding SBC lookup requests.

Register Name	SBC Performance Events Selection 1 Register
Mnemonic	INT.INT_VC.INT_VC_SBC_PERF_EVENT_SEL_1
Address	0000000005013260 (SCOM)
Description	4-bit configuration for each possible performance event. bit0: Count enable. bits 1:3 Performance counter selection. This register is located in IVC sub-unit. MMIO offset = 0xA58

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_IVC_PRF: count of IVC prefetch command.
4:7	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_IVC_DEMAND: count of IVC demand command.
8:11	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_EQC_COMMAND: count of EQC command.
12:15	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_NON_SPEC_EOI_OWNED: count of non speculative Software EOI processed to owned block.
16:19	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_NON_SPEC_EOI_NOTOWNED: count of non speculative Software EOI processed to not owned block.
20:23	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_SPEC_EOI: count of speculative Software EOI processed.
24:27	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_SPEC_EOI_CACHE_HIT: count of cache hit for a speculative request.
28:31	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_PRF_CACHE_HIT: count of cache hit for a prefetch request.
32:35	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_OTHER_CACHE_HIT: count of cache hit for a non prefetch and non speculative request.
36:39	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_VICTIM_IS_LRU: count of "selected victim is LRU".
40:43	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_VICTIM_IS_1ST_USABLE: count of "selected victim is first usable entry".
44:47	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_RETRY: count of command retry.
48:51	RWX	INT_VC_SBC_PERF_EVENT_SEL_1_CNT_TOO_MANY_ENTRIES: count of number of ISE writeback due to too many entries in modified state.
52:63	RO	Constant = 0b000000000000

Register Name	SBC Performance Events Selection 2 Register
Mnemonic	INT.INT_VC.INT_VC_SBC_PERF_EVENT_SEL_2
Address	0000000005013261 (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. This register is located in SBC sub-unit. MMIO offset = 0xA60

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_SBC_PERF_EVENT_SEL_2_CNT_ISB_FETCH: count of ISB fetch sent.
4:7	RWX	INT_VC_SBC_PERF_EVENT_SEL_2_CNT_IVVC_RESP: count of IVC response sent.
8:11	RWX	INT_VC_SBC_PERF_EVENT_SEL_2_Reserved_8_11: Spare bits.
12:15	RWX	INT_VC_SBC_PERF_EVENT_SEL_2_CNT_ISB_WRITE: count of ISB writeback sent.
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	SBC Performance Events Selection 3 Register
Mnemonic	INT.INT_VC.INT_VC_SBC_PERF_EVENT_SEL_3
Address	0000000005013262 (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. This register is located in SBC sub-unit. MMIO offset = 0xA68

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_SBC_PERF_EVENT_SEL_3_CNT_ISB_FETCH_REPLAY: count of ISB fetch replay.
4:7	RWX	INT_VC_SBC_PERF_EVENT_SEL_3_CNT_IVC_RESP_REPLAY: count of IVC response replay.
8:11	RWX	INT_VC_SBC_PERF_EVENT_SEL_3_CNT_EOI_RESP_REPLAY: count of Software EOI response replay.
12:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	SBC Additional Performance Register
Mnemonic	INT.INT_VC.INT_VC_SBC_ADDITIONAL_PERF
Address	0000000005013263 (SCOM)
Description	This register is located in SBC sub-unit. MMIO offset = 0xA70

Bits	SCOM	Field Mnemonic: Description
0	ROX	INT_VC_SBC_ADDITIONAL_PERF_P0_IS_IDLE: SBC P0 is idle.
1	ROX	INT_VC_SBC_ADDITIONAL_PERF_P1_IS_IDLE: SBC P1 is idle.
2:7	RO	Constant = 0b000000
8:15	ROX	INT_VC_SBC_ADDITIONAL_PERF_MAX_PTAG_IN_USE: Max reached number of ptag in use.
16:23	ROX	INT_VC_SBC_ADDITIONAL_PERF_MAX_OUTSTANDING_SOFT_EOI: Max reached number of outstanding Software EOI.
24:31	ROX	INT_VC_SBC_ADDITIONAL_PERF_MAX_UNLOCK_IN_FIFO: Max reached number of unlock command in the unlock FIFO.
32:47	RO	Constant = 0b0000000000000000
48:55	ROX	INT_VC_SBC_ADDITIONAL_PERF_MAX_OUTSTANDING_ISB_FETCH: Max reached number of outstanding ISB fetch.
56:63	ROX	INT_VC_SBC_ADDITIONAL_PERF_MAX_OUTSTANDING_ISB_WRITE: Max reached number of outstanding ISB writeback.

Register Name	IRQ Performance Events Selection 0 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_0
Address	0000000005013268 (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. MMIO offset = 0xA80,0xA88,0xA90,0xA98,0xAA0,0xAA8

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_IRQ_PERF_EVENT_SEL_0_CNT_TRIG_FROM_AIB: Count of triggers received from AIB.
4:7	RWX	INT_VC_IRQ_PERF_EVENT_SEL_0_CNT_TRIG_DROPPED: Count of triggers dropped by IRQ.

Bits	SCOM	Field Mnemonic: Description
8:11	RWX	INT_VC_IRQ_PERF_EVENT_SEL_0_CNT_TRIG_FWD_TO_EQC: Count of triggers forwarded to EQC.
12:15	RWX	INT_VC_IRQ_PERF_EVENT_SEL_0_CNT_IRQ_DMA_WR: Count of IRQ DMA Write.
16:19	RWX	INT_VC_IRQ_PERF_EVENT_SEL_0_CNT_IRQ_DMA_RD: Count of IRQ DMA Read.
20:23	RWX	INT_VC_IRQ_PERF_EVENT_SEL_0_CNT_IRQ_FIFO_FULL: Count of IRQ fifo full assertion.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	IRQ Performance Events Selection 1 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_1
Address	0000000005013269 (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. MMIO offset = 0xA80,0xA88,0xA90,0xA98,0xAA0,0xAA8

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_IRQ_PERF_EVENT_SEL_1_CNT_TRIG_FROM_AIB: Count of triggers received from AIB.
4:7	RWX	INT_VC_IRQ_PERF_EVENT_SEL_1_CNT_TRIG_DROPPED: Count of triggers dropped by IRQ.
8:11	RWX	INT_VC_IRQ_PERF_EVENT_SEL_1_CNT_TRIG_FWD_TO_EQC: Count of triggers forwarded to EQC.
12:15	RWX	INT_VC_IRQ_PERF_EVENT_SEL_1_CNT_IRQ_DMA_WR: Count of IRQ DMA Write.
16:19	RWX	INT_VC_IRQ_PERF_EVENT_SEL_1_CNT_IRQ_DMA_RD: Count of IRQ DMA Read.
20:23	RWX	INT_VC_IRQ_PERF_EVENT_SEL_1_CNT_IRQ_FIFO_FULL: Count of IRQ fifo full assertion.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	IRQ Performance Events Selection 2 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_2
Address	000000005013260A (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. MMIO offset = 0xA80,0xA88,0xA90,0xA98,0xAA0,0xAA8

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_IRQ_PERF_EVENT_SEL_2_CNT_TRIG_FROM_AIB: Count of triggers received from AIB.
4:7	RWX	INT_VC_IRQ_PERF_EVENT_SEL_2_CNT_TRIG_DROPPED: Count of triggers dropped by IRQ.
8:11	RWX	INT_VC_IRQ_PERF_EVENT_SEL_2_CNT_TRIG_FWD_TO_EQC: Count of triggers forwarded to EQC.
12:15	RWX	INT_VC_IRQ_PERF_EVENT_SEL_2_CNT_IRQ_DMA_WR: Count of IRQ DMA Write.
16:19	RWX	INT_VC_IRQ_PERF_EVENT_SEL_2_CNT_IRQ_DMA_RD: Count of IRQ DMA Read.
20:23	RWX	INT_VC_IRQ_PERF_EVENT_SEL_2_CNT_IRQ_FIFO_FULL: Count of IRQ fifo full assertion.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	IRQ Performance Events Selection 3 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_3
Address	000000000501326B (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. MMIO offset = 0xA80,0xA88,0xA90,0xA98,0xAA0,0xAA8

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_IRQ_PERF_EVENT_SEL_3_CNT_TRIG_FROM_AIB: Count of triggers received from AIB.
4:7	RWX	INT_VC_IRQ_PERF_EVENT_SEL_3_CNT_TRIG_DROPPED: Count of triggers dropped by IRQ.
8:11	RWX	INT_VC_IRQ_PERF_EVENT_SEL_3_CNT_TRIG_FWD_TO_EQC: Count of triggers forwarded to EQC.
12:15	RWX	INT_VC_IRQ_PERF_EVENT_SEL_3_CNT_IRQ_DMA_WR: Count of IRQ DMA Write.
16:19	RWX	INT_VC_IRQ_PERF_EVENT_SEL_3_CNT_IRQ_DMA_RD: Count of IRQ DMA Read.
20:23	RWX	INT_VC_IRQ_PERF_EVENT_SEL_3_CNT_IRQ_FIFO_FULL: Count of IRQ fifo full assertion.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	IRQ Performance Events Selection 4 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_4
Address	000000000501326C (SCOM)
Description	4-bit configuration for each possible performance event. bit 0: Count enable. bits 1:3 Performance counter selection. MMIO offset = 0xA80,0xA88,0xA90,0xA98,0xAA0,0xAA8

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_IRQ_PERF_EVENT_SEL_4_CNT_TRIG_FROM_AIB: Count of triggers received from AIB.
4:7	RWX	INT_VC_IRQ_PERF_EVENT_SEL_4_CNT_TRIG_DROPPED: Count of triggers dropped by IRQ.
8:11	RWX	INT_VC_IRQ_PERF_EVENT_SEL_4_CNT_TRIG_FWD_TO_EQC: Count of triggers forwarded to EQC.
12:15	RWX	INT_VC_IRQ_PERF_EVENT_SEL_4_CNT_IRQ_DMA_WR: Count of IRQ DMA Write.
16:19	RWX	INT_VC_IRQ_PERF_EVENT_SEL_4_CNT_IRQ_DMA_RD: Count of IRQ DMA Read.
20:23	RWX	INT_VC_IRQ_PERF_EVENT_SEL_4_CNT_IRQ_FIFO_FULL: Count of IRQ fifo full assertion.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	IRQ Performance Events Selection 5 Register
Mnemonic	INT.INT_VC.INT_VC_IRQ_PERF_EVENT_SEL_5
Address	000000000501326D (SCOM)
Description	4-bit configuration for each possible performance event. bit0: Count enable. bits 1:3 Performance counter selection. MMIO offset = 0xA80,0xA88,0xA90,0xA98,0xAA0,0xAA8

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	INT_VC_IRQ_PERF_EVENT_SEL_5_CNT_TRIG_FROM_AIB: Count of triggers received from AIB.

Bits	SCOM	Field Mnemonic: Description
4:7	RWX	INT_VC_IRQ_PERF_EVENT_SEL_5_CNT_TRIG_DROPPED: Count of triggers dropped by IRQ.
8:11	RWX	INT_VC_IRQ_PERF_EVENT_SEL_5_CNT_TRIG_FWD_TO_EQC: Count of triggers forwarded to EQC.
12:15	RWX	INT_VC_IRQ_PERF_EVENT_SEL_5_CNT_IRQ_DMA_WR: Count of IRQ DMA Write.
16:19	RWX	INT_VC_IRQ_PERF_EVENT_SEL_5_CNT_IRQ_DMA_RD: Count of IRQ DMA Read.
20:23	RWX	INT_VC_IRQ_PERF_EVENT_SEL_5_CNT_IRQ_FIFO_FULL: Count of IRQ fifo full assertion.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Errors Configuration Group 0 Register 0 Register
Mnemonic	INT.INT_VC.INT_VC_ERR_CFG_G0R0
Address	0000000005013270 (SCOM)
Description	This register along with the next one is used to configure P3VC group 0 errors. 2-bit configuration for each possible error. 00 Disable 01 Fatal 10 Recoverable 11 Informational. MMIO offset = 0xB00

Bits	SCOM	Field Mnemonic: Description
0:55	RWX	INT_VC_ERR_CFG_G0R0_ERROR_CONFIG: Bit n is config(0) for error bit n.
56:63	RO	Constant = 0b00000000

Register Name	Errors Configuration Group 0 Register 1 Register
Mnemonic	INT.INT_VC.INT_VC_ERR_CFG_G0R1
Address	0000000005013271 (SCOM)
Description	Refer to INT_VC_ERR_CFG_G0R0 description. MMIO offset = 0xB08

Bits	SCOM	Field Mnemonic: Description
0:55	RWX	INT_VC_ERR_CFG_G0R1_ERROR_CONFIG: Bit n is config(1) for error bit n.
56:63	RO	Constant = 0b00000000

Register Name	Errors Configuration Group 1 Register 0 Register
Mnemonic	INT.INT_VC.INT_VC_ERR_CFG_G1R0
Address	0000000005013272 (SCOM)
Description	This register along with the next one is used to configure P3VC group 1 errors. 2-bit configuration for each possible error. 00 Disable 01 Fatal 10 Recoverable 11 Informational. MMIO offset = 0xB10

Bits	SCOM	Field Mnemonic: Description
0:43	RWX	INT_VC_ERR_CFG_G1R0_ERROR_CONFIG: Bit n is config(0) for error bit n.

Bits	SCOM	Field Mnemonic: Description
44:63	RO	Constant = 0b00000000000000000000

Register Name	Errors Configuration Group 1 Register 1 Register
Mnemonic	INT.INT_VC.INT_VC_ERR_CFG_G1R1
Address	0000000005013273 (SCOM)
Description	Refer to INT_VC_ERR_CFG_G1R0 description. MMIO offset = 0xB18

Bits	SCOM	Field Mnemonic: Description
0:43	RWX	INT_VC_ERR_CFG_G1R1_ERROR_CONFIG: Bit n is config(1) for error bit n.
44:63	RO	Constant = 0b00000000000000000000

Register Name	Who's On First Errors Group 0 Register
Mnemonic	INT.INT_VC.INT_VC_WOF_ERR_G0
Address	0000000005013274 (SCOM)
Description	This register captures the first non disabled group0 error reported This register is cleared on read. MMIO offset = 0xB20

Bits	SCOM	Field Mnemonic: Description
0	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_INVALID_STATE: IRQ elastic fifo internal error: invalid state (default:fatal).
1	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_CRD_ERROR: IRQ elastic fifo internal error: credit error (default:fatal).
2	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_OFFSET_ERROR: IRQ elastic fifo internal error: offset error (default:fatal).
3	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_DATA_ERROR: IRQ elastic fifo internal error: data error (default:fatal).
4	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_ACCESS_ERROR: IRQ elastic fifo internal error: sram access error (default:fatal).
5	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_OVERFLOW: IRQ elastic fifo internal error: offset overflow (default:fatal).
6	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_IDX_ERROR: IRQ elastic fifo internal error: index overflow or underflow (default:fatal).
7	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_UNDERFLOW: IRQ elastic fifo internal error: offset underflow (default:fatal).
8	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_DIR_STATE_ERROR: IRQ elastic fifo internal error: dir state error (default:fatal).
9	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_DIR_WR_ERROR: IRQ elastic fifo internal error: dir wr offset error (default:fatal).
10	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_DIR_RD_ERROR: IRQ elastic fifo internal error: dir rd offset error (default:fatal).
11	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_ECC_UE: IRQ elastic FIFO SRAM uncorrectable ECC error (default:fatal).
12	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_EQC_CREDIT_ERROR: EQC credit error. A credit was returned by EQC whereas no credit was consumed (default:fatal).

Bits	SCOM	Field Mnemonic: Description
13	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_INT_TRIG_CRD_ERROR: Int trigger credit error. An int trigger is received whereas there is no credit (default:fatal).
14	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_EFIFO_DIN_ERROR: din_data_ack_err. din_data_ack is not asserted by efifo when din_data_vld is asserted (default:fatal).
15	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_INPUT_BUF_ERROR: Input buffer overflow: An int trigger comes in and both input buffers are busy (default:fatal).
16	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_EQ_ERROR: Interrupt trigger EQ error. Receiving an int trigger with EQ = 0 on a queue not connected to IVC (default:fatal).
17	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_INT_PQ_ERROR: Interrupt trigger PQ error. Receiving an int trigger with PQ = 0 on a queue not connected to IVC (default:fatal).
18	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_INT_EQPQ_ERROR: Interrupt trigger EQPQ error. Receiving an int trigger with EQ = 1 and PQ = 0 on IPI or HWD queue (default:fatal).
19	ROX_CLRPART	INT_VC_WOF_ERR_G0_IRQ_FIFO_ECC_CE: Elastic FIFO SRAM correctable ECC error (default:recov).
20	ROX_CLRPART	INT_VC_WOF_ERR_G0_ARX_CTRL_PTY_ERROR: aib control signals parity error (default:fatal).
21	ROX_CLRPART	INT_VC_WOF_ERR_G0_ARX_CMD_PTY_ERROR: aib command bus parity error (default:fatal).
22	ROX_CLRPART	INT_VC_WOF_ERR_G0_REGS_SCOM_INTERNAL_ERROR: SCOM satellite error (default:fatal).
23	ROX_CLRPART	INT_VC_WOF_ERR_G0_ARX_TAG_SRAM_ECC_UE: aib TAG sram uncorrectable ECC error (default:fatal).
24	ROX_CLRPART	INT_VC_WOF_ERR_G0_ARX_AIB_DATA_ECC_UE: AIB data bus uncorrectable ECC error (default:fatal).
25	ROX_CLRPART	INT_VC_WOF_ERR_G0_REGS_PARITY_ERROR: Register parity error. A parity error has been detected on one of the registers located in REGS (default:fatal).
26	ROX_CLRPART	INT_VC_WOF_ERR_G0_REGS_CMD_CRD_ERROR: aib regs access credit error. An inbound CI operation is received by REGS whereas there is no command. credit available (default:fatal).
27	ROX_CLRPART	INT_VC_WOF_ERR_G0_REGS_DATA_CRD_ERROR: aib regs write access credit error. An inbound CI store operation is received by REGS whereas there. is no data credit available (default:fatal).
28	ROX_CLRPART	INT_VC_WOF_ERR_G0_ARX_AIB_CMD_ERROR: aib command error. Receiving an AIB command that is not recognized (default:fatal).
29	ROX_CLRPART	INT_VC_WOF_ERR_G0_ARX_AIB_RESP_TIMEOUT: aib response timeout. An outbound request did not get response on defined time (default:fatal).
30	ROX_CLRPART	INT_VC_WOF_ERR_G0_ARX_AIB_DATA_ECC_CE: AIB data bus correctable ECC error (default:recov).
31	ROX_CLRPART	INT_VC_WOF_ERR_G0_ARX_TAG_SRAM_ECC_CE: aib TAG sram correctable ECC error (default:recov).
32	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_LACK_OF_TAG: Lack of tag. ATX sends a command that requires an aib tag over the aib but there is no tag available (default:fatal).
33	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_TAG_RELEASE_ERROR: AIB tag release error. An AIB tag is released whereas it was not in use (default:fatal).
34	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_BAD_CAM_STATE: AT macro internal error: Bad CAM entry state (default:fatal).
35	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_MULTIPLE_HIT: AT macro internal error: One BAR entry was found in multiple CAM cache slots (default:fatal).

Bits	SCOM	Field Mnemonic: Description
36	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_PARITY_ERROR: AT macro internal error: Parity error (default:fatal).
37	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_MULTIPLE_PRF_RQ: AT macro internal error: 1 ATX slot sent two prefetch requests (default:fatal).
38	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_TOO_LARGE_SLOTID: AT macro internal error: ATX used slotID that was too large (default:fatal).
39	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_PRF_OVERFLOW: AT macro internal error: Prefetch rd queue overflow (default:fatal).
40	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_PRF_UNDERFLOW: AT macro internal error: Prefetch rd queue underflow (default:fatal).
41	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_INVALID_CMD: AT macro internal error: Rd request was asked without valid command (default:fatal).
42	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_INVALID_IND_BAR: AT macro internal error: Requested indirect BAR entry is invalid (default:fatal).
43	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_INVALID_IND_PZ: AT macro internal error: Requested indirect BAR page size did not match root BAR page size (default:fatal).
44	ROX_CLRPART	INT_VC_WOF_ERR_G0_AT_INVALID_I: AT macro internal error: BAR entries that have the "i" bit set - which should not be the case (default:fatal).
45	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_CRD_PARITY_ERROR: AIB credits parity error (default:fatal).
46	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_AT_SRAM_ECC_UE: AT SRAM uncorrected ECC error (default:fatal).
47	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_BAR_SRAM_ECC_UE: BAR SRAM uncorrectable ecc error (default:fatal).
48	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_WB_SRAM_ECC_UE: Writeback SRAM uncorrectable ecc error (default:fatal).
49	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_SLOT_OVERFLOW: Command slot overflow. Acommand is received from a sub unit whereas there is no slot available (default:fatal).
50	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_CRD_OVERFLOW: AIB credit counter overflow. a credit is returned by AIB whereas the credit counter is at its max config value (default:fatal).
51	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_CRD_UNDERFLOW: AIB credit counter underflow. AIB logic triggers a credit counter decrement whereas the counter value is zero (default:fatal).
52	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_INVALID_BAR: Invalid BAR. A BAR SRAM lookup returns an invalid BAR. (default:fatal).
53	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_PAGE_OVERFLOW: AIB command page overflow: The offset given in the command overflows the page size defined in the BAR SRAM (default:fatal).
54	ROX_CLRPART	INT_VC_WOF_ERR_G0_ATX_SRAM_ECC_CE: ATX sram Correctable ECC error (default:recov).
55:63	RO	Constant = 0b000000000

Register Name	Error Group 0 WOF Detail Register
Mnemonic	INT.INT_VC.INT_VC_WOF_ERR_G0_DETAIL
Address	0000000005013275 (SCOM)
Description	This register captures the error detailed information that belongs to the error logged in WOF error 0 register. MMIO offset = 0xB28

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	INT_VC_WOF_ERR_G0_DETAIL_ERROR:

Register Name	Who's On First Errors Group 1 Register
Mnemonic	INT.INT_VC.INT_VC_WOF_ERR_G1
Address	0000000005013276 (SCOM)
Description	This register captures the first non disabled group1 error reported This register is cleared on read. MMIO offset = 0xB30

Bits	SCOM	Field Mnemonic: Description
0	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_CL_INDEX_ERROR: CL index CAM error or IRQ buffer load oveflow (default:fatal).
1	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_CRD_OR_RESP_ERROR: A credit or response is returned by P3CQ whereas number of outstanding operations is zero (default:fatal).
2	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_PTAG_ASSIGN_ERROR: Ptag assign error: P1 receives a new command from P0 with a ptag which is not idle (default:fatal).
3	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_PTAG_RELEASE_ERROR: Ptag release error (default:fatal).
4	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_REPLAY_ERROR: Replay command error (default:fatal).
5	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_PARITY_ERROR: Parity error (default:fatal).
6	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_TAG_SRAM_ECC_UE: Uncorrectable P0 tag sram ecc error (default:fatal).
7	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_STATE_SRAM_ECC_UE: Uncorrectable P0 state sram ecc error (default:fatal).
8	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_DATA_SRAM_ECC_UE: Uncorrectable P1 data sram ecc error (default:fatal).
9	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_CTRL_SRAM_ECC_UE: Uncorrectable P1 control sram ecc error (default:fatal).
10	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_ARX_DATA_ECC_UE: Uncorrectable ARX to EQC ecc error (default:fatal).
11	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_UNLOCK_FIFO_OVERFLOW: Unlock FIFO overflow (default:fatal).
12	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_EOI_OVERFLOW: Inbound EOI command overflow: Receiving an inbound EOI command whereas all the EOI engines are busy. P3CQ should never send more than 8 outstanding. EOI commands (default:fatal).
13	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_EOI_TAG_ERROR: Inbound EOI tag error: Receiving an inbound EOI command associated with an AIB tag which is already processing a non speculative command. Or. receiving a speculative EOI with an AIB tag already in used (default:fatal).
14	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_SRAM_ECC_CE: Correctable ECC error (default:recov).
15	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_PROCESSING_ERROR: EQ trigger or Software EOI processing error (default:info).
16	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_WATCH_ERROR: Watch command on non owned EQD blockid (default:info).
17	ROX_CLRPART	INT_VC_WOF_ERR_G1_EQC_CONFIG_ERROR: EQ trigger configuration error (default:info).

Bits	SCOM	Field Mnemonic: Description
18	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_AIB_RESP_ERROR: aib response error. Receiving DMA response whereas there is no pending DMA read (default:fatal).
19	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_PTAG_ASSIGN_ERROR: Ptag assign error: P1 receives a new command from P0 with a ptag which is not idle (default:fatal).
20	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_PTAG_RELEASE_ERROR: Ptag release error: A ptag is released whereas it was not assigned. (default:fatal).
21	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_REPLAY_ERROR: Replay command error (default:fatal).
22	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_PARITY_ERROR: Parity error (default:fatal).
23	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_TAG_SRAM_ECC_UE: Uncorrectable P0 tag sram ecc error (default:fatal).
24	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_STATE_SRAM_ECC_UE: Uncorrectable P0 state sram ecc error (default:fatal).
25	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_DATA_SRAM_ECC_UE: Uncorrectable P1 data sram ecc error (default:fatal).
26	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_UNLOCK_FIFO_OVERFLOW: Unlock FIFO overflow (default:fatal).
27	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_SRAM_ECC_CE: Correctable ECC error (default:recov).
28	ROX_CLRPART	INT_VC_WOF_ERR_G1_IVC_PROCESSING_ERROR: IVC trigger processing error (default:info).
29	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_CL_INDEX_ERROR: CL index CAM error (default:fatal).
30	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_CRD_OR_RESP_ERROR: A credit or response is returned by P3CQ whereas number of outstanding operations is zero (default:fatal).
31	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_PTAG_ASSIGN_ERROR: Ptag assign error: P1 receives a new command from P0 with a ptag which is not idle (default:fatal).
32	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_PTAG_RELEASE_ERROR: Ptag release error: A ptag is released whereas it was not assigned (default:fatal).
33	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_REPLAY_ERROR: Replay command error (default:fatal).
34	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_PARITY_ERROR: Parity error (default:fatal).
35	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_TAG_SRAM_ECC_UE: Uncorrectable P0 tag sram ecc error (default:fatal).
36	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_STATE_SRAM_ECC_UE: Uncorrectable P0 state sram ecc error (default:fatal).
37	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_DATA_SRAM_ECC_UE: Uncorrectable P1 data sram ecc error (default:fatal).
38	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_UNLOCK_FIFO_OVERFLOW: Unlock FIFO overflow (default:fatal).
39	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_EOI_OVERFLOW: Inbound EOI command overflow: Receiving an inbound EOI command whereas all the EOI engines are busy. P3CQ should never send more than 8 outstanding. EOI commands. (default:fatal).
40	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_EOI_TAG_ERROR: Inbound EOI tag error: Receiving an inbound EOI command associated with an AIB tag which is already processing a non speculative command. Or. receiving a speculative EOI with an AIB tag already in used (default:fatal).

Bits	SCOM	Field Mnemonic: Description
41	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_SRAM_ECC_CE: Correctable ECC error (default:recov).
42	ROX_CLRPART	INT_VC_WOF_ERR_G1_SBC_PROCESSING_ERROR: Software EOI or Software Write on not owned blockid (default:info).
43:63	RO	Constant = 0b00000000000000000000

Register Name	Error Group 1 WOF Detail Register
Mnemonic	INT.INT_VC.INT_VC_WOF_ERR_G1_DETAIL
Address	0000000005013277 (SCOM)
Description	This register captures the error detailed information that belongs to the error logged in WOF error 1 register. MMIO offset = 0xB38

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	INT_VC_WOF_ERR_G1_DETAIL_ERROR:

Register Name	Fatal Errors Group 0 Register
Mnemonic	INT.INT_VC.INT_VC_FATAL_ERR_G0
Address	0000000005013278 (SCOM)
Description	This register accumulates all the group 0 fatal errors This register is cleared on read. MMIO offset = 0xB40

Bits	SCOM	Field Mnemonic: Description
0:54	ROX_CLRPART	INT_VC_FATAL_ERR_G0_ERROR: Bit n in this register corresponds to group 0 error bit n.
55:63	RO	Constant = 0b000000000

Register Name	Recoverable Errors Group 0 Register
Mnemonic	INT.INT_VC.INT_VC_RECOV_ERR_G0
Address	0000000005013279 (SCOM)
Description	This register accumulates all the group 0 recoverable errors This register is cleared on read. MMIO offset = 0xB48

Bits	SCOM	Field Mnemonic: Description
0:54	ROX_CLRPART	INT_VC_RECOV_ERR_G0_ERROR: Bit n in this register corresponds to group 0 error bit n.
55:63	RO	Constant = 0b000000000

Register Name	Informational Errors Group 0 Register
Mnemonic	INT.INT_VC.INT_VC_INFO_ERR_G0
Address	000000000501327A (SCOM)
Description	This register accumulates all the group 0 informational errors This register is cleared on read. MMIO offset = 0xB50

Bits	SCOM	Field Mnemonic: Description
0:54	ROX_CLRPART	INT_VC_INFO_ERR_G0_ERROR: Bit n in this register corresponds to group 0 error bit n.
55:63	RO	Constant = 0b000000000

Register Name	Fatal Errors Group 1 Register
Mnemonic	INT.INT_VC.INT_VC_FATAL_ERR_G1
Address	000000000501327B (SCOM)
Description	This register accumulates all the group 1 fatal errors This register is cleared on read. MMIO offset = 0xB58

Bits	SCOM	Field Mnemonic: Description
0:42	ROX_CLRPART	INT_VC_FATAL_ERR_G1_ERROR: Bit n in this register corresponds to group 1 error bit n.
43:63	RO	Constant = 0b00000000000000000000

Register Name	Recoverable Errors Group 1 Register
Mnemonic	INT.INT_VC.INT_VC_RECOV_ERR_G1
Address	000000000501327C (SCOM)
Description	This register accumulates all the group 1 recoverable errors This register is cleared on read. MMIO offset = 0xB60

Bits	SCOM	Field Mnemonic: Description
0:42	ROX_CLRPART	INT_VC_RECOV_ERR_G1_ERROR: Bit n in this register corresponds to group 1 error bit n.
43:63	RO	Constant = 0b00000000000000000000

Register Name	Informational Errors Group 1 Register
Mnemonic	INT.INT_VC.INT_VC_INFO_ERR_G1
Address	000000000501327D (SCOM)
Description	This register accumulates all the group 1 informational errors This register is cleared on read. MMIO offset = 0xB68

Bits	SCOM	Field Mnemonic: Description
0:42	ROX_CLRPART	INT_VC_INFO_ERR_G1_ERROR: Bit n in this register corresponds to group 1 error bit n.
43:63	RO	Constant = 0b00000000000000000000

Register Name	Power Bus PBEN IOX Domain FIR0 Register
Mnemonic	PB.IOE.SCOM.PB_IOE_FIR_REG
Address	0000000005013400 (SCOM) 0000000005013401 (SCOM1) 0000000005013402 (SCOM2)
Description	Processor bus PBEN IOX domain FIR0 register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FMR00_TRAINED: fmr00 trained.
1	RWX	WOX_AND	WOX_OR	FMR01_TRAINED: fmr01 trained.
2	RWX	WOX_AND	WOX_OR	FMR02_TRAINED: fmr02 trained.
3	RWX	WOX_AND	WOX_OR	FMR03_TRAINED: fmr03 trained.
4	RWX	WOX_AND	WOX_OR	FMR04_TRAINED: fmr04 trained.
5	RWX	WOX_AND	WOX_OR	FMR05_TRAINED: fmr05 trained.
6	RWX	WOX_AND	WOX_OR	RSV6: rsv6.
7	RWX	WOX_AND	WOX_OR	RSV7: rsv7.
8	RWX	WOX_AND	WOX_OR	DOB01_UE: dob01 ue.
9	RWX	WOX_AND	WOX_OR	DOB01_CE: dob01 ce.
10	RWX	WOX_AND	WOX_OR	DOB01_SUE: dob01 sue.
11	RWX	WOX_AND	WOX_OR	DOB23_UE: dob23 ue.
12	RWX	WOX_AND	WOX_OR	DOB23_CE: dob23 ce.
13	RWX	WOX_AND	WOX_OR	DOB23_SUE: dob23 sue.
14	RWX	WOX_AND	WOX_OR	DOB45_UE: dob45 ue.
15	RWX	WOX_AND	WOX_OR	DOB45_CE: dob45 ce.
16	RWX	WOX_AND	WOX_OR	DOB45_SUE: dob45 sue.
17	RWX	WOX_AND	WOX_OR	RSV17: rsv17.
18	RWX	WOX_AND	WOX_OR	RSV18: rsv18.
19	RWX	WOX_AND	WOX_OR	RSV19: rsv19.
20	RWX	WOX_AND	WOX_OR	FRAMER00_ATTN: framer00 attn - X0 even link framer internal error, or outbound switch cmd/presp/cresp internal error.
21	RWX	WOX_AND	WOX_OR	FRAMER01_ATTN: framer01 attn - X0 odd link framer internal error.
22	RWX	WOX_AND	WOX_OR	FRAMER02_ATTN: framer02 attn - X1 even link framer internal error, or outbound switch cmd/presp/cresp internal error.
23	RWX	WOX_AND	WOX_OR	FRAMER03_ATTN: framer03 attn - X1 odd link framer internal error.
24	RWX	WOX_AND	WOX_OR	FRAMER04_ATTN: framer04 attn - X2 even link framer internal error, or outbound switch cmd/presp/cresp internal error.
25	RWX	WOX_AND	WOX_OR	FRAMER05_ATTN: framer05 attn - X2 odd link framer internal error.
26	RWX	WOX_AND	WOX_OR	RSV26: rsv26.
27	RWX	WOX_AND	WOX_OR	RSV27: rsv27.
28	RWX	WOX_AND	WOX_OR	PARSER00_ATTN: parser00 attn.
29	RWX	WOX_AND	WOX_OR	PARSER01_ATTN: parser01 attn.
30	RWX	WOX_AND	WOX_OR	PARSER02_ATTN: parser02 attn.
31	RWX	WOX_AND	WOX_OR	PARSER03_ATTN: parser03 attn.
32	RWX	WOX_AND	WOX_OR	PARSER04_ATTN: parser04 attn.
33	RWX	WOX_AND	WOX_OR	PARSER05_ATTN: parser05 attn.
34	RWX	WOX_AND	WOX_OR	RSV34: rsv34.
35	RWX	WOX_AND	WOX_OR	RSV35: rsv35.
36	RWX	WOX_AND	WOX_OR	MB00_SPATTN: mb00 spattn.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
37	RWX	WOX_AND	WOX_OR	MB01_SPATTN: mb01 spattn.
38	RWX	WOX_AND	WOX_OR	MB10_SPATTN: mb10 spattn.
39	RWX	WOX_AND	WOX_OR	MB11_SPATTN: mb11 spattn.
40	RWX	WOX_AND	WOX_OR	MB20_SPATTN: mb20 spattn.
41	RWX	WOX_AND	WOX_OR	MB21_SPATTN: mb21 spattn.
42	RWX	WOX_AND	WOX_OR	MB30_SPATTN: mb30 spattn.
43	RWX	WOX_AND	WOX_OR	MB31_SPATTN: mb31 spattn.
44	RWX	WOX_AND	WOX_OR	MB40_SPATTN: mb40 spattn.
45	RWX	WOX_AND	WOX_OR	MB41_SPATTN: mb41 spattn.
46	RWX	WOX_AND	WOX_OR	MB50_SPATTN: mb50 spattn.
47	RWX	WOX_AND	WOX_OR	MB51_SPATTN: mb51 spattn.
48:51	RWX	WOX_AND	WOX_OR	Reserved.
52	RWX	WOX_AND	WOX_OR	DOB01_ERR: data outbound switch internal error - links 01.
53	RWX	WOX_AND	WOX_OR	DOB23_ERR: data outbound switch internal error - links 23.
54	RWX	WOX_AND	WOX_OR	DOB45_ERR: data outbound switch internal error - links 45.
55	RWX	WOX_AND	WOX_OR	Reserved.
56	RWX	WOX_AND	WOX_OR	DIB01_ERR: data inbound switch internal error - links 01.
57	RWX	WOX_AND	WOX_OR	DIB23_ERR: data inbound switch internal error - links 23.
58	RWX	WOX_AND	WOX_OR	DIB45_ERR: data inbound switch internal error - links 45.
59:61	RWX	WOX_AND	WOX_OR	Reserved.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP: FIR SCOM err dup.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR: FIR SCOM err.

Register Name	**Power Bus PBEN IOX Domain FIR0 Mask Register**
Mnemonic	PB.IOE.SCOM.PB_IOE_FIR_MASK_REG
Address	0000000005013403 (SCOM) 0000000005013404 (SCOM1) 0000000005013405 (SCOM2)
Description	Processor bus PBEN IOX domain FIR0 Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FMR00_TRAINED_MASK: fmr00 trained mask.
1	RWX	WOX_AND	WOX_OR	FMR01_TRAINED_MASK: fmr01 trained mask.
2	RWX	WOX_AND	WOX_OR	FMR02_TRAINED_MASK: fmr02 trained mask.
3	RWX	WOX_AND	WOX_OR	FMR03_TRAINED_MASK: fmr03 trained mask.
4	RWX	WOX_AND	WOX_OR	FMR04_TRAINED_MASK: fmr04 trained mask.
5	RWX	WOX_AND	WOX_OR	FMR05_TRAINED_MASK: fmr05 trained.
6	RWX	WOX_AND	WOX_OR	RSV6_MASK: rsv6 mask.
7	RWX	WOX_AND	WOX_OR	RSV7_MASK: rsv7 mask.
8	RWX	WOX_AND	WOX_OR	DOB01_UE_MASK: dob01 ue mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	DOB01_CE_MASK: dob01 ce mask.
10	RWX	WOX_AND	WOX_OR	DOB01_SUE_MASK: dob01 sue mask.
11	RWX	WOX_AND	WOX_OR	DOB23_UE_MASK: dob23 ue mask.
12	RWX	WOX_AND	WOX_OR	DOB23_CE_MASK: dob23 ce mask.
13	RWX	WOX_AND	WOX_OR	DOB23_SUE_MASK: dob23 sue mask.
14	RWX	WOX_AND	WOX_OR	DOB45_UE_MASK: dob45 ue mask.
15	RWX	WOX_AND	WOX_OR	DOB45_CE_MASK: dob45 ce mask.
16	RWX	WOX_AND	WOX_OR	DOB45_SUE_MASK: dob45 sue mask.
17	RWX	WOX_AND	WOX_OR	RSV17_MASK: rsv17 mask.
18	RWX	WOX_AND	WOX_OR	RSV18_MASK: rsv18 mask.
19	RWX	WOX_AND	WOX_OR	RSV19_MASK: rsv19 mask.
20	RWX	WOX_AND	WOX_OR	FRAMER00_ATTN_MASK: framer00 attn mask.
21	RWX	WOX_AND	WOX_OR	FRAMER01_ATTN_MASK: framer01 attn mask.
22	RWX	WOX_AND	WOX_OR	FRAMER02_ATTN_MASK: framer02 attn mask.
23	RWX	WOX_AND	WOX_OR	FRAMER03_ATTN_MASK: framer03 attn mask.
24	RWX	WOX_AND	WOX_OR	FRAMER04_ATTN_MASK: framer04 attn mask.
25	RWX	WOX_AND	WOX_OR	FRAMER05_ATTN_MASK: framer05 attn mask.
26	RWX	WOX_AND	WOX_OR	RSV26_MASK: rsv26 mask.
27	RWX	WOX_AND	WOX_OR	RSV27_MASK: rsv27 mask.
28	RWX	WOX_AND	WOX_OR	PARSER00_ATTN_MASK: parser00 attn mask.
29	RWX	WOX_AND	WOX_OR	PARSER01_ATTN_MASK: parser01 attn mask.
30	RWX	WOX_AND	WOX_OR	PARSER02_ATTN_MASK: parser02 attn mask.
31	RWX	WOX_AND	WOX_OR	PARSER03_ATTN_MASK: parser03 attn mask.
32	RWX	WOX_AND	WOX_OR	PARSER04_ATTN_MASK: parser04 attn mask.
33	RWX	WOX_AND	WOX_OR	PARSER05_ATTN_MASK: parser05 attn mask.
34	RWX	WOX_AND	WOX_OR	RSV34_MASK: rsv34 mask.
35	RWX	WOX_AND	WOX_OR	RSV35_MASK: rsv35 mask.
36	RWX	WOX_AND	WOX_OR	MB00_SPATTN_MASK: mb00 spattn mask.
37	RWX	WOX_AND	WOX_OR	MB01_SPATTN_MASK: mb01 spattn mask.
38	RWX	WOX_AND	WOX_OR	MB10_SPATTN_MASK: mb10 spattn mask.
39	RWX	WOX_AND	WOX_OR	MB11_SPATTN_MASK: mb11 spattn mask.
40	RWX	WOX_AND	WOX_OR	MB20_SPATTN_MASK: mb20 spattn mask.
41	RWX	WOX_AND	WOX_OR	MB21_SPATTN_MASK: mb21 spattn mask.
42	RWX	WOX_AND	WOX_OR	MB30_SPATTN_MASK: mb30 spattn mask.
43	RWX	WOX_AND	WOX_OR	MB31_SPATTN_MASK: mb31 spattn mask.
44	RWX	WOX_AND	WOX_OR	MB40_SPATTN_MASK: mb40 spattn mask.
45	RWX	WOX_AND	WOX_OR	MB41_SPATTN_MASK: mb41 spattn mask.
46	RWX	WOX_AND	WOX_OR	MB50_SPATTN_MASK: mb50 spattn mask.
47	RWX	WOX_AND	WOX_OR	MB51_SPATTN_MASK: mb51 spattn mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
48:51	RWX	WOX_AND	WOX_OR	Reserved.
52	RWX	WOX_AND	WOX_OR	DOB01_ERR_MASK: data outbound switch internal error mask - links 01.
53	RWX	WOX_AND	WOX_OR	DOB23_ERR_MASK: data outbound switch internal error mask - links 23.
54	RWX	WOX_AND	WOX_OR	DOB45_ERR_MASK: data outbound switch internal error mask - links 45.
55	RWX	WOX_AND	WOX_OR	Reserved.
56	RWX	WOX_AND	WOX_OR	DIB01_ERR_MASK: data inbound switch internal error mask - links 01.
57	RWX	WOX_AND	WOX_OR	DIB23_ERR_MASK: data inbound switch internal error mask - links 23.
58	RWX	WOX_AND	WOX_OR	DIB45_ERR_MASK: data inbound switch internal error mask - links 45.
59:61	RWX	WOX_AND	WOX_OR	Reserved.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_MASK_DUP: FIR SCOM err mask dup.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_MASK: FIR SCOM err mask.

Register Name	**Power Bus PBEN IOX Domain FIR Action 0 Register**
Mnemonic	PB.IOE.SCOM.PB_IOE_FIR_ACTION0_REG
Address	0000000005013406 (SCOM)
Description	Processor bus PBEN IOX domain FIR Action 0 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PB_IOE_FIR_ACTION0: Processor bus IOE domain action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Special Attention to Service Processor. (1,1) = Invalid.

Register Name	**Power Bus PBEN IOX Domain FIR Action 1 Register**
Mnemonic	PB.IOE.SCOM.PB_IOE_FIR_ACTION1_REG
Address	0000000005013407 (SCOM)
Description	Processor bus PBEN IOX domain FIR Action 1 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PB_IOE_FIR_ACTION1: Processor bus FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Special Attention to Service Processor. (1,1) = Invalid.

Register Name	**Power Bus Electrical Framer/Parser 01 Configuration Register**
Mnemonic	PB.IOE.SCOM.PB_FP01_CFG
Address	000000000501340A (SCOM)
Description	Processor bus Electrical Framer/Parser 01 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	FP0_CREDIT_PRIORITY_4_NOT_8: fp0 credit priority 4 not 8.
1	RW	FP0_DISABLE_GATHERING: fp0 disable data gathering.
2	RW	FP0_DISABLE_CMD_COMPRESSION: fp0 disable command compression.
3	RW	FP0_DISABLE_PRSP_COMPRESSION: fp0 disable prsp compression.
4:11	RW	FP0_LL_CREDIT_LO_LIMIT: fp0 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(25.5 - (nest freq/elec freq)*10.75)).
12:19	RW	FP0_LL_CREDIT_HI_LIMIT: fp0 ll credit high limit - frames in flight limit during stop_cmds/replay.
20	RW	FP0_FMR_DISABLE: fp0 framer disable - turn the framer clocks OFF.
21	RW	FP0_FMR_SPARE: fp0 framer spare.
22:23	RW	FP01_CMD_EXP_TIME: obs/fmr/prs command expiration time = (value * 2) + 9.
24	RW	FP0_RUN_AFTER_FRAME_ERROR: fp0 run after frame error.
25	RW	FP0_PRS_DISABLE: fp0 parser disable - turn the parser clocks OFF.
26:31	RW	FP0_PRS_SPARE: fp0 parser spare.
32	RW	FP1_CREDIT_PRIORITY_4_NOT_8: fp1 credit priority 4 not 8.
33	RW	FP1_DISABLE_GATHERING: fp1 disable data gathering.
34	RW	FP1_DISABLE_CMD_COMPRESSION: fp1 disable command compression.
35	RW	FP1_DISABLE_PRSP_COMPRESSION: fp1 disable prsp compression.
36:43	RW	FP1_LL_CREDIT_LO_LIMIT: fp1 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(25.5 - (nest freq/elec freq)*10.75)).
44:51	RW	FP1_LL_CREDIT_HI_LIMIT: fp1 ll credit high limit - frames in flight limit during stop_cmds/replay.
52	RW	FP1_FMR_DISABLE: fp1 framer disable - turn the framer clocks OFF.
53:55	RW	FP1_FMR_SPARE: fp1 framer spare.
56	RW	FP1_RUN_AFTER_FRAME_ERROR: fp1 run after frame error.
57	RW	FP1_PRS_DISABLE: fp1 parser disable - turn the parser clocks OFF.
58:63	RW	FP1_PRS_SPARE: fp1 parser spare.

Register Name	**Power Bus Electrical Framer/Parser 23 Configuration Register**
Mnemonic	PB.IOE.SCOM.PB_FP23_CFG
Address	0000000005013408 (SCOM)
Description	Processor bus Electrical Framer/Parser 23 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	FP2_CREDIT_PRIORITY_4_NOT_8: fp2 credit priority 4 not 8.
1	RW	FP2_DISABLE_GATHERING: fp2 disable data gathering.
2	RW	FP2_DISABLE_CMD_COMPRESSION: fp2 disable command compression.
3	RW	FP2_DISABLE_PRSP_COMPRESSION: fp2 disable prsp compression.
4:11	RW	FP2_LL_CREDIT_LO_LIMIT: fp2 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(25.5 - (nest freq/elec freq)*10.75)).
12:19	RW	FP2_LL_CREDIT_HI_LIMIT: fp2 ll credit high limit - frames in flight limit during stop_cmds/replay.
20	RW	FP2_FMR_DISABLE: fp2 framer disable - turn the framer clocks OFF.

Bits	SCOM	Field Mnemonic: Description
21	RW	FP2_FMR_SPARE: fp2 framer spare.
22:23	RW	FP23_CMD_EXP_TIME: obs/fmr/prs command expiration time = (value * 2) + 9.
24	RW	FP2_RUN_AFTER_FRAME_ERROR: fp2 run after frame error.
25	RW	FP2_PRS_DISABLE: fp2 parser disable - turn the parser clocks OFF.
26:31	RW	FP2_PRS_SPARE: fp2 parser spare.
32	RW	FP3_CREDIT_PRIORITY_4_NOT_8: fp3 credit priority 4 not 8.
33	RW	FP3_DISABLE_GATHERING: fp3 disable data gathering.
34	RW	FP3_DISABLE_CMD_COMPRESSION: fp3 disable command compression.
35	RW	FP3_DISABLE_PRSP_COMPRESSION: fp3 disable prsp compression.
36:43	RW	FP3_LL_CREDIT_LO_LIMIT: fp3 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(25.5 - (nest freq/elec freq)*10.75)).
44:51	RW	FP3_LL_CREDIT_HI_LIMIT: fp3 ll credit high limit - frames in flight limit during stop_cmds/replay.
52	RW	FP3_FMR_DISABLE: fp3 framer disable - turn the framer clocks OFF.
53:55	RW	FP3_FMR_SPARE: fp3 framer spare.
56	RW	FP3_RUN_AFTER_FRAME_ERROR: fp3 run after frame error.
57	RW	FP3_PRS_DISABLE: fp3 parser disable - turn the parser clocks OFF.
58:63	RW	FP3_PRS_SPARE: fp3 parser spare.

Register Name	Power Bus Electrical Framer/Parser 45 Configuration Register
Mnemonic	PB.IOE.SCOM.PB_FP45_CFG
Address	000000000501340C (SCOM)
Description	Processor bus Electrical Framer/Parser 45 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	FP4_CREDIT_PRIORITY_4_NOT_8: fp4 credit priority 4 not 8.
1	RW	FP4_DISABLE_GATHERING: fp4 disable data gathering.
2	RW	FP4_DISABLE_CMD_COMPRESSION: fp4 disable command compression.
3	RW	FP4_DISABLE_PRSP_COMPRESSION: fp4 disable prsp compression.
4:11	RW	FP4_LL_CREDIT_LO_LIMIT: fp4 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(25.5 - (nest freq/elec freq)*10.75)).
12:19	RW	FP4_LL_CREDIT_HI_LIMIT: fp4 ll credit high limit - frames in flight limit during stop_cmds/replay.
20	RW	FP4_FMR_DISABLE: fp4 framer disable - turn the framer clocks OFF.
21	RW	FP4_FMR_SPARE: fp4 framer spare.
22:23	RW	FP45_CMD_EXP_TIME: obs/fmr/prs command expiration time = (value * 2) + 9.
24	RW	FP4_RUN_AFTER_FRAME_ERROR: fp4 run after frame error.
25	RW	FP4_PRS_DISABLE: fp4 parser disable - turn the parser clocks OFF.
26:31	RW	FP4_PRS_SPARE: fp4 parser spare.
32	RW	FP5_CREDIT_PRIORITY_4_NOT_8: fp5 credit priority 4 not 8.
33	RW	FP5_DISABLE_GATHERING: fp5 disable data gathering.
34	RW	FP5_DISABLE_CMD_COMPRESSION: fp5 disable command compression.

Bits	SCOM	Field Mnemonic: Description
35	RW	FP5_DISABLE_PRSP_COMPRESSION: fp5 disable prsp compression.
36:43	RW	FP5_LL_CREDIT_LO_LIMIT: fp5 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(25.5 - (nest freq/elec freq)*10.75)).
44:51	RW	FP5_LL_CREDIT_HI_LIMIT: fp5 ll credit high limit - frames in flight limit during stop_cmds/replay.
52	RW	FP5_FMR_DISABLE: fp5 framer disable - turn the framer clocks OFF.
53:55	RW	FP5_FMR_SPARE: fp5 framer spare.
56	RW	FP5_RUN_AFTER_FRAME_ERROR: fp5 run after frame error.
57	RW	FP5_PRS_DISABLE: fp5 parser disable - turn the parser clocks OFF.
58:63	RW	FP5_PRS_SPARE: fp5 parser spare.

Register Name	**Power Bus Electrical Link Delay 0123 Register**
Mnemonic	PB.IOE.SCOM.PB_ELINK_DLY_0123_REG
Address	000000000501340E (SCOM)
Description	Processor bus Electrical Link Delay 0123 Register

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b0000
4:15	ROX	Reserved.
16:19	RO	Constant = 0b0000
20:31	ROX	Reserved.
32:35	RO	Constant = 0b0000
36:47	ROX	Reserved.
48:51	RO	Constant = 0b0000
52:63	ROX	Reserved.

Register Name	**Power Bus Electrical Link Delay 45 Register**
Mnemonic	PB.IOE.SCOM.PB_ELINK_DLY_45_REG
Address	000000000501340F (SCOM)
Description	Processor bus Electrical Link Delay 45 Register

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b0000
4:15	ROX	Reserved.
16:19	RO	Constant = 0b0000
20:31	ROX	Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Power Bus Electrical Link Data Buffer 01 Configuration Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_DATA_01_CFG_REG
Address	0000000005013410 (SCOM)
Description	Processor bus Electrical Link Data Buffer 01 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1:7	RW	PB_CFG_LINK0_DOB_LIMIT: pb configuration link0 dob limit - total link credits avail.
8	RW	Reserved.
9:15	RW	PB_CFG_LINK0_DOB_VC0_LIMIT: pb configuration link0 dob vc0 limit - vc0 link credits max.
16	RW	Reserved.
17:23	RW	PB_CFG_LINK0_DOB_VC1_LIMIT: pb configuration link0 dob vc1 limit - vc1 link credits max.
24:28	RW	PB_CFG_LINK01_DIB_VC_LIMIT: pb configuration link01 dib vc limit - limit per VC for data inbound to pbien/s (set to 31/16/8 for 1/2/4 channels in use) (both links use same credit pool).
29:32	RW	Reserved.
33:39	RW	PB_CFG_LINK1_DOB_LIMIT: pb configuration link1 dob limit - total link credits avail.
40	RW	Reserved.
41:47	RW	PB_CFG_LINK1_DOB_VC0_LIMIT: pb configuration link1 dob vc0 limit - vc0 link credits max.
48	RW	Reserved.
49:55	RW	PB_CFG_LINK1_DOB_VC1_LIMIT: pb configuration link1 dob vc1 limit - vc1 link credits max.

Register Name	Power Bus Electrical Link Data Buffer 23 Configuration Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_DATA_23_CFG_REG
Address	0000000005013411 (SCOM)
Description	Processor bus Electrical Link Data Buffer 23 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1:7	RW	PB_CFG_LINK2_DOB_LIMIT: pb configuration link2 dob limit - total link credits avail.
8	RW	Reserved.
9:15	RW	PB_CFG_LINK2_DOB_VC0_LIMIT: pb configuration link2 dob vc0 limit - vc0 link credits max.
16	RW	Reserved.
17:23	RW	PB_CFG_LINK2_DOB_VC1_LIMIT: pb configuration link2 dob vc1 limit - vc1 link credits max.
24:28	RW	PB_CFG_LINK23_DIB_VC_LIMIT: pb configuration link23 dib vc limit - limit per VC for data inbound to pbien/s (set to 31/16/8 for 1/2/4 channels in use) (both links use same credit pool).
29:32	RW	Reserved.
33:39	RW	PB_CFG_LINK3_DOB_LIMIT: pb configuration link3 dob limit - total link credits avail.
40	RW	Reserved.
41:47	RW	PB_CFG_LINK3_DOB_VC0_LIMIT: pb configuration link3 dob vc0 limit - vc0 link credits max.
48	RW	Reserved.
49:55	RW	PB_CFG_LINK3_DOB_VC1_LIMIT: pb configuration link3 dob vc1 limit - vc1 link credits max.

Register Name	Power Bus Electrical Link Data Buffer 45 Configuration Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_DATA_45_CFG_REG
Address	0000000005013412 (SCOM)
Description	Processor bus Electrical Link Data Buffer 45 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1:7	RW	PB_CFG_LINK4_DOB_LIMIT: pb configuration link4 dob limit - total link credits avail.
8	RW	Reserved.
9:15	RW	PB_CFG_LINK4_DOB_VC0_LIMIT: pb configuration link4 dob vc0 limit - vc0 link credits max.
16	RW	Reserved.
17:23	RW	PB_CFG_LINK4_DOB_VC1_LIMIT: pb configuration link4 dob vc1 limit - vc1 link credits max.
24:28	RW	PB_CFG_LINK45_DIB_VC_LIMIT: pb configuration link45 dib vc limit - limit per VC for data inbound to pbien/s (set to 31/16/8 for 1/2/4 channels in use) (both links use same credit pool).
29:32	RW	Reserved.
33:39	RW	PB_CFG_LINK5_DOB_LIMIT: pb configuration link5 dob limit - total link credits avail.
40	RW	Reserved.
41:47	RW	PB_CFG_LINK5_DOB_VC0_LIMIT: pb configuration link5 dob vc0 limit - vc0 link credits max.
48	RW	Reserved.
49:55	RW	PB_CFG_LINK5_DOB_VC1_LIMIT: pb configuration link5 dob vc1 limit - vc1 link credits max.

Register Name	Power Bus Electrical Link 01 Syndrome Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_SYN_01_REG
Address	0000000005013414 (SCOM)
Description	Processor bus Electrical Link 01 Syndrome Register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved.
8:15	ROX	Reserved.
16:23	ROX	Reserved.
24:31	ROX	Reserved.
32:39	ROX	Reserved.
40:47	ROX	Reserved.
48:55	ROX	Reserved.
56:63	ROX	Reserved.

Register Name	Power Bus Electrical Link 23 Syndrome Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_SYN_23_REG
Address	0000000005013415 (SCOM)
Description	Processor bus Electrical Link 23 Syndrome Register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved.
8:15	ROX	Reserved.
16:23	ROX	Reserved.
24:31	ROX	Reserved.
32:39	ROX	Reserved.
40:47	ROX	Reserved.
48:55	ROX	Reserved.
56:63	ROX	Reserved.

Register Name	Power Bus Electrical Link 45 Syndrome Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_SYN_45_REG
Address	0000000005013416 (SCOM)
Description	Processor bus Electrical Link 45 Syndrome Register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved.
8:15	ROX	Reserved.
16:23	ROX	Reserved.
24:31	ROX	Reserved.
32:39	ROX	Reserved.
40:47	ROX	Reserved.
48:55	ROX	Reserved.
56:63	ROX	Reserved.

Register Name	Power Bus Electrical Link UE/CE/SUE Register
Mnemonic	PB.IOE.SCOM.PB_EN_DOB_ECC_ERR_REG
Address	0000000005013418 (SCOM)
Description	Processor bus Electrical Link UE/CE/SUE Register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved.
4:7	ROX	Reserved.
8:11	ROX	Reserved.
12:15	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
16:19	ROX	Reserved.
20:23	ROX	Reserved.
24:27	ROX	Reserved.
28:31	ROX	Reserved.
32:35	ROX	Reserved.

Register Name	Power Bus Electrical Round Trip Delay Control Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_RT_DELAY_CTL_REG
Address	0000000005013419 (SCOM)
Description	Trip Delay Control Register

Bits	SCOM	Field Mnemonic: Description
0:5	WO_1P	PB_ELINK_RT_DELAY_CTL_SET: Setting a bit to 1 (auto reset to 0) causes the matching link to attempt to do a round-trip delay calculation. Results end up in the PB_ELINK_DLY_*_REG regs.
6:7	WO_1P	Reserved.
8:13	RWX_WCLRPART	PB_ELINK_RT_DELAY_CTL_STAT: A write of the reg resets these bits. They get set to 1 when a requested round-trip calculation completes.

Register Name	Power Bus Electrical Link Performance Monitor Control Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_PMU_CTL_REG
Address	000000000501341A (SCOM)
Description	Processor bus Electrical Link Performance Monitor Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	PMU0_ENABLE: pmu0 enable (the selected half-link must also be active).
1	RW	PMU1_ENABLE: pmu1 enable (the selected half-link must also be active).
2	RW	PMU2_ENABLE: pmu2 enable (the selected half-link must also be active).
3	RW	PMU3_ENABLE: pmu3 enable (the selected half-link must also be active).
4	RW	PMU4_ENABLE: pmu4 enable (the selected half-link must also be active).
5	RW	PMU5_ENABLE: pmu5 enable (the selected half-link must also be active).
6	RW	PMU6_ENABLE: pmu6 enable (the selected half-link must also be active).
7	RW	PMU7_ENABLE: pmu7 enable (the selected half-link must also be active).
8	RW	PMULET_FREEZE_MODE: PMUlet freeze mode: 0 = freeze-on-full, 1 = freerun.
9	RW	COMMON_FREEZE_MODE: common freeze mode: 0 = independant per PMUlet, 1 = any counter full freezes all.
10	RW	PMULET_RESET_MODE: PMUlet reset mode: 0 = reset on read, 1 = reset on write.
11	RW	PMU_EVENT0_SEL: Event0 selection: 0 = cycles, 1 = available cycles.

Bits	SCOM	Field Mnemonic: Description
12:15	RW	PMU_EVENT1_SEL: Event1 selection - 16:1 encode selection 0 disabled - clocks gated off 1 any RCMD - event 2 CRESP - event 3 any presp - event 4 dhdr - event 5 data - event 6 credit - event 7 RCMD drop - event 8 presp drop - dropped at this chip - event 9 presp drop - dropped at remote chip - event A command utilization - 1 count per 16 B used per available cycle B presp util - 1 count per 16 B used per available cycle C dhdr + data util - 1 count per 16B used per available cycle D total utilization - 1 count per 16 B used per available cycle E cycles (available)(generally 4/5, unless replays happening) - event F tdm_mode cycles (raw) - event.
16:19	RW	PMU_EVENT2_SEL: Event2 selection - 16:1.
20:23	RW	PMU_EVENT3_SEL: Event3 selection - 16:1.
24:25	RW	PMU0_SIZE: pmu0 size 00 = 36 bits 01 = 32 bits 10 = 28 bits 11 = 20 bits (only the 16 MSB are readable).
26:27	RW	PMU1_SIZE: pmu1 size 00 = 36 bits 01 = 32 bits 10 = 28 bits 11 = 20 bits (only the 16 MSB are readable).
28:29	RW	PMU2_SIZE: pmu2 size 00 = 36 bits 01 = 32 bits 10 = 28 bits 11 = 20 bits (only the 16 MSB are readable).
30:31	RW	PMU3_SIZE: pmu3 size 00 = 36 bits 01 = 32 bits 10 = 28 bits 11 = 20 bits (only the 16 MSB are readable).
32	RW	PMU01_LINK_SELECT: pmu01 link select: 0 = X0, 1 = X1.
33	RW	PMU23_LINK_SELECT: pmu23 link select: 0 = X1, 1 = X0.
34	RW	PMU45_LINK_SELECT: pmu45 link select: 0 = X2, 1 = --
35	RW	PMU67_LINK_SELECT: pmu67 link select: 0 = --, 1 = X2.
36:37	RW	PMU0145_EVENT0_MODE: pmu0145 event0 mode: 10 = link_in, 01 = link_out, 11 = sum.
38:39	RW	PMU0145_EVENT1_MODE: pmu0145 event1 mode: 10 = link_in, 01 = link_out, 11 = sum.
40:41	RW	PMU0145_EVENT2_MODE: pmu0145 event2 mode: 10 = link_in, 01 = link_out, 11 = sum.
42:43	RW	PMU0145_EVENT3_MODE: pmu0145 event3 mode: 10 = link_in, 01 = link_out, 11 = sum.
44:45	RW	PMU2367_EVENT0_MODE: pmu2367 event0 mode: 10 = link_in, 01 = link_out, 11 = sum.
46:47	RW	PMU2367_EVENT1_MODE: pmu2367 event1 mode: 10 = link_in, 01 = link_out, 11 = sum.
48:49	RW	PMU2367_EVENT2_MODE: pmu2367 event2 mode: 10 = link_in, 01 = link_out, 11 = sum.
50:51	RW	PMU2367_EVENT3_MODE: pmu2367 event3 mode: 10 = link_in, 01 = link_out, 11 = sum.
52	RW	PMU_ENABLE_GLOBAL_RUN: Enable global controls 0 = ignore global run state; 1 = follow global run state.
53	RW	PMU_GLOBAL_RUN_MODE: Global behavior mode 0 = run/stop with global run state 1 = same as 0, plus reset upon rising edge of global run.
54:63	RW	PMU_SPARE: pmu spare.

Register Name	Power Bus Electrical Link Performance Monitor 0 Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_PMU0
Address	000000000501341B (SCOM)
Description	Processor bus Electrical Link PerfMon0 Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU0_COUNTER0: PMU0 performance counter0.
16:31	RWX_WCLRREG	PMU0_COUNTER1: PMU0 performance counter1.
32:47	RWX_WCLRREG	PMU0_COUNTER2: PMU0 performance counter2.
48:63	RWX_WCLRREG	PMU0_COUNTER3: PMU0 performance counter3.

Register Name	Power Bus Electrical Link Performance Monitor 1 Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_PMU1
Address	000000000501341C (SCOM)
Description	Processor bus Electrical Link PerfMon1 Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU1_COUNTER0: PMU1 performance counter0.
16:31	RWX_WCLRREG	PMU1_COUNTER1: PMU1 performance counter1.
32:47	RWX_WCLRREG	PMU1_COUNTER2: PMU1 performance counter2.
48:63	RWX_WCLRREG	PMU1_COUNTER3: PMU1 performance counter3.

Register Name	Power Bus Electrical Link Performance Monitor 2 Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_PMU2
Address	000000000501341D (SCOM)
Description	Processor bus Electrical Link PerfMon2 Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU2_COUNTER0: PMU2 performance counter0.
16:31	RWX_WCLRREG	PMU2_COUNTER1: PMU2 performance counter1.
32:47	RWX_WCLRREG	PMU2_COUNTER2: PMU2 performance counter2.
48:63	RWX_WCLRREG	PMU2_COUNTER3: PMU2 performance counter3.

Register Name	Power Bus Electrical Link Performance Monitor 3 Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_PMU3
Address	000000000501341E (SCOM)
Description	Processor bus Electrical Link PerfMon3 Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU3_COUNTER0: PMU3 performance counter0.

Bits	SCOM	Field Mnemonic: Description
16:31	RWX_WCLRREG	PMU3_COUNTER1: PMU3 performance counter1.
32:47	RWX_WCLRREG	PMU3_COUNTER2: PMU3 performance counter2.
48:63	RWX_WCLRREG	PMU3_COUNTER3: PMU3 performance counter3.

Register Name	Power Bus Electrical Link Performance Monitor 4 Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_PMU4
Address	000000000501341F (SCOM)
Description	Processor bus Electrical Link PerfMon4 Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU4_COUNTER0: PMU4 performance counter0.
16:31	RWX_WCLRREG	PMU4_COUNTER1: PMU4 performance counter1.
32:47	RWX_WCLRREG	PMU4_COUNTER2: PMU4 performance counter2.
48:63	RWX_WCLRREG	PMU4_COUNTER3: PMU4 performance counter3.

Register Name	Power Bus Electrical Link Performance Monitor 5 Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_PMU5
Address	0000000005013420 (SCOM)
Description	Processor bus Electrical Link PerfMon5 Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU5_COUNTER0: PMU5 performance counter0.
16:31	RWX_WCLRREG	PMU5_COUNTER1: PMU5 performance counter1.
32:47	RWX_WCLRREG	PMU5_COUNTER2: PMU5 performance counter2.
48:63	RWX_WCLRREG	PMU5_COUNTER3: PMU5 performance counter3.

Register Name	Power Bus Electrical Link Performance Monitor 6 Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_PMU6
Address	0000000005013421 (SCOM)
Description	Processor bus Electrical Link PerfMon6 Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU6_COUNTER0: PMU6 performance counter0.
16:31	RWX_WCLRREG	PMU6_COUNTER1: PMU6 performance counter1.
32:47	RWX_WCLRREG	PMU6_COUNTER2: PMU6 performance counter2.
48:63	RWX_WCLRREG	PMU6_COUNTER3: PMU6 performance counter3.

Register Name	Power Bus Electrical Link Performance Monitor 7 Register
Mnemonic	PB.IOE.SCOM.PB_ELINK_PMU7
Address	0000000005013422 (SCOM)
Description	Processor bus Electrical Link PerfMon7 Register

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU7_COUNTER0: PMU7 performance counter0.
16:31	RWX_WCLRREG	PMU7_COUNTER1: PMU7 performance counter1.
32:47	RWX_WCLRREG	PMU7_COUNTER2: PMU7 performance counter2.
48:63	RWX_WCLRREG	PMU7_COUNTER3: PMU7 performance counter3.

Register Name	Power Bus Electrical Miscellaneous Configuration Register
Mnemonic	PB.IOE.SCOM.PB_MISC_CFG
Address	0000000005013423 (SCOM)
Description	Processor bus Electrical Miscellaneous configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	PB_CFG_IOE01_IS_LOGICAL_PAIR: pb configuration ioe01 is logical pair.
1	RW	PB_CFG_IOE23_IS_LOGICAL_PAIR: pb configuration ioe23 is logical pair.
2	RW	PB_CFG_IOE45_IS_LOGICAL_PAIR: pb configuration ioe45 is logical pair.
3	RW	MISC_SPARE3: Miscellaneous spare3.
4	WO_1P	SCOM_LINK01_RESET_KEEPER: SCOM link01 reset keeper.
5	WO_1P	SCOM_LINK23_RESET_KEEPER: SCOM link23 reset keeper.
6	WO_1P	SCOM_LINK45_RESET_KEEPER: SCOM link45 reset keeper.
7	RW	MISC_SPARE7: Miscellaneous spare7.
8	RW	MISC_SPARE8: Miscellaneous spare8.
9	RW	MISC_SPARE9: Miscellaneous spare9.
10	RW	MISC_SPARE10: Miscellaneous spare10.
11	RW	MISC_SPARE11: Miscellaneous spare11.
12	RW	PB_LINK_CFG_AVP_MODE: pb link configuration AVP mode.
13	RW	MISC_SPARE13: Miscellaneous spare13.
14	RW	MISC_SPARE14: Miscellaneous spare14.
15	RW	MISC_SPARE15: Miscellaneous spare15.

Register Name	Power Bus Electrical Link Trace Configuration Register
Mnemonic	PB.IOE.SCOM.PB_TRACE_CFG
Address	0000000005013424 (SCOM)
Description	disabled 1 - inbound link 2 - inbnd dhdr position 0 3 - inbnd dhdr position 1 4 - inbnd dhdr position 2 5 - outbound link 6 - outbnd dhdr position 0 7 - outbnd dhdr position 1 8 - outbnd dhdr position 2 9 - dob1 pos 0 A - dob1 pos 1 B - dob2 pos 0 C - dob2 pos 1 D - dib pos 0 E - dib pos 1 F - Reserved

Bits	SCOM	Field Mnemonic: Description
0:3	RW	LINK00_HI_TRACE_CFG: link00 high trace configuration.
4:7	RW	LINK00_LO_TRACE_CFG: link00 low trace configuration.
8:11	RW	LINK01_HI_TRACE_CFG: link01 high trace configuration.
12:15	RW	LINK01_LO_TRACE_CFG: link01 low trace configuration.
16:19	RW	LINK02_HI_TRACE_CFG: link02 high trace configuration.
20:23	RW	LINK02_LO_TRACE_CFG: link02 low trace configuration.
24:27	RW	LINK03_HI_TRACE_CFG: link03 high trace configuration.
28:31	RW	LINK03_LO_TRACE_CFG: link03 low trace configuration.
32:35	RW	LINK04_HI_TRACE_CFG: link04 high trace configuration.
36:39	RW	LINK04_LO_TRACE_CFG: link04 low trace configuration.
40:43	RW	LINK05_HI_TRACE_CFG: link05 high trace configuration.
44:47	RW	LINK05_LO_TRACE_CFG: link05 low trace configuration.

Register Name	**Power Bus Electrical Link Framer0123 Error Readout Register**
Mnemonic	PB.IOE.SCOM.PB_FM0123_ERR
Address	0000000005013425 (SCOM)
Description	Processor bus ELink Framer0123 Error Readout Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13	ROX	Reserved.
14	ROX	Reserved.
15	ROX	Reserved.
16	ROX	Reserved.
17	ROX	Reserved.
18	ROX	Reserved.
19	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
20	ROX	Reserved.
21	ROX	Reserved.
22	ROX	Reserved.
23	ROX	Reserved.
24	ROX	Reserved.
25	ROX	Reserved.
26	ROX	Reserved.
27	ROX	Reserved.
28	ROX	Reserved.
29	ROX	Reserved.
30	ROX	Reserved.
31	ROX	Reserved.
32	ROX	Reserved.
33	ROX	Reserved.
34	ROX	Reserved.
35	ROX	Reserved.
36	ROX	Reserved.
37	ROX	Reserved.
38	ROX	Reserved.
39	ROX	Reserved.
40	ROX	Reserved.
41	ROX	Reserved.
42	ROX	Reserved.
43	ROX	Reserved.
44	ROX	Reserved.
45	ROX	Reserved.
46	ROX	Reserved.
47	ROX	Reserved.
48	ROX	Reserved.
49	ROX	Reserved.
50	ROX	Reserved.
51	ROX	Reserved.
52	ROX	Reserved.
53	ROX	Reserved.
54	ROX	Reserved.
55	ROX	Reserved.
56	ROX	Reserved.
57	ROX	Reserved.
58	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
59	ROX	Reserved.
60	ROX	Reserved.
61	ROX	Reserved.
62	ROX	Reserved.
63	ROX	Reserved.

Register Name	Power Bus Electrical Link Framer45 Error Readout Register
Mnemonic	PB.IOE.SCOM.PB_FM45_ERR
Address	0000000005013426 (SCOM)
Description	Processor bus ELink Framer45 Error Readout Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13	ROX	Reserved.
14	ROX	Reserved.
15	ROX	Reserved.
16	ROX	Reserved.
17	ROX	Reserved.
18	ROX	Reserved.
19	ROX	Reserved.
20	ROX	Reserved.
21	ROX	Reserved.
22	ROX	Reserved.
23	ROX	Reserved.
24	ROX	Reserved.
25	ROX	Reserved.
26	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
27	ROX	Reserved.
28	ROX	Reserved.
29	ROX	Reserved.
30	ROX	Reserved.
31	ROX	Reserved.

Register Name	Power Bus Electrical Link Parser0123 Error Readout Register
Mnemonic	PB.IOE.SCOM.PB_PR0123_ERR
Address	0000000005013427 (SCOM)
Description	Processor bus ELink Parser0123 Error Readout Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13:15	RO	Constant = 0b000
16	ROX	Reserved.
17	ROX	Reserved.
18	ROX	Reserved.
19	ROX	Reserved.
20	ROX	Reserved.
21	ROX	Reserved.
22	ROX	Reserved.
23	ROX	Reserved.
24	ROX	Reserved.
25	ROX	Reserved.
26	ROX	Reserved.
27	ROX	Reserved.
28	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
29:31	RO	Constant = 0b000
32	ROX	Reserved.
33	ROX	Reserved.
34	ROX	Reserved.
35	ROX	Reserved.
36	ROX	Reserved.
37	ROX	Reserved.
38	ROX	Reserved.
39	ROX	Reserved.
40	ROX	Reserved.
41	ROX	Reserved.
42	ROX	Reserved.
43	ROX	Reserved.
44	ROX	Reserved.
45:47	RO	Constant = 0b000
48	ROX	Reserved.
49	ROX	Reserved.
50	ROX	Reserved.
51	ROX	Reserved.
52	ROX	Reserved.
53	ROX	Reserved.
54	ROX	Reserved.
55	ROX	Reserved.
56	ROX	Reserved.
57	ROX	Reserved.
58	ROX	Reserved.
59	ROX	Reserved.
60	ROX	Reserved.
61:63	RO	Constant = 0b000

Register Name	Power Bus Electrical Link Parser45 Error Readout Register
Mnemonic	PB.IOE.SCOM.PB_PR45_ERR
Address	0000000005013428 (SCOM)
Description	Processor bus ELink Parser45 Error Readout Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13:15	RO	Constant = 0b000
16	ROX	Reserved.
17	ROX	Reserved.
18	ROX	Reserved.
19	ROX	Reserved.
20	ROX	Reserved.
21	ROX	Reserved.
22	ROX	Reserved.
23	ROX	Reserved.
24	ROX	Reserved.
25	ROX	Reserved.
26	ROX	Reserved.
27	ROX	Reserved.
28	ROX	Reserved.
29:31	RO	Constant = 0b000

Register Name	Power Bus Electrical Link Performance Trace Configuration Register
Mnemonic	PB.IOE.SCOM.PB_PERFTRACE_CFG_REG
Address	0000000005013429 (SCOM)
Description	Processor bus ELink Perftrace configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	PERFTRACE_HI_ENABLE: perftrace high enable - multiplexer perftrace data onto trace bus 0.
1	RW	PERFTRACE_HI_FIXED_WINDOW_MODE: perftrace high fixed window mode - take a sample every 255 or 255x128 cycles.
2	RW	PERFTRACE_HI_PRESCALE_MODE: perftrace high prescale mode - wide-angle view - perfcounts are prescaled by 128.
3	RW	PTSPARE6: ptspare6.
4	RW	PERFTRACE_LO_ENABLE: perftrace low enable - multiplexer perftrace data onto trace bus 1.

Bits	SCOM	Field Mnemonic: Description
5	RW	PERFTRACE_LO_FIXED_WINDOW_MODE: perftrace low fixed window mode - take a sample every 255 or 255x128 cycles.
6	RW	PERFTRACE_LO_PRESCALE_MODE: perftrace low prescale mode - wide-angle view - perfcounts are prescaled by 128.
7	RW	PTSPARE7: ptspare7.
8:11	RW	PERFTRACE_HI_SELECT: perftrace high select.
12:15	RW	PERFTRACE_LO_SELECT: perftrace low select.

Register Name	Power Bus Electrical Link Mailbox Control Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_CTL_REG
Address	000000000501342E (SCOM)
Description	Processor bus Electrical Link Mailbox Control Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	MB_VALID: written to 1 to start operation, reads 1 if in progress, 0 when done.
1	RW	MB_WR_NOT_RD: Written to 1 for a write operation, 0 for a read. To do a write, first write the PBE_MAILBOX_DATA_REG, when write this reg with a write command, and the mailbox_id and link_id bits set for your desired destination. When the data reaches the other chip, that chip will fire a SP_ATTN, and the appropriate bit 36:47 of PB_ELINK_fir_reg will get set on that chip. To do a read, write this reg with a read command, and the mailbox_id and link_id bits set for your desired destination. Monitor this reg to see when complete, then read the PBE_MAILBOX_DATA_REG to extract the resulting data. When you do a read, you only have access to the two regs on the other chip that are assigned to the physical link that connects the two chips. (In other words, remote reads aren't nearly as effective a tool as remote writes.
2	RWX_WCLRPART	MB_BAD_ADDR: (read-only) set if last operation was invalid (bad address).
3	RWX_WCLRPART	MB_LINK_DOWN: (read-only) set if link goes down during the op.
4	RWX_WCLRPART	MB_CORRUPT: (read-only) set if last operation corrupted (return response address mismatch).
5	RWX_WCLRPART	MB_SENT: (read-only) set when operation is sent to framer.
6	RWX_WCLRPART	MB_BAD_WRITE: (read-only) set on write to this register when already active.
7	WO_1P	MB_RESET: Write to a 1 to reset hung mailbox logic caused by a link going down. Auto reset to 0.
8	RW	MAILBOX_ID: 0/1 - there are two mailboxes per link.
9:11	RW	MB_LINK_ID: 0-5 - each half of a 32-lane electrical link is independently accessible.
12:15	RW	MB_SPARE: mb spare.

Register Name	Power Bus Electrical Link Mailbox Data Movement Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_DATA_REG
Address	000000000501342F (SCOM)
Description	This is the data source for a write of a remote mailbox write, or the holding reg for remote mailbox read return dataprocessor bus Electrical Link Mailbox Data Movement Register. This is the data source for a write of a remote mailbox write, or the holding reg for remote mailbox read return data.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 00 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_00_REG
Address	0000000005013430 (SCOM)
Description	Processor bus Electrical Link Mailbox 00 Register (X0_evn_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 01 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_01_REG
Address	0000000005013431 (SCOM)
Description	Processor bus Electrical Link Mailbox 01 Register (X0_evn_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 10 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_10_REG
Address	0000000005013432 (SCOM)
Description	Processor bus Electrical Link Mailbox 10 Register (X0_odd_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 11 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_11_REG
Address	0000000005013433 (SCOM)
Description	Processor bus Electrical Link Mailbox 11 Register (X0_odd_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 20 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_20_REG
Address	0000000005013434 (SCOM)
Description	Processor bus Electrical Link Mailbox 20 Register (X1_evn_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 21 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_21_REG
Address	0000000005013435 (SCOM)
Description	Processor bus Electrical Link Mailbox 21 Register (X1_evn_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 30 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_30_REG
Address	0000000005013436 (SCOM)
Description	Processor bus Electrical Link Mailbox 30 Register (X1_odd_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 31 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_31_REG
Address	0000000005013437 (SCOM)
Description	Processor bus Electrical Link Mailbox 31 Register (X1_odd_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 40 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_40_REG
Address	0000000005013438 (SCOM)
Description	Processor bus Electrical Link Mailbox 40 Register (X2_evn_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 41 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_41_REG
Address	0000000005013439 (SCOM)
Description	Processor bus Electrical Link Mailbox 41 Register (X2_evn_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 50 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_50_REG
Address	000000000501343A (SCOM)
Description	Processor bus Electrical Link Mailbox 50 Register (X2_odd_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Electrical Link Mailbox 51 Register
Mnemonic	PB.IOE.SCOM.PBE_MAILBOX_51_REG
Address	000000000501343B (SCOM)
Description	Processor bus Electrical Link Mailbox 51 Register (X2_odd_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus PBES IOO FIR0 Register
Mnemonic	PB.IOO.SCOM.PB_IOO_FIR_REG
Address	0000000005013800 (SCOM) 0000000005013801 (SCOM1) 0000000005013802 (SCOM2)
Description	Processor bus PBES IOO domain FIR0 register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FMR00_TRAINED: fmr00 trained.
1	RWX	WOX_AND	WOX_OR	FMR01_TRAINED: fmr01 trained.
2	RWX	WOX_AND	WOX_OR	FMR02_TRAINED: fmr02 trained.
3	RWX	WOX_AND	WOX_OR	FMR03_TRAINED: fmr03 trained.
4	RWX	WOX_AND	WOX_OR	FMR04_TRAINED: fmr04 trained.
5	RWX	WOX_AND	WOX_OR	FMR05_TRAINED: fmr05 trained.
6	RWX	WOX_AND	WOX_OR	FMR06_TRAINED: fmr06 trained.
7	RWX	WOX_AND	WOX_OR	FMR07_TRAINED: fmr07 trained.
8	RWX	WOX_AND	WOX_OR	DOB01_UE: dob01 ue.
9	RWX	WOX_AND	WOX_OR	DOB01_CE: dob01 ce.
10	RWX	WOX_AND	WOX_OR	DOB01_SUE: dob01 sue.
11	RWX	WOX_AND	WOX_OR	DOB23_UE: dob23 ue.
12	RWX	WOX_AND	WOX_OR	DOB23_CE: dob23 ce.
13	RWX	WOX_AND	WOX_OR	DOB23_SUE: dob23 sue.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
14	RWX	WOX_AND	WOX_OR	DOB45_UE: dob45 ue.
15	RWX	WOX_AND	WOX_OR	DOB45_CE: dob45 ce.
16	RWX	WOX_AND	WOX_OR	DOB45_SUE: dob45 sue.
17	RWX	WOX_AND	WOX_OR	DOB67_UE: dob67 ue.
18	RWX	WOX_AND	WOX_OR	DOB67_CE: dob67 ce.
19	RWX	WOX_AND	WOX_OR	DOB67_SUE: dob67 sue.
20	RWX	WOX_AND	WOX_OR	FRAMER00_ATTN: framer00 attn - A0 even link framer internal error, or outbound switch cmd/presp/cresp internal error.
21	RWX	WOX_AND	WOX_OR	FRAMER01_ATTN: framer01 attn - A0 odd link framer internal error.
22	RWX	WOX_AND	WOX_OR	FRAMER02_ATTN: framer02 attn - A1 even link framer internal error, or outbound switch cmd/presp/cresp internal error.
23	RWX	WOX_AND	WOX_OR	FRAMER03_ATTN: framer03 attn - A1 odd link framer internal error.
24	RWX	WOX_AND	WOX_OR	FRAMER04_ATTN: framer04 attn - A2 even link framer internal error, or outbound switch cmd/presp/cresp internal error.
25	RWX	WOX_AND	WOX_OR	FRAMER05_ATTN: framer05 attn - A2 odd link framer internal error.
26	RWX	WOX_AND	WOX_OR	FRAMER06_ATTN: framer06 attn - A3 even link framer internal error, or outbound switch cmd/presp/cresp internal error.
27	RWX	WOX_AND	WOX_OR	FRAMER07_ATTN: framer07 attn - A3 odd link framer internal error.
28	RWX	WOX_AND	WOX_OR	PARSER00_ATTN: parser00 attn.
29	RWX	WOX_AND	WOX_OR	PARSER01_ATTN: parser01 attn.
30	RWX	WOX_AND	WOX_OR	PARSER02_ATTN: parser02 attn.
31	RWX	WOX_AND	WOX_OR	PARSER03_ATTN: parser03 attn.
32	RWX	WOX_AND	WOX_OR	PARSER04_ATTN: parser04 attn.
33	RWX	WOX_AND	WOX_OR	PARSER05_ATTN: parser05 attn.
34	RWX	WOX_AND	WOX_OR	PARSER06_ATTN: parser06 attn.
35	RWX	WOX_AND	WOX_OR	PARSER07_ATTN: parser07 attn.
36	RWX	WOX_AND	WOX_OR	MB00_SPATTN: mailbox 00 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
37	RWX	WOX_AND	WOX_OR	MB01_SPATTN: mailbox 01 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
38	RWX	WOX_AND	WOX_OR	MB10_SPATTN: mailbox 10 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
39	RWX	WOX_AND	WOX_OR	MB11_SPATTN: mailbox 11 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
40	RWX	WOX_AND	WOX_OR	MB20_SPATTN: mailbox 20 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
41	RWX	WOX_AND	WOX_OR	MB21_SPATTN: mailbox 21 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
42	RWX	WOX_AND	WOX_OR	MB30_SPATTN: mailbox 30 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
43	RWX	WOX_AND	WOX_OR	MB31_SPATTN: mailbox 31 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
44	RWX	WOX_AND	WOX_OR	MB40_SPATTN: mailbox 40 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
45	RWX	WOX_AND	WOX_OR	MB41_SPATTN: mailbox 41 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
46	RWX	WOX_AND	WOX_OR	MB50_SPATTN: mailbox 50 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
47	RWX	WOX_AND	WOX_OR	MB51_SPATTN: mailbox 51 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
48	RWX	WOX_AND	WOX_OR	MB60_SPATTN: mailbox 60 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
49	RWX	WOX_AND	WOX_OR	MB61_SPATTN: mailbox 61 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
50	RWX	WOX_AND	WOX_OR	MB70_SPATTN: mailbox 70 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
51	RWX	WOX_AND	WOX_OR	MB71_SPATTN: mailbox 71 special attention. Gets set to 1 when a remote chip writes the corresponding mailbox register on this chip.
52	RWX	WOX_AND	WOX_OR	DOB01_ERR: data outbound switch internal error - links 01.
53	RWX	WOX_AND	WOX_OR	DOB23_ERR: data outbound switch internal error - links 23.
54	RWX	WOX_AND	WOX_OR	DOB45_ERR: data outbound switch internal error - links 45.
55	RWX	WOX_AND	WOX_OR	DOB67_ERR: data outbound switch internal error - links 67.
56	RWX	WOX_AND	WOX_OR	DIB01_ERR: data inbound switch internal error - links 01.
57	RWX	WOX_AND	WOX_OR	DIB23_ERR: data inbound switch internal error - links 23.
58	RWX	WOX_AND	WOX_OR	DIB45_ERR: data inbound switch internal error - links 45.
59	RWX	WOX_AND	WOX_OR	DIB67_ERR: data inbound switch internal error - links 67.
60:61	RWX	WOX_AND	WOX_OR	Reserved.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP: FIR SCOM err dup.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR: FIR SCOM err.

Register Name	Power Bus PBES IOO FIR0 Mask Register
Mnemonic	PB.IOO.SCOM.PB_IOO_FIR_MASK_REG
Address	0000000005013803 (SCOM) 0000000005013804 (SCOM1) 0000000005013805 (SCOM2)
Description	Processor bus PBES IOO domain FIR0 Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FMR00_TRAINED_MASK: fmr00 trained mask.
1	RWX	WOX_AND	WOX_OR	FMR01_TRAINED_MASK: fmr01 trained mask.
2	RWX	WOX_AND	WOX_OR	FMR02_TRAINED_MASK: fmr02 trained mask.
3	RWX	WOX_AND	WOX_OR	FMR03_TRAINED_MASK: fmr03 trained mask.
4	RWX	WOX_AND	WOX_OR	FMR04_TRAINED_MASK: fmr04 trained mask.
5	RWX	WOX_AND	WOX_OR	FMR05_TRAINED_MASK: fmr05 trained mask.
6	RWX	WOX_AND	WOX_OR	FMR06_TRAINED_MASK: fmr06 trained mask.
7	RWX	WOX_AND	WOX_OR	FMR07_TRAINED_MASK: fmr07 trained mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RWX	WOX_AND	WOX_OR	DOB01_UE_MASK: dob01 ue mask.
9	RWX	WOX_AND	WOX_OR	DOB01_CE_MASK: dob01 ce mask.
10	RWX	WOX_AND	WOX_OR	DOB01_SUE_MASK: dob01 sue mask.
11	RWX	WOX_AND	WOX_OR	DOB23_UE_MASK: dob23 ue mask.
12	RWX	WOX_AND	WOX_OR	DOB23_CE_MASK: dob23 ce mask.
13	RWX	WOX_AND	WOX_OR	DOB23_SUE_MASK: dob23 sue mask.
14	RWX	WOX_AND	WOX_OR	DOB45_UE_MASK: dob45 ue mask.
15	RWX	WOX_AND	WOX_OR	DOB45_CE_MASK: dob45 ce mask.
16	RWX	WOX_AND	WOX_OR	DOB45_SUE_MASK: dob45 sue mask.
17	RWX	WOX_AND	WOX_OR	DOB67_UE_MASK: dob67 ue mask.
18	RWX	WOX_AND	WOX_OR	DOB67_CE_MASK: dob67 ce mask.
19	RWX	WOX_AND	WOX_OR	DOB67_SUE_MASK: dob67 sue mask.
20	RWX	WOX_AND	WOX_OR	FRAMER00_ATTN_MASK: framer00 attn mask.
21	RWX	WOX_AND	WOX_OR	FRAMER01_ATTN_MASK: framer01 attn mask.
22	RWX	WOX_AND	WOX_OR	FRAMER02_ATTN_MASK: framer02 attn mask.
23	RWX	WOX_AND	WOX_OR	FRAMER03_ATTN_MASK: framer03 attn mask.
24	RWX	WOX_AND	WOX_OR	FRAMER04_ATTN_MASK: framer04 attn mask.
25	RWX	WOX_AND	WOX_OR	FRAMER05_ATTN_MASK: framer05 attn mask.
26	RWX	WOX_AND	WOX_OR	FRAMER06_ATTN_MASK: framer06 attn mask.
27	RWX	WOX_AND	WOX_OR	FRAMER07_ATTN_MASK: framer07 attn mask.
28	RWX	WOX_AND	WOX_OR	PARSER00_ATTN_MASK: parser00 attn mask.
29	RWX	WOX_AND	WOX_OR	PARSER01_ATTN_MASK: parser01 attn mask.
30	RWX	WOX_AND	WOX_OR	PARSER02_ATTN_MASK: parser02 attn mask.
31	RWX	WOX_AND	WOX_OR	PARSER03_ATTN_MASK: parser03 attn mask.
32	RWX	WOX_AND	WOX_OR	PARSER04_ATTN_MASK: parser04 attn mask.
33	RWX	WOX_AND	WOX_OR	PARSER05_ATTN_MASK: parser05 attn mask.
34	RWX	WOX_AND	WOX_OR	PARSER06_ATTN_MASK: parser06 attn mask.
35	RWX	WOX_AND	WOX_OR	PARSER07_ATTN_MASK: parser07 attn mask.
36	RWX	WOX_AND	WOX_OR	MB00_SPATTN_MASK: mailbox 00 special attention mask.
37	RWX	WOX_AND	WOX_OR	MB01_SPATTN_MASK: mailbox 01 special attention mask.
38	RWX	WOX_AND	WOX_OR	MB10_SPATTN_MASK: mailbox 10 special attention mask.
39	RWX	WOX_AND	WOX_OR	MB11_SPATTN_MASK: mailbox 11 special attention mask.
40	RWX	WOX_AND	WOX_OR	MB20_SPATTN_MASK: mailbox 20 special attention mask.
41	RWX	WOX_AND	WOX_OR	MB21_SPATTN_MASK: mailbox 21 special attention mask.
42	RWX	WOX_AND	WOX_OR	MB30_SPATTN_MASK: mailbox 30 special attention mask.
43	RWX	WOX_AND	WOX_OR	MB31_SPATTN_MASK: mailbox 31 special attention mask.
44	RWX	WOX_AND	WOX_OR	MB40_SPATTN_MASK: mailbox 40 special attention mask.
45	RWX	WOX_AND	WOX_OR	MB41_SPATTN_MASK: mailbox 41 special attention mask.
46	RWX	WOX_AND	WOX_OR	MB50_SPATTN_MASK: mailbox 50 special attention mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
47	RWX	WOX_AND	WOX_OR	MB51_SPATTN_MASK: mailbox 51 special attention mask.
48	RWX	WOX_AND	WOX_OR	MB60_SPATTN_MASK: mailbox 60 special attention mask.
49	RWX	WOX_AND	WOX_OR	MB61_SPATTN_MASK: mailbox 61 special attention mask.
50	RWX	WOX_AND	WOX_OR	MB70_SPATTN_MASK: mailbox 70 special attention mask.
51	RWX	WOX_AND	WOX_OR	MB71_SPATTN_MASK: mailbox 71 special attention mask.
52	RWX	WOX_AND	WOX_OR	DOB01_ERR_MASK: data outbound switch internal error mask - links 01.
53	RWX	WOX_AND	WOX_OR	DOB23_ERR_MASK: data outbound switch internal error mask - links 23.
54	RWX	WOX_AND	WOX_OR	DOB45_ERR_MASK: data outbound switch internal error mask - links 45.
55	RWX	WOX_AND	WOX_OR	DOB67_ERR_MASK: data outbound switch internal error mask - links 67.
56	RWX	WOX_AND	WOX_OR	DIB01_ERR_MASK: data inbound switch internal error mask - links 01.
57	RWX	WOX_AND	WOX_OR	DIB23_ERR_MASK: data inbound switch internal error mask - links 23.
58	RWX	WOX_AND	WOX_OR	DIB45_ERR_MASK: data inbound switch internal error mask - links 45.
59	RWX	WOX_AND	WOX_OR	DIB67_ERR_MASK: data inbound switch internal error mask - links 67.
60:61	RWX	WOX_AND	WOX_OR	Reserved.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_MASK_DUP: FIR SCOM err mask dup.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_MASK: FIR SCOM err mask.

Register Name	**Power Bus PBES IOE FIR Action 0 Register**
Mnemonic	PB.IOO.SCOM.PB_IOO_FIR_ACTION0_REG
Address	0000000005013806 (SCOM)
Description	Processor bus PBES IOE domain FIR Action 0 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PB_IOO_FIR_ACTION0: Processor bus PBES IOE domain action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Special Attention to Service Processor. (1,1) = Invalid.

Register Name	**Power Bus PBES IOE domain FIR Action 1 Register**
Mnemonic	PB.IOO.SCOM.PB_IOO_FIR_ACTION1_REG
Address	0000000005013807 (SCOM)
Description	Processor bus PBES IOE domain FIR Action 1 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PB_IOO_FIR_ACTION1: Processor bus FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable Error to Service Processor. (1,0) = Special Attention to Service Processor. (1,1) = Invalid.

Register Name	Power Bus Optical Framer/Parser 01 Configuration Register
Mnemonic	PB.IOO.SCOM.PB_FP01_CFG
Address	000000000501380A (SCOM)
Description	Processor bus Optical Framer/Parser 01 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	FP0_CREDIT_PRIORITY_4_NOT_8: fp0 credit priority 4 not 8.
1	RW	FP0_DISABLE_GATHERING: fp0 disable data gathering.
2	RW	FP0_DISABLE_CMD_COMPRESSION: fp0 disable command compression.
3	RW	FP0_DISABLE_PRSP_COMPRESSION: fp0 disable prsp compression.
4:11	RW	FP0_LL_CREDIT_LO_LIMIT: fp0 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(((nest_freq/olink_freq) * -15.8)+54).
12:19	RW	FP0_LL_CREDIT_HI_LIMIT: fp0 ll credit high limit - frames in flight limit during stop_cmds/replay.
20	RW	FP0_FMR_DISABLE: fp0 framer disable - turn the framer clocks OFF.
21	RW	FP0_FMR_SPARE: fp0 framer spare.
22:23	RW	FP01_CMD_EXP_TIME: obs/fmr/prs command expiration time = (value * 2) + 9.
24	RW	FP0_RUN_AFTER_FRAME_ERROR: fp0 run after frame error.
25	RW	FP0_PRS_DISABLE: fp0 parser disable - turn the parser clocks OFF.
26:31	RW	FP0_PRS_SPARE: fp0 parser spare.
32	RW	FP1_CREDIT_PRIORITY_4_NOT_8: fp1 credit priority 4 not 8.
33	RW	FP1_DISABLE_GATHERING: fp1 disable data gathering.
34	RW	FP1_DISABLE_CMD_COMPRESSION: fp1 disable command compression.
35	RW	FP1_DISABLE_PRSP_COMPRESSION: fp1 disable prsp compression.
36:43	RW	FP1_LL_CREDIT_LO_LIMIT: fp1 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(((nest_freq/olink_freq) * -15.8)+54).
44:51	RW	FP1_LL_CREDIT_HI_LIMIT: fp1 ll credit high limit - frames in flight limit during stop_cmds/replay.
52	RW	FP1_FMR_DISABLE: fp1 framer disable - turn the framer clocks OFF.
53:55	RW	FP1_FMR_SPARE: fp1 framer spare.
56	RW	FP1_RUN_AFTER_FRAME_ERROR: fp1 run after frame error.
57	RW	FP1_PRS_DISABLE: fp1 parser disable - turn the parser clocks OFF.
58:63	RW	FP1_PRS_SPARE: fp1 parser spare.

Register Name	Power Bus Optical Framer/Parser 23 Configuration Register
Mnemonic	PB.IOO.SCOM.PB_FP23_CFG
Address	000000000501380B (SCOM)
Description	Processor bus Optical Framer/Parser 23 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	FP2_CREDIT_PRIORITY_4_NOT_8: fp2 credit priority 4 not 8.
1	RW	FP2_DISABLE_GATHERING: fp2 disable data gathering.
2	RW	FP2_DISABLE_CMD_COMPRESSION: fp2 disable command compression.

Bits	SCOM	Field Mnemonic: Description
3	RW	FP2_DISABLE_PRSP_COMPRESSION: fp2 disable prsp compression.
4:11	RW	FP2_LL_CREDIT_LO_LIMIT: fp2 ll credit low limit - normal frames in flight limit.
12:19	RW	FP2_LL_CREDIT_HI_LIMIT: fp2 ll credit high limit - frames in flight limit during stop_cmds/replay.
20	RW	FP2_FMR_DISABLE: fp2 framer disable - turn the framer clocks OFF.
21	RW	FP2_FMR_SPARE: fp0 framer spare.
22:23	RW	FP23_CMD_EXP_TIME: obs/fmr/prs command expiration time = (value * 2) + 9.
24	RW	FP2_RUN_AFTER_FRAME_ERROR: fp2 run after frame error.
25	RW	FP2_PRS_DISABLE: fp2 parser disable - turn the parser clocks OFF.
26:31	RW	FP2_PRS_SPARE: fp2 parser spare.
32	RW	FP3_CREDIT_PRIORITY_4_NOT_8: fp3 credit priority 4 not 8.
33	RW	FP3_DISABLE_GATHERING: fp3 disable data gathering.
34	RW	FP3_DISABLE_CMD_COMPRESSION: fp3 disable command compression.
35	RW	FP3_DISABLE_PRSP_COMPRESSION: fp3 disable prsp compression.
36:43	RW	FP3_LL_CREDIT_LO_LIMIT: fp3 ll credit low limit - normal frames in flight limit.
44:51	RW	FP3_LL_CREDIT_HI_LIMIT: fp3 ll credit high limit - frames in flight limit during stop_cmds/replay.
52	RW	FP3_FMR_DISABLE: fp3 framer disable - turn the framer clocks OFF.
53:55	RW	FP3_FMR_SPARE: fp3 framer spare.
56	RW	FP3_RUN_AFTER_FRAME_ERROR: fp3 run after frame error.
57	RW	FP3_PRS_DISABLE: fp3 parser disable - turn the parser clocks OFF.
58:63	RW	FP3_PRS_SPARE: fp3 parser spare.

Register Name	Power Bus Optical Framer/Parser 45 Configuration Register
Mnemonic	PB.IOO.SCOM.PB_FP45_CFG
Address	000000000501380C (SCOM)
Description	Processor bus Optical Framer/Parser 45 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	FP4_CREDIT_PRIORITY_4_NOT_8: fp4 credit priority 4 not 8.
1	RW	FP4_DISABLE_GATHERING: fp4 disable data gathering.
2	RW	FP4_DISABLE_CMD_COMPRESSION: fp4 disable command compression.
3	RW	FP4_DISABLE_PRSP_COMPRESSION: fp4 disable prsp compression.
4:11	RW	FP4_LL_CREDIT_LO_LIMIT: fp4 ll credit low limit - normal frames in flight limit.
12:19	RW	FP4_LL_CREDIT_HI_LIMIT: fp4 ll credit high limit - frames in flight limit during stop_cmds/replay.
20	RW	FP4_FMR_DISABLE: fp4 framer disable - turn the framer clocks OFF.
21	RW	FP4_FMR_SPARE: fp0 framer spare.
22:23	RW	FP45_CMD_EXP_TIME: obs/fmr/prs command expiration time = (value * 2) + 9.
24	RW	FP4_RUN_AFTER_FRAME_ERROR: fp4 run after frame error.
25	RW	FP4_PRS_DISABLE: fp4 parser disable - turn the parser clocks OFF.
26:31	RW	FP4_PRS_SPARE: fp4 parser spare.

Bits	SCOM	Field Mnemonic: Description
32	RW	FP5_CREDIT_PRIORITY_4_NOT_8: fp5 credit priority 4 not 8.
33	RW	FP5_DISABLE_GATHERING: fp5 disable data gathering.
34	RW	FP5_DISABLE_CMD_COMPRESSION: fp5 disable command compression.
35	RW	FP5_DISABLE_PRSP_COMPRESSION: fp5 disable prsp compression.
36:43	RW	FP5_LL_CREDIT_LO_LIMIT: fp5 ll credit low limit - normal frames in flight limit.
44:51	RW	FP5_LL_CREDIT_HI_LIMIT: fp5 ll credit high limit - frames in flight limit during stop_cmds/replay.
52	RW	FP5_FMR_DISABLE: fp5 framer disable - turn the framer clocks OFF.
53:55	RW	FP5_FMR_SPARE: fp5 framer spare.
56	RW	FP5_RUN_AFTER_FRAME_ERROR: fp5 run after frame error.
57	RW	FP5_PRS_DISABLE: fp5 parser disable - turn the parser clocks OFF.
58:63	RW	FP5_PRS_SPARE: fp5 parser spare.

Register Name	Power Bus Optical Framer/Parser 67 Configuration Register
Mnemonic	PB.IOO.SCOM.PB_FP67_CFG
Address	000000000501380D (SCOM)
Description	Processor bus Optical Framer/Parser 67 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	FP6_CREDIT_PRIORITY_4_NOT_8: fp6 credit priority 4 not 8.
1	RW	FP6_DISABLE_GATHERING: fp6 disable data gathering.
2	RW	FP6_DISABLE_CMD_COMPRESSION: fp6 disable command compression.
3	RW	FP6_DISABLE_PRSP_COMPRESSION: fp6 disable prsp compression.
4:11	RW	FP6_LL_CREDIT_LO_LIMIT: fp6 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(((nest_freq/olink_freq) * -10.17)+36).
12:19	RW	FP6_LL_CREDIT_HI_LIMIT: fp6 ll credit high limit - frames in flight limit during stop_cmds/replay.
20	RW	FP6_FMR_DISABLE: fp6 framer disable - turn the framer clocks OFF.
21	RW	FP6_FMR_SPARE: fp0 framer spare.
22:23	RW	FP67_CMD_EXP_TIME: obs/fmr/prs command expiration time = (value * 2) + 9.
24	RW	FP6_RUN_AFTER_FRAME_ERROR: fp6 run after frame error.
25	RW	FP6_PRS_DISABLE: fp6 parser disable - turn the parser clocks OFF.
26:31	RW	FP6_PRS_SPARE: fp6 parser spare.
32	RW	FP7_CREDIT_PRIORITY_4_NOT_8: fp7 credit priority 4 not 8.
33	RW	FP7_DISABLE_GATHERING: fp7 disable data gathering.
34	RW	FP7_DISABLE_CMD_COMPRESSION: fp7 disable command compression.
35	RW	FP7_DISABLE_PRSP_COMPRESSION: fp7 disable prsp compression.
36:43	RW	FP7_LL_CREDIT_LO_LIMIT: fp7 ll credit low limit - normal frames in flight limit. Set to ROUNDUP(((nest_freq/olink_freq) * -10.17)+36).
44:51	RW	FP7_LL_CREDIT_HI_LIMIT: fp7 ll credit high limit - frames in flight limit during stop_cmds/replay.
52	RW	FP7_FMR_DISABLE: fp7 framer disable - turn the framer clocks OFF.
53:55	RW	FP7_FMR_SPARE: fp7 framer spare.

Bits	SCOM	Field Mnemonic: Description
56	RW	FP7_RUN_AFTER_FRAME_ERROR: fp7 run after frame error.
57	RW	FP7_PRS_DISABLE: fp7 parser disable - turn the parser clocks OFF.
58:63	RW	FP7_PRS_SPARE: fp7 parser spare.

Register Name	**Power Bus Optical Link Delay 0123 Register**
Mnemonic	PB.IOO.SCOM.PB_OLINK_DLY_0123_REG
Address	000000000501380E (SCOM)
Description	Processor bus Optical Link Delay 0123 Register

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b0000
4:15	ROX	Reserved.
16:19	RO	Constant = 0b0000
20:31	ROX	Reserved.
32:35	RO	Constant = 0b0000
36:47	ROX	Reserved.
48:51	RO	Constant = 0b0000
52:63	ROX	Reserved.

Register Name	**Power Bus Optical Link Delay 4567 Register**
Mnemonic	PB.IOO.SCOM.PB_OLINK_DLY_4567_REG
Address	000000000501380F (SCOM)
Description	Processor bus Optical Link Delay 4567 Register

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b0000
4:15	ROX	Reserved.
16:19	RO	Constant = 0b0000
20:31	ROX	Reserved.
32:35	RO	Constant = 0b0000
36:47	ROX	Reserved.
48:51	RO	Constant = 0b0000
52:63	ROX	Reserved.

Register Name	**Power Bus Optical Link Data Buffer 01 Configuration Register**
Mnemonic	PB.IOO.SCOM.PB_OLINK_DATA_01_CFG_REG
Address	0000000005013810 (SCOM)
Description	Processor bus Optical Link Data Buffer 01 configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	PB_CFG_LINK01_CAPP_MODE: Processor bus configuration link01 capp mode.
1	RW	PB_CFG_LINK01_HRB_INIT_STATE: Processor bus configuration link01 hrb init state.
2:7	RW	PB_CFG_LINK0_SPARE: Processor bus configuration link0 spare.
8:15	RW	PB_CFG_LINK0_DOB_VC0_LIMIT: pb configuration link0 dob vc0 limit - vc0 link credits, 128 max.
16:23	RW	PB_CFG_LINK0_DOB_VC1_LIMIT: pb configuration link0 dob vc1 limit - vc1 link credits, 128 max.
24:28	RW	PB_CFG_LINK01_DIB_VC_LIMIT: pb configuration link01 dib vc limit - limit per VC for data inbound to trunk (set to 31/16 for 1/2 channels in use) (both links use same credit pool).
29:31	RW	PB_CFG_DIB01_SPARE: pb configuration dib01 spare.
32:39	RW	PB_CFG_LINK1_SPARE: pb configuration link1 spare.
40:47	RW	PB_CFG_LINK1_DOB_VC0_LIMIT: pb configuration link1 dob vc0 limit - vc0 link credits, 128 max.
48:55	RW	PB_CFG_LINK1_DOB_VC1_LIMIT: pb configuration link1 dob vc1 limit - vc1 link credits, 128 max.

Register Name	Power Bus Optical Link Data Buffer 23 Configuration Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_DATA_23_CFG_REG
Address	0000000005013811 (SCOM)
Description	Processor Bus Optical Link Data Buffer 23 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.
1:7	RW	PB_CFG_LINK2_DOB_LIMIT: Processor bus configuration link2 dob limit - total link credits avail.
8	RW	Reserved.
9:15	RW	PB_CFG_LINK2_DOB_VC0_LIMIT: Processor bus configuration link2 dob vc0 limit - vc0 link credits max.
16	RW	Reserved.
17:23	RW	PB_CFG_LINK2_DOB_VC1_LIMIT: Processor bus configuration link2 dob vc1 limit - vc1 link credits max.
24:28	RW	PB_CFG_LINK23_DIB_VC_LIMIT: Processor bus configuration link23 dib vc limit - limit per VC for data inbound to trunk (set to 31/16 for 1/2 channels in use) (both links use same credit pool).
29:32	RW	Reserved.
33:39	RW	PB_CFG_LINK3_DOB_LIMIT: Processor bus configuration link3 dob limit - total link credits avail.
40	RW	Reserved.
41:47	RW	PB_CFG_LINK3_DOB_VC0_LIMIT: Processor bus configuration link3 dob vc0 limit - vc0 link credits max.
48	RW	Reserved.
49:55	RW	PB_CFG_LINK3_DOB_VC1_LIMIT: Processor bus configuration link3 dob vc1 limit - vc1 link credits max.

Register Name	Power Bus Optical Link Data Buffer 45 Configuration Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_DATA_45_CFG_REG
Address	0000000005013812 (SCOM)
Description	Processor bus Optical Link Data Buffer 45 Configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
1:7	RW	PB_CFG_LINK4_DOB_LIMIT: Processor bus configuration link4 dob limit - total link credits avail.
8	RW	Reserved.
9:15	RW	PB_CFG_LINK4_DOB_VC0_LIMIT: Processor bus configuration link4 dob vc0 limit - vc0 link credits max.
16	RW	Reserved.
17:23	RW	PB_CFG_LINK4_DOB_VC1_LIMIT: Processor bus configuration link4 dob vc1 limit - vc1 link credits max.
24:28	RW	PB_CFG_LINK45_DIB_VC_LIMIT: Processor bus configuration link45 dib vc limit - limit per VC for data inbound to trunk (set to 31/16 for 1/2 channels in use) (both links use same credit pool).
29:32	RW	Reserved.
33:39	RW	PB_CFG_LINK5_DOB_LIMIT: Processor bus configuration link5 dob limit - total link credits avail.
40	RW	Reserved.
41:47	RW	PB_CFG_LINK5_DOB_VC0_LIMIT: Processor bus configuration link5 dob vc0 limit - vc0 link credits max.
48	RW	Reserved.
49:55	RW	PB_CFG_LINK5_DOB_VC1_LIMIT: Processor bus configuration link5 dob vc1 limit - vc1 link credits max.

Register Name	**Power Bus Optical Link Data Buffer 67 Configuration Register**
Mnemonic	PB.IOO.SCOM.PB_OLINK_DATA_67_CFG_REG
Address	0000000005013813 (SCOM)
Description	Processor bus Optical Link Data Buffer 67 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	PB_CFG_LINK67_CAPP_MODE: pb configuration link67 capp mode.
1	RW	PB_CFG_LINK67_HRB_INIT_STATE: Links 6/7 CAPP Hold Read Buffer initial state: 0 = Release 1 = Hold.
2:7	RW	PB_CFG_LINK6_SPARE: pb configuration link6 spare.
8:15	RW	PB_CFG_LINK6_DOB_VC0_LIMIT: Processor bus configuration link6 dob vc0 limit - vc0 link credits, 128 max.
16:23	RW	PB_CFG_LINK6_DOB_VC1_LIMIT: Processor bus configuration link6 dob vc1 limit - vc1 link credits, 128 max.
24:28	RW	PB_CFG_LINK67_DIB_VC_LIMIT: Processor bus configuration link67 dib vc limit - limit per VC for data inbound to trunk (set to 31/16 for 1/2 channels in use) (both links use same credit pool).
29:31	RW	PB_CFG_DIB67_SPARE: Processor bus configuration dib67 spare.
32:39	RW	PB_CFG_LINK7_SPARE: Processor bus configuration link7 spare.
40:47	RW	PB_CFG_LINK7_DOB_VC0_LIMIT: Processor bus configuration link7 dob vc0 limit - vc0 link credits, 128 max.
48:55	RW	PB_CFG_LINK7_DOB_VC1_LIMIT: Processor bus configuration link7 dob vc1 limit - vc1 link credits, 128 max.

Register Name	Power Bus Optical Link 01 Syndrome Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_SYN_01_REG
Address	0000000005013814 (SCOM)
Description	Processor bus Optical Link 01 Syndrome Register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved.
8:15	ROX	Reserved.
16:23	ROX	Reserved.
24:31	ROX	Reserved.
32:39	ROX	Reserved.
40:47	ROX	Reserved.
48:55	ROX	Reserved.
56:63	ROX	Reserved.

Register Name	Power Bus Optical Link 23 Syndrome Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_SYN_23_REG
Address	0000000005013815 (SCOM)
Description	Processor bus Optical Link 23 Syndrome Register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved.
8:15	ROX	Reserved.
16:23	ROX	Reserved.
24:31	ROX	Reserved.
32:39	ROX	Reserved.
40:47	ROX	Reserved.
48:55	ROX	Reserved.
56:63	ROX	Reserved.

Register Name	Power Bus Optical Link 45 Syndrome Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_SYN_45_REG
Address	0000000005013816 (SCOM)
Description	Processor bus Optical Link 45 Syndrome Register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved.
8:15	ROX	Reserved.
16:23	ROX	Reserved.
24:31	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
32:39	ROX	Reserved.
40:47	ROX	Reserved.
48:55	ROX	Reserved.
56:63	ROX	Reserved.

Register Name	**Power Bus Optical Link 67 Syndrome Register**
Mnemonic	PB.IOO.SCOM.PB_OLINK_SYN_67_REG
Address	0000000005013817 (SCOM)
Description	Processor bus Optical Link 67 Syndrome Register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved.
8:15	ROX	Reserved.
16:23	ROX	Reserved.
24:31	ROX	Reserved.
32:39	ROX	Reserved.
40:47	ROX	Reserved.
48:55	ROX	Reserved.
56:63	ROX	Reserved.

Register Name	**Power Bus Optical Link UE/CE/SUE Register**
Mnemonic	PB.IOO.SCOM.PB_EN_DOB_ECC_ERR_REG
Address	0000000005013818 (SCOM)
Description	Processor bus Optical Link UE/CE/SUE Register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved.
4:7	ROX	Reserved.
8:11	ROX	Reserved.
12:15	ROX	Reserved.
16:19	ROX	Reserved.
20:23	ROX	Reserved.
24:27	ROX	Reserved.
28:31	ROX	Reserved.
32:35	ROX	Reserved.
36:39	ROX	Reserved.
40:43	ROX	Reserved.
44:47	ROX	Reserved.

Register Name	Power Bus Optical Round Trip Delay Control Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_RT_DELAY_CTL_REG
Address	0000000005013819 (SCOM)
Description	Trip Delay Control Register

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PB_OLINK_RT_DELAY_CTL_SET: Setting a bit to 1 (auto reset to 0) causes the matching link to attempt to do a round-trip delay calculation. Results end up in the PB_OLINK_DLY_*_REG regs.
8:15	RW	PB_OLINK_RT_DELAY_CTL_STAT: A write of the reg resets these bits. They get set to 1 when a requested round-trip calculation completes.

Register Name	Power Bus Optical Performance Monitor Control Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_PMU_CTL_REG
Address	000000005013814A (SCOM)
Description	Processor bus Optical Performance Monitor Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	PMU0_ENABLE: pmu0 enable (the selected half-link must also be active).
1	RW	PMU1_ENABLE: pmu1 enable (the selected half-link must also be active).
2	RW	PMU2_ENABLE: pmu2 enable (the selected half-link must also be active).
3	RW	PMU3_ENABLE: pmu3 enable (the selected half-link must also be active).
4	RW	PMU4_ENABLE: pmu4 enable (the selected half-link must also be active).
5	RW	PMU5_ENABLE: pmu5 enable (the selected half-link must also be active).
6	RW	PMU6_ENABLE: pmu6 enable (the selected half-link must also be active).
7	RW	PMU7_ENABLE: pmu7 enable (the selected half-link must also be active).
8	RW	PMULET_FREEZE_MODE: PMUlet freeze mode 0 = freeze-on-full. 1 = freerun.
9	RW	COMMON_FREEZE_MODE: Common freeze mode 0 = Independent per PMUlet 1 = Any counter full freezes all
10	RW	PMULET_RESET_MODE: PMUlet reset mode 0 = Reset on read 1 = Reset on write
11	RW	PMU_EVENT0_SEL: Event0 selection 0 = cycles 1 = available cycles

Bits	SCOM	Field Mnemonic: Description
12:15	RW	PMU_EVENT1_SEL: Event1 selection 16:1 = encode selection 0 = disabled - clocks gated off 1 = any RCMD - event 2 = CRESP - event 3 = any presp - event 4 = dhdr - event 5 = data - event 6 = credit - event 7 = RCMD drop - event 8 = presp drop - dropped at this chip - event 9 = presp drop - dropped at remote chip - event A = command utilization - 1 count per 16 B used per available cycle B = presp util - 1 count per 16 B used per available cycle C = dhdr+data util - 1 count per 16 B used per available cycle D = total utilization - 1 count per 16 B used per available cycle E = cycles (available)(generally 4/5, unless replays happening) - event F = tdm_mode cycles (raw) - event.
16:19	RW	PMU_EVENT2_SEL: Event2 selection - 16:1.
20:23	RW	PMU_EVENT3_SEL: Event3 selection - 16:1.
24:25	RW	PMU0_SIZE: pmu0 size 00 = 36 bits 01 = 32 bits 10 = 28 bits 11 = 20 bits (only the 16 MSB are readable).
26:27	RW	PMU1_SIZE: pmu1 size 00 = 36 bits 01 = 32 bits 10 = 28 bits 11 = 20 bits (only the 16 MSB are readable).
28:29	RW	PMU2_SIZE: pmu2 size 00 = 36 bits 01 = 32 bits 10 = 28 bits 11 = 20 bits (only the 16 MSB are readable).
30:31	RW	PMU3_SIZE: pmu3 size 00 = 36 bits 01 = 32 bits 10 = 28 bits 11 = 20 bits (only the 16 MSB are readable).
32	RW	PMU01_LINK_SELECT: pmu01 link select 0 = A0 1 = A1
33	RW	PMU23_LINK_SELECT: pmu23 link select 0 = A1 1 = A0
34	RW	PMU45_LINK_SELECT: pmu45 link select 0 = A2 1 = A3
35	RW	PMU67_LINK_SELECT: pmu67 link select 0 = A3 1 = A2

Bits	SCOM	Field Mnemonic: Description
36:37	RW	PMU0145_EVENT0_MODE: pmu0145 event0 mode 10 = link_in 01 = link_out 11 = sum
38:39	RW	PMU0145_EVENT1_MODE: pmu0145 event1 mode 10 = link_in 01 = link_out 11 = sum
40:41	RW	PMU0145_EVENT2_MODE: pmu0145 event2 mode 10 = link_in 01 = link_out 11 = sum
42:43	RW	PMU0145_EVENT3_MODE: pmu0145 event3 mode 10 = link_in 01 = link_out 11 = sum
44:45	RW	PMU2367_EVENT0_MODE: pmu2367 event0 mode 10 = link_in 01 = link_out 11 = sum
46:47	RW	PMU2367_EVENT1_MODE: pmu2367 event1 mode 10 = link_in 01 = link_out 11 = sum
48:49	RW	PMU2367_EVENT2_MODE: pmu2367 event2 mode 10 = link_in 01 = link_out 11 = sum
50:51	RW	PMU2367_EVENT3_MODE: pmu2367 event3 mode 10 = link_in 01 = link_out 11 = sum
52	RW	PMU_ENABLE_GLOBAL_RUN: Enable global controls 0 = ignore global run state 1 = follow global run state
53	RW	PMU_GLOBAL_RUN_MODE: Global behavior mode 0 = run/stop with global run state 1 = same as 0, plus reset upon rising edge of global run
54:63	RW	PMU_SPARE: pmu spare

Register Name	Power Bus Optical Link PMU0 Counters Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_PMU0
Address	000000000501381B (SCOM)
Description	Processor bus optical link PMU0 counters

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU0_COUNTER0: PMU0 performance counter0.
16:31	RWX_WCLRREG	PMU0_COUNTER1: PMU0 performance counter1.
32:47	RWX_WCLRREG	PMU0_COUNTER2: PMU0 performance counter2.

Bits	SCOM	Field Mnemonic: Description
48:63	RWX_WCLRREG	PMU0_COUNTER3: PMU0 performance counter3.

Register Name	Power Bus Optical Link PMU1 Counters Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_PMU1
Address	000000000501381C (SCOM)
Description	Processor bus optical link PMU1 Counters

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU1_COUNTER0: PMU1 performance counter0.
16:31	RWX_WCLRREG	PMU1_COUNTER1: PMU1 performance counter1.
32:47	RWX_WCLRREG	PMU1_COUNTER2: PMU1 performance counter2.
48:63	RWX_WCLRREG	PMU1_COUNTER3: PMU1 performance counter3.

Register Name	Power Bus Optical Link PMU2 Counters Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_PMU2
Address	000000000501381D (SCOM)
Description	Processor bus optical link PMU2 counters

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU2_COUNTER0: PMU2 performance counter0.
16:31	RWX_WCLRREG	PMU2_COUNTER1: PMU2 performance counter1.
32:47	RWX_WCLRREG	PMU2_COUNTER2: PMU2 performance counter2.
48:63	RWX_WCLRREG	PMU2_COUNTER3: PMU2 performance counter3.

Register Name	Power Bus Optical Link PMU3 Counters Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_PMU3
Address	000000000501381E (SCOM)
Description	Processor bus optical link PMU3 counters

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU3_COUNTER0: PMU3 performance counter0.
16:31	RWX_WCLRREG	PMU3_COUNTER1: PMU3 performance counter1.
32:47	RWX_WCLRREG	PMU3_COUNTER2: PMU3 performance counter2.
48:63	RWX_WCLRREG	PMU3_COUNTER3: PMU3 performance counter3.

Register Name	Power Bus Optical Link PMU4 Counters Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_PMU4
Address	000000000501381F (SCOM)
Description	Processor bus optical link PMU4 counters

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU4_COUNTER0: PMU4 performance counter0.
16:31	RWX_WCLRREG	PMU4_COUNTER1: PMU4 performance counter1.
32:47	RWX_WCLRREG	PMU4_COUNTER2: PMU4 performance counter2.
48:63	RWX_WCLRREG	PMU4_COUNTER3: PMU4 performance counter3.

Register Name	Power Bus Optical Link PMU5 Counters Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_PMU5
Address	0000000005013820 (SCOM)
Description	Processor bus optical link PMU5 counters

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU5_COUNTER0: PMU5 performance counter0.
16:31	RWX_WCLRREG	PMU5_COUNTER1: PMU5 performance counter1.
32:47	RWX_WCLRREG	PMU5_COUNTER2: PMU5 performance counter2.
48:63	RWX_WCLRREG	PMU5_COUNTER3: PMU5 performance counter3.

Register Name	Power Bus Optical Link PMU6 Counters Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_PMU6
Address	0000000005013821 (SCOM)
Description	Processor bus optical link PMU6 counters

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU6_COUNTER0: PMU6 performance counter0.
16:31	RWX_WCLRREG	PMU6_COUNTER1: PMU6 performance counter1.
32:47	RWX_WCLRREG	PMU6_COUNTER2: PMU6 performance counter2.
48:63	RWX_WCLRREG	PMU6_COUNTER3: PMU6 performance counter3.

Register Name	Power Bus Optical Link PMU7 Counters Register
Mnemonic	PB.IOO.SCOM.PB_OLINK_PMU7
Address	0000000005013822 (SCOM)
Description	Processor bus optical link PMU7 counters

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PMU7_COUNTER0: PMU7 performance counter0.

Bits	SCOM	Field Mnemonic: Description
16:31	RWX_WCLRREG	PMU7_COUNTER1: PMU7 performance counter1.
32:47	RWX_WCLRREG	PMU7_COUNTER2: PMU7 performance counter2.
48:63	RWX_WCLRREG	PMU7_COUNTER3: PMU7 performance counter3.

Register Name	Power Bus Optical Miscellaneous Configuration Register
Mnemonic	PB.IOO.SCOM.PB_MISC_CFG
Address	0000000005013823 (SCOM)
Description	Processor bus optical miscellaneous configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	PB_CFG_IOO01_IS_LOGICAL_PAIR: Processor bus configuration ioo01 is logical pair.
1	RW	PB_CFG_IOO23_IS_LOGICAL_PAIR: Processor bus configuration ioo23 is logical pair.
2	RW	PB_CFG_IOO45_IS_LOGICAL_PAIR: Processor bus configuration ioo45 is logical pair.
3	RW	PB_CFG_IOO67_IS_LOGICAL_PAIR: Processor bus configuration ioo67 is logical pair.
4	WO_1P	SCOM_LINK01_RESET_KEEPER: link01 reset keeper.
5	WO_1P	SCOM_LINK23_RESET_KEEPER: link23 reset keeper.
6	WO_1P	SCOM_LINK45_RESET_KEEPER: link45 reset keeper.
7	WO_1P	SCOM_LINK67_RESET_KEEPER: link67 reset keeper.
8	RW	LINKS01_TOD_ENABLE: links01 TOD path enable.
9	RW	LINKS23_TOD_ENABLE: links23 TOD path enable.
10	RW	LINKS45_TOD_ENABLE: links45 TOD path enable.
11	RW	LINKS67_TOD_ENABLE: links67 TOD path enable.
12	RW	PB_LINK_CFG_AVP_MODE: pb link configuration AVP mode.
13	RW	SEL_03_NPU_NOT_PB: Choose what to multiplex onto the common transport bus 03 - +npu3/-pb05.
14	RW	SEL_04_NPU_NOT_PB: Choose what to multiplex onto the common transport bus 04 - +npu4/-pb06.
15	RW	SEL_05_NPU_NOT_PB: Choose what to multiplex onto the common transport bus 05 - +npu5/-pb07.
16:19	RW	MISC_SPARE: Miscellaneous spare.

Register Name	Power Bus Optical Link Trace Configuration Register
Mnemonic	PB.IOO.SCOM.PB_TRACE_CFG
Address	0000000005013824 (SCOM)
Description	Trace group encodes: 0 = disabled 1 = inbound link 2 = inbound dhdr position 0 3 = inbound dhdr position 1 4 = inbound dhdr position 2 5 = outbound link 6 = outbound dhdr position 0 7 = outbound dhdr position 1 8 = outbound dhdr position 2 9 = dob1 pos 0 A = dob1 pos 1 B = dob2 pos 0 C = dob2 pos D = dib pos 0 E = dib pos 1 F = Reserved.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	LINK00_HI_TRACE_CFG: link00 high trace configuration.
4:7	RW	LINK00_LO_TRACE_CFG: link00 low trace configuration.
8:11	RW	LINK01_HI_TRACE_CFG: link01 high trace configuration.
12:15	RW	LINK01_LO_TRACE_CFG: link01 low trace configuration.
16:19	RW	LINK02_HI_TRACE_CFG: link02 high trace configuration.
20:23	RW	LINK02_LO_TRACE_CFG: link02 low trace configuration.
24:27	RW	LINK03_HI_TRACE_CFG: link03 high trace configuration.
28:31	RW	LINK03_LO_TRACE_CFG: link03 low trace configuration.
32:35	RW	LINK04_HI_TRACE_CFG: link04 high trace configuration.
36:39	RW	LINK04_LO_TRACE_CFG: link04 low trace configuration.
40:43	RW	LINK05_HI_TRACE_CFG: link05 high trace configuration.
44:47	RW	LINK05_LO_TRACE_CFG: link05 low trace configuration.
48:51	RW	LINK06_HI_TRACE_CFG: link06 high trace configuration.
52:55	RW	LINK06_LO_TRACE_CFG: link06 low trace configuration.
56:59	RW	LINK07_HI_TRACE_CFG: link07 high trace configuration.
60:63	RW	LINK07_LO_TRACE_CFG: link07 low trace configuration.

Register Name	Power Bus Optical Link Framer0123 Error Readout Register
Mnemonic	PB.IOO.SCOM.PB_FM0123_ERR
Address	0000000005013825 (SCOM)
Description	Processor bus OLink Framer0123 Error Readout Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13	ROX	Reserved.
14	ROX	Reserved.
15	ROX	Reserved.
16	ROX	Reserved.
17	ROX	Reserved.
18	ROX	Reserved.
19	ROX	Reserved.
20	ROX	Reserved.
21	ROX	Reserved.
22	ROX	Reserved.
23	ROX	Reserved.
24	ROX	Reserved.
25	ROX	Reserved.
26	ROX	Reserved.
27	ROX	Reserved.
28	ROX	Reserved.
29	ROX	Reserved.
30	ROX	Reserved.
31	ROX	Reserved.
32	ROX	Reserved.
33	ROX	Reserved.
34	ROX	Reserved.
35	ROX	Reserved.
36	ROX	Reserved.
37	ROX	Reserved.
38	ROX	Reserved.
39	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
40	ROX	Reserved.
41	ROX	Reserved.
42	ROX	Reserved.
43	ROX	Reserved.
44	ROX	Reserved.
45	ROX	Reserved.
46	ROX	Reserved.
47	ROX	Reserved.
48	ROX	Reserved.
49	ROX	Reserved.
50	ROX	Reserved.
51	ROX	Reserved.
52	ROX	Reserved.
53	ROX	Reserved.
54	ROX	Reserved.
55	ROX	Reserved.
56	ROX	Reserved.
57	ROX	Reserved.
58	ROX	Reserved.
59	ROX	Reserved.
60	ROX	Reserved.
61	ROX	Reserved.
62	ROX	Reserved.
63	ROX	Reserved.

Register Name	**Power Bus Optical Link Framer4567 Error Readout Register**
Mnemonic	PB.IOO.SCOM.PB_FM4567_ERR
Address	0000000005013826 (SCOM)
Description	Processor bus OLink Framer4567 Error Readout Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13	ROX	Reserved.
14	ROX	Reserved.
15	ROX	Reserved.
16	ROX	Reserved.
17	ROX	Reserved.
18	ROX	Reserved.
19	ROX	Reserved.
20	ROX	Reserved.
21	ROX	Reserved.
22	ROX	Reserved.
23	ROX	Reserved.
24	ROX	Reserved.
25	ROX	Reserved.
26	ROX	Reserved.
27	ROX	Reserved.
28	ROX	Reserved.
29	ROX	Reserved.
30	ROX	Reserved.
31	ROX	Reserved.
32	ROX	Reserved.
33	ROX	Reserved.
34	ROX	Reserved.
35	ROX	Reserved.
36	ROX	Reserved.
37	ROX	Reserved.
38	ROX	Reserved.
39	ROX	Reserved.
40	ROX	Reserved.
41	ROX	Reserved.
42	ROX	Reserved.
43	ROX	Reserved.
44	ROX	Reserved.
45	ROX	Reserved.
46	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
47	ROX	Reserved.
48	ROX	Reserved.
49	ROX	Reserved.
50	ROX	Reserved.
51	ROX	Reserved.
52	ROX	Reserved.
53	ROX	Reserved.
54	ROX	Reserved.
55	ROX	Reserved.
56	ROX	Reserved.
57	ROX	Reserved.
58	ROX	Reserved.
59	ROX	Reserved.
60	ROX	Reserved.
61	ROX	Reserved.
62	ROX	Reserved.
63	ROX	Reserved.

Register Name	Power Bus Optical Link Parser0123 Error Readout Register
Mnemonic	PB.IOO.SCOM.PB_PR0123_ERR
Address	0000000005013827 (SCOM)
Description	Processor bus OLink Parser0123 Error Readout Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13:15	RO	Constant = 0b000
16	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
17	ROX	Reserved.
18	ROX	Reserved.
19	ROX	Reserved.
20	ROX	Reserved.
21	ROX	Reserved.
22	ROX	Reserved.
23	ROX	Reserved.
24	ROX	Reserved.
25	ROX	Reserved.
26	ROX	Reserved.
27	ROX	Reserved.
28	ROX	Reserved.
29:31	RO	Constant = 0b000
32	ROX	Reserved.
33	ROX	Reserved.
34	ROX	Reserved.
35	ROX	Reserved.
36	ROX	Reserved.
37	ROX	Reserved.
38	ROX	Reserved.
39	ROX	Reserved.
40	ROX	Reserved.
41	ROX	Reserved.
42	ROX	Reserved.
43	ROX	Reserved.
44	ROX	Reserved.
45:47	RO	Constant = 0b000
48	ROX	Reserved.
49	ROX	Reserved.
50	ROX	Reserved.
51	ROX	Reserved.
52	ROX	Reserved.
53	ROX	Reserved.
54	ROX	Reserved.
55	ROX	Reserved.
56	ROX	Reserved.
57	ROX	Reserved.
58	ROX	Reserved.
59	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
60	ROX	Reserved.
61:63	RO	Constant = 0b000

Register Name	Power Bus Optical Link Parser4567 Error Readout Register
Mnemonic	PB.IOO.SCOM.PB_PR4567_ERR
Address	0000000005013828 (SCOM)
Description	Processor bus OLink Parser4567 Error Readout Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13:15	RO	Constant = 0b000
16	ROX	Reserved.
17	ROX	Reserved.
18	ROX	Reserved.
19	ROX	Reserved.
20	ROX	Reserved.
21	ROX	Reserved.
22	ROX	Reserved.
23	ROX	Reserved.
24	ROX	Reserved.
25	ROX	Reserved.
26	ROX	Reserved.
27	ROX	Reserved.
28	ROX	Reserved.
29:31	RO	Constant = 0b000
32	ROX	Reserved.
33	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
34	ROX	Reserved.
35	ROX	Reserved.
36	ROX	Reserved.
37	ROX	Reserved.
38	ROX	Reserved.
39	ROX	Reserved.
40	ROX	Reserved.
41	ROX	Reserved.
42	ROX	Reserved.
43	ROX	Reserved.
44	ROX	Reserved.
45:47	RO	Constant = 0b000
48	ROX	Reserved.
49	ROX	Reserved.
50	ROX	Reserved.
51	ROX	Reserved.
52	ROX	Reserved.
53	ROX	Reserved.
54	ROX	Reserved.
55	ROX	Reserved.
56	ROX	Reserved.
57	ROX	Reserved.
58	ROX	Reserved.
59	ROX	Reserved.
60	ROX	Reserved.
61:63	RO	Constant = 0b000

Register Name	Power Bus Optical Link Performance Trace Configuration Register
Mnemonic	PB.IOO.SCOM.PB_PERFTRACE_CFG_REG
Address	0000000005013829 (SCOM)
Description	Processor bus OLink Perftrace Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	PERFTRACE_HI_ENABLE: perftrace high enable - multiplexer perftrace data onto trace bus 0.
1	RW	PERFTRACE_HI_FIXED_WINDOW_MODE: perftrace high fixed window mode - take a sample every 255 or 255x128 cycles.
2	RW	PERFTRACE_HI_PRESCALE_MODE: perftrace high prescale mode - wide-angle view - perfcounts are prescaled by 128.
3	RW	PTSPARE6: ptspare6.
4	RW	PERFTRACE_LO_ENABLE: perftrace low enable - multiplexer perftrace data onto trace bus 1.

Bits	SCOM	Field Mnemonic: Description
5	RW	PERFTRACE_LO_FIXED_WINDOW_MODE: perftrace low fixed window mode - take a sample every 255 or 255x128 cycles.
6	RW	PERFTRACE_LO_PRESCALE_MODE: perftrace low prescale mode - wide-angle view - perfcounts are prescaled by 128.
7	RW	PTSPARE7: ptspare7.
8:11	RW	PERFTRACE_HI_SELECT: perftrace high select.
12:15	RW	PERFTRACE_LO_SELECT: perftrace low select.

Register Name	Power Bus Optical Link Mailbox Control Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_CTL_REG
Address	000000000501382E (SCOM)
Description	Processor bus Optical Link Mailbox Control Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	MB_VALID: written to 1 to start operation, reads 1 if in progress, 0 when done.
1	RW	MB_WR_NOT_RD: Written to 1 for a write operation, 0 for a read. To do a write, first write the PBO_MAILBOX_DATA_REG, when write this reg with a write command, and the mailbox_id and link_id bits set for your desired destination. To do a read, write this reg with a read command, and the mailbox_id and link_id bits set for your desired destination. Monitor this reg to see when complete, then read the PBO_MAILBOX_DATA_REG to extract the resulting data. When you do a read, you only have access to the two regs on the other chip that are assigned to the physical link that connects the two chips. (In other words, remote reads aren't nearly as effective a tool as remote writes.
2	RWX_WCLRPART	MB_BAD_ADDR: (read-only) set if last operation was invalid (bad address).
3	RWX_WCLRPART	MB_LINK_DOWN: (read-only) set if link goes down during the op.
4	RWX_WCLRPART	MB_CORRUPT: (read-only) set if last operation corrupted (return response address mismatch).
5	RWX_WCLRPART	MB_SENT: (read-only) set when operation is sent to framer.
6	RWX_WCLRPART	MB_BAD_WRITE: (read-only) set on write to this register when already active.
7	WO_1P	MB_RESET: Write to a 1 to reset hung mailbox logic caused by a link going down. Auto reset to 0.
8	RW	MAILBOX_ID: 0/1 - there are two mailboxes per link.
9:11	RW	MB_LINK_ID: 0-7 - each half of a 24-lane optical link is independently accessible.
12:15	RW	MB_SPARE: mb spare.

Register Name	Power Bus Optical Link Mailbox Data Movement Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_DATA_REG
Address	000000000501382F (SCOM)
Description	This is the data source for a write of a remote mailbox write, or the holding reg for remote mailbox read return data processor bus Optical Link Mailbox Data Movement Register. This is the data source for a write of a remote mailbox write, or the holding reg for remote mailbox read return data.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 00 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_00_REG
Address	0000000005013830 (SCOM)
Description	Processor bus Optical Link Mailbox 00 Register (A0_evn_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 01 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_01_REG
Address	0000000005013831 (SCOM)
Description	Processor bus Optical Link Mailbox 01 Register (A0_evn_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 10 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_10_REG
Address	0000000005013832 (SCOM)
Description	Processor bus Optical Link Mailbox 10 Register (A0_odd_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 11 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_11_REG
Address	0000000005013833 (SCOM)
Description	Processor bus Optical Link Mailbox 11 Register (A0_odd_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 20 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_20_REG
Address	0000000005013834 (SCOM)
Description	rocessor bus Optical Link Mailbox 20 Register (A1_evn_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 21 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_21_REG
Address	0000000005013835 (SCOM)
Description	Processor bus Optical Link Mailbox 21 Register (A1_evn_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 30 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_30_REG
Address	0000000005013836 (SCOM)
Description	Processor bus Optical Link Mailbox 30 Register (A1_odd_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 31 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_31_REG
Address	0000000005013837 (SCOM)
Description	Processor bus Optical Link Mailbox 31 Register (A1_odd_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 40 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_40_REG
Address	0000000005013838 (SCOM)
Description	Processor bus Optical Link Mailbox 40 Register (A2_evn_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 41 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_41_REG
Address	0000000005013839 (SCOM)
Description	Processor bus Optical Link Mailbox 41 Register (A2_evn_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 50 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_50_REG
Address	000000000501383A (SCOM)
Description	Processor bus Optical Link Mailbox 50 Register (A2_odd_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 51 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_51_REG
Address	000000000501383B (SCOM)
Description	Processor bus Optical Link Mailbox 51 Register (A2_odd_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 60 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_60_REG
Address	000000000501383C (SCOM)
Description	Processor bus Optical Link Mailbox 60 Register (A3_evn_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 61 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_61_REG
Address	000000000501383D (SCOM)
Description	Processor bus Optical Link Mailbox 61 Register (A3_evn_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 70 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_70_REG
Address	000000000501383E (SCOM)
Description	Processor bus Optical Link Mailbox 70 Register (A3_odd_0).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Power Bus Optical Link Mailbox 71 Register
Mnemonic	PB.IOO.SCOM.PBO_MAILBOX_71_REG
Address	000000000501383F (SCOM)
Description	Processor bus Optical Link Mailbox 71 Register (A3_odd_1).

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	Reserved.

Register Name	Synchronization Configuration Register
Mnemonic	TP.TCN3.N3.SYNC_CONFIG
Address	0000000005030000 (SCOM)
Description	configuration of CC counters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay incoming sync pulse. Default are 8 latches including Async. 0000 = 8 0010 = 3 0011 = 4 0100 = 5 0101 = 6 0110 = 7 0111 = 8 1000 = 9 1001 = 10 1010 = 11 1011 = 12 1100 = 13 1101 = 14 1110 = 15 1111 = 16 Delay of the reset of the phase counter.
4	RW	LISTEN_TO_SYNC_PULSE_DIS: Disable phase counter synchronization by sync_pulse signal (default is enabled) ATTENTION: when ENABLE listen_to_sync, chiplet gets corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: default is 0, when set to 1, the alternative input of the sync_pulse will be used ATTENTION: when toggle the input select, chiplet gets corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: if set, use opcg initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit will clear the chiplet_is_aligned bit - see cplt_stat register.
8	RW	UNIT_REGION_CLKCMD_ENABLE: Enable the unit interface to start/stop one dedicate region - Used for POWER9 Cache/Core.
9	RW	DISABLE_PCB_ITR: Disable interrupt generation within CC - interrupt sent on each hld event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enable the vitl align check to compare alignment of incoming sync pulse with 2:1 vitl lcb.
11	RW	SYNC_PULSE_OUT_DIS: Disable sync_pulse output when set to 1, master chiplet will not sending sync pulses to slave chiplets anymore.
12:19	RW	UNUSED1219: Unused.

Register Name	OPCG Alignment Register
Mnemonic	TP.TCN3.N3.OPCG_ALIGN
Address	0000000005030001 (SCOM)
Description	OPCG ALIGN

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
4:7	RW	SNOP_ALIGN: SNOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
8:11	RW	ENOP_ALIGN: ENOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
12:19	RW	INOP_WAIT: INOP cycle delay (0-255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0-4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0-255).
40	RW	INOP_FORCE_SG: INOP: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: SNOP: Set SG high during SNOP.
42	RW	ENOP_FORCE_SG: ENOP: Set SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: 0: A clock change request will first wait the OPCG_WAIT cycles. 1: A clock change request will not wait, when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0: use inopa setting from opcg_reg0, 1: use rising edge of sync pulse, 2: use unit0_sync_lvl to align (for AVP - refresh0) 3: use unit1_sync_lvl to align (for AVP - refresh1).
46	RW	UNUSED46: Unused.
47:51	RW	SCAN_RATIO: scan_ratio (n = 0 - 15: (n + 1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1) - Default 4:1 = 00011.
52:63	RW	OPCG_WAIT_CYCLES: old PAD value, delay at the begin and end of the OPCG run, to allow DC signals to be there at the right time (0 4095), needs to be higher than plat depth ! Default = 0x020.

Register Name	OPCG Control 0 Register
Mnemonic	TP.TCN3.N3.OPCG_REG0
Address	0000000005030002 (SCOM)
Description	OPCG Control Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST-mode used for LBIST / 1 = RUNN-mode used for ABIST/IOBIST.
1	RWX	OPCG_GO: opcg go (start OPCG) - bit will b cleared when OPCG is done - poll for opcg_done in cplt_start reg.
2	RWX	RUN_SCAN0: run scan0 (will override all BIST mode settings but the scan_ratio) - will start a scan0 run, bit gets cleared when OPCG is done - poll for opcg_done in cplt_start reg.
3	RW	SCAN0_MODE: set PRPGs in scan0_mode but do not run automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: when selected, OPCG will wait for Master chiplet to get started. When Keep_MS_Mode is 0, SLAVE_MODE will be cleared after incoming trigger.

Bits	SCOM	Field Mnemonic: Description
5	RWX	OPCG_IN_MASTER_MODE: when selected, OPCG will send out trigger to all Slave chiplets - When Keep_MS_MODE = 0, MASTER_MODE gets cleared after sending out one Master trigger.
6	RW	KEEP_MS_MODE: when set to 1, OPCG in M/S mode bits will not be cleared after one incoming OPCG trigger. Default is clear M/S mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types, will clear the chiplet at all.
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run scan0 on all regions and types, will clear the chiplet at all exclude PLL region PLL can keep running.
11	RW	RUN_OPCG_ON_UPDATE_DR: start opcg engine when scan updated (update_dr) received (set pulse) Cronus requires this bit = 1 for a setpulse WRITE.
12	RW	RUN_OPCG_ON_CAPTURE_DR: start opcg engine when scan updated (capture_dr) received (set pulse) Cronus requires this bit = 1 for a setpulse READ.
13	RW	STOP_RUNN_ON_XSTOP: runn-mode: stop RUNN on checkstop.
14	RW	OPCG_STARTS_BIST: runn-mode: OPCG engine controls start_bist for ABIST or IOBIST (see BIST register).
15:20	RW	UNUSED1520: Unused.
21:63	RWX	LOOP_COUNT: Loop counter for LBIST and RUNN - write: target value - read: current counter value - will count from 0 to target value.

Register Name	OPCG Control 1 Register
Mnemonic	TP.TCN3.N3.OPCG_REG1
Address	0000000005030003 (SCOM)
Description	OPCG Control Register 1

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) runn-mode: start_bist match value(0:11).
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture, runn-mode: start_bist match value(12:23).
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture, runn-mode: start_bist match value(24:35).
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture, MISRs get active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG will only create even and not odd clocks. Used for RUNN to create only one clock in fast domain. Default is 0.
49	RW	SCAN_CLK_USE_EVEN: Generate scan clock in even cycle instead of odd. Default is 0 = odd for scan.
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: force rtim_thold low when not in test_dc mode (must be 0 at all time).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0: prevent fire of ARY HLD during NSL-fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0: Hold SG high during NSL-fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode: 00: Enable skitter during lbist_ip, 01: Enable skitter when misr_active - see misr_init_wait 10: skitter OPCG_GO mode - falling edge = start, rising edge = stop 11 - unused.
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end).
58	RW	INFINITE_MODE: infinite mode - RUNN and LBIST will run forever and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31).

Register Name	OPCG Control 2 Register
Mnemonic	TP.TCN3.N3.OPCG_REG2
Address	0000000005030004 (SCOM)
Description	OPCG Control Register 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: opcg go for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16.
4:15	RWX	PRPG_VALUE: set to 0 for prpg always on, else seed.
16:27	RW	PRPG_A_VAL: a value for PRPG aperture.
28:39	RW	PRPG_B_VAL: b value for PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end).
41:63	RW	UNUSED41_63: Unused.

Register Name	Scan Region and Type Register
Mnemonic	TP.TCN3.N3.SCAN_REGION_TYPE
Address	0000000005030005 (SCOM)
Description	Scan Region and Type

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: Default is 0, when its set to 1, the MASK bits in the CMSK chain decide, which part will be scanned or scan0. MASK = 1 = scan0, MASK = 0-part or scan chain.
1:2	RO	Constant = 0b00
3	NCX	SCAN_REGION_VITL: scan clock region vitl (Vital = Clock).
4	RWX	SCAN_REGION_PERV: scan clock region perv (Pervasive).
5	RWX	SCAN_REGION_UNIT1: scan clock region pb.
6	RWX	SCAN_REGION_UNIT2: scan clock region br - tp.
7	RWX	SCAN_REGION_UNIT3: scan clock region np - npu.
8	RWX	SCAN_REGION_UNIT4: scan clock region mm - nmmu.
9	RWX	SCAN_REGION_UNIT5: scan clock region int.
10	RWX	SCAN_REGION_UNIT6: scan clock region unused.
11	RWX	SCAN_REGION_UNIT7: scan clock region unused.
12	RWX	SCAN_REGION_UNIT8: scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: scan clock region unused.
14	RWX	SCAN_REGION_UNIT10: scan clock region Reserved.
15:47	RO	Constant = 0b00000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: scan chain func (functional).
49	RW	SCAN_TYPE_CFG: scan chain mode (boot config and debug config).
50	RW	SCAN_TYPE_CCFG_GPTR: scan chain ccfg / gptr (Pervasive: CC config, Others: GPTR).
51	RW	SCAN_TYPE_REGF: scan chain regf (register files).
52	RW	SCAN_TYPE_LBIST: scan chain lbst (LBIST).

Bits	SCOM	Field Mnemonic: Description
53	RW	SCAN_TYPE_ABIST: scan chain abst (ABIST).
54	RW	SCAN_TYPE_REPR: scan chain repr (Array Repair).
55	RW	SCAN_TYPE_TIME: scan chain time (Array Timing).
56	RW	SCAN_TYPE_BNDY: scan chain bndy (Boundary IO's).
57	RW	SCAN_TYPE_FARR: scan chain farr (fast array unload).
58	RW	SCAN_TYPE_CMSK: scan chain cmsk (lbist channel mask).
59	RW	SCAN_TYPE_INEX: scan chain idex (c14 asic).
60:63	RO	Constant = 0b0000

Register Name	Clock Region Register
Mnemonic	TP.TCN3.N3.CLK_REGION
Address	0000000005030006 (SCOM)
Description	start/stop of Clocks

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: command for clock control: 00 NOP 01 START 10 STOP 11 PULSE (one pulse).
2	RWX	SLAVE_MODE: when selected, Clock Command will wait for Master chiplet to get started. Bit gets cleared after incoming Slave trigger and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: when selected, Clock Command will send out trigger to all Slave chiplets - Bit gets cleared after sending out one Master trigger and Keep_MS_Mode_after_trigger is set to 0.
4	RWX	CLOCK_REGION_PERV: for clock region perv (Pervasive).
5	RWX	CLOCK_REGION_UNIT1: for clock region pb.
6	RWX	CLOCK_REGION_UNIT2: for clock region br - tp.
7	RWX	CLOCK_REGION_UNIT3: for clock region np - npu.
8	RWX	CLOCK_REGION_UNIT4: for clock region mm - nmmu.
9	RWX	CLOCK_REGION_UNIT5: for clock region int.
10	RWX	CLOCK_REGION_UNIT6: for clock region unused.
11	RWX	CLOCK_REGION_UNIT7: for clock region unused.
12	RWX	CLOCK_REGION_UNIT8: for clock region unused.
13	RWX	CLOCK_REGION_UNIT9: for clock region unused.
14	RWX	CLOCK_REGION_UNIT10: for clock region Reserved.
15:47	RO	Constant = 0b00000000000000000000000000000000
48	RWX	SEL_THOLD_SL: select sl tholds.
49	RWX	SEL_THOLD_NSL: select nsl tholds.
50	RWX	SEL_THOLD_ARY: select array thold.
51	RO	Constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support: default for pulse is ODD phase, when this bit is set, pulse will by applied on EVEN phase.
53:63	RO	Constant = 0b00000000000

Register Name	Clock Status SL Register
Mnemonic	TP.TCN3.N3.CLOCK_STAT_SL
Address	0000000005030008 (SCOM)
Description	Clocks running sl

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: status of perv sl hld 0 = run, 1 = stop.
5	ROX	CLOCK_STATUS_UNIT1_SL: status of pb sl hld 0 = run, 1 = stop.
6	ROX	CLOCK_STATUS_UNIT2_SL: status of br - tp sl hld 0 = run, 1 = stop.
7	ROX	CLOCK_STATUS_UNIT3_SL: status of np - npu sl hld 0 = run, 1 = stop.
8	ROX	CLOCK_STATUS_UNIT4_SL: status of mm - nmmu sl hld 0 = run, 1 = stop.
9	ROX	CLOCK_STATUS_UNIT5_SL: status of int sl hld 0 = run, 1 = stop.
10	ROX	CLOCK_STATUS_UNIT6_SL: status of unused sl hld 0 = run, 1 = stop.
11	ROX	CLOCK_STATUS_UNIT7_SL: status of unused sl hld 0 = run, 1 = stop.
12	ROX	CLOCK_STATUS_UNIT8_SL: status of unused sl hld 0 = run, 1 = stop.
13	ROX	CLOCK_STATUS_UNIT9_SL: status of unused sl hld 0 = run, 1 = stop.
14	ROX	CLOCK_STATUS_UNIT10_SL: status of Reserved sl hld 0 = run, 1 = stop.
15:63	RO	Constant = 0b11111111111111111111111111111111111111111111111111111111

Register Name	Clock Status NSL Register
Mnemonic	TP.TCN3.N3.CLOCK_STAT_NSL
Address	0000000005030009 (SCOM)
Description	Clocks running nsl

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: status of perv nsl hld 0 = run, 1 = stop.
5	ROX	CLOCK_STATUS_UNIT1_NSL: status of pb nsl hld 0 = run, 1 = stop.
6	ROX	CLOCK_STATUS_UNIT2_NSL: status of br - tp nsl hld 0 = run, 1 = stop.
7	ROX	CLOCK_STATUS_UNIT3_NSL: status of np - npu nsl hld 0 = run, 1 = stop.
8	ROX	CLOCK_STATUS_UNIT4_NSL: status of mm - nmmu nsl hld 0 = run, 1 = stop.
9	ROX	CLOCK_STATUS_UNIT5_NSL: status of int nsl hld 0 = run, 1 = stop.
10	ROX	CLOCK_STATUS_UNIT6_NSL: status of unused nsl hld 0 = run, 1 = stop.
11	ROX	CLOCK_STATUS_UNIT7_NSL: status of unused nsl hld 0 = run, 1 = stop.
12	ROX	CLOCK_STATUS_UNIT8_NSL: status of unused nsl hld 0 = run, 1 = stop.
13	ROX	CLOCK_STATUS_UNIT9_NSL: status of unused nsl hld 0 = run, 1 = stop.
14	ROX	CLOCK_STATUS_UNIT10_NSL: status of Reserved nsl hld 0 = run, 1 = stop.
15:63	RO	Constant = 0b11111111111111111111111111111111111111111111111111111111

Register Name	Clock Status ARY Register
Mnemonic	TP.TCN3.N3.CLOCK_STAT_ARY
Address	000000000503000A (SCOM)
Description	Clocks running ary

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: status of perv ary hld 0 = run, 1 = stop.
5	ROX	CLOCK_STATUS_UNIT1_ARY: status of pb ary hld 0 = run, 1 = stop.
6	ROX	CLOCK_STATUS_UNIT2_ARY: status of br - tp ary hld 0 = run, 1 = stop.
7	ROX	CLOCK_STATUS_UNIT3_ARY: status of np - npu ary hld 0 = run, 1 = stop.
8	ROX	CLOCK_STATUS_UNIT4_ARY: status of mm - nmmu ary hld 0 = run, 1 = stop.
9	ROX	CLOCK_STATUS_UNIT5_ARY: status of int ary hld 0 = run, 1 = stop.
10	ROX	CLOCK_STATUS_UNIT6_ARY: status of unused ary hld 0 = run, 1 = stop.
11	ROX	CLOCK_STATUS_UNIT7_ARY: status of unused ary hld 0 = run, 1 = stop.
12	ROX	CLOCK_STATUS_UNIT8_ARY: status of unused ary hld 0 = run, 1 = stop.
13	ROX	CLOCK_STATUS_UNIT9_ARY: status of unused ary hld 0 = run, 1 = stop.
14	ROX	CLOCK_STATUS_UNIT10_ARY: status of Reserved ary hld 0 = run, 1 = stop.
15:63	RO	Constant = 0b11111111111111111111111111111111111111111111111111111111

Register Name	ABIST and IOBIST Register
Mnemonic	TP.TCN3.N3.BIST
Address	000000000503000B (SCOM)
Description	ABIST and IOBIST per region

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: keep this 0 during ABIST/IOBIST. It could be used to bypass the RUNN start. When this bit is set, the BIST_START_TEST will go high immediately without waiting for RUNN. BIST will start with the first hld clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: select the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: select the ABIST engines for EDRAMs.
3	RW	TC_IOBIST_MODE_DC: select the IOBIST engines.
4	RW	BIST_PERV: region perv: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
5	RW	BIST_UNIT1: region pb: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
6	RW	BIST_UNIT2: region br - tp: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
7	RW	BIST_UNIT3: region np - npu: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.

Bits	SCOM	Field Mnemonic: Description
8	RW	BIST_UNIT4: region mm - nmmu: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
9	RW	BIST_UNIT5: region int: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
10	RW	BIST_UNIT6: region unused: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
11	RW	BIST_UNIT7: region unused: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
12	RW	BIST_UNIT8: region unused: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
13	RW	BIST_UNIT9: region unused: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
14	RW	BIST_UNIT10: region Reserved: 1 = BIST_START_TEST for this region will be triggered 0 = region take not part of the ABIST/IOBIST run.
15:47	RO	Constant = 0b00000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: Enable Strobe window only in TE = 1 mode OPCGGO tester pin is enabling ABIST compare, once ABIST has been started. Special setup in ABIST engine is required. default is 0. System mode can not enable this feature.
49:63	RO	Constant = 0b000000000000000

Register Name	**Checkstop 1 Register**
Mnemonic	TP.TCN3.N3.XSTOP1
Address	000000000503000C (SCOM)
Description	XSTOP per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: mask for checkstop to clockstop of select regions(see xstop_perv,xstop_unit0..n), 0 = ignore checkstop, 1 = stop on checkstop.
1	RW	XSTOP1_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP1: trigger opcg on checkstop instead of performing clockstop.
3	RW	XSTOP1_WAIT_ALLWAYS: when set to 1, checkstop will wait independent from flush, default is no wait, when flush in not set.
4	RW	XSTOP1_PERV: region perv: 1 = region will be stopped 0 = region will keep running on checkstop.
5	RW	XSTOP1_UNIT1: region pb: 1 = region will be stopped. 0 = region will keep running on checkstop.
6	RW	XSTOP1_UNIT2: region br - tp 1 = region will be stopped 0 = region will keep running on checkstop.

Bits	SCOM	Field Mnemonic: Description
7	RW	XSTOP1_UNIT3: region np - npu 1 = region will be stopped 0 = region will keep running on checkstop.
8	RW	XSTOP1_UNIT4: region mm - nmmu: 1 = region will be stopped 0 = region will keep running on checkstop.
9	RW	XSTOP1_UNIT5: region int: 1 = region will be stopped 0 = region will keep running on checkstop.
10	RW	XSTOP1_UNIT6: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
11	RW	XSTOP1_UNIT7: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
12	RW	XSTOP1_UNIT8: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
13	RW	XSTOP1_UNIT9: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
14	RW	XSTOP1_UNIT10: region Reserved: 1 = region will be stopped 0 = region will keep running on checkstop.
15:47	RO	Constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP1_WAIT_CYCLES: Defines, how many cycle checkstop will wait after dropping flush, before tholds get dropped. 0-4095 cycles possible.
60:63	RO	Constant = 0b0000

Register Name	Checkstop 2 Register
Mnemonic	TP.TCN3.N3.XSTOP2
Address	000000000503000D (SCOM)
Description	XSTOP per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: mask for checkstop to clockstop of select regions(see xstop_perv,xstop_unit0..n), 0 = ignore checkstop, 1 = stop on checkstop.
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: trigger opcg on checkstop instead of performing clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: when set to 1, checkstop will wait independent from flush, default is no wait, when flush in not set.
4	RW	XSTOP2_PERV: region perv: 1 = region will be stopped 0 = region will keep running on checkstop.
5	RW	XSTOP2_UNIT1: region pb: 1 = region will be stopped 0 = region will keep running on checkstop.

Bits	SCOM	Field Mnemonic: Description
6	RW	XSTOP2_UNIT2: region br - tp: 1 = region will be stopped 0 = region will keep running on checkstop.
7	RW	XSTOP2_UNIT3: region np - npu: 1 = region will be stopped 0 = region will keep running on checkstop.
8	RW	XSTOP2_UNIT4: region mm - nmmu: 1 = region will be stopped 0 = region will keep running on checkstop.
9	RW	XSTOP2_UNIT5: region int: 1 = region will be stopped 0 = region will keep running on checkstop.
10	RW	XSTOP2_UNIT6: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
11	RW	XSTOP2_UNIT7: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
12	RW	XSTOP2_UNIT8: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
13	RW	XSTOP2_UNIT9: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
14	RW	XSTOP2_UNIT10: region Reserved: 1 = region will be stopped 0 = region will keep running on checkstop.
15:47	RO	Constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Defines, how many cycle checkstop will wait after dropping flush, before tholds get dropped. 0-4095 cycles possible.
60:63	RO	Constant = 0b0000

Register Name	Checkstop 3 Register
Mnemonic	TP.TCN3.N3.XSTOP3
Address	000000000503000E (SCOM)
Description	XSTOP per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: mask for checkstop to clockstop of select regions(see xstop_perv,xstop_unit0..n), 0 = ignore checkstop, 1 = stop on checkstop.
1	RW	XSTOP3_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP3: trigger opcg on checkstop instead of performing clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: when set to 1, checkstop will wait independent from flush, default is no wait, when flush in not set.
4	RW	XSTOP3_PERV: region perv: 1 = region will be stopped 0 = region will keep running on checkstop.

Bits	SCOM	Field Mnemonic: Description
5	RW	XSTOP3_UNIT1: region pb: 1 = region will be stopped 0 = region will keep running on checkstop.
6	RW	XSTOP3_UNIT2: region br - tp: 1 = region will be stopped 0 = region will keep running on checkstop.
7	RW	XSTOP3_UNIT3: region np - npu: 1 = region will be stopped 0 = region will keep running on checkstop.
8	RW	XSTOP3_UNIT4: region mm - nmmu: 1 = region will be stopped 0 = region will keep running on checkstop.
9	RW	XSTOP3_UNIT5: region int: 1 = region will be stopped 0 = region will keep running on checkstop.
10	RW	XSTOP3_UNIT6: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
11	RW	XSTOP3_UNIT7: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
12	RW	XSTOP3_UNIT8: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
13	RW	XSTOP3_UNIT9: region unused: 1 = region will be stopped 0 = region will keep running on checkstop.
14	RW	XSTOP3_UNIT10: region Reserved: 1 = region will be stopped 0 = region will keep running on checkstop.
15:47	RO	Constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Defines, how many cycle checkstop will wait after dropping flush, before tholds get dropped. 0-4095 cycles possible.
60:63	RO	Constant = 0b0000

Register Name	Error Status Register
Mnemonic	TP.TCN3.N3.ERROR_STATUS
Address	000000000503000F (SCOM)
Description	Error Status of CC

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: write on read only register.
1	RWX	PCB_READ_NOT_ALLOWED_ERR: read not allowed, maybe write only register.
2	RWX	PCB_PARITY_ON_CMD_ERR: Parity error on command.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on address.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.

Bits	SCOM	Field Mnemonic: Description
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on spcif.
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: pcb write while OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: scan read when opcg is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: clock command in progress.
11	RWX	SCAN_COLLISION_ERR: scan region selected of running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set scan region which is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG gets triggered while OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: phase counters inside chiplet out of sync.
15	RWX	CLOCK_CMD_PREVENTED_ERR: security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on OPCG state machine.
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on scan/clock region/type or clock status reg.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG regs.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on sync config reg.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on checkstop reg.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0,4,5,6 regs.
22	RWX	CLKCMD_REQUEST_ERR: region clkcmd has one reqest pending but get a second one.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error - REQ / ACK sequence wrong.
24	RWX	VITL_ALIGN_ERR: VITL alignment is out of sync to sync pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 sync lvl pulse are not in sync - AVP broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on selfboot command state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	**OPCG Control Capture 1 Register**
Mnemonic	TP.TCN3.N3.OPCG_CAPT1
Address	0000000005030010 (SCOM)
Description	OPCG Control Register Capture1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000 = 12 cycle 0001 - 1100 = cycle 1-12 1101-1111 = 24 normal, no fast.
4:8	RW	SEQ_01: sequence cycle 1 for normal/slow region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_02: sequence cycle 2 for normal/slow region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_03: sequence cycle 3 for normal/slow region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_04: sequence cycle 4 for normal/slow region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_05: sequence cycle 5 for normal/slow region (sl, nsl, ary, se, fce).

Bits	SCOM	Field Mnemonic: Description
29:33	RW	SEQ_06: sequence cycle 6 for normal/slow region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_07: sequence cycle 7 for normal/slow region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_08: sequence cycle 8 for normal/slow region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_09: sequence cycle 9 for normal/slow region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_10: sequence cycle 10 for normal/slow region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_11: sequence cycle 11 for normal/slow region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_12: sequence cycle 12 for normal/slow region (sl, nsl, ary, se, fce).

Register Name	OPCG Control Capture 2 Register
Mnemonic	TP.TCN3.N3.OPCG_CAPT2
Address	0000000005030011 (SCOM)
Description	OPCG Control Register Capture 2

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2:
4:8	RW	SEQ_13_01EVEN: sequence cycle 1 - even - for fast region or cycle 13 for normal region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_14_01ODD: sequence cycle 1 - odd - for fast region or cycle 14 for normal region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_15_02EVEN: sequence cycle 2 - even - for fast region or cycle 15 for normal region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_16_02ODD: sequence cycle 2 - odd - for fast region or cycle 16 for normal region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_17_03EVEN: sequence cycle 3 - even - for fast region or cycle 17 for normal region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_18_03ODD: sequence cycle 3 - odd - for fast region or cycle 18 for normal region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_19_04EVEN: sequence cycle 4 - even - for fast region or cycle 19 for normal region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_20_04ODD: sequence cycle 4 - odd - for fast region or cycle 20 for normal region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_21_05EVEN: sequence cycle 5 - even - for fast region or cycle 21 for normal region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_22_05ODD: sequence cycle 5 - odd - for fast region or cycle 22 for normal region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_23_06EVEN: sequence cycle 6 - even - for fast region or cycle 23 for normal region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_24_06ODD: sequence cycle 6 - odd - for fast region or cycle 24 for normal region (sl, nsl, ary, se, fce).

Register Name	OPCG Control Capture 3 Register
Mnemonic	TP.TCN3.N3.OPCG_CAPT3
Address	0000000005030012 (SCOM)
Description	OPCG Control Register Capture 3

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:

Bits	SCOM	Field Mnemonic: Description
4:8	RW	SEQ_07EVEN: sequence cycle 7 - even - for fast region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_07ODD: sequence cycle 7 - odd - for fast region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_08EVEN: sequence cycle 8 - even - for fast region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_08ODD: sequence cycle 8 - odd - for fast region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_09EVEN: sequence cycle 9 - even - for fast region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_09ODD: sequence cycle 9 - odd - for fast region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_10EVEN: sequence cycle 10 - even - for fast region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_10ODD: sequence cycle 10 - odd - for fast region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_11EVEN: sequence cycle 11 - even - for fast region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_11ODD: sequence cycle 11 - odd - for fast region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_12EVEN: sequence cycle 12 - even - for fast region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_12ODD: sequence cycle 12 - odd - for fast region (sl, nsl, ary, se, fce).

Register Name	Debug CBS CC Register
Mnemonic	TP.TCN3.N3.DBG_CBS_CC
Address	0000000005030013 (SCOM)
Description	Debug CBS CC Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset Endpoint - Is the CC and CTRL in reset state.
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped, when enabled, need plat-depth cycles to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test Enable.
4	ROX	DBG_CBS_REQ: CBS Interface - Request (Latched).
5:7	ROX	DBG_CBS_CMD: CBS Interface - Command (Latched).
8:12	ROX	DBG_CBS_STATE: CBS Command State Machine 00000 = Idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: status of the security mode bit.
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS Protocol Error - REQ raised, although state machine is not in IDLE - need reset_ep to clear this bit. No impact on IPL.
15	ROX	DBG_PCB_IDLE: PCB Interface in IDLE state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: current / latest OPCG MODE - 0 = NOP 1 = LBIST 2 = ABIST 3 = RUNN 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN with CaptureDR 9 = CLK Change Request 10-15 = unused.
20:23	ROX	DBG_LAST_OPCG_MODE: previous OPCG MODE.

Bits	SCOM	Field Mnemonic: Description
24	ROX	DBG_PCB_ERROR: PCB Interface Error, read CC Error Reg or set CBS_CMD = 001 to switch FSI CBS Debug Information to CC Error Register.
25	ROX	DBG_PARITY_ERROR: Any Parity Error, non PCB Parity - read CC Error Reg or set CBS_CMD = 001 to switch FSI CBS Debug Information to CC Error Register.
26	ROX	DBG_CC_ERROR: Any other CC Error - read CC Error Reg or set CBS_CMD = 001 to switch FSI CBS Debug Information to CC Error Register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: Is 1 when the a valid align pulse ws send out.
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: RESET will clear that bit, the first PCB request will set it.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: rising or falling edge on test enable, after reset - need reset_ep to clear, no impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: rising or falling edge on vitl_clkoff, after reset - need reset_ep to clear, no impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: only represenation of CC ack signal going to FSI.

Register Name	**CC Protect Mode Register**
Mnemonic	TP.TCN3.N3.CC_PROTECT_MODE_REG
Address	00000000050303FE (SCOM)
Description	CC Protect Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	**Atomic Lock Register**
Mnemonic	TP.TCN3.N3.CC_ATOMIC_LOCK_REG
Address	00000000050303FF (SCOM)
Description	Atomic Lock Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	CC_ATOMIC_ID: Atomic ID.
5:7	RO	Constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	**Global Checkstop FIR Register**
Mnemonic	TP.TCN3.N3.XFIR
Address	0000000005040000 (SCOM)
Description	Global checkstop FIR

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: summary bit(any checkstop).

Bits	SCOM	Field Mnemonic: Description
1	RWX	XFIR_IN1: Checkstop broadcast via OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from pervasive unit.
4	RWX	XFIR_IN4: Checkstop from MCS01_0.
5	RWX	XFIR_IN5: Checkstop from MCS01_1.
6	RWX	XFIR_IN6: Checkstop from PB_0 FIR.
7	RWX	XFIR_IN7: Checkstop from PB_1 FIR.
8	RWX	XFIR_IN8: Checkstop from PB_2 FIR.
9	RWX	XFIR_IN9: Checkstop from BR FIR.
10	RWX	XFIR_IN10: Checkstop from NP FIR.
11	RWX	XFIR_IN11: Checkstop from MM FIR.
12	RWX	XFIR_IN12: Checkstop from MM FIR Unstaged.
13	RWX	XFIR_IN13: Checkstop from PB_3 FIR.
14	RWX	XFIR_IN14: Checkstop from PB_4 FIR.
15	RWX	XFIR_IN15: Checkstop from PB_5 FIR.
16	RWX	XFIR_IN16: Checkstop from PB_5 FIR Unstaged.
17	RWX	XFIR_IN17: Checkstop from INT FIR.
18:25	RWX	XFIR_IN18: Unused.
26	RWX	XFIR_IN26: Checkstop on debug trigger.

Register Name	Global Recoverable FIR Register
Mnemonic	TP.TCN3.N3.RFIR
Address	0000000005040001 (SCOM)
Description	Global recoverable FIR

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Unused.
1	ROX	LFIR_RECOV_ERR: recoverable error from pervasive unit.
2	ROX	RFIR_IN4: recov from MCS01_0.
3	ROX	RFIR_IN5: recov from MCS01_1.
4	ROX	RFIR_IN6: recov from PB_0 FIR.
5	ROX	RFIR_IN7: recov from PB_1 FIR.
6	ROX	RFIR_IN8: recov from PB_2 FIR.
7	ROX	RFIR_IN9: recov from BR FIR.
8	ROX	RFIR_IN10: recov from NP FIR.
9	ROX	RFIR_IN11: recov from MM FIR.
10	ROX	RFIR_IN12: recov from MM FIR Unstaged.
11	ROX	RFIR_IN13: recov from PB_3 FIR.
12	ROX	RFIR_IN14: recov from PB_4 FIR.

Bits	SCOM	Field Mnemonic: Description
13	ROX	RFIR_IN15: recov from PB_5 FIR.
14	ROX	RFIR_IN16: recov from PB_5 FIR Unstaged.
15	ROX	RFIR_IN17: recov from INT FIR.
16:23	ROX	RFIR_IN18: Unused.

Register Name	FIR Mask Register
Mnemonic	TP.TCN3.N3.FIR_MASK
Address	0000000005040002 (SCOM)
Description	FIR Mask

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: mask for xfir summary bit(any checkstop).
1	RW	FIR_MASK_IN1: mask for xfir from other chiplets.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: mask for xfir from pervasive unit.
4	RW	FIR_MASK_IN4: mask for MCS01_0 XFIR and RFIR.
5	RW	FIR_MASK_IN5: mask for MCS01_1 XFIR and RFIR.
6	RW	FIR_MASK_IN6: mask for PB_0 XFIR and RFIR.
7	RW	FIR_MASK_IN7: mask for PB_1 XFIR and RFIR.
8	RW	FIR_MASK_IN8: mask for PB_2 XFIR and RFIR.
9	RW	FIR_MASK_IN9: mask for BR XFIR and RFIR.
10	RW	FIR_MASK_IN10: mask for NP XFIR and RFIR.
11	RW	FIR_MASK_IN11: mask for MM XFIR and RFIR.
12	RW	FIR_MASK_IN12: mask for MM XFIR and RFIR Unstaged.
13	RW	FIR_MASK_IN13: mask for PB_3 XFIR and RFIR.
14	RW	FIR_MASK_IN14: mask for PB_4 XFIR and RFIR.
15	RW	FIR_MASK_IN15: mask for PB_5 XFIR and RFIR.
16	RW	FIR_MASK_IN16: mask for PB_5 XFIR and RFIR Unstaged.
17	RW	FIR_MASK_IN17: mask for INT XFIR and RFIR.
18:25	RW	FIR_MASK_IN18: Unused.
26	RW	FIR_MASK_IN26: mask for debug trigger and local checkstop to recoverable error.

Register Name	Special Attention Register
Mnemonic	TP.TCN3.N3.SPATTN
Address	0000000005040004 (SCOM) 0000000005040005 (SCOM1) 0000000005040006 (SCOM2)
Description	Special Attention

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: spec attn from mcs01_0.
1	ROX	NCX	NCX	SPATTN_IN1: spec attn from mcs01_1.
2	ROX	NCX	NCX	SPATTN_IN2: spec attn from PB_0.
3:5	ROX	NCX	NCX	SPATTN_IN3: Unused special attentions.
6	ROX	NCX	NCX	SPATTN_IN6: spec attn from INT.
7	ROX	NCX	NCX	SPATTN_IN7: spec attn from PB_3.
8	ROX	NCX	NCX	SPATTN_IN8: spec attn from PB_4.
9	ROX	NCX	NCX	SPATTN_IN9: spec attn from PB_5.

Register Name	Special Attention Mask Register
Mnemonic	TP.TCN3.N3.SPA_MASK
Address	0000000005040007 (SCOM)
Description	Special Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: special attention mask.

Register Name	FIR Mode Register
Mnemonic	TP.TCN3.N3.EPS.FIR.MODE_REG
Address	0000000005040008 (SCOM)
Description	Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop Chip TOD on Checkstop (Unused in POWER9).
5	RW	MODE_IN5: Stop Chip TOD on Recoverable (Unused in POWER9).
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enable checkstop on special attention.
9	RW	MODE_IN9: mask_direct/local_error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention Register
Mnemonic	TP.TCN3.N3.HOSTATTN
Address	0000000005040009 (SCOM)
Description	Host Attention

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host Attention Summary Bit.
1	ROX	HOSTATTN_IN1: Host Attention from mcs01 bit 0.
2	ROX	HOSTATTN_IN2: Host Attention from mcs01 bit 1.
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	Local FIR Register
Mnemonic	TP.TCN3.N3.LOCAL_FIR
Address	000000000504000A (SCOM) 000000000504000B (SCOM1) 000000000504000C (SCOM2)
Description	Local FIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Local errors from GPIO (PCB error).
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, ...).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from Thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from Thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from Thermal (Trip error critical).
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from Thermal (Trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: therm volttrip error.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from Debug (error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from Trace Array0 (SCOM error).
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Local errors from Trace Array0.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Local errors from Trace Array1 (SCOM error).
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Local errors from Trace Array1.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Local errors from Trace Array2 (SCOM error).
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Local errors from Trace Array2.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Local errors from Trace Array3 (SCOM error).
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Local errors from Trace Array3.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Local errors from Trace Array4 (SCOM error).
21	RWX	WOX_AND	WOX_OR	FIR_IN21: Local errors from Trace Array4.
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Local errors from Trace Array5 (SCOM error).
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Local errors from Trace Array5.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Errors from Bsense IO.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Unused.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Unused.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Unused.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Reserved for Firmware usage.
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Reserved for Firmware usage.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Reserved for Firmware usage.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Reserved for Firmware usage.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Reserved for Firmware usage.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Reserved for Firmware usage.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Reserved for Firmware usage.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Reserved for Firmware usage.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: malfunction alert broadcast via OOB.

Register Name	Local FIR Mask Register
Mnemonic	TP.TCN3.N3.EPS.FIR.LOCAL_FIR_MASK
Address	000000000504000D (SCOM) 000000000504000E (SCOM1) 000000000504000F (SCOM2)
Description	Local FIR Mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: mask for LEM error collection vector.

Register Name	Local FIR Action 0 Register
Mnemonic	TP.TCN3.N3.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000005040010 (SCOM)
Description	Local FIR Action0

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: action0 mask.

Register Name	Local FIR Action 1 Register
Mnemonic	TP.TCN3.N3.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000005040011 (SCOM)
Description	Local FIR Action1

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: action1 mask.

Register Name	Group Checkstop Mask Register
Mnemonic	TP.TCN3.N3.EPS.FIR.GXSTOP_TRIG_REG
Address	0000000005040013 (SCOM)
Description	Group Xstop MASK Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for System Checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for Recoverable Error.
2	RW	GXSTP_TRIG_IN2: Mask bit for Special Attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for Local Checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for Type 4 Error (Host Attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for group checkstop input (0).

Bits	SCOM	Field Mnemonic: Description
8	RW	GXSTP_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for Debug Checkstop on Trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group0 Checkstop Mask Register
Mnemonic	TP.TCN3.N3.EPS.FIR.GXSTOP0_MASK_REG
Address	0000000005040014 (SCOM)
Description	Group0 Xstop Mask Reg

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for System Checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for Recoverable Error.
2	RW	GXSTP0_TRIG_IN2: Mask bit for Special Attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for Local Checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for Type 4 Error (Host Attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for Debug Checkstop on Trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group1 Checkstop Mask Register
Mnemonic	TP.TCN3.N3.EPS.FIR.GXSTOP1_MASK_REG
Address	0000000005040015 (SCOM)
Description	Group1 Xstop Mask Reg

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for System Checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for Recoverable Error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for Special Attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for Local Checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for Type 4 Error (Host Attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for group checkstop input (1).

Bits	SCOM	Field Mnemonic: Description
9	RW	GXSTP1_TRIG_IN9: Mask bit for Debug Checkstop on Trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group2 Checkstop Mask Register
Mnemonic	TP.TCN3.N3.EPS.FIR.GXSTOP2_MASK_REG
Address	0000000005040016 (SCOM)
Description	Group2 Xstop Mask Reg

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for System Checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for Recoverable Error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for Special Attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for Local Checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for Type 4 Error (Host Attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for Debug Checkstop on Trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	FIR Summary Mask Register
Mnemonic	TP.TCN3.N3.EPS.FIR.SUM_MASK_REG
Address	0000000005040017 (SCOM)
Description	Summary Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System Checkstop Summary Bit.
1	RW	SMASK_IN1: Recoverable Summary Bit.
2	RW	SMASK_IN2: Special Attention Summary Bit.
3	RW	SMASK_IN3: Local Checkstop Summary Bit.
4	RW	SMASK_IN4: Type4 (Host Attention Summary Bit.

Register Name	Local Checkstop Error Register
Mnemonic	TP.TCN3.N3.LOCAL_XSTOP_ERR
Address	0000000005040018 (SCOM)
Description	Local checkstop error

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit.
1	ROX	LOCAL_XSTOP_IN1: Local checkstop from mcs01, bit 0.
2	ROX	LOCAL_XSTOP_IN2: Local checkstop from mcs01, bit 1.
3	ROX	LOCAL_XSTOP_IN3: Unused.
4	ROX	LOCAL_XSTOP_IN4: Unused.
5	ROX	LOCAL_XSTOP_IN5: Unused.
6	ROX	LOCAL_XSTOP_IN6: Local checkstop from np, bit 0.
7	ROX	LOCAL_XSTOP_IN7: Local checkstop from np, bit 1.
8	ROX	LOCAL_XSTOP_IN8: Local checkstop from mm bit 0.
9	ROX	LOCAL_XSTOP_IN9: Local checkstop from mm bit 1.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask Register
Mnemonic	TP.TCN3.N3.LOCAL_XSTOP_MASK
Address	0000000005040019 (SCOM)
Description	Local Checkstop Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask Register
Mnemonic	TP.TCN3.N3.HOSTATTN_MASK
Address	000000000504001A (SCOM)
Description	Host Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Thermal Sensor Result 0 Register
Mnemonic	TP.TCN3.N3.EPS.THERM.DTS_RESULT0
Address	0000000005050000 (SCOM)
Description	DTS Thermal Sensor loop1 Results

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results Register
Mnemonic	TP.TCN3.N3.EPS.THERM.DTS_TRC_RESULT
Address	0000000005050003 (SCOM)
Description	DTS Trace Results

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	Constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.

Register Name	Thermal Mode Register
Mnemonic	TP.TCN3.N3.EPS.THERM.THERM_MODE_REG
Address	000000000505000F (SCOM)
Description	CPM and DTS enables and cntl's

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: force tpc_therm_thres_mac clock gating off and activates clocks.
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables. 1xx: trip0 - warning. x1x: trip1 - critical. xx1: trip2 - fatal.

Bits	SCOM	Field Mnemonic: Description
5	RW	THERM_DTS_SAMPLE_ENA: 0: no dts sampling, 1: dts sampling is enabled and below counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is feed into an 18 Bit counter, with the therm_sample_pulse_cnt it is possible to select a highorder bit of the counter. to enable a resolutions of sampling dtss between 2.5 us and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a dts sample. 0000: 16 ms. 0001: 8 ms. 0010: 4 ms. 0011: 2 ms. 0100: 1 ms. 0101: 0.5 ms. 0110: 250 us. 0111: 125 us. 1000: 62 .5us. 1001: 31.3 us. 1010: 15.6 us. 1011: 7.8 us. 1100: 3.9 us. 1101: 2 us. 1110: 1 us. 1111: 0.5 us.
10:11	RW	THERM_THRES_MODE_ENA: forces max or min mode in threshold unit: 00: is off. 11: is ilegal. 10: max mode. 01: min mode.
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: 0 - therm_overflow_err will be enabled. 1 - therm_overflow_err will be disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which dts result will be provided with pcb read addr_v(4): 0000: DTS 0. 0001: DTS 1. 0010: DTS 2. 0100: DTS 4. 1111: Worst Case Sensor.
20:21	RW	THERM_DTS_ENABLE_L1: loop1 dts enables: 1x: DTS 0 available. x1: DTS 1 available.
22:34	RO	Constant = 0b0000000000000
35:36	RW	Reserved.

Register Name	Skitter Control Register
Mnemonic	TP.TCN3.N3.EPS.THERM.SKITTER_MODE_REG
Address	0000000005050010 (SCOM)
Description	Skitter Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: forces skitter to hold current sample.

Bits	SCOM	Field Mnemonic: Description
1	RW	DISABLE_SKITTER_STICKINESS: if '0' accumulation mode, '1' samples new value each cycle and resets sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0: hold_on_trigger0. bit1: _on_trigger1.
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0: reset_sticky_on_trigger0. bit1: reset_sticky_on_trigger1.
8:9	RW	SKITTER_SAMPLE_GUTS: Selects guts to measure: 00: guts1. 01: guts2. 10: guts3. 11: guts4.
10:43	RO	Constant = 0b00000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: forces skitter to hold current sample on dbg trigger, this has highest priority.
45	ROX	SKITTER_DATA_V_LT: if '1' the data requested by a skitter force read register has finished and data is present in skitter data register in the collector macro. The data be read by any combination of V25/V26/V27 pcb reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TCN3.N3.EPS.THERM.INJECT_REG
Address	0000000005050011 (SCOM)
Description	Error Injection Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00: no injection. 01: warning trip level injection. 10: crtical trip level injection. 11: fatal trip level injection.
2:3	RW	THERM_INJECT_MODE: 00: no injection. 01: injection on the next dts sample. 10: solid injection for the next dts samples till bit setting changes. 11: not used.

Register Name	Control / Force Reset Register
Mnemonic	TP.TCN3.N3.EPS.THERM.CONTROL_REG
Address	0000000005050012 (SCOM)
Description	Control / Force Reset Register

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved.
1	WO_1P	Reserved.
2	WO_1P	Reserved.
3	WO_1P	Reserved.
4	WO_1P	Reserved.

Bits	SCOM	Field Mnemonic: Description
5	WO_1P	Reserved.
6	WO_1P	Reserved.
7	WO_1P	Reserved.
8	WO_1P	Reserved.
9	WO_1P	Reserved.
10	WO_1P	Reserved.
11	WO_1P	Reserved.
12	WO_1P	Reserved.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCN3.N3.EPS.THERM.ERR_STATUS_REG
Address	0000000005050013 (SCOM)
Description	Thermal Error Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13	ROX	Reserved.
14	ROX	Reserved.
15	ROX	Reserved.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: serial shift count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: therm mode reg parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: skitter mode register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: skitter force register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: scan init version register parity error mask.
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: volt mode reg parity error mask.
22	RO	Constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: count state machine error mask.

Bits	SCOM	Field Mnemonic: Description
24	ROX	RUN_STATE_ERR_MASK: run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: thres state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: force skitter read one hot error mask.
31	ROX	PCB_ERR_MASK: pervasive control bus error mask.
32:39	RO	Constant = 0b00000000
40:43	ROX	Reserved.
44:46	ROX	Reserved.
47	ROX	Reserved.
48	ROX	Reserved.
49:50	ROX	Reserved.
51:54	ROX	Reserved.
55	ROX	Reserved.
56	ROX	Reserved.
57	ROX	Reserved.
58	ROX	Reserved.
59	ROX	Reserved.
60:63	RO	Constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCN3.N3.EPS.THERM.SKITTER_FORCE_REG
Address	0000000005050014 (SCOM)
Description	Skitter Force Read Register

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter.

Register Name	Skitter Clock Source Control Register
Mnemonic	TP.TCN3.N3.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000005050016 (SCOM)
Description	Skitter clock source control register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects clock to measure: 000 = Local mesh clock. 001 = External pin skitter_c1_1_in. 010 = Local d1clk only if d_mode = 1. 011 = External pin skitter_c1_2_in. 100 = Local lclk only if d_mode = 1. 101 = External pin skitter_c1_3_in. 110 = Unused. 111 = External pin skitter_c1_4_in.
3:35	RO	Constant = 0b00000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: To select delay to be added between clock source multiplexer and the inverter chain (base line delay is 12.2 psec) of skitter0. 00 = No delay. 01 = 0.6 psec. 10 = 1.8 psec. 11 = 5 psec.

Register Name	Skitter Data 0 Register
Mnemonic	TP.TCN3.N3.EPS.THERM.SKITTER_DATA0
Address	0000000005050019 (SCOM)
Description	Skitter data register read bit0:63

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data 1 Register
Mnemonic	TP.TCN3.N3.EPS.THERM.SKITTER_DATA1
Address	000000005050001A (SCOM)
Description	Skitter data register read bit32:95

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data 2 Register
Mnemonic	TP.TCN3.N3.EPS.THERM.SKITTER_DATA2
Address	000000005050001B (SCOM)
Description	Skitter data register read bit64:127

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Timestamp Counter Read Register
Mnemonic	TP.TCN3.N3.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000505001C (SCOM)
Description	Timestamp counter read

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.